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Data handbook

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Electronic components and materials

Signetics integrated circuits 1976

Logic

Memories

Interface

Analog

Microprocessor

Milrel

signetics

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As one of the world's largest manufacturers of integrated circuits, Signetics designs, develops, manufactures and sells over 1600 different types of integrated circuits. Signetics produces digital and linear circuits, utilizing both bipolar and metal-oxide-semiconductor (MOS) manufacturing processes.

This 1976 issue of our data book covers the full expanse of our broad product line. For ease of use, we have grouped our products into 6 major families. They are: Logic—covering 54/74, 8200 series devices and 10,000 series ECL; Memories—covering bipolar and MOS shift registers and memories; Interface—covering both logic and analog devices; Analog—covering general and consumer analog devices including D-MOS; Microprocessors—covering bipolar, MOS and system logic devices; MilRel—covering the high reliability programs available in our product line.

This issue represents a unique approach in the presentation of integrated circuits data. In keeping with our intent of presenting the maximum amount of data requiring the minimum amount of effort by the user, we have grouped product family information at the beginning of the section covering that particular family. The information covered usually includes an introduction to that family, a table of the complete family electrical characteristics, and a grouping of the general parameter measurement information and other pertinent data. We feel that this format allows the reader to quickly insure that he is aware of all possible devices that are available from Signetics to help him with his design.

Signetics reserves the right to make changes in the products contained in this book in order to improve design or performance and to supply the best possible products. Signetics also assumes no responsibility for the use of any circuits described herein and makes no representations that they are free from patent infringement.

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GENERAL DESCRIPTION

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted)

Supply Voltage V_{CC} (See Note 1)	7V
Input Voltage V_{in} (See Note 1)	5.5V
Interemitter Voltage (See Note 2)	5.5V
Resistor Node Voltage, 54121, 74121 (See Note 1)	-5.5V to 7V
Operating Free-Air Temperature Range:	
Series 54 Circuits	-55°C to 125°C
Series 74 Circuits	0°C to 70°C
Storage Temperature Range	-65°C to 150°C

NOTES:

1. Voltage values, except interemitter voltage, are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter transistor.
3. Output sink current tests 1 output at a time.

Series 54/74 Logic Family

The 54/74XX logic family is medium speed TTL, and high speed TTL integrated circuits. The family includes a multiple number of functions in a variety of packages. The 54XX devices are characterized for the full military temperature range of -55°C to +125°C. The 74XX devices are characterized for the limited temperature range of 0°C to +70°C.

INPUT CLAMPING DIODES

Although not shown on all schematic diagrams, all of these SSI circuits incorporate input diodes. Each clamping diode is capable of limiting negative excursions at the input to a maximum of 1.5 volts below ground, even if -12mA of current is drawn.

DESIGN CONSIDERATIONS

Logic Definition

Series 54/74 logic is defined in terms of standard POSITIVE LOGIC using the following definitions:
LOW VOLTAGE = LOGICAL "0"
HIGH VOLTAGE = LOGICAL "1"

Unused Inputs

For optimum switching times and minimum noise susceptibility unused inputs should be maintained at a positive voltage greater than 2.4V but not to exceed the absolute maximum rating of 5.5V. This eliminates the distributed capacitance associated with the floating-input-transitor emitter, bond wire, and package load, and ensures that no degradation will occur in the propagation delay times. Some possible ways of handling input emitters are:

a. Connect unused inputs to a supply voltage. Preferably, this voltage should be between 2.4V and 5.5V.
b. Connect unused inputs to a used input if maximum fanout of the driving output will not be exceeded. Each input presents a full load in the logical "1" state to the driving output.

Input-Current Requirements

Input-current requirements reflect worse-case V_{CC} and temperature condition. Currents into the input terminals are specified as positive values.

54/74 Logic

Each input of the multiple-emitter input transistor that utilizes a 4KΩ resistor requires no more than -1.6 mA flow out of the input at a logical "0" voltage level; therefore, one load (N=1) for 54/74 logic is -1.6 mA maximum. Each input requires current into the input at a logical "1" voltage level. This current is 40μA maximum for each emitter input.

Fanout Capability

Fanout reflects the ability of an output to sink current from a number of loads (N) at a logical "0" voltage level and to supply current at a logical "1" voltage level. Each standard 54/74 output is capable of sinking current or supplying current to 10 loads (N = 10.) The buffer gate (54/7440) is capable of sinking current or supplying current to 30 loads (N = 30).

ELECTRICAL CHARACTERISTICS

These are guaranteed over the applicable operating free-air temperature range, unless otherwise noted, as shown in Section 2 of the handbook.

NOTE

Any product available in an A or B package can also be supplied in the F cerdip package.

S54

↓

TEMPERATURE RANGE*

S54 = -55°C to +125°C (Military Range)

N74 = 0°C to +70°C (Industrial Range)

40

↓

PART IDENTIFICATION

Must contain two to four characters.

Examples:
00
H20
107

W

↓

PACKAGE*

"A"	=	14-pin dual in-line silicone package (TO-116)
"B"	=	16-pin dual in-line silicone package
"F"	=	14-16 pin cerdip
"N"	=	24-lead dual in-line silicone package
"Q"	=	24-pin ceramic flat-pak
"W"	=	14-16 pin flat cerpac
"F"	=	24-pin ceramic dual in-line package

*Availability of a circuit device in a particular package and temperature range is indicated on the appropriate device. Electrical Characteristics Data Sheet is shown in Section 2 of this handbook.

Manufacturer reserves the right to make design and process changes and improvements.

INTRODUCTION TO SIGNETICS LS

FEATURES OF LOW POWER SCHOTTKY TTL

Low Power, High Speed Operation

- 7ns typical gate propagation delay time (avg.)
- 2mw per gate power dissipation at 50% duty cycle — speed-power product = 19 picojoules typ.
- 45 MHz typical J-K Flip-Flop maximum clock frequency (D.C. coupled)

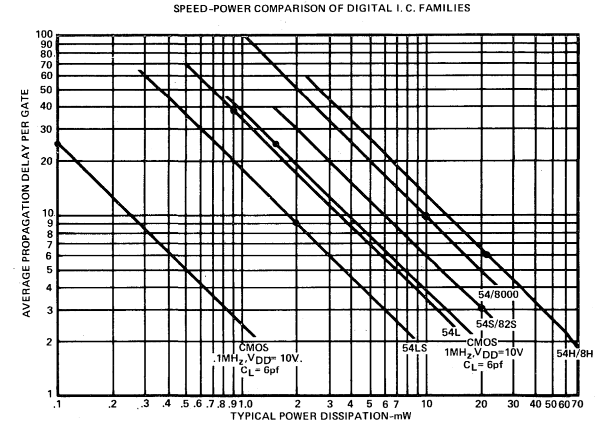
54/74 TTL performance at one fifth the power makes it possible to reduce size and cost of power supplies and eliminate cooling fans in 7400 type system designs. Manufacturing costs can be reduced by up to $.10 per package by using Signetics Low Power Schottky in place of 54/74. The speed-power characteristics of Low Power Schottky are also such that many systems previously designed with a combination of 54/74 and 54L/74L can be immediately upgraded with 54LS/74LS resulting in little or no increase in power and possible reduction in component cost.

Fully Compatible with Other TTL Families

- Fan out of 5 7400 (2.5 5400) inputs or 4 74S/74H (2 54S/54H) loads.
- Low input current (.36 mA max) zero level input current.
- Pin, function speed compatible with 54/74.

Low Power Schottky has sufficient drive capability to interface with other TTL families in most applications without the need for buffer circuits. Thus it is possible to upgrade designs to Low Power Schottky as functions become available, using 5400/7400 functtions where 54LS/74LS functions aren't yet available. The low input currents of Low Power Schottky make it an ideal interface between TTL compatible MOS devices and other systems.

SPEED-POWER COMPARISON OF DIGITAL I. C. FAMILIES



Notes: 1. Dots represent actual operating points
2. Diagonal lines represent constant power/speed product curves

Figure 1

The high output current capability of 54LS/74LS Low Power Schottky enables it to drive a wide range of capacitive loads with minimum affect on device performance. This low impedance output characteristic also enables Low Power Schottky to drive reasonably long lines (up to 36 inches) without the need for terminated, controlled impedance lines.

ADVANTAGES OF LOW POWER SCHOTTKY

Circuit Density

74LS is fabricated using a thin epitaxial process to reduce parasitic capacitance. Low internal currents permit design of transistor geometries and metal widths to be the smallest allowable using state of the art mask and fabrication techniques. Further circuit density improvements are made by the use of ion implanted resistors. Greater than five times reduction in resistor geometries is made possible by this technique. A comparison of 5400/7400 geometries versus 54LS/74LS geometries is shown in Figure 2. These techniques result in Low Power Schottky die areas being 60 to 75 percent the area of the equivalent 5400/7400 function. For example, the die size of the 54LS/74LS181 4-bit ALU is:

72 mils by 84 mils or 6048 square mils versus 90 mils by 92 mils, or 8280 square mils for the 54181/74181, or 75 percent of the area.

Future Trends

High circuit density, high speed and low power make Signetics Low Power Schottky a natural choice for high performance bipolar LSI designs such as microprocessors and large custom logic blocks. An example of an LSI product that has been developed by Signetics is a custom logic chip containing 270 equivalent logic gates on a 140x160 mil chip containing 1,590 components. This design resulted in a 40% improvement in performance, 80% reduction in power and 2:1 reduction in manufacturing cost. (see Table 1)

Table 1
COMPARISON OF TTL LSI VS. STANDARD TTL

	LSI	STD
Packages	1	26
Equivalent Gates	270	270
Power Dissipation	.65 watts	2.7 watts
Power/Gate	2.4 mW typ.	10.0 mW typ.
Speed	7ns/gate typ.	12ns /gate typ.

Thermal Considerations

TTL technology has now reached the level where maximum circuit complexity is often limited by package power capabilities. When standard TTL circuit designs are done with Low Power Schottky, circuit complexities can increase by a factor of five greater than standard designs without exceeding package power limitations as shown by Table 2.

Low Power Schottky's reduced power can also have a significant impact on component reliability in a system. For example, if we compare the reliability of a typical MSI function in a system with an operating ambient temperature of 55°C a four times improvement in component failure rate can result from the lower junction temperature of a Low Power Schottky function versus a standard 5400/7400 function. The Table 3 below and Figure 3 show a specific example of this improvement.

DEVICE SIZE COMPARISON

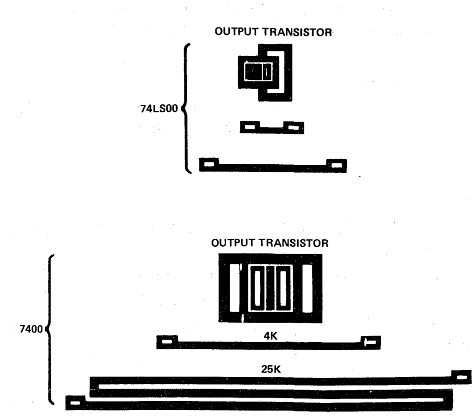


Figure 2

Table 2

	Military	Commercial
Maximum junction temperature	175°C	150°C
Maximum ambient temperature	125°C	70°C
Allowable thermal rise ambient to junction	50°C	80°C
Maximum allowable power dissipation	330 mw plastic[1] 500 mw Cerdip[2]	500 mw plastic[1] 800 mw Cerdip[2]
Maximum numbers of 5400 gates (at 10 mw/gate)	33 plastic 50 Cerdip	50 plastic 80 Cerdip
Maximum number of 54LS gates (at 2 mw/gate)	165 plastic 250 Cerdip	250 plastic 400 Cerdip

1 θ_{ja} for plastic = 160° C/watt (16 pin) 2 θ_{ja} for Cerdip = 100° C/watt (16 pin)

Table 3

	Standard 54/74	54/74LS
Device Power	250mW	50 mW
Thermal impedance	150°C/watt	160°C/watt
Thermal rise	40°C	8°C
Junction temperature	95°C	63°C
Reliability factor*	22.5	5

$$\text{*The reliability factor} = \frac{\text{Failure rate at operating junction temperature}}{\text{Failure rate at 25°C junction temperature}}$$

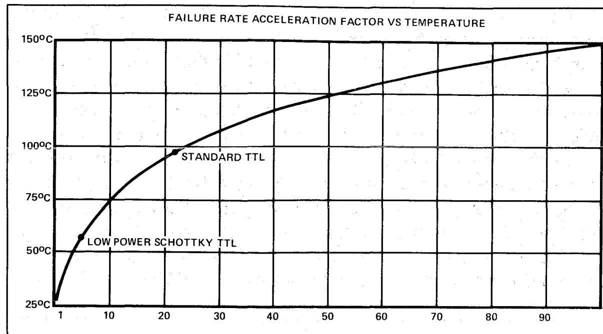


Figure 3

COST REDUCTION

In comparing the cost of designing a system with a particular logic family, the project engineer should compare the total cost including reductions in manufacturing cost which may offset higher prices of a particular family. With low power logic, the cost savings associated with smaller, lower cost power supplies can be significant. As an example, a comparison will be made for the same system, using 54/74 logic, 54/74LS logic, CMOS logic and 54/74L. For purposes of comparison, a controller will be used. It consists of 500 packages, 200 quad NAND gates, 150 dual type D flip-flops and 150 presettable decade counters. It will be assumed that half of the system will operate at 200 kHz and half at 1 MHz. The CMOS system will operate at V_{DD} = 10 Volts with 15 pf. capacitance on each output. The part types used are shown in table 4.

Table 4

DEVICE	QUANTITY	54/74LS TYPE	STD TYPE	CMOS TYPE
Quad NAND Gate	200	54/74LS00	54/7400	4011
Dual D Flip-Flop	150	54/74LS74	54/7474	4013
Presettable Counter	150	54/74LS196	8280	4018

Table 5
DEVICE POWER REQUIREMENTS — Per Package (mW)

	54/74LS	STD TTL	CMOS	54/74L
Quad NAND Gate	8mW	40mW	Static-.05μWatt 200kHz-2.4mW 1MHz-10mW	4mW
Dual D Flip-Flop	20mW	85mW	Static-.2μWatt 200kHz-1.2mW 1MHz-4mW	10mW
Presettable Counter	60mW	185mW	Static-10μWatts 200kHz-1.2mW 1MHz-7mW	30mW

Table 6
SYSTEM POWER CONSUMPTION

		54/74LS	STD TTL	CMOS	54/74L
Gates	Static	1.6watts	8watts	.01mW	.8watts
	Dynamic	1.6watts	8watts	1.3watts	.8watts
Flip-Flops	Static	3watts	12.8watts	.03mW	1.5watts
	Dynamic	3watts	12.8watts	.4watts	1.5watts
Counters	Static	3watts	27.8watts	1.5watts	4.5watts
	Dynamic	9watts	27.8watts	.4watts	4.5watts
Total	Static	13.6watts	48.6watts	1.5mW	6.8watts
	Dynamic	13.6watts	48.6watts	2.1watts	6.8watts
Cost of Power	Static	$13.60	$48.60	0	$6.80
	Dynamic	$13.60	$48.60	$2.10	$6.80
Cost of Power Per Package		$.027	$.097	$.004	$.014

*Assume Power Costs $1.00 Per Watt.

Although standard TTL is the lowest priced logic available today, and probably will be for some time to come, Signetics Low Power Schottky is the *most cost effective* form of logic to design your system with. Low Power Schottky prices are rapidly approaching 7400 as shown by Figure 4. Over the production life of your system, Low Power Schottky will result in the lowest overall manufacturing cost. If you are presently using low power TTL in your design you can affect an immediate cost reduction by replacing it with Low Power Schottky. Similarly, before designing a system with CMOS for lowest power supply costs, compare prices with Low Power Schottky. The difference in price may well offset the power supply savings. You also don't have the easy upgradability with CMOS.

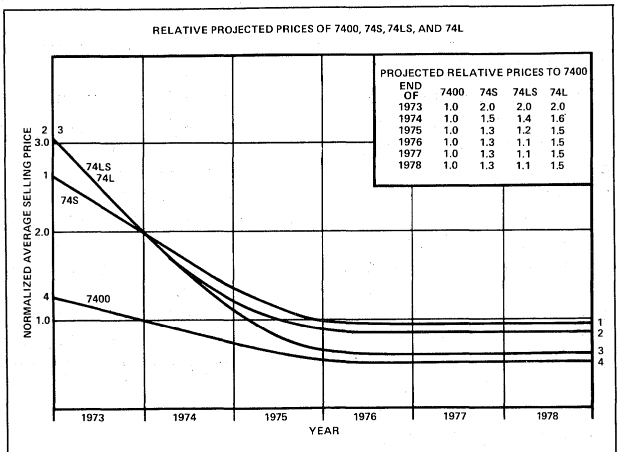


Figure 4

UPGRADING A SYSTEM TO LOW POWER SCHOTTKY

To verify that 54/74LS can be plugged directly into a 54/74 system design, an experiment was conducted using an actual operating system. The system used for the experiment was a communications adapter that is designed to plug into a mini-computer frame. The board contains 103 TTL packages of which two thirds were MSI. All of the 7400 gates and flip-flops were replaced with equivalent 74LS types. System operation was not affected by the use of 74LS in place of 7400 in these sockets. In fact, in addition to the five to one reduction in power requirements for the devices replaced, the system power supply noise was reduced 25% from 80 millivolts to 60 millivolts as shown by Figure 5.

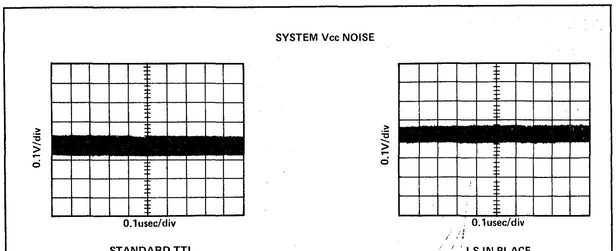


Figure 5

Based on results from this experiment and the characteristic data shown in the section on electrical characteristics, it is concluded that by observing a few simple guidelines, any system can be easily upgraded from 7400 to 74LS resulting in significant reduction in power consumption, system cooling requirements, and improved component reliability in the system.

DESIGN RULES FOR UPGRADING 54/74 SYSTEM TO 54/74LS

1. Check fan out requirements at each output node where a 54/74LS device may have to drive a 54/7400 device. Do not exceed 5 7400 loads or 2.5 5400 loads.
2. Check system set up and hold times for sequential functions to assure that data is available at the correct time for Low Power Schottky functions. These specifications are sometimes slightly different for 54/74LS types than they are for the corresponding 54/74 type.
3. Use standard 54/74 where it is necessary to drive heavy capacitive loads greater than 100pf—150pf.

Three benefits can be derived from the ability to upgrade 5400/7400 designs to 54/74LS.

1. The ability to immediately eliminate thermal heating problems in systems where it has been necessary to put a lot of logic in a small package such as terminals, point of sale systems, etc. A substantial reduction in heat generation can be affected by simply plugging in 54/74LS.
2. Reduced power supply cost.
3. Upgrade system capability by adding plug in logic boards without having to redesign the power supply.

DESIGN RULES FOR UPGRADING 54/74L SYSTEM TO 54/74LS

1. Check power supply capability. 54/74LS SSI functions consume approximately twice the power of 54/74LS SSI. However, a great many systems are a mix of 54/74L and standard 54/74. In these systems total power can often be reduced by replacing both the standard 54/74 and the 54L/74L with 54/74LS.
2. Check loading rules. The loading rules for 54/74L are almost identical to 54/74LS (See Tables 8 & 9). Generally, the only areas of concern are inputs from non-TTL elements such as linear devices, MOS, memories, CMOS or other devices with limited drive capability.
3. Check system timing. 54/74LS logic is much faster than 54/74L. Therefore, the designer should verify that no race conditions will be created which could affect system operation.

BENEFITS FROM REPLACING 54/74L WITH 54/74LS

1. Cost reduction — 54/74LS is less expensive than 54/74L. The cost difference will become even more significant in the future. (See Figure 4).
2. Availability — 54/74L is an obsolete logic family. Future availability of these devices could be a problem as IC manufacturers phase out production.
3. Inventory — By placing both 54/74 and 54/74L with 54/74LS, the total number of different devices to be tested and stored can be reduced.

CIRCUIT DESIGN

The standard gate circuit for the Signetics 54/74LS00 is shown in Figure 6. The threshold level is set at 1.5V at 25°C by the three base emitter diodes up from ground minus the input diode. This threshold provides a zero level noise immunity of 1.5—0.3 = 1.2V at 25°C by substracting the low output level of the driving gate. At 125°C the noise immunity becomes 1.05—0.20 = .85V which is the worst case zero level. The worst case "one" level noise immunity is V_{OH}—V_{THRESH} or 2.80—1.70 = 1.10V at −55°C. This circuit allows the guarantee of 0.8V for low level input voltage over the −55° to +125°C temperature range including open collector inverters specified at 100 micro amps high level output current. The combination of high threshold and fast turn-on speed is achieved with "kicker" transistor Q_2 which supplies an initial current surge during turn-on. D_3 also helps turn-on by supplying a quick discharge path of the IOS transistor Q_6. The active pull down circuit consisting of Q_4, R_6, and R_7, provides a good V_{in} vs V_{out} characteristic for best noise immunity. The IOS resistor R_3 is low at 120 ohms. The IOS current is typically 30mA which makes it near the capability of standard 7400 in charging highly capacitive bus lines. The base drive to the output transistor Q_5 is at least 0.3mA. With a typical beta of 40 the output sink current will generally be more than 12 mA through a collector resistance of 20 ohm.

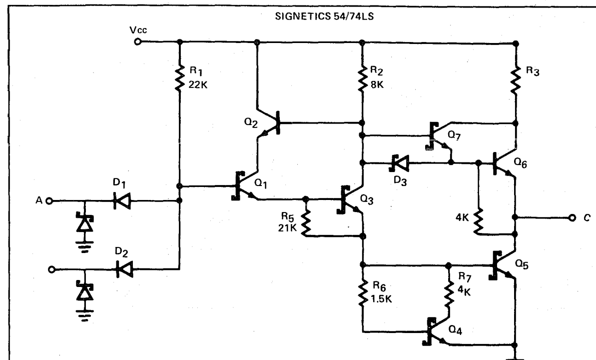


Figure 6

D.C. CHARACTERISTICS

Low Power Schottky has basically the same input and output voltage levels as standard TTL. Input current requirements are reduced to −0.36mA for logic "0" state and 20μa for logic "1" state. Output currents are also reduced to 4mA/8mA for 54/74LS in logic "0" state and −400μA for logic "1" state. Table 7 shows the d.c. characteristics for both 54/74LS and 54/74.

Table 7

PARAMETER		54LS	74LS	54	74	UNIT
V_{IH}	High level input voltage	2 (min)	2 (min)	2 (min)	2 (min)	V
V_{IL}	Low level input voltage	0.8 (max)	0.8 (max)	0.8 (max)	0.8 (max)	V
V_{OH}	High level output voltage	2.5 (min)	2.7 (min)	2.4 (min)	2.4 (min)	V
V_{OL}	Low level output voltage	0.4 (max)	0.5 (max)	0.4 (max)	0.4 (max)	V
I_{IH}	High level input current	20 (max)	20 (max)	40 (max)	40 (max)	μA
I_{IL}	Low level input current	−0.36 (max)	−0.36 (max)	−1.6 (max)	−1.6 (max)	mA
I_{OH}	High level output current	−400 (min)	−400 (min)	−400 (min)	−400 (min)	μA
I_{OL}	Low level output current	4 (min)	8 (min)	16 (min)	16 (min)	mA

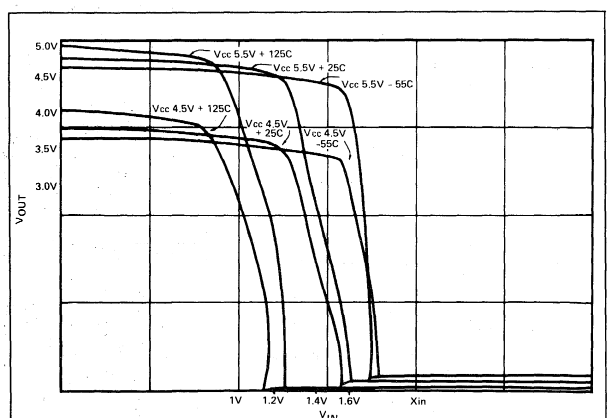


Figure 7

DC NOISE MARGIN

54/74LS devices have slightly higher minimum logic "1" output voltage while maintaining the same maximum logic "1" input voltage, therefore noise margin for 54/74LS in the logic "1" state is improved over that of 54/74. Noise margin in logic "0" state remains the same except for 74LS devices, which have a maximum of 0.5V output, instead of 0.4V, thus have a reduction of 100mv in logic "0" state. Table 8 shows the noise margin for both families.

Table 8 D.C. NOISE MARGIN (VOLTS)

	54	74	54LS	74LS
Logic "1"	0.4	0.4	0.7	0.5
Logic "0"	0.4	0.4	0.4	*0.3

*74LS NOISE MARGIN IS 0.4V at 4ma out (11 loads)

UNUSED INPUTS OF POSITIVE AND/NAND GATES

For optimum switching times and minimum noise susceptibility, unused inputs of AND or NAND gates should be maintained at a voltage greater than 2.7V, but not exceed the absolute maximum rating of 5.5V. This eliminates the distributed capacitance associated with the floating input, bond wire, and package lead, and ensures that no degradation will occur in the propagation delay times.

Possible ways of handling unused inputs are:

1. Connect unused inputs to an independent supply voltage. Preferably this voltage should be between 2.7V and 3.5V.
2. Connect unused inputs to a used input if maximum fan-out of the driving output will not be exceeded. Each additional input presents a full load to the driving output at a high level voltage but adds no loading at a low level voltage.
3. Connect unused inputs to V_{CC} through a 1K ohm resistor so that if a transient which exceeds the 5.5V maximum rating should occur, the impedance will be high enough to protect the input. One to 25 unused inputs may be connected to each 1K ohm resistor.
4. Connect unused inputs to the output of an inverter that has its input grounded.
5. Inputs with a maximum rating of 7V may be tied directly to VCC.

LOGIC

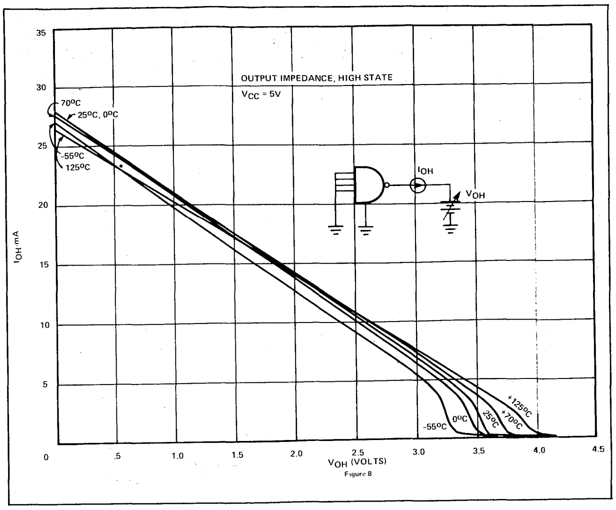


Figure 8

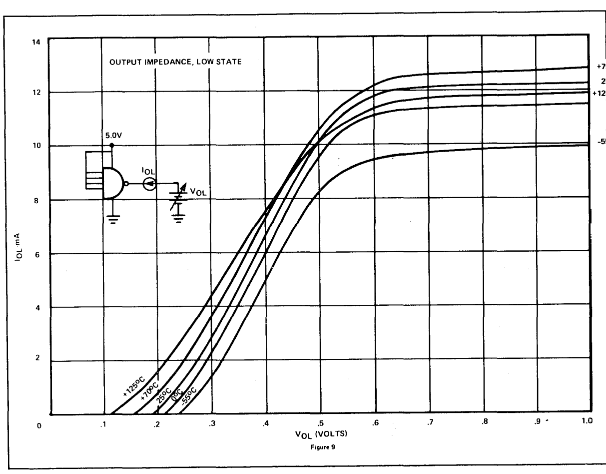


Figure 9

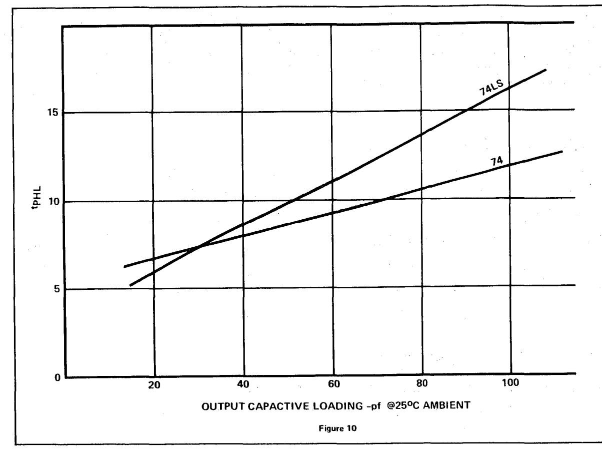


Figure 10

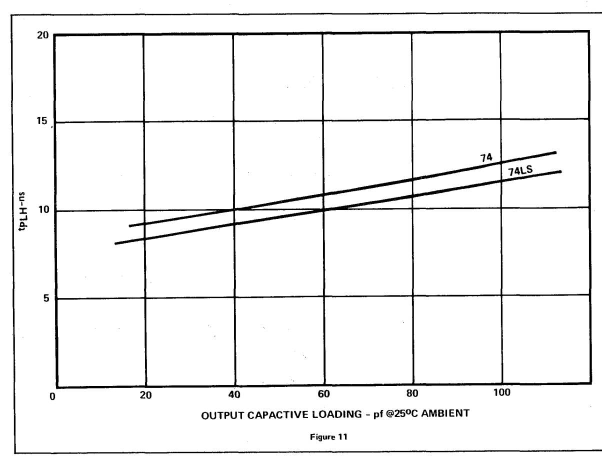


Figure 11

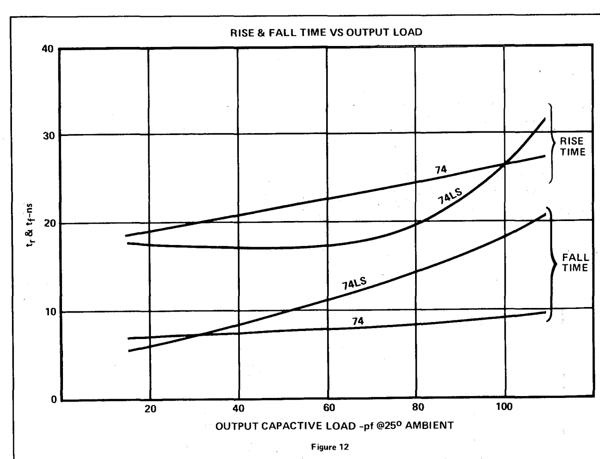


Figure 12

A.C. CHARACTERISTICS

Fig. 10 to 14 illustrate the propagation delays, rise and fall times, and AC over temperature. The LS devices display similar transfer characteristics as standard TTL and meet all the worst case conditions. Propagtion delays are similar on turn off and faster on turn on. Edge speed is generally slower in LS than standard, thus creates less cross-talk, V_{CC} noise, etc.

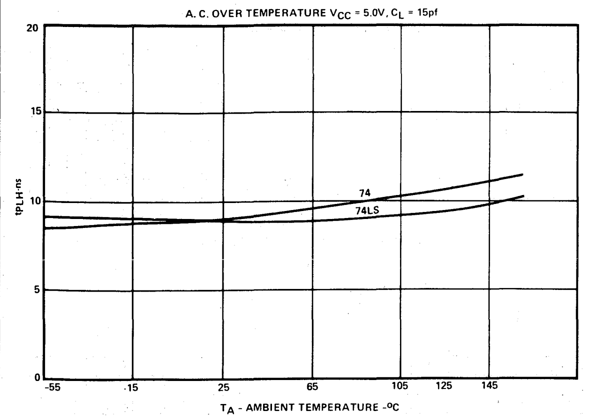


Figure 13

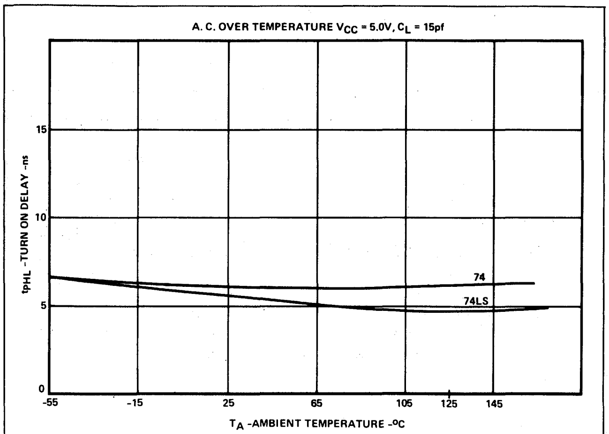


Figure 14

DESIGN GUIDELINES

Fanout Capabilities

Low Power Schottky has high fan-out capabilities both in the logic "0" and logic "1" state. Within the family Low Power Schottky can fan-out to 22 in logic "0" state and 20 in logic "1" state.

Fan-out capability is calculated by dividing the output current of the driving gate by the input current of the driven gate. For example, if a 74 gate is driving another 74 gate, the fan-out capability would be:

$$\text{F.O.} = \frac{400\mu a}{40\mu a} = 10 \text{ for logic "1" state} \quad \text{and} \quad \text{F.O.} = \frac{16ma}{1.6ma} = 10 \text{ for logic "0" state}$$

Referring to Table 7 for current requirements, we can calculate the fan-out for 54/74LS and 54/74 families. Tables 9 and 10 show the fan-out capabilities between these two families.

TABLE 9
FANOUT (0°—70°C) LOGIC 1/LOGIC 0
DRIVING GATES

	74	74L	74LS
74	10/10	5/2	10/5
74L	40/89	20/20	40/44
74LS	20/44	10/10	20/22

DRIVEN GATES

TABLE 10
FANOUT (−55°C TO +125°C) LOGIC 1/LOGIC 0
DRIVING GATES

	54	54L	54LS
54	10/10	2/1	10/2
54L	40/89	10/11	40/22
54LS	20/44	5/5	20/11

DRIVEN GATES

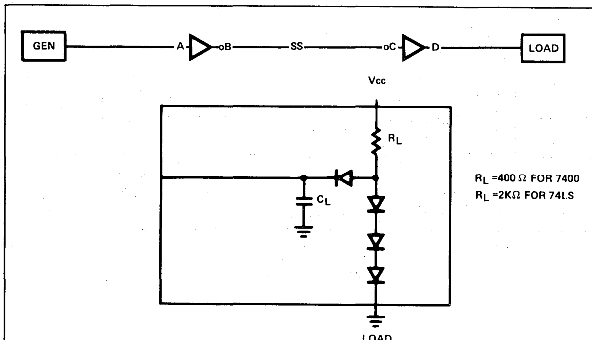
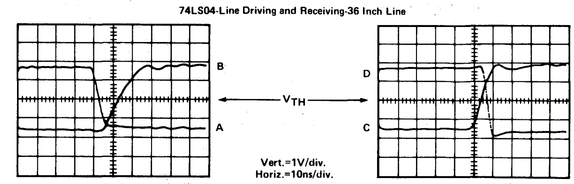


Figure 15

LINE DRIVING AND RECEIVING

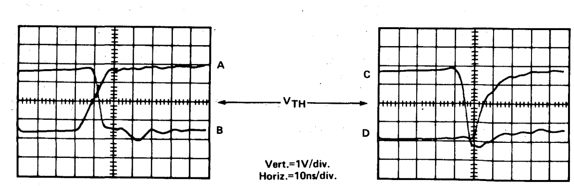
The Low Power Schottky displays similar line driving and receiving capability as the standard TTL logic. Low Power Schottky is slightly more sensitive to the transmission line effect when driving longer lines due to the low output impedance of the circuit. Figures 15 through 22 show the driving and receiving capability of the LS and standard TTL over 12 and 36 inch lines. Even though the LS is more sensitive to transmission line effects, the point to be noted is that the LS output of the receiver display has a much cleaner waveform than the standard logic. The ringing effect of the standard logic is almost negligible in the LS. Test configuration is shown as follows with V_{CC} = 5.0V, T_A = 25°C, and C_L = 15pf.

74LS04-Line Driving and Receiving-36 Inch Line



Input Pulse-Negative Going
Total Propagation Delay=14ns+Line Delay

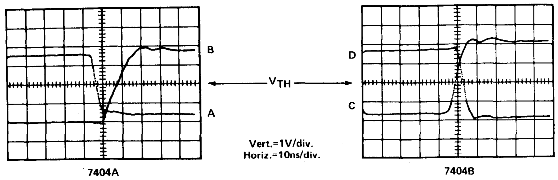
Figure 16



Input Pulse-Positive Going
Total Propagation Delay=15ns+Line Delay

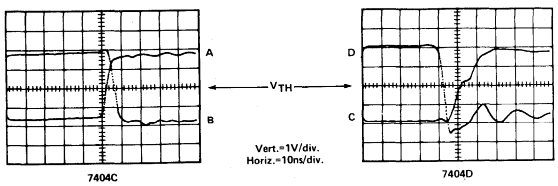
Figure 17

7404-Line Driving and Receiving-36 Inch Line



Input Pulse-Negative Going
Total Propagation Delay=15.5ns+Line Delay

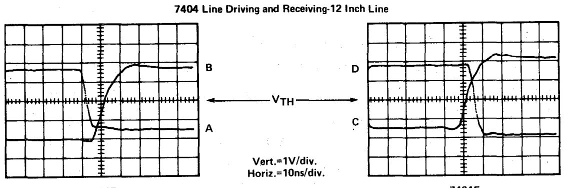
Figure 18



Input Pulse-Positive Going
Total Propagation Delay=15ns+Line Delay

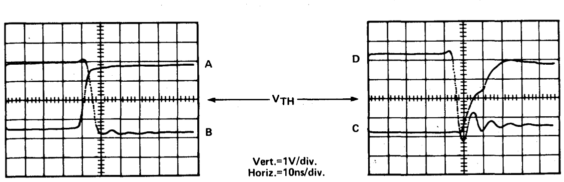
Figure 19

7404 Line Driving and Receiving-12 Inch Line



Input Pulse-Negative Going
Total Propagation Delay from A to D-13.5ns+Line Delay

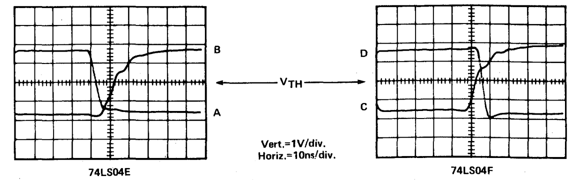
Figure 20



Input Pulse-Positive Going
Total Propagation Delay from A to D-12.5ns Line Delay

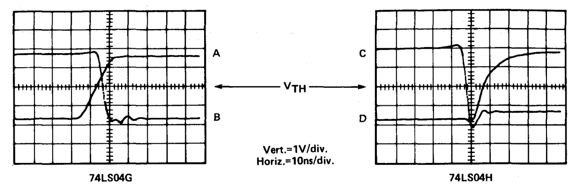
Figure 21

74LS04-Line Driving and Receiving-12 Inch Line



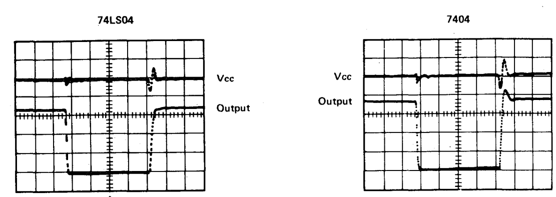
Input Pulse-Negative Going
Total Propagation Delay=13ns+Line Delay

Figure 22



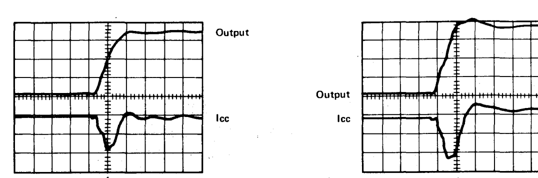
Input Pulse-Positive Going
Total Propagation Delay=13ns+Line Delay

Figure 23



C_L = 25pf Vcc = 0.5V/div. Output = 1.0V/div.

Figure 24



C_L = 25pf Output = 1.0V/div. Icc = 4ma/div. t = 20ns/div.

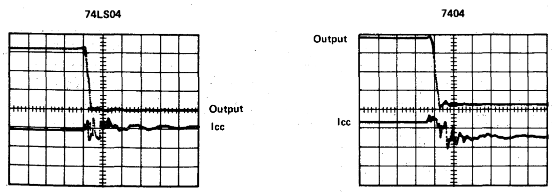
Figure 25

POWER SUPPLY CONSIDERATIONS

Decoupling

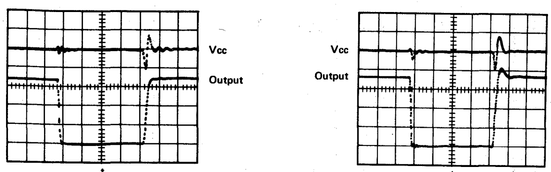
Current spiking and V_{CC} noise are generated internally within the circuits due to overlap in conduction of the upper and lower transistors in the totem pole outputs, the difference in Icc_H and Icc_L and the changing of load capacitances. The power supply decoupling rules for standard TTL apply to Low Power Schottky also, i.e. 0.0lufd per synchronously driven gate and at least 0.1ufd per 20 gates regardless of synchronization.

Figure 24 to 29 display the current spikes and V_{CC} noise generated by a 7404 and 74LS04 with two different capacitive loading @ V_{CC} = 5.0V and TA = 25°C. In both cases, the LS device generates less V_{CC} noise and smaller current spikes for 25 pf. and 50 pf. capacitive loading. This is because Low Power Schottky generally switches approximately 25% of the current as a standard TTL would, thus less current spiking and less V_{CC} noise generated.



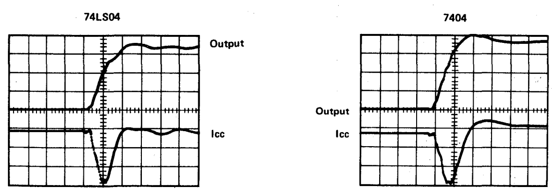
C_L = 25pf Output = 1.0V/div. Icc = 2ma/div. t = 20ns/div.

Figure 26



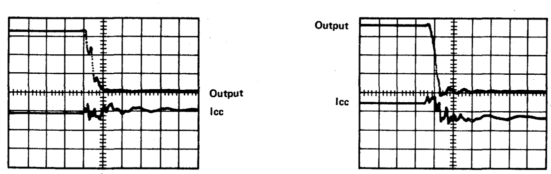
C_L = 50pf Output = 1.0V/div. Vcc = 0.5V/div.

Figure 27



C_L = 50pf Output = 1.0Vdiv. Icc = 4ma/div. t = 20ns/div.

Figure 28



C_L = 50pf Output = 1.0V/div. Icc = 2ma/div. t = 20ns/div.

Figure 29

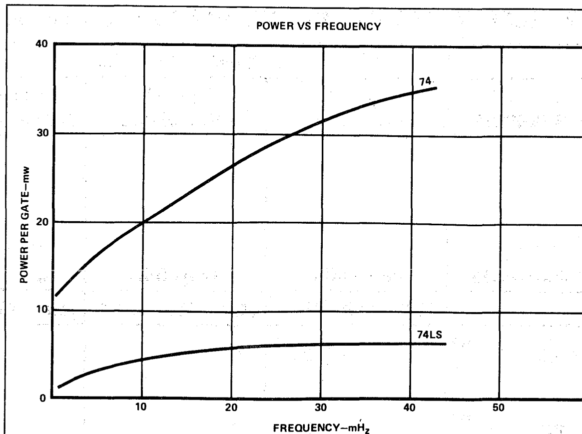


Figure 30

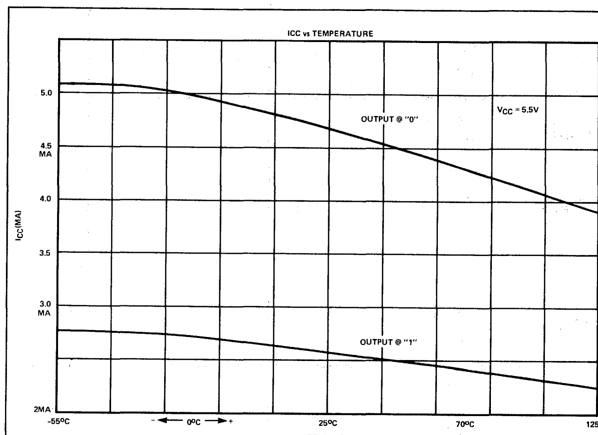


Figure 31

ON-BOARD REGULATION

In most digital systems, there is a large current requirement, and the current supplied usually comes from a main supply. TTL logic tends to generate current spikes during switching due to the overlap in conduction of both upper and lower transisters, thus creating V_{CC} noise. An on-board voltage regulator could be used not only to regulate the power supplied to the circuits on-board, but also would isolate the noise otherwise propagated to the rest of the system. Systems designed using this technique would not need tight regulation on the main power supply.

Most voltage regulator circuits can supply up to 1 Amp of current. For systems with large boards (150 or more IC's), two or three regulator circuits might be needed to supply enough current to standard TTL logic. However, for Low Power Schottky systems, one regulator per board should be sufficient. This represents approximately 1 cent per package of Low Power Schottky vs 5 cents per package for standard TTL for large boards.

LOGIC

54/74 ELECTRICAL CHARACTERISTICS (See Notes - Page 50)

PARAMETER	INPUT VOLTAGE									OUTPUT VOLTAGE						INPUT CURRENT		
	V_{IL} (V) LOW LEVEL			V_{IH} (V) HIGH LEVEL			V_{IC} (V) CLAMP VOLTAGE			V_{OL} (V) LOW LEVEL			V_{OH} (V) HIGH LEVEL			I_{IL} (mA) LOW LEVEL		
TEST CONDITIONS	V_{CC}=MIN			V_{CC}=MIN			V_{CC}=MIN $I_I = -12$ mA			V_{CC}=MIN V_{IN}=* I_{OL}=16mA V_{OL}=0.4V			V_{CC}=MIN V_{IN}=* I_{OH}=-400μA			V_{CC}=MAX V_{IN}=0.4V		
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
54/7400 54 / 74			0.8	2					-1.5		0.22	0.4	2.4	3.3				-1.6
54/7401 54 / 74			0.8	2					-1.5			0.4						-1.6
54/7402 54 / 74			0.8	2					-1.5		0.22	0.4	2.4	3.3				-1.6
54/7403 54 / 74			0.8	2					-1.5			0.4						-1.6
54/7404 54 / 74			0.8	2					-1.5		0.22	0.4	2.4	3.3				-1.6
54/7405 54 / 74			0.8	2					-1.5			0.4						-1.6
54/7406 54 / 74			0.8	2					-1.5	I_{OL}=30mA(54) I_{OL}=40mA(74)		0.4 / 0.7						-1.6
54/7407 54 / 74			0.8	2					-1.5	I_{OL}=30mA(54) I_{OL}=40mA(74)		0.4 / 0.7						-1.6
54/7408 54 / 74			0.8	2					-1.5		0.22	0.4	I_{OH}=-800μA 2.4	3.3				-1.6
54/7409 54 / 74			0.8	2					-1.5			0.4						-1.6
54/7410 54 / 74			0.8	2					-1.5		0.22	0.4	2.4	3.3				-1.6
54/7411 54 / 74			0.8	2					-1.5		0.22	0.4	I_{OH}=-800μA 2.4	3.3				-1.6
54/7413 54 / 74	See Data Sheet			See Data Sheet					-1.5		0.22	0.4	I_{OH}=-800μA 2.4	3.3			-1	-1.6
54/7414 54 / 74	See Data Sheet			See Data Sheet					-1.5		0.22	0.4	I_{OH}=-800μA 2.4	3.3			-0.8	-1.2

		INPUT CURRENT						POWER SUPPLY CURRENT											
PARAMETER		I_{IH} (μA) HIGH LEVEL			I_I (mA) INPUT CURRENT			I_{OS} (mA) SHORT CIRCUIT			I_{CCL} (mA) LOW LEVEL			I_{CCH} (mA) HIGH LEVEL			I_{OH} (μA) REVERSE		
TEST CONDITIONS		V_{CC}=MAX V_{IN}=2.4V			V_{CC}=MAX V_{IN}=5.5V			V_{CC}=MAX			V_{CC}=MAX V_{IN}=5V			V_{CC}=MAX V_{IN}=0V			V_{CC}=MIN V_{IN}=* V_{OH}=5.5V		
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
54/7400	54 74			40			1	-20 -18		-55 -55		12	22		4	8			
54/7401	54 74			40			1					12	22		4	8			250
54/7402	54 74			40			1	-20 -18		-55 -55		14	27		8	16			
54/7403	54 74			40			1					12	22		4	8			250
54/7404	54 74			40			1	-20 -18		-55 -55		18	33		6	12			
54/7405	54 74			40			1					18	33		6	12			250
																		V_{OH}=30V	
54/7406	54 74			40			1					27	38		30	42			250
												V_I=0V			V_I=5V			V_{OH}=30V	
54/7407	54 74			40			1					21	30		29	41			250
												V_{IN}=0V			V_{IN}=5V				
54/7408	54 74			40			1	-20 -18		-55 -55		18	26		10	15			
												V_I=0V			V_I=5V				
54/7409	54 74			40			1					18	26		10	15			250
54/7410	54 74			40			1	-20 -18		-55 -55		9	16.5		3	6			
												V_{IN}=0V			V_{IN}=5V				
54/7411	54 74			40			1	-20 -18		-55 -55		13.5	20		7.5	12			
54/7413	54 74			40			1	-18		-55		20	32		14	23			
												V_{IN}=4.5V							
54/7414	54 74			40			1	-18		-55		39	60		22.2	36			

54/74 ELECTRICAL CHARACTERISTICS (See Notes - Page 50)

		INPUT VOLTAGE									OUTPUT VOLTAGE						INPUT CURRENT		
PARAMETER		V_{IL} (V) LOW LEVEL			V_{IH} (V) HIGH LEVEL			V_{IC} (V) CLAMP VOLTAGE			V_{OL} (V) LOW LEVEL			V_{OH} (V) HIGH LEVEL			I_{IL} (mA) LOW LEVEL		
TEST CONDITIONS		V_{CC}=MIN			V_{CC}=MIN			V_{CC}=MIN I_I= −12 mA			V_{CC}=MIN V_{IN}=* I_{OL}=16mA V_{OL}=0.4V			V_{CC}=MIN V_{IN}=* I_{OH}=-400μA			V_{CC}=MAX V_{IN}=0.4V		
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
54/7416	54 74			0.8	2					-1.5	I_{OL}=30mA(54) I_{OL}=40mA(74)		0.4 0.7						-1.6
54/7417	54 74			0.8	2					-1.5	I_{OL}=30mA(54) I_{OL}=40mA(74)		0.4 0.7						-1.6
54/7420	54 74			0.8	2					-1.5		0.22	0.4	2.4	3.3				-1.6
54/7421	54 74			0.8	2					-1.5		0.22	0.4	I_{OH}=-800μA 2.4	3.3				-1.6
54/7426	54 74			0.8	2					-1.5			0.4						-1.6
54/7427	54 74			0.8	2					-1.5		0.22	0.4	I_{OH}=-800μA 2.4	3.3				-1.6
54/7428	54 74			0.8	2					-1.5	I_{OL}=48mA	0.26	0.4	I_{OH}=-2.4mA 2.4	3.3				-1.6
54/7430	54 74			0.8	2					-1.5		0.22	0.4	2.4	3.3				-1.6
54/7432	54 74			0.8	2					-1.5		0.22	0.4	I_{OH}=-800μA 2.4	3.3				-1.6
54/7433	54 74			0.8	2					-1.5	I_{OL}=48mA		0.4						-1.6
54/7437	54 74			0.8	2					-1.5	I_{OL}=48mA	0.22	0.4	I_{OH}=-1.2mA 2.4	3.3				-1.6
54/7438	54 74			0.8	2					-1.5	I_{OL}=48mA	0.22	0.4						-1.6
54/7439	54 74			0.8	2					-1.5	I_{OL}=48mA	0.22	0.4						-1.6

	INPUT CURRENT						POWER SUPPLY CURRENT												
PARAMETER	I_{IH} (μA) HIGH LEVEL			I_I (mA) INPUT CURRENT			I_{OS} (mA) SHORT CIRCUIT			I_{CCL} (mA) LOW LEVEL			I_{CCH} (mA) HIGH LEVEL			I_{OH} (μA) REVERSE		
TEST CONDITIONS	V_{CC}=MAX V_{IN}=2.4V			V_{CC}=MAX V_{IN}=5.5V			V_{CC}=MAX			V_{CC}=MAX V_{IN}=5V			V_{CC}=MAX V_{IN}=OV			V_{CC}=MIN V_{IN}=* V_{OH}=5.5V		
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
54/7416 54 74			40			1					27	38		30	42		V_{OH}=15V	250
54/7417 54 74			40			1					V_I=OV 21	30		V_I=5V 29	41		V_{OH}=15V	250
54/7420 54 74			40			1	-20 -18		-55 -55		6	11		2	4			
54/7421 54 74			40			1	-20 -18		-55 -55		V_{IN}=0V 9	13		V_{IN}=5V 5	8			
54/7426 54 74			40			1					12	22		4	8		V_{OH}=12V V_{OH}=15V	50 1000
54/7427 54 74			40			1	-20 -18		-55 -55		16	26		10	16			
54/7428 54 74			40			1	-70		-180		33	57		12	21			
54/7430 54 74			40			1	-20 -18		-55 -55		3	6		1	2			
54/7432 54 74			40			1	-20 -18		-55 -55		V_{IN}=OV 23	38		V_{IN}=5V 15	22			
54/7433 54 74			40			1					6.9	13.8		1.8	3.6			250
54/7437 54 74			40			1	-20 -18		-55 -55		34	54		9	15.5			
54/7438 54 74			40			1					34	54			8.5			250
54/7439 54 74			40			1					34	54			8.5			250

54/74 ELECTRICAL CHARACTERISTICS (See Notes - Page 50)

PARAMETER		INPUT VOLTAGE									OUTPUT VOLTAGE						INPUT CURRENT		
		V_{IL} (V) LOW LEVEL			V_{IH} (V) HIGH LEVEL			V_{IC} (V) CLAMP VOLTAGE			V_{OL} (V) LOW LEVEL			V_{OH} (V) HIGH LEVEL			I_{IL} (mA) LOW LEVEL		
TEST CONDITIONS		V_{CC}=MIN			V_{CC}=MIN			V_{CC}=MIN $I_I=-12$ mA			V_{CC}=MIN V_{IN}=* I_{OL}=16 mA V_{OL}=0.4V			V_{CC}=MIN V_{IN}=* $I_{OH}=-400\mu A$			V_{CC}=MAX V_{IN}=0.4V		
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
											I_{OL}=48mA			I_{OH}=-1.2mA					
54/7440	54 74			0.8	2							0.28	0.4	2.4	3.3				-1.6
														$I_{OH}=-800\mu A$					
54/7442A	54 74			0.8	2					-1.5			0.4	2.4					-1.6
54/7443	54 74			0.8	2					-1.5			0.4	2.4					-1.6
54/7444	54 74			0.8	2					-1.5			0.4	2.4					-1.6
54/7445	54 74			0.8	2					-1.5									-1.6
											I_{OL}=8mA			$I_{OH}=-200\mu A$			Any input except B1/RBO node		
7446A				0.8	2					-1.5		0.3	0.4	2.4	3.7				-1.6
											B1/RBO node			B1/RBO node			B1/RBO node		-4.2
											I_{OL}=8mA			$I_{OH}=-200\mu A$			Any input except B1/RBO node		
7447A				0.8	2					-1.5		0.3	0.4	2.4	3.7				-1.6
											B1/RBO node			B1/RBO node			B1/RBO node		-4.2
											I_{OL}=6.4 mA						Any output except		
54/7448	54 74			0.8	2					-1.5			0.4						
											outputs A-G		0.4	outputs A-G 2.4	4.2		B1/RBO node		-1.6
											I_{OL}=8mA B1/RBO node		0.4	$I_{OH}=-200\mu A$ B1/RBO node 2.4	3.7		B1/RBO node		-4.2
54/7450	54 74			0.8	2							0.22	0.4	2.4	3.3				-1.6
54/7451	54 74			0.8	2							0.22	0.4	2.4	3.3				-1.6
54/7453	54 74			0.8	2							0.22	0.4	2.4	3.3				-1.6
54/7454	54 74			0.8	2							0.22	0.4	2.4	3.3				-1.6
54/7460	54 74			0.8	2														-1.6

		INPUT CURRENT						POWER SUPPLY CURRENT											
PARAMETER		I_{IH} (μA) HIGH LEVEL			I_I (mA) INPUT CURRENT			I_{OS} (mA) SHORT CIRCUIT			I_{CCL} (mA) LOW LEVEL			I_{CCH} (mA) HIGH LEVEL			I_{OH} (μA) REVERSE		
TEST CONDITIONS		V_{CC}=MAX V_{IN}=2.4V			V_{CC}=MAX V_{IN}=5.5V			V_{CC}=MAX			V_{CC}=MAX V_{IN}=5V			V_{CC}=MAX V_{IN}=OV			V_{CC}=MIN V_{IN}=* V_{OH}=5.5V		
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
54/7440	54			40			1	-20		-70		17	27		4	6.8			
	74							-18		-70									
54/7442A	54			40			1	-20		-55		28	41						
	74							-18		-55		28	56						
54/7443	54			40			1	-20		-55		28	41						
	74							-18		-55		28	56						
54/7444	54			40			1	-20		-55		28	41						
	74							-18		-55		28	56						
54/7445	54			40			1					43	62						
	74											43	70						
7446A		Any input except B1/RBO node		40	Any input except B1/RBO node		1	B1/RBO node		-4			85						
													103						
7447A		Any input except B1/RBO node		40	Any input except B1/RBO node		1	B1/RBO node		-4			85						
													103						
54/7448	54	Any output except B1/RBO node		40	Any output except B1/RBO node		1			-4									
	74																		
54/7450	54			40			1	-20		-55		7.4	14		4	8			
	74							-18		-55									
54/7451	54			40			1	-20		-55		7.4	14		4	8			
	74							-18		-55									
54/7453	54			40			1	-20		-55		5.1	9.5		4	8			
	74							-18		-55									
74/7454	54			40			1	-20		-55		5.1	9.5		4	8			
	74							-18		-55									
54/7460	54			40			1					1.2	2.5		2	4			
	74																		

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54/74 ELECTRICAL CHARACTERISTICS (See Notes - Page 50)

		INPUT VOLTAGE									OUTPUT VOLTAGE						INPUT CURRENT		
PARAMETER		V_{IL} (V) LOW LEVEL			V_{IH} (V) HIGH LEVEL			V_{IC} (V) CLAMP VOLTAGE			V_{OL} (V) LOW LEVEL			V_{OH} (V) HIGH LEVEL			I_{IL} (mA) LOW LEVEL		
TEST CONDITIONS		V_{CC}=MIN			V_{CC}=MIN			V_{CC}=MIN $I_I = -12$ mA			V_{CC}=MIN V_{IN}=* I_{OL}=16mA V_{OL}=0.4V			V_{CC}=MIN V_{IN}=* I_{OH}=-400μA			V_{CC}=MAX V_{IN}=0.4V		
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
54/7470	54 74			0.8	2							0.22	0.4	2.4	3.5				J1,J2,J,K1, K2,K or clock -1.6 Preset or clear -3.2
54/7472	54 74			0.8	2							0.22	0.4	2.4	3.5				J1,J2,J3,K1, K2 or K3 -1.6 Preset, clear or clock -3.2
54/7473	54 74			0.8	2							0.22	0.4	2.4	3.5				J or K -1.6 Clear or clock -3.2
54/7474	54 74			0.8	2					-1.5		0.22	0.4	2.4	3.5				Preset or D -1.6 Clear or clock -3.2
54/7475	54 74			0.8	2					-1.5			0.4	2.4					D -3.2 Clock -6.4
54/7476	54 74			0.8	2					-1.5		0.22	0.4	2.4	3.5				J or K -1.6 Clear preset or clock -3.2
54/7477	54 74			0.8	2					-1.5			0.4	2.4					D -3.2 Clock -6.4
54/7480	54 74			0.8	2					-1.5		0.22	0.4	2.4	3.5				A_1,A_2,B_1,B_2, A_c or B_c -1.6 A* or B* -2.6 C_n -8
54/7483	54 74			0.8	2					-1.5			0.4	2.4					A_1,A_3,B_1,B_3, or C_o -3.2 A_2,A_4,B_2 or B_4 -1.6

		INPUT CURRENT						POWER SUPPLY CURRENT											
PARAMETER		I_{IH} (μA) HIGH LEVEL			I_I (mA) INPUT CURRENT			I_{OS} (mA) SHORT CIRCUIT			I_{CCL} (mA) LOW LEVEL			I_{CCH} (mA) HIGH LEVEL			I_{OH} (μA) REVERSE		
TEST CONDITIONS		V_{CC}=MAX V_{IN}=2.4V			V_{CC}=MAX V_{IN}=5.5V			V_{CC}=MAX			V_{CC}=MAX V_{IN}=5V			V_{CC}=MAX V_{IN}=0V			V_{CC}=MIN V_{IN}=* V_{OH}=5.5V		
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
54/7470	54 74		J1,J2,J,K1 K2,K or clock Preset or clear	 40 80			1 1	-20 -18	V_{IN}=0V	-75 -75		13	26						
54/7472	54 74		J1,J2,K3,K1 K2 or K3 Preset, clear or clock	 40 80		V_{IN}=0	1 1	-20 -18		-57 -57		10	20						
54/7473	54 74		J or K Clear or clock	 40 80			1 1	-20 -18		-57 -57		20	40						
54/7474	54 74		D Present or clock Clear	40 80 120			1 1	-20 -18		-57 -57		17	30						
54/7475	54 74		D Clock	 80 160			1	-20 -18	V_{OUT}=0V	-57 -57		32 32	46 53						
54/7476	54 74		J or K Clear preset or clock	 40 80			1	-20		-57		20	40						
54/7477	54 74		D Clock	 80 160			1	-20	V_{OUT}=0V	-57		32	46						
54/7480	54 74		A_1,A_2,B_1,B_2, A_C or B_C C_n	 15 200			1	@Σ or $\overline{\Sigma}$ -20 -18 @C_{n+1} -20 -18		 -57 -57 -70 -70		21 21	31 35						
54/7483	54 74		A_1,A_3,B_1, B_3 or C_0 A_2,A_4,B_2,B_4	 80 40			1	@Σ_1,Σ_2,Σ_3,Σ_4, -20 -18 @C_4 -20 -18		 -55 -55 -70 -70		58	79						

54/74 ELECTRICAL CHARACTERISTICS (See Notes - Page 50)

	INPUT VOLTAGE									OUTPUT VOLTAGE						INPUT CURRENT		
PARAMETER	V_{IL} (V) LOW LEVEL			V_{IH} (V) HIGH LEVEL			V_{IC} (V) CLAMP VOLTAGE			V_{OL} (V) LOW LEVEL			V_{OH} (V) HIGH LEVEL			I_{IL} (mA) LOW LEVEL		
TEST CONDITIONS	V_{CC}=MIN			V_{CC}=MIN			V_{CC}=MIN I_I= −12 mA			V_{CC}=MIN V_{IN}=* I_{OL}=16mA V_{OL}=0.4V			V_{CC}=MIN V_{IN}=* I_{OH}= −400 mA			V_{CC}=MAX V_{IN}=0.4V		
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
54/7485 54 74			0.8	2					-1.5			0.4	2.4					A<B,A>B -1.6 All other inputs -4.8
54/7486 54 74			0.8	2								0.4	I_{OH}=-800µA 2.4					-1.6
54/7490 54 74			0.8	2					-1.5			0.4	2.4					$R_{0(1)}$,$R_{0(2)}$, $R_{9(1)}$,$R_{9(2)}$ -1.6 Input A -3.2 Input BD -6.4
54/7491 54 74			0.8	2					-1.5		0.22	0.4	2.4	3.5				-1.6
54/7492 54 74			0.8	2					-1.5			0.4	2.4					$R_{0(1)}$,$R_{0(2)}$, -1.6 Input A -3.2 Input BC -6.4
54/7493 54 74			0.8	2					-1.5			0.4	2.4					$R_{0(1)}$,$R_{0(2)}$, -1.6 A or B -3.2
54/7494 54 74			0.8	2					-1.5		0.22	0.4	2.4	3.5				Any input except Preset 1&2 -1.6 Preset 1&2 -6.4
54/7495 54 74			0.8	2					-1.5			0.4	I_{OH}=-800µA 2.4					Any input except Mode control -1.6 Mode control -3.2
54/7496 54 74			0.8	2					-1.5		0.22	0.4	2.4	3.5				Any input except Preset -1.6 Preset -8
54/74100 54 74			0.8	2					-1.5			0.4	2.4					D -3.2 Clock -12.8

		INPUT CURRENT		POWER SUPPLY CURRENT			
PARAMETER		I_{IH} (µA) HIGH LEVEL	I_I (mA) INPUT CURRENT	I_{OS} (mA) SHORT CIRCUIT	I_{CCL} (mA) LOW LEVEL	I_{CCH} (mA) HIGH LEVEL	I_{OH} (µA) REVERSE
TEST CONDITIONS		V_{CC}=MAX V_{IN}=2.4V	V_{CC}=MAX V_{IN}=5.5V	V_{CC}=MAX	V_{CC}=MAX V_{IN}=5V	V_{CC}=MAX V_{IN}=OV	V_{CC}=MIN V_{IN}=* V_{OH}=5.5V
		MIN TYP MAX	MIN TYP MAX	MIN TYP MAX	MIN TYP MAX	MIN TYP MAX	MIN TYP MAX
54/7485	54 74	A<B,A>B 40 All other inputs 120	1	V_O=0V -20 -55 -18 -55	55 88		
54/7486	54 74	40	1	V_{IH}=4.5V V_{IL}=0 -20 -55 -18 -55	V_{IN}=4.5V 30 43 30 50		
54/7490	54 74	$R_{0(1)}$,$R_{0(2)}$ $R_{9(1)}$,$R_{9(2)}$ Input A 80 Input BD 160	1	V_{OUT}=0V -20 -57 -18 -57	V_{IN}=4.5V 32 46 32 53		
54/7491	54 74	40	1	-20 -57 -18 -57	V_{IN}=4.5V 35 50 35 58		
54/7492	54 74	$R_{0(1)}$,$R_{0(2)}$ 40 Input A 80 Input BC 160	1	V_{OUT}=0V -20 -57 -18 -57	V_{IN}=4.5V 31 44 31 51		
54/7493	54 74	$R_{0(1)}$,$R_{0(2)}$ 40 A or B 80	1	-20 -57 -18 -57	32 46 32 53		
54/7494	54 74	Any input except Preset 1&2 40 Preset 1&2 160	1	V_{OUT}=0V -20 -57 -18 -57	35 50 35 58		
54/7495	54 74	Any input except Mode control 40 Mode control 80	1	-18 -57	50 63		
54/7496	54 74	Any input except Preset 40 Preset 200	1	V_{OUT}=0V -20 -57 -18 -57	48 68 48 79		
54/74100	54 74	D 80 Clock 160 320	1	V_{OUT}=0V -20 -57 -18 -57		64 92 64 106	

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54/74 ELECTRICAL CHARACTERISTICS (See Notes - Page 50)

		INPUT VOLTAGE									OUTPUT VOLTAGE						INPUT CURRENT
PARAMETER		V_{IL} (V) LOW LEVEL			V_{IH} (V) HIGH LEVEL			V_{IC} (V) CLAMP VOLTAGE			V_{OL} (V) LOW LEVEL			V_{OH} (V) HIGH LEVEL			I_{IL} (mA) LOW LEVEL
TEST CONDITIONS		V_{CC}=MIN			V_{CC}=MIN			V_{CC}=MIN I_I=−12 mA			V_{CC}=MIN V_{IN}=* I_{OL}=16mA V_{OL}=0.4V			V_{CC}=MIN V_{IN}=* I_{OH}=−400 mA			V_{CC}=MAX V_{IN}=0.4V
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN TYP MAX
54/74107	54 74			0.8	2					-1.5		0.22	0.4	2.4	3.5		J or K -1.6 Clear or clock -3.2
54/74109	54 74			0.8	2					-1.5		0.2	0.4	I_{OH}=-800µA 2.4	2.7		J or K -1.6 Clock or preset -3.2 Clear -4.8
54/74116	54 74			0.8	2					-1.5		0.2	0.4	I_{OH}=-800µA V_{IH}=2V 2.4 2.4	3.4 3.4		$\overline{G1}$,$\overline{G2}$ or clear -1.6 Any D, initial peak -2.4 Any D steady state -1.6
54/74121	54 74	VT-(A)= 0.8 VT-(B)= 0.8	1.4 1.35		VT+(A)= VT+(B)=	1.4 1.55	2 2			-1.5		0.22	0.4	2.4	3.3		A_1 of A_2 -1 -1.6 B -2 -3.2
54/74122	54 74			0.8	2					-1.5		0.22	0.4	I_{OH}=-800µA 2.4			Data inputs -1.6 Clear inputs -3.2
54/74123	54 74			0.8	2					-1.5		0.22	0.4	I_{OH}=-800µA 2.4			Data inputs -1.6 Clear inputs -3.2
54/74125	54 74			0.8	2					-1.5			0.4	I_{OH}=-2m(54) I_{OH}=-5.2m(74) 2.4			-1.6
54/74126	54 74			0.8	2					-1.5			0.4	I_{OH}=2m(54) I_{OH}=-5.2m(74) 2.4			-1.6
54/74128	54 74			0.8	2					-1.5		I_{OL}=48mA 0.26	0.4	I_{OH}=-29mA(54) I_{OH}=-42.4mA(74) 2.4 2			-1.6

PARAMETER		INPUT CURRENT						POWER SUPPLY CURRENT											
		I_{IH} (μA) HIGH LEVEL			I_I (mA) INPUT CURRENT			I_{OS} (mA) SHORT CIRCUIT			I_{CCL} (mA) LOW LEVEL			I_{CCH} (mA) HIGH LEVEL			I_{OH} (μA) REVERSE		
TEST CONDITIONS		V_{CC}=MAX V_{IN}=2.4V			V_{CC}=MAX V_{IN}=5.5V			V_{CC}=MAX			V_{CC}=MAX V_{IN}=5V			V_{CC}=MAX V_{IN}=0V			V_{CC}=MIN V_{IN}=* V_{OH}=5.5V		
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
54/74107	54 74	J or K		40				-20 -18		-57 -57		20	40						
		Clear or clock		80															
54/74109	54 74	J or K		40			1	-30		-85			30 28						
		Clock or preset		80															
		Clear		160															
54/74116	54 74	$\overline{G1}$,$\overline{G2}$ or clear		40			1	-20 -18		-57 -57	V_{IN}=0V $\overline{G}$=0V OTHERS=4.5V	60 40	100 70						
		Any D		60															
54/74121	54 74	A_1 of A_2	2	40		0.05	1	-20 -18	-25 -25	-55 -55	Quiescent state	13	25						
		B	4	80							Fired state	23	40						
54/74122	54 74	Data inputs		40			1	-10		-40		23	28						
		Clear input		80															
54/74123	54 74	Data inputs		40			1	-10		-40		46	66						
		Clear input		80															
54/74125	54 74			40			1	-30 -28		-70 -70		32	54						
54/74126	54 74			40			1	-30 -28		-70 -70		36	62						
54/74128	54 74			40			1	-70		-180		33	57	12		21			

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54/74 ELECTRICAL CHARACTERISTICS (See Notes - Page 50)

		INPUT VOLTAGE									OUTPUT VOLTAGE						INPUT CURRENT		
PARAMETER		V_{IL} (V) LOW LEVEL			V_{IH} (V) HIGH LEVEL			V_{IC} (V) CLAMP VOLTAGE			V_{OL} (V) LOW LEVEL			V_{OH} (V) HIGH LEVEL			I_{IL} (mA) LOW LEVEL		
TEST CONDITIONS		V_{CC}=MIN			V_{CC}=MIN			V_{CC}=MIN $I_I = -12$ mA			V_{CC}=MIN V_{IN}=* I_{OL}=16mA V_{OL}=0.4V			V_{CC}=MIN V_{IN}=* $I_{OH} = -400$ mA			V_{CC}=MAX V_{IN}=0.4V		
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
54/74132	54 74	V_{CC}=5V VT− = 0.6	0.9	1.1	V_{CC}=5V VT+ = 1.5	1.7	2			-1.5		0.22	0.4	I_{OH}=-800µA 2.4	3.3			-0.8	-1.2
54/74145	54 74			0.8	2					-1.5									-1.6
54/74147	54 74			0.8	2					-1.5		0.2	0.4	I_{OH}=-800µA 2.4	3.3				-1.6
54/74148	54 74			0.8	2					-1.5		0.2	0.4	I_{OH}=-800µA 2.4	3.3				0 Input -1.6 All others -3.2
54/74150	54 74			0.8	2					-1.5			0.4	I_{OH}=-800µA 2.4					-1.6
54/74151	54 74			0.8	2					-1.5			0.4	I_{OH}=-800µA					-1.6
54/74152	54 74			0.8	2					-1.5			0.4	I_{OH}=-800µA 2.4					-1.6
54/74153	54 74			0.8	2					-1.5		0.2	0.4	I_{OH}=-800µA 2.4	3.1				-1.6
54/74154	54 74			0.8	2					-1.5			0.4	I_{OH}=-800µA 2.4					-1.6
54/74155	54 74			0.8	2					-1.5			0.4	I_{OH}=-800µA 2.4					-1.6
54/74156	54 74			0.8	2					-1.5			0.4						-1.6
54/74157	54 74			0.8	2					-1.5			0.4	I_{OH}=-800µA 2.4					-1.6
54/74158	54 74			0.8	2					-1.5			0.4	I_{OH}=-800µA 2.4					-1.6

PARAMETER		INPUT CURRENT I_{IH} (µA) HIGH LEVEL			INPUT CURRENT I_I (mA) INPUT CURRENT			POWER SUPPLY CURRENT I_{OS} (mA) SHORT CIRCUIT			POWER SUPPLY CURRENT I_{CCL} (mA) LOW LEVEL			POWER SUPPLY CURRENT I_{CCH} (mA) HIGH LEVEL			POWER SUPPLY CURRENT I_{OH} (µA) REVERSE		
TEST CONDITIONS		V_{CC}=MAX V_{IN}=2.4V			V_{CC}=MAX V_{IN}=5.5V			V_{CC}=MAX			V_{CC}=MAX V_{IN}=5V			V_{CC}=MAX V_{IN}=0V			V_{CC}=MIN V_{IN}=* V_{OH}=5.5V		
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
54/74132	54 74			40			1	-18		-55		V_I=4.5V 26	 40	14.8		24			
54/74145	54 74			40			1					43 43	62 70						
54/74147	54 74			40			1	-35		-85		Input 7=0V 50 Inputs=Open 42	 70 62						
54/74148	54 74		0 Input All others	 40 80			1	-35		-85		Input 7&E1=0V 40 Inputs=Open 35	 60 55						
54/74150	54 74			40			1	V_{OUT}=0V -20 -18		 -55 -55		V_{IN}=4.5V 40	 68						
54/74151	54 74			40			1	V_{OUT}=0V -20 -18		 -55 -55		V_{IN}=4.5V 29	 48						
54/74152	54 74			40			1	V_{OUT}=0V -20 -18		 -55 -55		V_{IN}=4.5V 26	 43						
54/74153	54 74			40			1	-20 -18		-55 -57		36 36	52 60						
54/74154	54 74			40			1	-20 -18		-55 -57		34 34	49 56						
54/74155	54 74			40			1	-20 -18		-55 -57		25 25	35 40						
54/74156	54 74			40			1	-20 -18		-55 -57		25 25	35 40						
54/74157	54 74			40			1	-20 -18		-55 -55		30	48						
54/74158	54 74			40			1	-20 -18		-55 -55									

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	INPUT VOLTAGE									OUTPUT VOLTAGE						INPUT CURRENT		
PARAMETER	V_{IL} (V) LOW LEVEL			V_{IH} (V) HIGH LEVEL			V_{IC} (V) CLAMP VOLTAGE			V_{OL} (V) LOW LEVEL			V_{OH} (V) HIGH LEVEL			I_{IL} (mA) LOW LEVEL		
TEST CONDITIONS	V_{CC}=MIN			V_{CC}=MIN			V_{CC}=MIN $I_I = -12$ mA			V_{CC}=MIN V_{IN}=* I_{OL}=16mA V_{OL}=0.4V			V_{CC}=MIN V_{IN}=* $I_{OH} = -400$ mA			V_{CC}=MAX V_{IN}=0.4V		
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
54/74160 54 74			0.8	2					-1.5			0.4	I_{OH}=-800µA 2.4					Clock or enable -3.2 Other inputs -1.6
54/74161 54 74			0.8	2					-1.5			0.4	I_{OH}=-800µA 2.4					Clock or enable -3.2 Other inputs -1.6
54/74162 54 74			0.8	2					-1.5			0.4	I_{OH}=-800µA					Clock or enable -3.2 Other inputs -1.6
54/74163 54 74			0.8	2					-1.5			0.4	I_{OH}=-800µA 2.4					Clock or enable -3.2 Other inputs -1.6
54/74164 54 74			0.8	2					-1.5			0.4	2.4					-1.6
54/74165 54 74			0.8	2					-1.5			0.4	I_{OH}=-800µA 2.4					Load input -3.2 Other inputs -1.6
54/74166 54 74			0.8	2					-1.5			0.4	2.4					-1.6
54/74170 54 74			0.8	2					-1.5			0.4						-1.6
54/74172 54 74			0.8	2					-1.5			0.4	I_{OH}=-5.2mA 2.4					2W/RO,2W/R1, 2W/R2, 1GW, 2GW or clock -1.6 Any other input -0.8
54/74174 54 74			0.8	2					-1.5			0.4	2.4					-1.6
54/74175 54 74			0.8	2					-1.5			0.4	2.4					-1.6
54/74176																		

		INPUT CURRENT						POWER SUPPLY CURRENT											
PARAMETER		I_{IH} (µA) HIGH LEVEL			I_I (mA) INPUT CURRENT			I_{OS} (mA) SHORT CIRCUIT			I_{CCL} (mA) LOW LEVEL			I_{CCH} (mA) HIGH LEVEL			I_{OH} (µA) REVERSE		
TEST CONDITIONS		V_{CC}=MAX V_{IN}=2.4V			V_{CC}=MAX V_{IN}=5.5V			V_{CC}=MAX			V_{CC}=MAX V_{IN}=5V			V_{CC}=MAX V_{IN}=OV			V_{CC}=MIN V_{IN}=* V_{OH}=5.5V		
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
		Clock or enable T																	
54/74160	54						1	-20		-57		63	91		59	85			
	74			80				-18		-57		63	101		59	94			
		Other inputs																	
				40															
54/74161	54	Clock enable T					1	-20		-57		63	91		59	85			
	74			80				-18		-57		63	101		59	94			
		Other inputs																	
				40															
54/74162	54	Clock or enable T					1	-20		-57		63	91		59	85			
	74			80				-18		-57		63	101		59	94			
		Other inputs																	
				40															
54/74163	54	Clock or enable T					1	-20		-57		63	91		59	85			
	74			80				-18		-57		63	101		59	94			
		Other inputs																	
				40															
54/74164	54			40			1	-10		-27.5	VI(Clk)=0.4V								
	74							- 9		-27.5		30							
											VI(Clk)=2.4V								
												37	54						
54/74165	54	Load input					1	-20		-55		42	63						
	74			80				-18		-55									
		Other inputs																	
				40															
54/74166	54			40			1	-20		-57		72	104						
	74							-18		-57		72	116						
54/74170	54			40			1					125	140					30	
	74											125	150						
54/74172	54			40			1	-18		-55		112	170						
	74																		
54/74174	54			40			1	-20		-57		45	65						
	74							-18		-57									
54/74175	54			40			1	-20		-57		30	45						
	74							-18		-57									
54/74176																			

LOGIC

54/74 ELECTRICAL CHARACTERISTICS (See Notes - Page 50)

		INPUT VOLTAGE									OUTPUT VOLTAGE						INPUT CURRENT		
PARAMETER		V_{IL} (V) LOW LEVEL			V_{IH} (V) HIGH LEVEL			V_{IC} (V) CLAMP VOLTAGE			V_{OL} (V) LOW LEVEL			V_{OH} (V) HIGH LEVEL			I_{IL} (mA) LOW LEVEL		
TEST CONDITIONS		V_{CC}=MIN			V_{CC}=MIN			V_{CC}=MIN $I_I = -12$ mA			V_{CC}=MIN V_{IN}=* I_{OL}=16mA V_{OL}=0.4V			V_{CC}=MIN V_{IN}=* $I_{OH} = -400$ mA			V_{CC}=MAX V_{IN}=0.4V		
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
54/74177																			
54/76178																			
54/74179																			
54/74180	54 74			0.8	2					-1.5			0.4	2.4					@Ea. data input -1.6 @Even or odd input -3.2
54/74181	54 74			0.8	2					-1.5		Any output except A=B	0.4	2.4					Mode -1.6 Any A or B -4.8 Any S -6.4 Carry -8
54/74182	54 74			0.8	2					-1.5			0.4	2.4					C_n input -3.2 P3 -4.8 P2 -6.4 P9, P1 or G3 -8 G0 or G2 -14.4 G1 -16
54/74190	54 74			0.8	2					-1.5			0.4	2.4					Any input except enable -1.6 At enable -4.8
54/74191	54 74			0.8	2					-1.5			0.4	2.4					Any input except enable -1.6 At enable -4.8
54/74192	54 74			0.8	2					-1.5		0.2	0.4	2.4	3.4				-1.6
54/74193	54 74			0.8	2					-1.5		0.2	0.4	2.4	3.4				-1.6
54/74194	54 74			0.8	2					-1.5			0.4	2.4					-1.6
54/74195	54 74			0.8	2					-1.5			0.4	2.4					-1.6
54/74196																			
54/74197																			
54/74198	54 74			0.8	2					-1.5			0.4	2.4					-1.6

PARAMETER		INPUT CURRENT						POWER SUPPLY CURRENT											
PARAMETER		I_{IH} (μA) HIGH LEVEL			I_I (mA) INPUT CURRENT			I_{OS} (mA) SHORT CIRCUIT			I_{CCL} (mA) LOW LEVEL			I_{CCH} (mA) HIGH LEVEL			I_{OH} (μA) REVERSE		
TEST CONDITIONS		V_{CC}=MAX V_{IN}=2.4V			V_{CC}=MAX V_{IN}=5.5V			V_{CC}=MAX			V_{CC}=MAX V_{IN}=5V			V_{CC}=MAX V_{IN}=OV			V_{CC}=MIN V_{IN}=* V_{OH}=5.5V		
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
54/74177																			
54/76178																			
54/74179																			
54/74180	54	@Ea. data input					1	-20		-55		34	49						
	74			40				-18		-55		34	56						
		@Even or odd input		80															
54/74181	54	Mode		40			1	-20		-55			127				A=B output only		
	74	Any A or B		120				-18		-57			140						250
		Any S		160															
		Carry		200															
54/74182	54	C_n input		80			1	-40		-100		45	65		27				
	74	P3 input		120								45	72						
		P2 input		160															
		P0, P1 or G3		200															
		G0 or G2		360															
		G1 input		400															
54/74190	54	Any input except					1	-20		-65		65	99						
	74	enable		40				-18		-65		65	105						
		At enable		120															
54/74191	54	Any input except					1	-20		-65		65	99						
	74	enable		40				-18		-65		65	105						
		At enable		120															
54/74192	54			40			1	-20		-65		65	89						
	74							-18		-65		65	102						
54/74193	54			40			1	-20		-65		65	89						
	74							-18		-65		65	102						
54/74194	54			40			1	-20		-57		39	63						
	74							-18		-57									
54/74195	54			40			1	-20		-57		39	63						
	74							-18		-57									
54/74196																			
54/74197																			
54/74198	54			40			1	-20		-57		72	104						
	74							-18		-57		72	116						

54/74 ELECTRICAL CHARACTERISTICS (See Notes - Page 50)

PARAMETER	INPUT VOLTAGE V_{IL} (V) LOW LEVEL			INPUT VOLTAGE V_{IH} (V) HIGH LEVEL			INPUT VOLTAGE V_{IC} (V) CLAMP VOLTAGE			OUTPUT VOLTAGE V_{OL} (V) LOW LEVEL			OUTPUT VOLTAGE V_{OH} (V) HIGH LEVEL			INPUT CURRENT I_{IL} (mA) LOW LEVEL		
TEST CONDITIONS	V_{CC}=MIN			V_{CC}=MIN			V_{CC}=MIN I_I=−12 mA			V_{CC}=MIN V_{IN}=* I_{OL}=16mA V_{OL}=0.4V			V_{CC}=MIN V_{IN}=* I_{OH}=−400 mA			V_{CC}=MAX V_{IN}=0.4V		
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
54/74199 54 74			0.8	2					-1.5			0.4	2.4					-1.6
54/74221 54 74	VT-(A)=			VT+(A)=														Input A
	0.8	1.4			1.4	2			-1.5		0.2	0.4	2.4	3.4				-1.6
	VT-(B)=			VT+(B)=														Input B, clear
	0.8	1.35			1.55	2												-3.2
54/74232 54 74	VT-			VT+														
	0.6	0.9	1.1	1.5	1.7	2			-1.5		0.22	0.4	2.4	3.3			-0.8	-1.2
54/74279 54 74			0.8	2					-1.5			0.4	2.4					-1.6
54/74298 54 74			0.8	2					-1.5			0.4	2.4	3.2				-1.6

54H ELECTRICAL CHARACTERISTICS (See Notes - Page 50)

PARAMETER	INPUT VOLTAGE V_{IL}(V) LOW LEVEL			INPUT VOLTAGE V_{IH} (V) HIGH LEVEL			INPUT VOLTAGE V_{IC} (V) CLAMP VOLTAGE			OUTPUT VOLTAGE V_{OL} (V) LOW LEVEL			OUTPUT VOLTAGE V_{OH} (V) HIGH LEVEL			INPUT CURRENT I_{IL} (mA) LOW LEVEL		
TEST CONDITIONS	V_{CC}=MIN			V_{CC}=MIN			V_{CC}=5V I_{IN}=−12 mA			V_{CC}=MIN V_{IN}=* I_{OL}=20 mA			V_{CC}=MIN V_{IN}=* I_{OH}=−500 μA			V_{CC}=MAX V_{IN}=0.4V		
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
54/74H00			0.8	2					-1.5			0.4	2.4					-2
54/74H01			0.8	2					-1.5			0.4						-2
54/74H04			0.8	2					-1.5			0.4	2.4					-2
54/74H05			0.8	2					-1.5			0.4						-2
54/74H08			0.8	2					-1.5			0.4	2.4					-2
54/74H10			0.8	2					-1.5			0.4	2.4					-2
54/74H11			0.8	2					-1.5			0.4	2.4					-2
54/74H20			0.8	2					-1.5			0.4	2.4					-2
54/74H21			0.8	2					-1.5			0.4	2.4					-2
54/74H22			0.8	2					-1.5			0.4						-2
54/74H30			0.8	2					-1.5			0.4	2.4					-2

	INPUT CURRENT						POWER SUPPLY CURRENT											
PARAMETER	I_{IH} (µA) HIGH LEVEL			I_I (mA) INPUT CURRENT			I_{OS} (mA) SHORT CIRCUIT			I_{CCL} (mA) LOW LEVEL			I_{CCH} (mA) HIGH LEVEL			I_{OH} (µA) REVERSE		
TEST CONDITIONS	V_{CC}=MAX V_{IN}=2.4V			V_{CC}=MAX V_{IN}=5.5V			V_{CC}=MAX			V_{CC}=MAX V_{IN}=5V			V_{CC}=MAX V_{IN}=0V			V_{CC}=MIN V_{IN}=* V_{OH}=5.5V		
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
54/74199 54			40			1	-20		-57		72	104						
74							-18		-57		72	116						
54/74221 54			Input A 40			1	-20		-55		Quiescent							
74							-18		-55		26	50						
			Input B, clear								Triggered							
			80								46	80						
54/74232 54 74			40			1	-18		-55		30	44		19	28			
54/74279 54			40			1	-18		-55		18	30						
74							-18		-57									
54/74298 54			40			1	-20		-57		39	65						
74							-18		-57									

	INPUT CURRENT						POWER SUPPLY CURRENT											
PARAMETER	I_{IH} (µA) HIGH LEVEL			I_I (mA) INPUT CURRENT			I_{OS} (mA) SHORT CIRCUIT			I_{CCL} (mA) LOW LEVEL			I_{CCH} (mA) HIGH LEVEL			I_{OH} (µA) REVERSE		
TEST CONDITIONS	V_{CC}=MAX V_{IN}=2.4V			V_{CC}=MAX V_{IN}=5.5V			V_{CC}=MAX			V_{CC}=MAX V_{IN}=4.5V			V_{CC}=MAX V_{IN}=0V			V_{CC}=MIN V_{IN}=* V_{OH}=5.5V		
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
54/74H00			50			1	-40		-100		26	40		10	16.8			
54/74H01			50			1					26	40		6.8	10			250
54/74H04			50			1	-40		-100		40	58		16	26			
54/74H05			50			1					40	58		16	26			250
											V_{IN}=0V			V_{IN}=4.5V				
54/74H08			50			1	-40		-100		40	64		24	40			
54/74H10			50			1	-40		-100		19.5	30		7.5	12.6			
											V_{IN}=0V			V_{IN}=4.5V				
54/74H11			50			1	-40		-100		30	48		18	30			
54/74H20			50			1	-40		-100		13	20		5	8.4			
											V_{IN}=0V			V_{IN}=4.5V				
54/74H21			50			1	-40		-100		20	32		12	20			
54/74H22			50			1					13	20		3.4	5.0			250
54/74H30			50			1	-40		-100		6.5	10		2.5	4.2			

54H ELECTRICAL CHARACTERISTICS (See Notes - Page 50)

	INPUT VOLTAGE									OUTPUT VOLTAGE						INPUT CURRENT		
PARAMETER	V_{IL}(V) LOW LEVEL			V_{IH} (V) HIGH LEVEL			V_{IC} (V) CLAMP VOLTAGE			V_{OL} (V) LOW LEVEL			V_{OH} (V) HIGH LEVEL			I_{IL} (mA) LOW LEVEL		
TEST CONDITIONS	V_{CC}=MIN			V_{CC}=MIN			V_{CC}=5V $I_{IN}=-12$ mA			V_{CC}=MIN V_{IN}=* I_{OL}=20 mA			V_{CC}=MIN V_{IN}=* $I_{OH}=-500$ μA			V_{CC}=MAX V_{IN}=0.4V		
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
											I_{OL}=60mA			I_{OH}=-1.5mA				
54/74H40			0.8	2					-1.5			0.4	2.4					-4
54/74H50			0.8	2					-1.5			0.4	2.4					-2
54/74H51			0.8	2					-1.5			0.4	2.4					-2
54/74H52			0.8	2					-1.5			0.4	2.4					-2
54/74H53			0.8	2					-1.5			0.4	2.4					-2
54/74H54			0.8	2					-1.5			0.4	2.4					-2
54/74H55			0.8	2								0.4	2.4					-2
									-1.5									
54/74H60			0.8	2					-1.5									-2
54/74H61			0.8	2					-1.5									-2
54/74H62			0.8	2					-1.5									-2
54/74H71			0.8	2					-1.5			0.4	2.4					-2
54/74H72			0.8	2					-1.5			0.4	2.4			J1,J2,J3,K1,K2, K3, CLOCK		-2
																PRESET, CLR		-4
54/74H73			0.8	2					-1.5			0.4	2.4					-2
													$I_{OH}=-1$mA					
54/74H74			0.8	2					-1.5		0.22	0.4	2.4	3.5		PRE or D		-2
																CLK or CLR		-4
54/74H76			0.8	2					-1.5			0.4	2.4			J, K, or CLK		-2
																CLR or PRE		-4
													I_{OH}=500μA					
54/74H101			0.8	2					-1.5		0.25	0.4	2.4	3.2			-1	-2
																(CLK)	-3	-4.8
													I_{OH}=500μA					
54/74H102			0.8	2					-1.5		0.25	0.4	2.4	3.2			-1	-2
																(CLK)	-3	-4.8
54/74H103			0.8	2					-1.5		0.25	0.4	2.4	3.2			-1	-2
																(CLK)	-3	-4.8
54/74H106			0.8	2					-1.5		0.25	0.4	2.4	3.2			-1	-2
																(CLK)	-3	-4.8
54/74H108			0.8	2					-1.5		0.25	0.4	2.4	3.2		J,K,PRE	-1	-2
																CLK	-6	-9.6
																CLR	-2	-4

	INPUT CURRENT						POWER SUPPLY CURRENT												
PARAMETER	I_{IH} (μA) HIGH LEVEL			I_I (mA) INPUT CURRENT			I_{OS} (mA) SHORT CIRCUIT			I_{CCL} (mA) LOW LEVEL			I_{CCH} (mA) HIGH LEVEL			I_{OH} (μA) REVERSE		
TEST CONDITIONS	V_{CC}=MAX V_{IN}=2.4V			V_{CC}=MAX V_{IN}=5.5V			V_{CC}=MAX			V_{CC}=MAX V_{IN}=4.5V			V_{CC}=MAX V_{IN}=0V			V_{CC}=MIN V_{IN}=* V_{OH}=5.5V		
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
54/74H40			100			1	-40		-125		25	40		10.4	16			
54/74H50			50			1	-40		-100		15.2	24		8.2	12.8			
54/74H51			50			1	-40		-100		15.2	24		8.2	12.8			
54/74H52			50			1	-40		-100		V_{IN}=OV 15.2	24		V_{IN}=4.5V 20	31			
54/74H53			50			1	-40		-100		9.4	14		7.1	11			
54/74H54			50			1	-40		-100		9.4	14		7.1	11			
54/74H55			50			1	-40		-100		7.5	12		4.5	6.4			
54/74H60			50			1					1.9	3.5		3	4.5			
54/74H61			50			1					11	16		5	7			
54/74H62			50			1					3.8	7		6	9			
54/74H71			50 J1,J2,J3,K1,K2 K3, or CLK			1	-40		-100		19	30						
54/74H72			50 PRE or CLR 100			1	-40		-100		16	25						
54/74H73			50			1	-40		-100									
54/74H74			D=50 PRE or CLK=100 CLR=150			1	-40		-100	S54 N74	30 30	42 50						
54/74H76			J,K or CLK 50 CLR or PRE 100			1	-40		-100		32	50						
54/74H101	 0		(J or K) 50 (PRE) 100 (CLK) -1mA			1	-40		-100		20	38						
54/74H102	 0		(J or K) 50 (CLK) -1mA (PRE or CLR) 100			1	-40		-100		20	38						
54/74H103	 0		(J or K) 50 (CLR) 100 (CLK) -1mA			1	-40		-100		40	76						
54/74H106	 0		(J or K) 50 CLR 100 (CLK) -1mA			1	-40		-100		40	76						
54/74H108	 0		(J or K) 50 (CLK) -1mA PRE 100 CLR 200			1	-40		-100		40	76						

54/74LS ELECTRICAL CHARACTERISTICS (See Notes - Page 50)

PARAMETER		INPUT VOLTAGE (V) V_{IL} LOW LEVEL	V_{IH} HIGH LEVEL	V_{IC} CLAMP VOLTAGE	OUTPUT VOLTAGE (V) V_{OL} LOW LEVEL			V_{OH} HIGH LEVEL		INPUT CURRENT I_{IL}(mA) LOW LEVEL	I_{IH}(μA) HIGH LEVEL
TEST CONDITIONS				V_{CC}=MIN I_{IN}=-18mA	V_{CC}=MIN V_{IN}=* I_{OL}=4mA V_{OL} 0.4V I_{OL}=8mA@V_{OL}=0.5V			V_{CC}=MIN V_{IN}=* I_{OH}=-400μA		V_{CC}=MAX V_{IL}=.4V	V_{CC}=MAX V_{CC}=MAX
		MIN TYP MAX	MIN TYP MAX	MIN TYP MAX	MIN	TYP	MAX	MIN	TYP	MIN TYP MAX	MIN TYP MAX
54/74LS00	54	0.7	2	-1.5	54/74		0.4	2.5	3.4	-0.36	20
	74	0.8			74		0.5	2.7	3.4		
54/74LS01		0.7	2	-1.5	54/74		0.4	N/A		-0.36	20
	74	0.8			74		0.5				
54/74LS02	54	0.7	2	-1.5	54/74		0.4	2.5	3.4	-0.36	20
	74	0.8			74		0.5	2.7	3.4		
54/74LS03	54	0.7	2	-1.5	54/74		0.4	N/A		-0.36	20
	74	0.8			74		0.5				
54/74LS04	54	0.7	2	-1.5	54/74		0.4	2.5	3.4	-0.36	20
	74	0.8			74		0.5	2.7	3.4		
54/74LS05	54	0.7	2	-1.5	54/74		0.4	N/A		-0.36	20
	74	0.8			74		0.5				
54/74LS08	54	0.7	2	-1.5	54/74	0.25	0.4	2.5	3.4	-0.36	20
	74	0.8			74	0.35	0.5	2.7	3.4		
54/74LS09	54	0.7	2	-1.5	54/74		0.4	N/A		-0.36	20
	74	0.8			74		0.5				
54/74LS10	54	0.7	2	-1.5	54/74		0.4	2.5	3.4	-0.36	20
	74	0.8			74			2.7	3.4		
54/74LS11	54	0.7	2	-1.5	54/74	0.25	0.4	2.5	3.4	-0.36	20
	74	0.8			74	0.35	0.5	2.7	3.4		
54/74LS12	54	0.7	2	-1.5	54/74	0.25	0.4	N/A		-0.36	20
	74	0.8			74	0.35	0.5				
								V_I=0.6V			
54/74LS13	54	See Data	Sheet	-1.5	54/74	0.25	0.4	2.5	3.4	-0.4	20
	74				74	0.35	0.5	2.7	3.4		
54/74LS14	54	See Data	Sheet	-1.5	54/74	0.25	0.4	V_I=0.6V		-0.4	20
	74				74	0.35	0.5	2.5	3.4		
								2.7	3.4		
54/74LS15	54	0.7	2	-1.5	54/74		0.4	N/A		-0.36	20
	74	0.8			74		0.5				
54/74LS20	54	0.7	2	-1.5	54/74		0.4	2.5	3.4	-0.36	20
	74	0.8			74		0.5	2.7	3.4		
54/74LS21	54	0.7	2	-1.5	54/74	0.25	0.4	2.5	3.4	-0.36	20
	74	0.8			74	0.35	0.5	2.7	3.4		
54/74LS22	54	0.7	2	-1.5	54/74		0.4	N/A		-0.36	20
	74	0.8			74		0.5				
54/74LS26	54	0.7	2	-1.5	54/74	0.25	0.4	N/A		-0.36	20
	74	0.8			74	0.35	0.5				
54/74LS27	54	0.7	2	-1.5	54/74	0.25	0.4	2.5	3.4	-0.36	20
	74	0.8			74	0.35	0.5	2.7	3.4		
					I_{OL} = 12mA						
54/74LS28	54	0.7	2	-1.5	54/74	0.25	0.4	2.5	3.4	-0.36	20
					I_{OL}=24mA						
	74	0.8			74	0.35	0.5	2.7	3.4		
54/74LS30	54	0.7	2	-1.5	54/74		0.4	2.5	3.4	-0.36	20
	74	0.8			74		0.5	2.7	3.4		
54/74LS32	54	0.7	2	-1.5	54/74	0.25	0.4	2.5	3.4	-0.36	20
	74	0.8			74	0.35	0.5	2.7	3.4		
					I_{OL}=12mA						
54/74LS33	54	0.7	2	-1.5	54/74		0.4	N/A		-0.36	20
	74	0.8			74 I_{OL}=24mA		0.5				
					I_{OL}=12mA						
54/74LS37	54	0.7	2	-1.5	54/74		0.4	2.5	3.4	-0.36	20
					I_{OL}=24mA						
	74	0.8			74		0.5	2.7	3.4		

	INPUT CURRENT (mA)			OUTPUT CURRENT (mA)			POWER SUPPLY CURRENT (mA)									OFF-STATE OUTPUT CURRENT (μA)					
PARAMETER	I_{IN}			I_{OS} SHORT CIRCUIT			I_{CCL} LOW LEVEL			I_{CCH} HIGH LEVEL			I_{OH}(μA) LEAKAGE			I_{OZL} LOW LEVEL VOLTAGE SUPPLIED			I_{OZH} HIGH LEVEL VOLTAGE SUPPLIED		
TEST CONDITIONS	V_{CC}=MAX V_{IN}=7.0V						V_{CC}=MAX V_{IH}=4.5V V_{IL}=0V as appropriate						V_{CC}=MIN V_{IN}=* V_{OH}=5.5V			V_{CC}=MAX V_O=0.4V			V_{CC}=MAX V_O=2.7V		
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
54/74LS00 54 74	V_I=5.5V		0.1	-15		-100		2.4	4.4		0.8	1.6		N/A			N/A			N/A	
54/74LS01 54 74	V_I=5.5V		0.1		N/A			2.4	4.4		0.8	1.6			100		N/A			N/A	
54/74LS02 54 74	V_I=5.5V		0.1	-15		-100		2.8	5.4		1.6	3.2		N/A			N/A			N/A	
54/74LS03 54 74	V_I=5.5V		0.1		N/A			2.4	4.4		0.8	1.6			100		N/A			N/A	
54/74LS04 54 74			0.1	-15		-100		3.6	6.6		1.2	2.4		N/A			N/A			N/A	
54/74LS05 54 74			0.1		N/A			3.6	6.6		1.2	2.4			100		N/A			N/A	
54/74LS08 54 74	V_I=5.5V		0.1	-15		-100		6.8	8.8		2.4	4.8		N/A			N/A			N/A	
54/74LS09 54 74	V_I=5.5V		0.1		N/A			4.4	8.8		2.4	4.8			100		N/A			N/A	
54/74LS10 54 74	V_I=5.5V		0.1	-15		-100		1.8	3.3		0.6	1.2		N/A			N/A			N/A	
54/74LS11 54 74	V_I=5.5V		0.1	-15		-100		3.3	6.6		1.8	3.6		N/A			N/A			N/A	
54/74LS12 54 74	V_I=5.5V		0.1		N/A			1.8	3.3		0.7	1.4			100		N/A			N/A	
54/74LS13 54 74			0.1	-15		-100		4.1	7		2.9	6		N/A			N/A			N/A	
54/74LS14 54 74			0.1	-15		-100		4.1	7		8.6	16		N/A			N/A			N/A	
54/74LS15 54 74	V_I=5.5V		0.1		N/A			3.3	6.6		1.8	3.6			100		N/A			N/A	
54/74LS20 54 74			0.1	-15		-100		1.2	2.2		0.4	0.8		N/A			N/A			N/A	
54/74LS21 54 74			0.1	-15		-100		2.2	4.4		1.2	2.4		N/A			N/A			N/A	
54/74LS22 54 74			0.1		N/A			1.2	2.2		0.4	0.8			100		N/A			N/A	
54/74LS26 54 74			0.1		N/A			2.4	4.4		0.8	1.6		V_{IL}=MAX V_{OH}=12V V_{OH}=15V	 50 1MA		N/A			N/A	
54/74LS27 54 74	V_I=5.5V		0.1	-15		-100		3.4	6.8		2.0	4.0		N/A			N/A			N/A	
54/74LS28 54			0.1	-15		-100		6.9	13.8		1.8	3.6		N/A			N/A			N/A	
54/74LS30 54 74			0.1	-15		-100		0.6	1.1		.35	0.5		N/A			N/A			N/A	
54/74LS32 54 74	V_I=5.5V		0.1	-15		-100		4.9	9.8		3.1	6.2		N/A			N/A			N/A	
54/74LS33 54 74			0.1		N/A			6.9	13.8		1.8	3.6			250		N/A			N/A	
54/74LS37 54 74			0.1	-15		-100		6.0	12.0		0.9	2.0		N/A			N/A			N/A	

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54/74LS ELECTRICAL CHARACTERISTICS (See Notes - Page 50)

PARAMETER		INPUT VOLTAGE (V)									OUTPUT VOLTAGE (V)						INPUT CURRENT					
		V_{IL} LOW LEVEL			V_{IH} HIGH LEVEL			V_{IC} CLAMP VOLTAGE			V_{OL} LOW LEVEL			V_{OH} HIGH LEVEL			I_{IL}(mA) LOW LEVEL			I_{IH}(μA) HIGH LEVEL		
TEST CONDITIONS								V_{CC}=MIN I_{IN}=-18mA			V_{CC}=MIN V_{IN}=* I_{OL}=4mA V_{OL}MAX I_{OL}=8mA@V_{OL}=0.5V			V_{CC}=MIN I_{OH}=-400μA			V_{IL}=.4V			V_{CC}=MAX		
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
												I_{OL}=12mA										
54/74LS38	54			0.7	2					-1.5	54/74		0.4		N/A				-0.36			20
												I_{OL}=24mA										
	74			0.8							74		0.5									
												I_{OL}=12mA										
54/74LS40	54			0.7	2					-1.5	54/74		0.4	2.5	3.4				-0.36			20
												I_{OL}=24mA										
	74			0.8							74		0.5	2.7	3.4							
54/74LS42	54			0.7	2					-1.5	54/74	0.25	0.4	2.5	3.5				-0.4			20
	74			0.8							74	0.35	0.5	2.7	3.5							
54/74LS51	54			0.7	2					-1.5	54/74	0.25	0.4	2.5	3.4				-0.36			20
	74			0.8							74	0.35	0.5	2.7	3.4							
54/74LS54	54			0.7	2					-1.5	54/74	0.25	0.4	2.5	3.4				-0.36			20
	74			0.8							74	0.35	0.5	2.7	3.4							
54/74LS55	54			0.7	2					-1.5	54/74	0.25	0.4	2.5	3.4				-0.36			20
	74			0.8							74	0.35	0.5	2.7	3.4							
54/74LS73	54			0.7	2					-1.5	54/74	0.25	0.4	2.5	3.4		J/K Input		-0.36	J/K Input		20
	74			0.8							74	0.35	0.5	2.7	3.4		CLear		-0.8	Clear		60
																	Clock		-0.72	Clock		80
54/74LS74	54			0.7	2					-1.5	54/74	0.25	0.4	2.5	3.4		D Input		-0.36	D Input		20
	74			0.8							74	0.35	0.5	2.7	3.4		Clk/Preset		-0.8	Clk/Preset		40
																	Clear		-1.15	Clear		60
54/74LS75	54			0.7	2					-1.5	54/74	0.25	0.4	2.5	3.4		D Input		-0.4	D Input		20
	74			0.8							74	0.35	0.5	2.7	3.4		G Input		-1.6	G Input		80
54/74LS76	54			0.7	2					-1.5	54/74	0.25	0.4	2.5	3.4		J/K Input		-0.36	J/K Input		20
	74			0.8							74	0.35	0.5	2.7	3.4		Clock		-0.72	Clock		80
																	Preset/Clr		-0.8	Preset/Clr		60
54/74LS78	54			0.7	2					-1.5	54/74	0.25	0.4	2.5	3.4		J/K Input		-0.36	J/K Input		20
	74			0.8							74	0.35	0.5	2.7	3.4		Preset		-0.8	Preset		60
																	Clear		-1.6	Clear		120
																	Clock		-1.44	Clock		160
54/74LS83A	54			0.7	2					-1.5	54/74	0.25	0.4	2.5	3.4		Any A or B		-.8	Any A or B		40
	74			0.8							74	0.35	0.5	2.7			CO		-.4	CO		20
54/74LS85	54			0.7	2					-1.5	54/74	0.25	0.4	2.4	3.4		A<B,A>B		-0.4	A<B,A>B		20
	74			0.8							74	0.35	0.5				Others		-1.2	Others		60
54/74LS86	54			0.7	2					-1.5	54/74	0.25	0.4	2.5	3.4				-0.6			40
	74			0.8							74	0.35	0.5	2.7	3.4							
54/74LS90	54			0.7	2					-1.5	54/74	0.25	0.4	2.5	3.4		Any Reset		-0.4	Any Reset		20
	74			0.8							74	0.35	0.5	2.7	3.4		A Input		-2.4	A Input		40
																	B Input		-3.2	B Input		80
54/74LS92	54			0.7	2					-1.5	54/74	0.25	0.4	2.5	3.4		Any Reset		-0.4	Any Reset		20
	74			0.8							74	0.35	0.5	2.7	3.4		A Input		-2.4	A Input		40
																	B Input		-3.2	B Input		80
54/74LS93	54			0.7	2					-1.5	54/74	0.25	0.4	2.5	3.4		Any Reset		-0.4	Any Reset		20
	74			0.8							74	0.35	0.5	2.7	3.4		A Input		-2.4	A Input		120
																	B Input		-1.6	B Input		40

PARAMETER		INPUT CURRENT (mA) I_{IN}		OUTPUT CURRENT (mA) I_{OS} SHORT CIRCUIT		POWER SUPPLY CURRENT (mA) I_{CCL} LOW LEVEL			I_{CCH} HIGH LEVEL			$I_{OH}(\mu A)$ LEAKAGE	OFF-STATE OUTPUT CURRENT (μA) I_{OZL} LOW LEVEL VOLTAGE SUPPLIED	I_{OZH} HIGH LEVEL VOLTAGE SUPPLIED
TEST CONDITIONS		V_{CC}=MAX V_{IN}=7.0V				V_{CC}=MAX V_{IH}=4.5V V_{IL}=0V as appropriate						V_{CC}=MIN V_{IN}=* V_{OH}=5.5V	V_{CC}=MAX V_O=0.4V	V_{CC}=MAX V_O=2.7V
		MIN TYP	MAX	MIN TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN TYP MAX	MIN TYP MAX	MIN TYP MAX
54/74LS38	54 74		0.1	N/A			6.0	12.0		0.9	2.0	250	N/A	N/A
54/74LS40	54 74		0.1	-15	-100		3	6		0.45	1	N/A	N/A	N/A
54/74LS42	54 74		0.1	-15	-100		N/A			7 NOTE 1	13	N/A	N/A	N/A
54/74LS51	54 74		0.1	-15	-100		1.4	2.8		0.8	1.6	N/A	N/A	N/A
54/74LS54	54 74		0.1	-15	-100		1.0	2.0		0.8	1.6	N/A	N/A	N/A
54/74LS55	54 74		0.1	-15	-100		0.7	1.3		0.4	0.8	N/A	N/A	N/A
54/74LS73	54 74	V_I=5.5V J/K Input Clear Clock	 0.1 0.3 0.4	-15	-100		N/A			4.0 NOTE 2	8.0	N/A	N/A	N/A
54/74LS74	54 74	D Input Clk Preset Clear	0.1 0.2 0.3	-15	-100		N/A			4.0 NOTE 2	8.0	N/A	N/A	N/A
54/74LS75	54 74	D Input G Input	0.1 0.4	-15	-100		N/A			6.3 NOTE 1	12.0	N/A	N/A	N/A
54/74LS76	54 74	V_I=5.5V J/K Input Clock Preset/Clr	 0.1 0.4 0.3	-15	-100		N/A			4.0 NOTE 2	8.0	N/A	N/A	N/A
54/74LS78	54 74	V_I=5.5V J/K Input Preset Clear Clock	 0.1 0.3 0.6 0.8	-15	-100		N/A			4.0	8.0	N/A	N/A	N/A
54/74LS83A	54 74	Any A or B CO	.2 -1	-15	-100	COND.A NOTE 21	22	39	COND.B NOTE 28	19	34	N/A	N/A	N/A
54/74LS85	54 74	A<B, A>B Others	0.1 0.3	-15	-100		N/A			10.4 NOTE 3	20.0	N/A	N/A	N/A
54/74LS86	54 74		0.2	-15	-100		N/A			6.1 NOTE 1	10.0	N/A	N/A	N/A
54/74LS90	54 74	V_I=7V Any Reset V_I=5.5V A Input B Input	 0.1 0.4 0.8	-15	-100		N/A			9.0 NOTE 4	15.0	N/A	N/A	N/A
54/74LS92	54 74	V_I=7V Any Reset V_I=5.5V A Input B Input	 0.1 0.4 0.8	-15	-100		N/A			9.0 NOTE 4	15.0	N/A	N/A	N/A
54/74LS93	54 74	V_I=7V Any Reset V_I=5.5 A or B Input	 0.1 0.4	-15	-100		N/A			9.0 NOTE 4	15.0	N/A	N/A	N/A

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		INPUT VOLTAGE (V)			OUTPUT VOLTAGE (V)					INPUT CURRENT			
PARAMETER		V_{IL} LOW LEVEL	V_{IH} HIGH LEVEL	V_{IC} CLAMP VOLTAGE	V_{OL} LOW LEVEL			V_{OH} HIGH LEVEL		I_{IL}(mA) LOW LEVEL		I_{IH}(μA) HIGH LEVEL	
TEST CONDITIONS				V_{CC}=MIN I_{IN}=-18mA	V_{CC}=MIN V_{IN}=* I_{OL}=4mA V_{OL}MAX I_{OL}=8mA@V_{OL}=0.5V			V_{CC}=MIN I_{OH}=-400μA		V_{CC}=MAX V_{IL}=.4V		V_{IH}=2.7V V_{CC}=MAX	
		MIN TYP MAX	MIN TYP MAX	MIN TYP MAX	MIN	TYP	MAX	MIN	TYP	MIN	TYP MAX	MIN	TYP MAX
54/74LS95B	54 74	0.7 0.8	2	-1.5	54/74 74	0.25 0.35	0.4 0.5	2.5 2.7	3.5 3.5		-0.4		20
54/74LS96	54 74	0.7 0.8	2	-1.5	54/74 74	0.25 0.35	0.4 0.5	2.5 2.7	3.5 3.5	Preset Enable Others	-2.0 -0.4	Preset Enable Others	100 20
54/74LS107	54 74	0.7 0.8	2	-1.5	54/74 74		0.4 0.5	2.5 2.7	3.4 3.4	J/K Input Clear Clock	-0.36 -0.8 -0.72	J/K Input Clear Clock	20 60 80
54/74LS109	54 74	0.7 0.8	2	-1.5	54/74 74		0.4 0.5	2.5 2.7	3.4 3.4	J or K̄ Clk/Preset Clear	-0.4 -0.8 -1.6	J or K̄ Clk/Preset Clear	20 40 80
54/74LS112	54 74	0.7 0.8	2	-1.5	54/74 74		0.4 0.5	2.5 2.7	3.4 3.4	J/K Input Clock Preset/Clr	-0.36 -0.72 -0.8	J/K Input Clock Preset/Clr	20 80 60
54/74LS113	54 74	0.7 0.8	2	-1.5	54/74 74		0.4 0.5	2.5 2.7	3.4 3.4	J/K Input Preset Clock	-0.36 -0.8 -0.72	J/K Input Preset Clock	20 60 80
54/74LS114	54 74	0.7 0.8	2	-1.5	54/74 74		0.4 0.5	2.5 2.7	3.4 3.4	J/K Input Preset Clear Clock	-0.36 -0.8 -1.6 -1.44	J/K Input Preset Clear Clock	20 60 120 160
54/74LS132	54 74	See Data	Sheet	-1.5	54/74 74	0.25 0.35	0.4 0.5	V_I=0.6V 2.5 2.7	 3.4 3.4		-0.4		20
54/74LS136	54 74	0.7 0.8	2	-1.5	54/74 74	0.25 0.35	0.4 0.5		N/A		-0.6		40
54/74LS138	54 74	0.7 0.8	2	-1.5	54/74 74	0.25 0.35	0.4 0.5	2.5 2.7	3.4 3.4		-0.36		20
54/74LS139	54 74	0.7 0.8	2	-1.5	54/74 74	0.25 0.35	0.4 0.5	2.5 2.7	3.4 3.4		-0.36		20
54/74LS145	54 74	0.7 0.8	2	-1.5	I_{OL}=12MA 54/74 I_{OL}=24MA 74 I_{OL}=80MA 74		 0.4 0.5 1.7		N/A		-0.4		20
54/74LS151	54 74	0.7 0.8	2	-1.5	54/74 74	0.25 0.35	0.4 0.5	2.5 2.7	3.4 3.4		-0.4		20
54/74LS153	54 74	0.7 0.8	2	-1.5	54/74 74	0.25 0.35	0.4 0.5	2.5 2.7	3.4 3.4		-0.36		20
54/74LS157	54 74	0.7 0.8	2	-1.5	54/74 74	0.25 0.35	0.4 0.5	2.5 2.7	3.4 3.4	S/G Inputs A/B Inputs	-0.8 -0.4	S/G Inputs A/B Inputs	40 20
54/74LS158	54 74	0.7 0.8	2	-1.5	54/74 74	0.25 0.35	0.4 0.5	2.5 2.7	3.4 3.4	S/G Inputs A/B Inputs	-0.8 -0.4	S/G Inputs A/B Inputs	40 20
54/74LS160	54 74	0.7 0.8	2	-1.5	54/74 74	0.25 0.35	0.4 0.5	2.5 2.7	3.4 3.4	D/EP LD, ET CLR CLK	-0.4 -0.8 -0.4 -1.2	D/EP LD,CLK,ET CLR	20 40 20
54/74LS161	54 74	0.7 0.8	2	-1.5	54/74 74	0.25 0.35	0.4 0.5	2.5 2.7	3.4 3.4	D/EP LD, ET CLR CLK	-0.4 -0.8 -0.4 -1.2	D/EP LD,CLK,ET CLR	20 40 20

		INPUT CURRENT (mA)		OUTPUT CURRENT (mA)		POWER SUPPLY CURRENT (mA)					OFF-STATE OUTPUT CURRENT (μA)	
PARAMETER		I_{IN}		I_{OS} SHORT CIRCUIT		I_{CCL} LOW LEVEL		I_{CCH} HIGH LEVEL		I_{OH}(μA) LEAKAGE	I_{OZL} LOW LEVEL VOLTAGE SUPPLIED	I_{OZH} HIGH LEVEL VOLTAGE SUPPLIED
TEST CONDITIONS		V_{CC}=MAX V_{IN}=7.0V				V_{CC}=MAX V_{IH}=4.5V V_{IL}=0V as appropriate				V_{CC}=MIN V_{IN}=* V_{OH}=5.5V	V_{CC}=MAX V_O=0.4V	V_{CC}=MAX V_O=2.7V
		MIN TYP	MAX	MIN	TYP MAX	MIN TYP	MAX	MIN TYP	MAX	MIN TYP MAX	MIN TYP MAX	MIN TYP MAX
54/74LS95B	54 74		0.1	-15	-100	N/A		12.0 NOTE 6	20.0	N/A	N/A	N/A
54/74LS96	54 74	Others Preset Enable	0.1 0.5	-15	-100	N/A		12.0 NOTE 6	20.0	N/A	N/A	N/A
54/74LS107	54 74	V_I=5.5V J/K Input Clear Clock	 0.1 0.3 0.4	-15	-100	N/A		4.0 NOTE 2	8.0	N/A	N/A	N/A
54/74LS109	54 74	J or K Clk/preset Clear	0.1 0.2 0.4	-15	-100	N/A		4.0 NOTE 2	8.0	N/A	N/A	N/A
54/74LS112	54 74	V_I=5.5 J/K Input Clock Preset/Clr	 0.1 0.4 0.3	-15	-100	N/A		4.0 NOTE 2	8.0	N/A	N/A	N/A
54/74LS113	54 74	V_I=5.5 J/K Input Preset Clock	 0.1 0.3 0.4	-15	-100	N/A		4.0 NOTE 2	8.0	N/A	N/A	N/A
54/74LS114	54 74	V_I=5.5 J/K Input Preset Clear Clock	 0.1 0.3 0.6 0.8	-15	-100	N/A		4.0 NOTE 2	8.0	N/A	N/A	N/A
54/74LS132	54 74		0.1	-15	-100	8.2	14	5.9	11	N/A	N/A	N/A
54/74LS136	54 74		0.2	N/A		N/A		6.1 NOTE 8	10.0	100	N/A	N/A
54/74LS138	54 74		0.1	-15	-100	N/A		6.3 NOTE 1	10.0	N/A	N/A	N/A
54/74LS139	54 74		0.1	-15	-100	N/A		6.8 NOTE 1	11.0	N/A	N/A	N/A
54/74LS145	54 74		0.1	N/A		N/A		7.0 NOTE 1	13.0	250	N/A	N/A
54/74LS151	54 74		0.1	-15	-100	N/A		6.0 NOTE 8	10.0	N/A	N/A	N/A
54/74LS153	54 74		0.1	-15	-100	N/A		6.2	10.0	N/A	N/A	N/A
54/74LS157	54 74	S/G Inputs A/B Inputs	0.2 0.1	-15	-100	N/A		9.7 NOTE 8	16.0	N/A	N/A	N/A
54/74LS158	54 74	S/G Inputs A/B Inputs	0.2 0.1	-15	-100	N/A		4.8 NOTE 8	8.0	N/A	N/A	N/A
54/74LS160	54 74	D/EP LD,CLK,ET CLR	0.1 0.2 0.1	-15	-100	19	32	18	31	N/A	N/A	N/A
54/74LS161	54 74	D/EP LD,CLK,ET CLR	0.1 0.2 0.1	-15	-100	19	32	18 NOTE 10	31	N/A	N/A	N/A

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54/74LS ELECTRICAL CHARACTERISTICS (See Notes - Page 50)

PARAMETER		INPUT VOLTAGE (V) V_{IL} LOW LEVEL	V_{IH} HIGH LEVEL	V_{IC} CLAMP VOLTAGE	OUTPUT VOLTAGE (V) V_{OL} LOW LEVEL			V_{OH} HIGH LEVEL		INPUT CURRENT I_{IL}(mA) LOW LEVEL		I_{IH}(μA) HIGH LEVEL	
TEST CONDITIONS				V_{CC}=MIN I_{IN}=-18mA	V_{CC}=MIN V_{IN}=* I_{OL}=4mA V_{OL}MAX I_{OL}=8mA@V_{OL}=0.5V			V_{CC}=MIN I_{OH}=-400μA		V_{IL}=.4V		V_{CC}=MAX	
		MIN TYP MAX	MIN TYP MAX	MIN TYP MAX	MIN	TYP	MAX	MIN	TYP MAX	MIN TYP	MAX	MIN TYP	MAX
54/74LS162	54	0.7	2	-1.5	54/74	0.25	0.4	2.5	3.4	D/EP	-0.4	D/EP	20
	74	0.8			74	0.35	0.5	2.7	3.4	LD, ET	-0.8	LDCLK,ET	40
										CLR	-0.8	CLR	40
										CLK	-1.2		
54/74LS163	54	0.7	2	-1.5	54/74	0.25	0.4	2.5	3.4	D/EP	-0.4	D/EP	20
	74	0.8			74	0.35	0.5	2.7	3.4	LD, ET	-0.8	LDCLK,ET	40
										CLR	-0.8	CLR	40
										CLK	-1.2		
54/74LS164	54	0.7	2	-1.5	54/74	0.25	0.4	2.5	3.5		-0.4		20
	74	0.8			74	0.35	0.5	2.7	3.5				
54/74LS170	54	0.7	2	-1.5	54/74	0.25	0.4	N/A		Any D,R,W	-0.4	Any D,R,W	20
	74	0.8			74	0.35	0.5			G_R or G_W	-0.8	G_R or G_W	40
54/74LS174	54	0.7	2	-1.5	54/74	0.25	0.4	2.5	3.5	Clock Input, Clear	-0.4		20
	74	0.8			74	0.35	0.5	2.7	3.5	Other Inputs	-0.36		
54/74LS175	54	0.7	2	-1.5	54/74	0.25	0.4	2.5	3.5	Clock Input	-0.4		20
	74	0.8			74	0.35	0.5	2.7	3.5	Other Inputs	-0.36		
54/74LS181	54	0.7	2	-1.5	54/74	0.25	0.4	2.5	3.4	Mode Input	-0.36	Mode Input	20
	74	0.8			74	0.35	0.5	2.7	3.4	A/B Inputs	-1.08	A/B Inputs	60
										S Inputs	-1.44	S Inputs	80
										Carry Input	-2	Carry Input	100
54/74LS190	54	0.7	2	-1.5	54/74	0.25	0.4	2.5	3.4	Enable	-1.08	Enable	60
	74	0.8			74	0.35	0.5	2.7	3.4	Others	-0.4	Others	20
54/74LS191	54	0.7	2	-1.5	54/74	0.25	0.4	2.5	3.4	Enable	-1.08	Enable	60
	74	0.8			74	0.35	0.5	2.7	3.4	Others	-0.4	Others	20
54/74LS192	54	0.7	2	-1.5	54/74	0.25	0.4	2.5	3.4		-0.4		20
	74	0.8			74	0.35	0.5	2.7	3.4				
54/74LS193	54	0.7	2	-1.5	54/74	0.25	0.4	2.5	3.4		-0.4		20
	74	0.8			74	0.35	0.5	2.7	3.4				
54/74LS194A	54	0.7	2	-1.5	54/74	0.25	0.4	2.5	3.4		-0.4		20
	74	0.8			74	0.35	0.5	2.7	3.4				
54/74LS195A	54	0.7	2	-1.5	54/74	0.25	0.4	2.5	3.4	CLK	-0.44		20
	74	0.8			74	0.35	0.5	2.7	3.4	Others	-0.36		
54/74LS196	54	0.7	2	-1.5	54/74		0.4	2.5	3.4	Data, Count/Load	-0.36	Data, Count/Load	20
	74	0.8			74		0.5	2.7	3.4	Clear	-0.72	Clear,Clock 1	40
										Clock 1	-2.4	Clock 2	80
										Clock 2	-2.8		
54/74LS197	54	0.7	2	-1.5	54/74	0.25	0.4	2.5	3.4	Data, Count/Load	-0.36	Data, Count/Load	20
	74	0.8			74	0.35	0.5	2.7	3.4	Clear	-0.72	Clear, Clock 1	40
										Clock 1	-2.4	Clock 2	40
										Clock 2	-1.3		
54/74LS221	54	0.7	2	-1.5	54/74	0.25	0.4	2.5	3.5	Input A	-0.36		20
										Input B	-0.6		
	74	0.8				0.35	0.5	2.7	3.5	Clear	-0.6		
								I_{OH}=-1mA (54) I_{OH}=-2.6mA (74)					
54/74LS251	54	0.7	2	-1.5	54/74	0.25	0.4	2.5	3.4		-0.4		20
	74	0.8			74	0.35	0.5	2.7	3.4				
								I_{OH}=-1mA (54) I_{OH}=-2.6mA (74)					
54/74LS253	54	0.7	2	-1.5	54/74	0.25	0.4	2.4	3.4		-0.36		20
	74	0.8			74	0.35	0.5	2.4	3.4				
								I_{OH}=-1mA (54) I_{OH}=-2.6mA (74)					
54/74LS257	54	0.7	2	-1.5	54/74	0.25	0.4	2.4	3.4	S Input	-0.8	S Input	40
	74	0.8			74	0.35	0.5	2.4	3.4	Others	-0.4	Others	20

	INPUT CURRENT (mA)			OUTPUT CURRENT (mA)			POWER SUPPLY CURRENT (mA)									OFF-STATE OUTPUT CURRENT (μA)					
PARAMETER	I_{IN}			I_{OS} SHORT CIRCUIT			I_{CCL} LOW LEVEL			I_{CCH} HIGH LEVEL			I_{OH}(μA) LEAKAGE			I_{OZL} LOW LEVEL VOLTAGE SUPPLIED			I_{OZH} HIGH LEVEL VOLTAGE SUPPLIED		
TEST CONDITIONS	V_{CC}=MAX V_{IN}=7.0V						V_{CC}=MAX V_{IH}=4.5V V_{IL}=0V as appropriate						V_{CC}=MAX V_{IN}=* V_{OH}=5.5V			V_{CC}=MAX V_O=0.4V			V_{CC}=MAX V_O=2.7V		
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
54/74LS162	D/EP LD,CLK,ET CLR		0.1 0.2 0.2	-15		-100		19	32		18 NOTE 10	31		N/A			N/A			N/A	
54/74LS163 54 74	D/EP LD,CLK,ET CLR		0.1 0.2 0.2	-15		-100		19	32		18 NOTE 10	31		N/A			N/A			N/A	
54/74LS164 54 74			0.1	-15		-100		N/A			16.0	27.0		N/A			N/A			N/A	
54/74LS170 54 74	Any D,R,W G_R or G_W		0.1 0.2		N/A			N/A			26.0 NOTE 12	40.0			100		N/A			N/A	
54/74LS174 54 74			0.1	-15		-100		N/A			16.0 NOTE 7	26.0		N/A			N/A			N/A	
54/74LS175 54 74			0.1	-15		-100		N/A			11.0 NOTE 7	18.0		N/A			N/A			N/A	
54/74LS181 54 74	V_I=5.5V Mode Input A/B Inputs S Inputs Carry Input		 0.1 0.3 0.4 0.5	-15		-100			35 37		20.0 21.0	32.0 34	A=B Output		100		N/A			N/A	
54/74LS190 54 74	Enable Others		0.3 0.1	-15		-100		20.0 NOTE 1	35.0		N/A			N/A			N/A			N/A	
54/74LS191 54 74	Enable Others		0.3 0.1	-15		-100		20.0 NOTE 1	35.0		N/A			N/A			N/A			N/A	
54/74LS192 54 74			0.1	-15		-100		20.0 NOTE 14	34.0		N/A			N/A			N/A			N/A	
54/74LS193 54 74			0.1	-15		-100		20.0 NOTE 14	34.0		N/A			N/A			N/A			N/A	
54/74LS194A 54 74			0.1	-15		-100		15.0 NOTE 15	23.0		N/A			N/A			N/A			N/A	
54/74LS195A 54 74			0.1	-15		-100		14.0 NOTE 16	21.0		N/A			N/A			N/A			N/A	
54/74LS196 54 74	Data, Count/Load, CLR V_I=5.5V Clock 1 Clock 2		0.1 0.2 0.4	-15		-100		16.0 NOTE 1	27.0		N/A			N/A			N/A			N/A	
54/74LS197 54 74	CLR, Data, Count/Load V_I=5.5V Clock 1 Clock 2		0.1 0.2 0.2	-15		-100		16.0 NOTE 1	27.0		N/A			N/A			N/A			N/A	
54/74LS221 54 74			0.1	-15		-100		19	27		N/A			N/A			N/A			N/A	
54/74LS251 54 74			0.1	-15		-100		N/A		Cond A Cond B	6.1 7.1 NOTE 17	10.0 12.0		N/A				-20			20
54/74LS253 54 74			0.1	-15		-100		N/A		Cond A Cond B	7.0 8.5 NOTE 18	12.0 14.0		N/A			V_{CC}=MAX	-20		V_{CC}=MAX	20
54/74LS257 54 74	S Input Others		0.2 0.1	-15		-100		N/A		Cond.A Cond.B Cond.C	9.2 5.9 10.0 NOTE 19	16.0 10.0 17.0		N/A			V_o=0.5V	-20		V_o=2.4V	-20

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54/74LS ELECTRICAL CHARACTERISTICS (See Notes - Page 50)

		INPUT VOLTAGE (V)			OUTPUT VOLTAGE (V)					INPUT CURRENT			
PARAMETER		V_{IL} LOW LEVEL	V_{IH} HIGH LEVEL	V_{IC} CLAMP VOLTAGE	V_{OL} LOW LEVEL			V_{OH} HIGH LEVEL		I_{IL}(mA) LOW LEVEL		I_{IH}(μA) HIGH LEVEL	
TEST CONDITIONS				V_{CC}=MIN I_{IN}=-18mA	V_{CC}=MIN V_{IN}=* I_{OL}=4mA V_{OL}MAX I_{OL}=8mA@V_{OL}=0.5V			V_{CC}=MIN I_{OH}=-400μA		V_{IL}=.4V		V_{CC}=MAX	
		MIN TYP MAX	MIN TYP MAX	MIN TYP MAX	MIN	TYP	MAX	MIN	TYP	MIN	MAX	MIN TYP	MAX
								I_{OH}=-1mA (54) I_{OH}=-2.6mA (74)					
54/74LS258	54	0.7	2	-1.5	54/74	0.25	0.4	2.4	3.4	S Input	-0.8	S Input	40
	74	0.8			74	0.35	0.5	2.4	3.4	Others	-0.4	Others	20
54/74LS260	54	0.7	2	-1.5	54/74	0.25	0.4	2.5	3.4		0.36		20
	74	0.8			74	0.35	0.5	2.7	3.4				
54/74LS261	54	0.7	2	-1.5	54/74	0.25	0.4	2.5	3.4	M_{01} M_1	-0.8	M_{01} M_1	40
	74	0.8			74	0.35	0.5	2.7	3.4	Others	-0.4	Others	20
54/74LS266	54	0.7	2	-1.5	54/74	0.25	0.4	N/A			-0.6		40
	74	0.8			74	0.35	0.5						
54/74LS283	54	0.7	2	-1.5	54/74	0.25	0.4	2.5	3.6	Any A or B	-0.8	Any A or B	40
	74	0.8			74	0.35	0.5	2.7	3.6	CO	-0.4	CO	20
54/74LS290	54	0.7	2	-1.5	54/74	0.25	0.4	2.5	3.4	Any Reset	-0.4	Any Reset	20
	74	0.8			74	0.35	0.5	2.7	3.4	A Input	-2.4	A Input	40
										B Input	-3.2	B Input	80
54/74LS293	54	0.7	2	-1.5	54/74	0.25	0.4	2.5	3.4	Any Reset	-0.4	Any Reset	20
	74	0.8			74	0.35	0.5	2.7	3.4	A Input	-2.4	A Input	40
										B Input	-1.6	B Input	40
								I_{OH}=-1mA (54) I_{OH}=-2.6mA (74)					
54/74LS295A	54	0.7	2	-1.5	54/74	0.25	0.4	2.4	3.4		-0.4		20
	74	0.8			74	0.35	0.5	2.4	3.4				
54/74LS386	54	0.7	2	-1.5	54/74	0.25	0.4	2.5	3.4		-0.6		40
	74	0.8			74	0.35	0.5	2.7	3.4				
								I_{OH}=-1mA (54) I_{OH}=-2.6mA (74)					
54/74LS670	54	0.7	2	-1.5	54/74	0.25	0.4	2.4	3.4	Any D,R,W	-0.4	Any D,R,W	20
	74	0.8			74	0.35	0.5	2.4	3.4	GW Input	-0.8	CW Input	40
										GR Input	-1.2	GR Input	60

PARAMETER		INPUT CURRENT (mA) I_{IN}			OUTPUT CURRENT (mA) I_{OS} SHORT CIRCUIT			POWER SUPPLY CURRENT (mA) I_{CCL} LOW LEVEL			I_{CCH} HIGH LEVEL			I_{OH} (μA) LEAKAGE			OFF-STATE OUTPUT CURRENT (μA) I_{OZL} LOW LEVEL VOLTAGE SUPPLIED			I_{OZH} HIGH LEVEL VOLTAGE SUPPLIED		
TEST CONDITIONS		V_{CC}=MAX V_{IN}=7.0V						V_{CC}=MAX, V_{IH}=4.5V, V_{IL}=0V as appropriate						V_{CC}=MIN V_{IN}=* V_{OH}=5.5V			V_{CC}=MAX V_O=0.4V			V_{CC}=MAX V_O=2.7V		
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
54/74LS258	54 74	S Input Others		0.2 0.1	-15		-100		N/A		Cond.A Cond.B Cond.C	6.2 4.1 7.0 NOTE 19	11.0 7.0 12.0		N/A			V_o=0.5V	-20		V_o=2.4V	-20
54/74LS260	54 74			0.1	-15		-100		2.6	5.2		1.4	2.7		N/A			N/A			N/A	
54/74LS261	54 74	M_{01} M_1 Others		0.2 0.1	-15		-100		N/A			22.0 NOTE 1	38.0		N/A			N/A			N/A	
54/74LS266	54 74			0.2		N/A			N/A			8.0 NOTE 20	13.0			100		N/A			N/A	
54/74LS283	54 74	Any A or B CO		0.2 0.1	-15		-100	Cond.A	22.0 NOTE 21	39.0	Cond.B	19.0 NOTE 21	34.0		N/A			N/A			N/A	
54/74LS290	54 74	V_I=7.0V Any Reset V_I=5.5V A Input B Input		 0.1 0.2 0.4	-15		-100		N/A			9.0 NOTE 4	15.0		N/A			N/A			N/A	
54/74LS293	54 74	V_I=7.0V Any Reset A Input B Input		 0.1 0.2 0.2	-15		-100		N/A			9.0 NOTE 4	15.0		N/A			N/A			N/A	
54/74LS295A	54 74			0.1	-15		-100		N/A		Cond.A Cond.B	14.0 15.0 NOTE 22	23.0 25.0		N/A			N/A			N/A	
54/74LS386	54 74			0.2	-15		-100		N/A			6.1 NOTE 1	10.0		N/A			N/A			N/A	
54/74LS670	54 74	Any D,R,W GW Input GR Input		0.1 0.2 0.3	-15		-100		N/A			30.0	50.0		N/A			V_{CC}=MAX	-20		V_{CC}=MAX	20

54/74S ELECTRICAL CHARACTERISTICS (See Notes — Page 50)

		INPUT VOLTAGE									OUTPUT VOLTAGE						INPUT CURRENT		
PARAMETER		V_{IL} (V) LOW LEVEL			V_{IH} (V) HIGH LEVEL			V_{IC} (V) CLAMP VOLTAGE			V_{OL} (V) LOW LEVEL			V_{OH} (V) HIGH LEVEL			I_{IL} (mA) LOW LEVEL		
TEST CONDITIONS		V_{CC}=MIN			V_{CC}=MIN			V_{CC}=MIN I_I=-18 mA			V_{CC}=MIN V_{IN}=* I_{OL}=20 mA			V_{CC}=MIN V_{IN}=* I_{OH}=- 1 mA			V_{CC}=MAX V_I=0.5V		
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
54/74S00	54 74			0.8	2					-1.2			0.5	2.5 2.7	3.4 3.4				-2
54/74S02	54 74			0.8	2					-1.2			0.5	2.5 2.7	3.4 3.4				-2
54/74S03	54 74			0.8	2					-1.2			0.5						-2
54/74S04	54 74			0.8	2					-1.2			0.5	2.5 2.7	3.4 3.4				-2
54/74S05	54 74			0.8	2					-1.2			0.5						-2
54/74S08	54 74			0.8	2					-1.2			0.5	2.5 2.7	3.4 3.4				-2
54/74S09	54 74			0.8	2					-1.2			0.5					V_I=0.4V	-2
54/74S10	54 74			0.8	2					-1.2			0.5	2.5 2.7	3.4 3.4				-2
54/74S11	54 74			0.8	2					-1.2			0.5	2.5 2.7	3.4 3.4				-2
54/74S15	54 74			0.8	2					-1.2			0.5		N/A				-2
54/74S20	54 74			0.8	2					-1.2			0.5	2.5 2.7	3.4 3.4				-2
54/74S22	54 74			0.8	2					-1.2			0.5						-2
54/74S37	54 74			0.8	2					-1.2		I_{OL}=60mA	0.5	I_{OH}=-3mA 2.5 2.7	3.4 3.4				-4
54/74S38	54 74			0.8	2					-1.2		I_{OL}=60mA	0.5						-4
54/74S40	54 74			0.8	2					-1.2		I_{OL}=60mA	0.5	I_{OH}=-3mA 2.5 2.7	3.4 3.4				-4
54/74S51	54 74			0.8	2					-1.2			0.5	I_{OH}=MAX 2.5 2.7	3.4 3.4				-2
54/74S64	54 74			0.8	2					-1.2			0.5	2.5 2.7	3.4 3.4				-2
54/74S65	54 74			0.8	2					-1.2			0.5						-2

		INPUT CURRENT						POWER SUPPLY CURRENT											
PARAMETER		I_{IH} (μA) HIGH LEVEL			I_I (mA) INPUT CURRENT			I_{OS} (mA) SHORT CIRCUIT			I_{CCL} (mA) LOW LEVEL			I_{CCH} (mA) HIGH LEVEL			I_{OH} (μA) HIGH LEVEL		
TEST CONDITIONS		V_{CC}=MAX V_I=2.7V			V_{CC}=MAX V_I=5.5V			V_{CC}=MAX			NOTE 24 V_{CC}=MAX V_{IN}=5V			NOTE 24 V_{CC}=MAX V_{IN}=0V			V_{CC}=MIN V_{IN}=* V_{OH}=5.5V		
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
54/74S00	54 74			50			1	-40		-100		5	9		2.5	4			
54/74S02	54 74			50			1	-40		-100		6.5	11.25		4.25	7.25			
54/74S03	54 74			50			1					5	9		1.5	3.3			250
54/74S04	54 74			50			1	-40		-100		5	9		2.5	4			
54/74S05	54 74			50			1					5	9		1.5	3.3			250
54/74S08	54 74			50			1	-40		-100		8.0	14.25		4.5	8			
54/74S09	54 74			50			1					8.0	14.25		4.5	8			250
54/74S10	54 74			50			1	-40		-100		5	9		2.5	4			
												V_{IN}=OV			V_{IN}=5V				
54/74S11	54 74			50			1	-40		-100		8	14		4.5	8		N/A	
												V_{IN}=OV			V_{IN}=5V				
54/74S15	54 74			50			1		N/A			8	14		3.5	6.5			250
54/74S20	54 74			50			1	-40		-100		5	9		2.5	4			
54/74S22	54 74			50			1					5	9		1.5	3.3			250
54/74S37	54 74			100			1	-50		-225		11.5	20		5	9			
54/74S38	54 74			100			1					11.5	20		5	9			250
54/74S40	54 74			100			1	-50		-225		12.5	22		5	9			
54/74S51	54 74			50			1	-40		-100		13.6	22		8.2	17.8			
54/74S64	54 74			50			1	-40		-100		8.5	16		7	12.5			
54/74S65	54 74			50			1					8.5	16		6	11			250

54/74S ELECTRICAL CHARACTERISTICS (See Notes - Page 50)

		INPUT VOLTAGE									OUTPUT VOLTAGE						INPUT CURRENT		
PARAMETER		V_{IL} (V) LOW LEVEL			V_{IH} (V) HIGH LEVEL			V_{IC} (V) CLAMP VOLTAGE			V_{OL} (V) LOW LEVEL			V_{OH} (V) HIGH LEVEL			I_{IL} (mA) LOW LEVEL		
TEST CONDITIONS		V_{CC}=MIN			V_{CC}=MIN			V_{CC}=MIN I_I=-18 mA			V_{CC}=MIN V_{IN}=* I_{OL}=20 mA			V_{CC}=MIN V_{IN}=* I_{OH}=- 1 mA			V_{CC}=MAX V_I=0.5V		
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
54/74S74	54 74			0.8	2					-1.2			0.5	2.5 2.7	3.4 3.4		Clock or Preset Clear D		-4 -6 -2
54/74S85	54 74			0.8	2					-1.2			0.5	2.5 2.7	3.4 3.4		A<B,A>B All other inputs		-2 -6
54/74S86	54 74			0.8	2					-1.2			0.5	2.5 2.7	3.4 3.4		V_I=50μA		-2
54/74S112	54 74			0.8	2					-1.2			0.5	2.5 2.7	3.4 3.4		J or K Clock Preset or Clear		-1.6 -4 -7
54/74S113	54 74			0.8	2					-1.2			0.5	2.5 2.7	3.4 3.4		J or K Clock Preset		1.6 -4 -7
54/74S114	54 74			0.8	2					-1.2			0.5	2.5 2.7	3.4 3.4		J or K Clock Preset Clear		-1.6 -8 -7 -14
54/74S133	54 74			0.8	2					-1.2			0.5	2.5 2.7	3.4 3.4				-2
54/74S134+	54 74			0.8	2					-1.2			0.5	I_{OH}=-2mA 2.4 I_{OH}=-6.5mA 2.4	 3.4 3.2				-2
54/74S135	54 74			0.8	2					-1.2			0.5	2.5 2.7	3.4 3.4				-2
54/74S138	54 74			0.8	2					-1.2			0.5	2.5 2.7	3.4 3.4				-2
54/74S139	54 74			0.8	2					-1.2			0.5	2.5 2.7	3.4 3.4				-2
54/74S151	54 74			0.8	2					-1.2			0.5	2.5 2.7	3.4 3.4				-2
54/74S153	54 74			0.8	2					-1.2			0.5	2.5 2.7	3.4 3.4				-2
54/74S157	54 74			0.8	2					-1.2			0.5	2.5 2.7	3.4 3.4		S or G Input A or B Input		-4 -2
54/74S158	54 74			0.8	2					-1.2			0.5	2.5 2.7	3.4 3.4		S or G Input A or B Input		-4 -2

		INPUT CURRENT						POWER SUPPLY CURRENT											
PARAMETER		I_{IH} (µA) HIGH LEVEL			I_I (mA) INPUT CURRENT			I_{OS} (mA) SHORT CIRCUIT			I_{CCL} (mA) LOW LEVEL			I_{CCH} (mA) HIGH LEVEL			I_{OH} (µA) HIGH LEVEL		
TEST CONDITIONS		V_{CC}=MAX V_I=2.7V			V_{CC}=MAX V_I=5.5V			V_{CC}=MAX			V_{CC}=MAX V_{IN}=5V			V_{CC}=MAX V_{IN}=0V			V_{CC}=MIN V_{IN}=* V_{OH}=5.5V		
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
54/74S74	54 74			Clock or Preset 100 Clear 150 D 50			1	-40		-100		30	38						
54/74S85	54 74			All other inputs 150 A<B,A>B 50			1	-40		-100		73 (54 W Pkg)	115 110						
54/74S86	54 74			50			1	-40		-100			75						
54/74S112	54 74			J or K 50 Clock, Preset or Clear 100			1	-40		-100		30	50						
54/74S113	54 74			Clock 50 Preset or Clear 100			1	-40		-100		30	50						
54/74S114	54 74			J or K 50 Clock or Clear 200 Preset 100			1	-40		-100		30	50						
54/74S133	54 74			50			1	-40		-100		5.5	10		3	5			
54/74S134	54 74			50			1	-40		-100	Output Control=OV Others=5V	9	16		7	13			
											Output Off Input=5V	14	25						
54/74S135	54 74			50			1	-40		-100		65	99						
54/74S138	54 74			50			1	-40		-100		49 60	74 90						
54/74S139	54 74			50			1	-40		-100		49 60	74 90						
54/74S151	54 74			50			1	-40		-100		45	70						
54/74S153	54 74			50			1	-40		-100		45	70						
54/74S157	54 74			S or G Input 100 A or B Input 50			1	-40		-100		50	78						
54/74S158	54 74			S or G Input 100 A or B Input 50			1	-40		-100		39	61						

54/74S ELECTRICAL CHARACTERISTICS (See Notes - Page 50)

		INPUT VOLTAGE									OUTPUT VOLTAGE						INPUT CURRENT		
PARAMETER		V_{IL} (V) LOW LEVEL			V_{IH} (V) HIGH LEVEL			V_{IC} (V) CLAMP VOLTAGE			V_{OL} (V) LOW LEVEL			V_{OH} (V) HIGH LEVEL			I_{IL} (mA) LOW LEVEL		
TEST CONDITIONS		V_{CC}=MIN			V_{CC}=MIN			V_{CC}=MIN, I_I=-18 mA			V_{CC}=MIN, V_{IN}=*, I_{OL}=20 mA			V_{CC}=MIN, V_{IN}=*, I_{OH}=- 1 mA			V_{CC}=MAX, V_I=0.5V		
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
								I_I=-12mA			I_{OL}=16mA			I_{OH}=5.2mA			V_I=0.4V		
54/74S172	54 74			0.8	2					-1.5			0.4	2.4					2W/R0, 2W/R1, 2W/R2, 1GW, 2GW or Clock -1.6 Any Other -.8
54/74S174	54 74			0.8	2					-1.2			0.5	2.5 2.7	3.4 3.4				-2
54/74S175	54 74			0.8	2					-1.2			0.5	2.5 2.7	3.4 3.4				-2
54/74S181	54 74			0.8	2					-1.2			0.5	2.5 2.7	3.4 3.4				V_I=0.4V Mode -2 Any A or S -6 Any S -8 Carry -10
54/74S182	54 74			0.8	2					-1.2			0.5	2.5 2.7	3.4 3.4				C_N -2 P3 -4 P2 -6 P0,P1,G3 -8 G0,G2 -14 G1 -16
54/74S194	54 74			0.8	2					-1.5			0.5	2.5 2.7	3.4 3.4				-2
								I_I=-12mA						I_{OH}=-800μA			V_I=0.4V		
54/74S195	54 74			0.8	2					-1.5	0.2	0.4		2.4	3.4				-1.6
											I_{OL}=16mA			I_{OH}=-10.3mA			V_{IL}=0.45V		
54/74S200	54			0.8	2				-0.8	-1.2		0.35	0.50	2.4 (54)				-10	-250
	74			0.85								0.35	0.45	I_{OH}=5.2mA 2.4 (74)				-10	-100
											I_{OL}=16mA			I_{OH}=-10.3mA			V_{IL}=0.45V		
54/74S201	54			0.8	2				-0.8	-1.2		0.35	0.50	2.4 (54)				-10	-250
	74			0.85								0.35	0.45	I_{OH}=5.2mA 2.4 (74)				-10	-100
											I_{OL}=16mA						V_{IL}=0.45V		
74S206	74			0.85	2				-0.8	-1.2		0.35	0.45	2.4				-10	-100

PARAMETER		INPUT CURRENT						POWER SUPPLY CURRENT											
		I_{IH} (μA) HIGH LEVEL			I_I (mA) INPUT CURRENT			I_{OS} (mA) SHORT CIRCUIT			I_{CCL} (mA) LOW LEVEL			I_{CCH} (mA) HIGH LEVEL			I_{OH} (μA) HIGH LEVEL		
TEST CONDITIONS		V_{CC}=MAX V_I=2.7V			V_{CC}=MAX V_I=5.5V			V_{CC}=MAX			V_{CC}=MAX V_{IN}=5V			V_{CC}=MAX V_{IN}=0V			V_{CC}=MIN V_{IN}=* V_{OH}=5.5V		
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
54/74S172	54 74	V_I=2.4V		40			1	-18		-55		112	170						
54/74S174	54 74			50			1	-40		-100		90							
54/74S175	54 74			50			1	-40		-100		60							
54/74S181	54 74	V_I=2.4V Mode Any a or B Any S Carry		 50 150 200 250			1	-40		-100		120 120	159 220	ICC (S54) N Pkg only		135			
54/74S182	54 74	C_N INPUT P3 P2 P0,P1 or G3 G0 or G2 G1		50 100 150 200 350 400			1	-40		-100		69 69	99 109		35				
54/74S194	54 74			50			1	-40		-100		85	135	(ICC S54S194) B pkg - 99 W pkg - 110					
54/74S195	54 74	V_I=2.4V		50			1	-40		-100		39	63						
54/74S200	54 74		1	25			1	-30		-100		80	115						
54/74S201	54 74		1	25			1	-30		-100									
74S206	74		1	25			1					80	115					1	40

54/74S ELECTRICAL CHARACTERISTICS (See Notes - Page 50)

		INPUT VOLTAGE									OUTPUT VOLTAGE						INPUT CURRENT		
PARAMETER		V_{IL} (V) LOW LEVEL			V_{IH} (V) HIGH LEVEL			V_{IC} (V) CLAMP VOLTAGE			V_{OL} (V) LOW LEVEL			V_{OH} (V) HIGH LEVEL			I_{IL} (mA) LOW LEVEL		
TEST CONDITIONS		V_{CC}=MIN			V_{CC}=MIN			V_{CC}=MIN I_I=-18 mA			V_{CC}=MIN V_{IN}=* I_{OL}=20 mA			V_{CC}=MIN V_{IN}=* I_{OH}=- 1 mA			V_{CC}=MAX V_I=0.5V		
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
54/74S251+	54			0.8	2					-1.2			0.5	I_{OH}=-2mA 2.4	3.2				-2
	74													I_{OH}=-6.5mA 2.4	3.2				
54/74S253+	54			0.8	2					-1.2			0.5	2.4	3.4				-2
	74													2.7	3.4				
54/74S257+	54			0.8	2					-1.2			0.5	I_{OH}=-2mA 2.4	3.4		S Input		-4
	74													I_{OH}=-6.5mA 2.4	3.2		Any Other		-2
54/74S258	54			0.8	2					-1.2			0.5	I_{OH}=-2mA 2.5	3.4		S Input		-4
	74													I_{OH}=-6.5mA 2.4	3.2		Any Other		-2
54/74S260	54			0.8	2					-1.2			0.5	I_{OH}=MAX 2.5	3.4				-2
	74													2.7	3.4				
54/74S280	54			0.8	2					-1.2			0.5	2.5	3.4				-2
	74													2.7	3.4				
54/74S301	54			0.8	2				-0.8	-1.2	I_{OL}=16mA	0.35	0.50				V_{IL}=0.45V	-10	-250
	74			0.85								0.35	0.45					-10	-100

†OFF-STATE INPUT CURRENT —

I_{OLL} (mA) LOW LEVEL VOLTAGE SUPPLIED	I_{OLH} (mA) HIGH LEVEL VOLTAGE SUPPLIED
V_{CC}=MAX V_O=0.4V	V_{CC}=MAX V_O=2.4V
MAX	MAX
-50	50

PARAMETER		INPUT CURRENT						POWER SUPPLY CURRENT											
		I_{IH} (μA) HIGH LEVEL			I_I (mA) INPUT CURRENT			I_{OS} (mA) SHORT CIRCUIT			I_{CCL} (mA) LOW LEVEL			I_{CCH} (mA) HIGH LEVEL			I_{OH} (μA) HIGH LEVEL		
TEST CONDITIONS		V_{CC}=MAX V_I=2.7V			V_{CC}=MAX V_I=5.5V			V_{CC}=MAX			V_{CC}=MAX V_{IN}=5V			V_{CC}=MAX V_{IN}=0V			V_{CC}=MIN V_{IN}=* V_{OH}=5.5V		
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
54/74S251	54 74			50			1	-40		-100									
54/74S253	54 74			50			1	-40		-100		45	70						
54/74S257	54 74	S Input Any Other		100 50			1	-40		-100		44	68	 HiZ	60	93 99			
54/74S258	54 74	S Input Any Other		100 50			1	-40		-100		36	56	 HiZ	52	81 87			
54/74S260	54 74			50			1	-40		-100		10.0	17.5		8.5	14.5			
54/74S280	54 74			50			1	-40		-100		67 67	99 105		ICC (S54-W Pkg)	94			
54/74S301	54 74		1	25															

LOGIC

9300/9600 SERIES ELECTRICAL CHARACTERISTICS

	INPUT VOLTAGE						OUTPUT VOLTAGE						INPUT CURRENT											
PARAMETER	V_{IL}(V) LOW LEVEL			V_{IH}(V) HIGH LEVEL			V_{OL}(V) LOW LEVEL			V_{OH}(V) HIGH LEVEL			I_{IL}(MA) LOW LEVEL			I_{IH}(UA) HIGH LEVEL			I_F LOAD CURRENT			I_R LEAKAGE CURRENT		
TEST CONDITIONS	V_{CC}=MIN			V_{CC}=MIN			V_{CC}=MIN I_{OL}=16mA			V_{CC}=MIN I_{OH}=1.2mA			V_{CC}=MAX V_{IN}=0.4V			V_{CC}=MAX V_{IN}=2.4V			V_{CC}=MAX V_F=0.45V			V_{CC}=MAX V_R=4.5V		
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
9300																								
0°C			0.85	1.9					0.45	2.4											-1.6		N/A	
+25°C			0.85	1.8				0.2	0.45	2.4	3.0			N/A			N/A			-1.0	-1.6		15	60
+75°C			0.85	1.6					0.45	2.4											-1.6			60
																				V_{CC}=4.75V				
																					-1.41			
																				-0.9	-1.41			
																					-1.41			
9301	SEE 8252 ELECTRICAL SPECIFICATIONS																							
9309																								
0°C			0.85	1.9					0.45	2.4											-1.6		N/A	
+25°C			0.85	1.8				0.21	0.45	2.4	3.0			N/A			N/A			-10	-1.6		15	60
+75°C			0.85	1.6					0.45	2.4											-1.6			60
																				V_{CC}=4.75V				
																					-1.41			
																				-91	-1.41			
																					-1.41			
-55°C			0.8	2.0					0.4	2.4											-1.6		N/A	
+25°C			0.9	1.7				0.21	0.4	2.4	2.7			N/A			N/A			-1.1	-1.6		15	60
+125°C			0.8	1.4					0.4	2.4											-1.6			60
																				V_{CC}=4.75V				
																					-1.24			
																				-.85	-1.24			
																					-1.24			
9312	SEE 8230 ELECTRICAL SPECIFICATIONS																							
											I_{OH}=-800μA													
9324			0.8	2.0				92	0.4	2.4	3.6			-1.92	-3.2		20	80		N/A			N/A	
																	V_{IN}=5V							
																		1.0mA						
								I_{OL}=9.6mA			I_{OH}=-720μA			A_O,A_1,A_2,D,$\bar{C}$			V_{IN}=5.5V							
			0.8	2.0				0.2	0.4	2.4	3.6			10	40			1.0		N/A			N/A	
														$\bar{E}$										
														15	60									
9601	SEE 8T22 ELECTRICAL SPECIFICATIONS																							
9602								I_{OL}=11.3mA			I_{OH}=0.96mA													
0°C			0.85	1.9					0.45	2.4					-1.6		N/A							
+25°C			0.85	1.8				0.2	0.45	2.4	3.6			-10	-1.6		10	60		N/A			N/A	
+75°C			0.85	1.65					0.45	2.4				V_{CC}=4.75V				60						
															-1.41									
															-1.41									
															-1.41									
								I_{OL}=9.92mA			I_{OH}=-0.96mA													
-55°C			0.85	2.0					0.4	2.4					-1.6		N/A							
+25°C			0.90	1.7				0.2	0.4	2.4	3.3			-1.1	-1.6		10	60		N/A			N/A	
+125°C			0.85	1.5					0.4	2.4					-1.6			60						
														V_{CC}=4.5V										
															-1.24									
														-0.97	-1.24									
															-1.24									

54/74 ELECTRICAL CHARACTERISTICS NOTES

1. All inputs grounded, outputs open.
2. With all outputs open, ICC is measured with Q and Q outputs high in turn. At the time of measurement, the clock input is grounded.
3. ICC is measured with outputs open, A = B grounded, and all other inputs at 4.5V.
4. ICC is measured with all outputs open, Both RO inputs grounded following momentary connection to 4.5V and all other inputs grounded.
5. ICC is measured with all outputs and serieal inputs open; A,B,C, and D inputs grounded, mode control at 4.5V and a momentary 3V then ground, applied to both clock inputs.
6. ICC is measured with clear input grounded and all other inputs and outputs open.
7. ICC is measured with outputs open and 4.5V applied to all data and clear inputs. the measurement is made after a momentary ground, then 4.5V is applied to the clock.
8. ICC is measured with inputs at 4.5V, outputs open.
9. ICCL is measured with clock input high, then again with the clock input low with all other inputs low and all outputs open.
10. ICCH is measured with the load input high, then again with the load input low, with all other inputs high and all outputs open.
11. ICC is measured with outputs open, serial inputs grounded, the clock input at 2.4V, and a momentary ground, then 4.5V applied to clear.
12. ICC is measured under the following worst case conditions. 4.5V are applied to all data inputs and both enable inputs, all address inputs are grounded, and all outputs are open.
13. With outputs open, ICC is measured for the following conditions:
    Condition A — S0 through S3, M and A inputs are at 4.5V, all other inputs grounded.
    Conditon B — S0 through S3 and M are at 4.5V, all other inputs are grounded.
14. ICC is measured with outputs open, clear and load inputs grounded, and all other inputs at 4.5V.
15. With all outputs open, inputs A through D grounded, and 4.5V applied to S0, S1, clear and the serial inputs, ICC is tested with a momentary ground then 4.5V applied to the clock.
16. With all outputs open, shift/load grounded and 4.5V applied to the J,K and data inputs, ICC is measured by applying a momentary ground, followed by 4.5V to clear, then applying a momentary ground followed by a 4.5V to clock.
17. ICC is measured with the outputs open and all data and select inputs at 4.5V under the following conditions:
    Condition A — Strobe grounded
    Condition B — Strobe grounded
18. ICC is measured with the outputs open and all data and select inputs at 4.5V under the following conditions:
    Condition A — All inputs grounded.
    Condition B — Output control at 4.5V, all inputs grounded.
19. ICC is measured with all outputs open and all possible inputs grounded while achieving the stated output conditions.
20. ICC is measured with one input of each gate at 4.5V, the other inputs grounded, and the outputs open.
21. ICC is measured with outputs open under the following conditions:
    Condition A — All inputs grounded.
    Condition B — All B inputs low, other at 4.5V
    Condition C — All inputs at 4.5V
22. ICC is measured with the outputs open, the serial input and mode control at 4.5V, and the data inputs grounded under the following conditions:
    Condition A — Output control at 4.5V and a momentary 3v then ground applied to clock input.
    Condition B — Output control and clock input grounded.
23. ICCL
24. 54/74S ICC limits are per gate.

ABSOLUTE MAXIMUM RATINGS

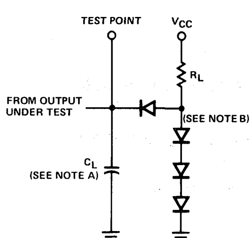
(Over Operating Free-Air Temperature Range Unless Otherwise Noted)

V_{CC}	Supply Voltage[1]	7V
V_{IN}	Input Voltage[1]	5.5V
	Intermitter Voltage[2]	5.5V
T_A	Operating Free-Air Temperature Range	
	Series 54 Circuits	−55 C to 125 C
	Series 74 Circuits	0 C to 70 C
	Storage Temperature Range	−65 C to 150 C

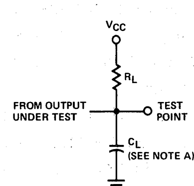
NOTES
1. Voltage values, except intermitter voltage, are with respect to network ground terminals.
2. This is the voltage between two emitters of a multiple-emitter transistor.
3. Output sink current tests one output at a time.

TEST CIRCUITS

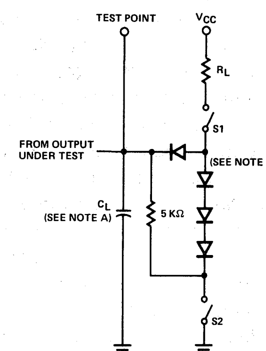
LOAD CIRCUIT FOR BI-STATE TOTEM-POLE OUTPUTS



LOAD CIRCUIT FOR OPEN-COLLECTOR OUTPUTS



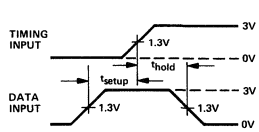
LOAD CIRCUIT FOR THREE-STATE OUTPUTS



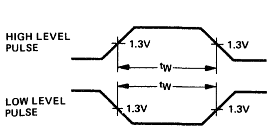
NOTES
A. C_L includes probe and jig capacitance.
B. All diodes are 1N916 or 1N3064.

WAVEFORMS

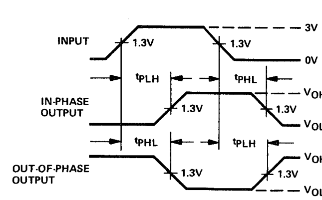
VOLTAGE WAVEFORMS SETUP AND HOLD TIMES



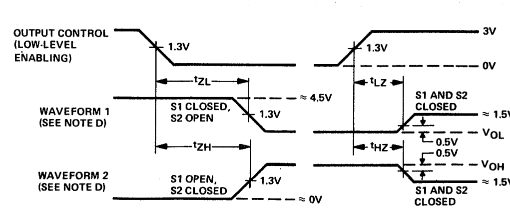
VOLTAGE WAVEFORMS PULSE WIDTHS



VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS



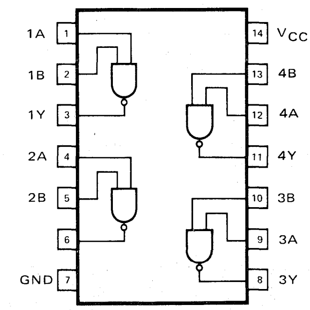
NOTES
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.
E. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1MHz, $Z_{out} \approx 50\Omega$ and $t_r \leq 15$ ns, $t_f \leq 6$ ns.

SPEED/PACKAGE AVAILABILITY

54	F,W	74	A,F
54H	F,W	74H	A,F
54LS	F,W	74LS	A,F
54S	F,W	74S	A,F

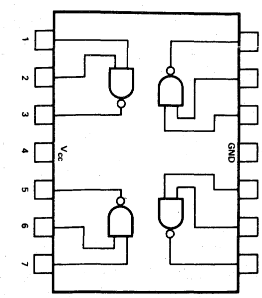
PIN CONFIGURATION

54/74, 54/74LS, 54S
A,F,W PACKAGE



Positive logic: $Y = \overline{AB}$

54/74H
W PACKAGE



SWITCHING CHARACTERISTICS $V_{CC} = 5V$, $T_A = 25°C$

TEST CONDITIONS	54/74 C_L=15pF R_L=400Ω			54/74H C_L=25pF R_L=280Ω			54/74LS C_L=15pF R_L=2kΩ			54/74S C_L=15pF R_L=280Ω			
PARAMETER	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
Propagation delay time t_{PLH} Low-to-high		11	22		5.9	10		9	15	2	3 C_L=50pF 4.5	4.5	ns
t_{PHL} High-to-low		7	15		6.2	10		10	15	2	3 C_L=50pF 5	5	ns

Load circuit and typical waveforms are shown at the front of section.

LOGIC

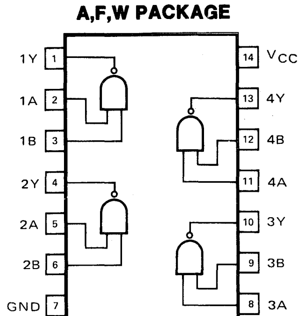
QUAD 2-INPUT NAND GATE W/OPEN COLLECTOR OUTPUTS 54/7401

SPEED/PACKAGE AVAILABILITY

54	F,W	74	A,F
54H	F,W	74H	A,F
54LS	F,W	74LS	A,F

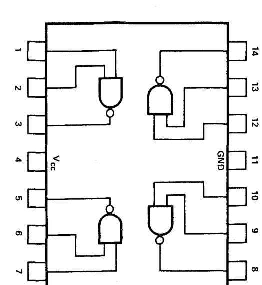
PIN CONFIGURATION

74,54/74LS
A,F,W PACKAGE

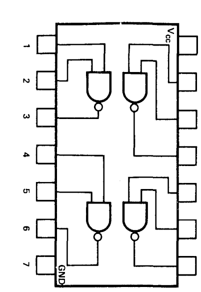


Positive logic: $Y = \overline{AB}$

54,54H
W PACKAGE



54H/74H
A,F PACKAGE



QUAD 2-INPUT NAND GATE W/OPEN COLLECTOR OUTPUTS — 54/7401

SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

TEST CONDITIONS	54/74 C_L=15pF R_L=400Ω			54/74H C_L=25pF R_L=280Ω			54/74LS C_L=15pF R_L=2kΩ			
PARAMETER	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
Propagation delay time										
t_{PLH} Low-to-high		35	45		10	15		17	32	ns
t_{PHL} High-to-low		8	15		7.5	12		15	28	ns

Load circuit and typical waveforms are shown at the front of section.

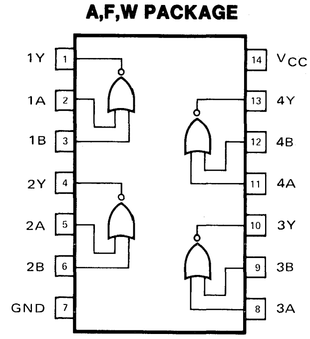
QUAD 2-INPUT NOR GATE — 54/7402

SPEED/PACKAGE AVAILABILITY

54	F,W	74	A,F
54LS	F,W	74LS	A,F
54S	F,W	74S	A,F

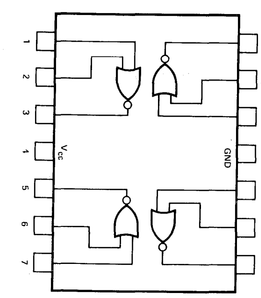
PIN CONFIGURATION

74,54/74LS, 54/74S
A,F,W PACKAGE



Positive logic: $Y = \overline{A+B}$

54
W PACKAGE



SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

TEST CONDITIONS	54/74 C_L=15pF R_L=400Ω			54/74LS C_L=15pF R_L=2kΩ			54/74S C_L=15pF R_L=280Ω			
PARAMETER	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
Propagation delay time										
t_{PLH} Low-to-high		12	22		8	15		3.5	5.5	ns
t_{PHL} High-to-low		8	15		8	15		3.5	5.5	ns

Load circuit and typical waveforms are shown at the front of section.

QUAD 2-INPUT NAND GATE W/OPEN COLLECTOR OUTPUTS 54/7403

SPEED/PACKAGE AVAILABILITY

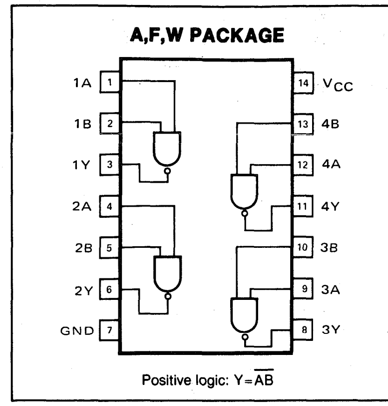
54	F	74	A,F
54LS	F,W	74LS	A,F
54S	F,W	74S	A,F

SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

TEST CONDITIONS	54/74 C_L=15pF R_L=400Ω			54/74LS C_L=15pF R_L=2kΩ			54/74S C_L=15pF R_L=280Ω			
PARAMETER	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
Propagation delay time t_{PLH} Low-to-high		35	45		17	32	2	5 (C_L=50pF: 7.5)	7.5	ns
t_{PHL} High-to-low		8	15		15	28	2	4.5 (C_L=50pF: 7)	7	ns

Load circuit and typical waveforms are shown at the front of section.

PIN CONFIGURATION



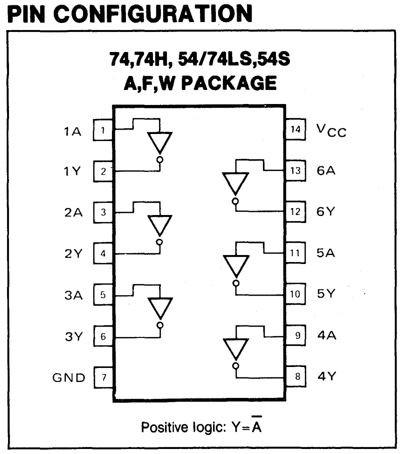
Positive logic: Y=$\overline{AB}$

HEX INVERTER 54/7404

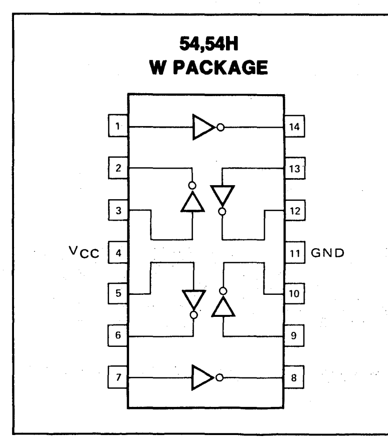
SPEED/PACKAGE AVAILABILITY

54	F,W	74	A,F
54H	F,W	74H	A,F
54LS	F,W	74LS	A,F
54S	F,W	74S	A,F

PIN CONFIGURATION



Positive logic: Y=$\overline{A}$



SWITCHING CHARACTERISTICS V_{CC}= 5V, T_A = 25°C

TEST CONDITIONS	54/74 C_L=15pF R_L=400Ω			54/74H C_L=25pF R_L=280Ω			54/74LS C_L=15pF R_L=2kΩ			54/74S C_L=15pF R_L=280Ω			
PARAMETER	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
Propagation delay time t_{PLH} Low-to-high		12	22		6	10		5	15	2	3 (C_L=50pF: 4.5)	4.5	ns
t_{PHL} High-to-low		8	15		6.5	10		9	15	2	3 (C_L=50pF: 5)	5	ns

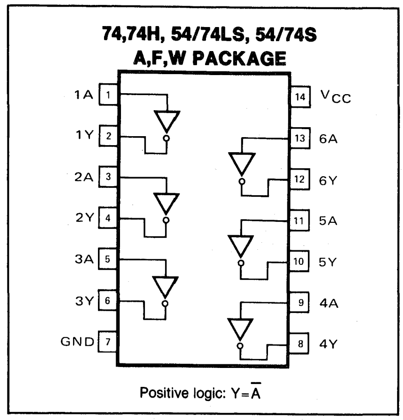
Load circuit and typical waveforms are shown at the front of section.

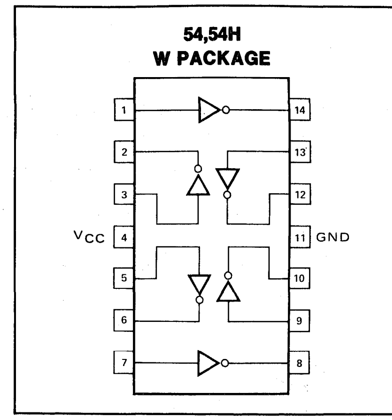
HEX INVERTER W/OPEN COLLECTOR OUTPUTS — 54/7405

SPEED/PACKAGE AVAILABILITY

54	F,W	74	A,F
54H	F,W	74H	A,F
54LS	F,W	74LS	A,F
54S	F,W	74S	A,F

PIN CONFIGURATION





SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

TEST CONDITIONS	54/74 C_L=15pF R_L=400Ω			54/74H C_L=25pF R_L=280Ω			54/74LS C_L=15pF R_L=2kΩ			54/74S C_L=15pF R_L=280Ω			
PARAMETER	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNIT**
Propagation delay time t_{PLH} Low-to-high		40	55		10	15		17	32	2	5 C_L=50pF 7.5	7.5	ns
t_{PHL} High-to-low		8	15		7.5	12		15	28	2	4.5 C_L=50pF 7	7	ns

Load circuit and typical waveforms are shown at the front of section.

HEX INVERTER BUFFER/DRIVER — 54/7406

SPEED/PACKAGE AVAILABILITY

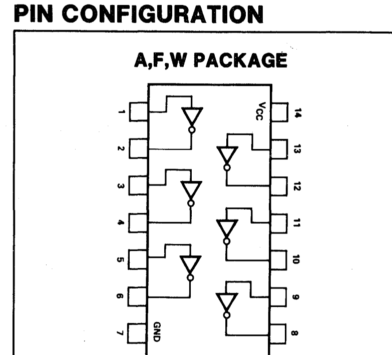
54 F,W 74 A,F

SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

TEST CONDITIONS	54/74 C_L=15pF R_L=110Ω			
PARAMETER	**MIN**	**TYP**	**MAX**	**UNIT**
Propagation delay time t_{PLH} Low-to-high		10	15	ns
t_{PHL} High-to-low				

Load circuit and typical waveforms are shown at the front of section.

PIN CONFIGURATION



HEX BUFFER/DRIVER 54/7407

SPEED/PACKAGE AVAILABILITY

54 F,W 74 A,F

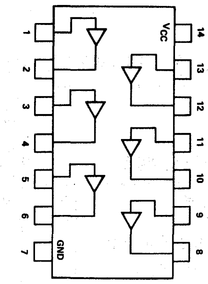
SWITCHING CHARACTERISTICS V_{CC}= 5V, T_A = 25°C

TEST CONDITIONS	54/74 C_L=15pF R_L=110Ω			
PARAMETER	MIN	TYP	MAX	UNIT
Propagation delay time t_{PLH} Low-to-high		6	10	ns
t_{PHL} High-to-low		20	30	ns

Load circuit and typical waveforms are shown at the front of section.

PIN CONFIGURATION

A,F,W PACKAGE



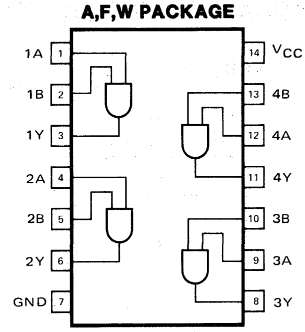
QUAD 2-INPUT AND GATE 54/7408

SPEED/PACKAGE AVAILABILITY

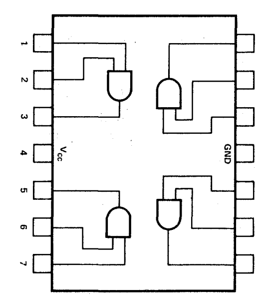
54 F,W 74 A,F
54H F,W 74H A,F
54LS F,W 74LS A,F
54S F,W 74S A,F

PIN CONFIGURATION

54/74,74H,54/74LS, 54/74S
A,F,W PACKAGE



54H
W PACKAGE



SWITCHING CHARACTERISTICS V_{CC}= 5V, T_A = 25°C

TEST CONDITIONS	54/74 C_L=15pF R_L=400Ω			54/74H C_L=25pF R_L=280Ω			54/74LS C_L=15pF R_L=2kΩ			54/74S C_L=15pF R_L=280Ω			
PARAMETER	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
Propagation delay time t_{PLH} Low-to-high		17.5	27		7.6	12		8.5	15		4.5 C_L=50pF 6	7	ns
t_{PHL} High-to-low		12	19		8.8	12		8	20		5 C_L=50pF 7.5	7.5	ns

Load circuit and typical waveforms are shown at the front of section.

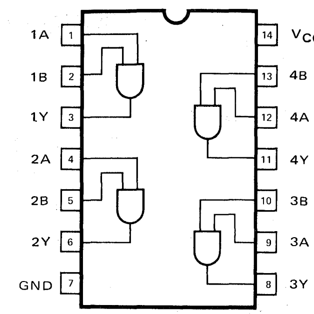
QUAD 2-INPUT AND GATE W/OPEN COLLECTOR OUTPUTS 54/7409

SPEED/PACKAGE AVAILABILITY

54	F,W	74	A,F
54LS	F,W	74LS	A,F
54S	F,W	74S	A,F

PIN CONFIGURATION

A,F,W PACKAGE



Positive logic: Y = AB

SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

TEST CONDITIONS	54/74 C_L=15pF R_L=400Ω			54/74LS C_L=15pF R_L=2kΩ			54/74S C_L=15pF R_L=280Ω			
PARAMETER	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
Propagation delay time t_{PLH} Low-to-high		21	32		20	35		6.5 C_L=50pF 9	10	ns
t_{PHL} High-to-low		16	24		20	35		6.5 C_L=50pF 9	10	ns

Load circuit and typical waveforms are shown at the front of section.

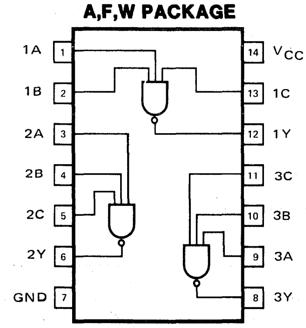
TRIPLE 3-INPUT NAND GATE 54/7410

SPEED/PACKAGE AVAILABILITY

54	F,W	74	A,F
54H	F,W	74H	A,F
54LS	F,W	74LS	A,F
54S	F,W	74S	A,F

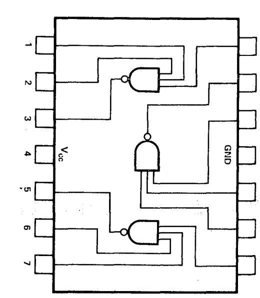
PIN CONFIGURATION

74,74H,54/74LS, 54/74S
A,F,W PACKAGE



Positive logic: Y=$\overline{ABC}$

54,54H
W PACKAGE



SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

TEST CONDITIONS	54/74 C_L=15pF R_L=400Ω			54/74H C_L=25pF R_L=280Ω			54/74LS C_L=15pF R_L=2kΩ			54/74S C_L=15pF R_L=280Ω			
PARAMETER	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
Propagation delay time t_{PLH} Low-to-high		11	22		5.9	10		5	15	2	3 C_L=50pF 4.5	4.5	ns
t_{PHL} High-to-low		7	15		6.3	10		9	15	2	3 C_L=50pF 5	5	ns

Load circuit and typical waveforms are shown at the front of section.

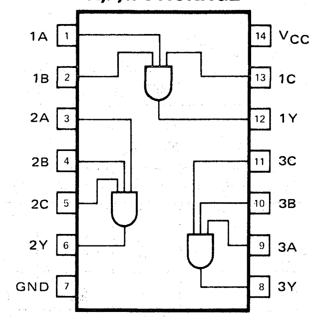
TRIPLE 3-INPUT AND GATE 54/7411

SPEED/PACKAGE AVAILABILITY

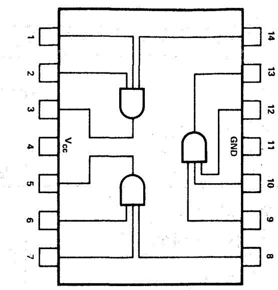
54	F,W	74	A,F
54H	F,W	74H	A,F
54LS	F,W	74LS	A,F
54S	F,W	74S	A,F

PIN CONFIGURATION

74,74H,54/74LS, 54/74S
A,F,W PACKAGE



54,54H
W PACKAGE



SWITCHING CHARACTERISTICS V_{CC}= 5V, T_A = 25°C

TEST CONDITIONS	54/74 C_L=15pF R_L=400Ω			54/74H C_L=25pF R_L=280Ω			54/74LS C_L=15pF R_L=2kΩ			54/74S C_L=15pF R_L=280Ω			
PARAMETER	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
Propagation delay time t_{PLH} Low-to-high		17.5	27		7.6	12		9	15	2.5	4.5 C_L=50pF 6	7	ns
t_{PHL} High-to-low		12	19		8.8	12		9	20	2.5	5 C_L=50pF 7.5	7.5	ns

Load circuit and typical waveforms are shown at the front of section.

LOGIC

TRIPLE 3-INPUT NAND GATE W/OPEN COLLECTOR OUTPUTS 54/7412

SPEED/PACKAGE AVAILABILITY

54LS F,W 74LS A,F

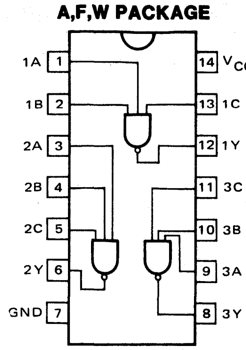
SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

PARAMETER		TEST CONDITIONS	LIMITS MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 15pF, R_L = 2kΩ		17	32	ns
t_{PHL}	Propagation delay time, high-to-low-level output			15	28	ns

Load circuit and typical waveforms are shown at the front of section.

PIN CONFIGURATION

A,F,W PACKAGE

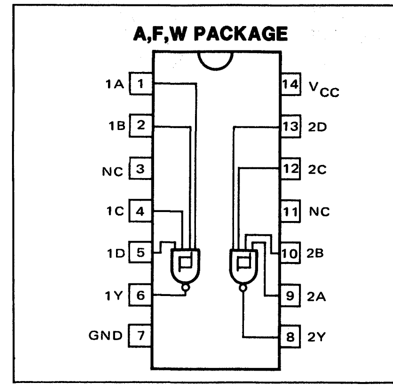


positive logic: $Y=\overline{ABC}$

SPEED/PACKAGE AVAILABILITY

54	F,W	74	A,F
54LS	F,W	74LS	A,F

PIN CONFIGURATION



SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

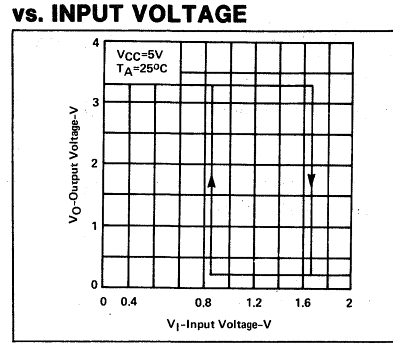
TEST CONDITIONS	54/74 C_L=15pF R_L=400Ω			54/74LS C_L=15pF R_L=2kΩ			
PARAMETER	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
Propagation delay time t_{PLH} Low-to-high		18	27		18	27	ns
t_{PHL} High-to-low		15	22		15	22	ns

Load circuit and typical waveforms are shown at the front of section.

HYSTERESIS THRESHOLDS

PARAMETER	54/74			54/74LS			
	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
VT + positive going threshold	1.5	1.7	2.0	1.5	1.7	1.9	V
VT - negative going threshold	0.6	0.9	1.1	0.6	0.8	1.0	V
Hysteresis	0.4	0.8					V

OUTPUT VOLTAGE vs. INPUT VOLTAGE



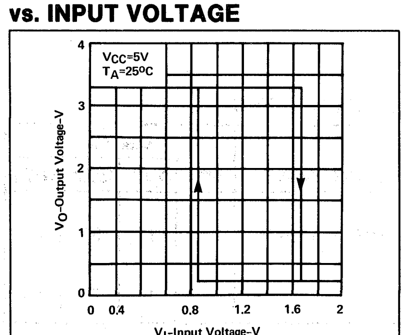
HYSTERESIS VS. TEMPERATURE-TYPICAL VALUES

PARAMETER		54/74LS			UNIT
		-55°C	25°C	+125°C	
V_{T+}	Positive going threshold	1.75	1.71	1.68	V
V_{T-}	Negative going threshold	.91	.83	.86	V
	Hysteresis	.84	.83	.82	V

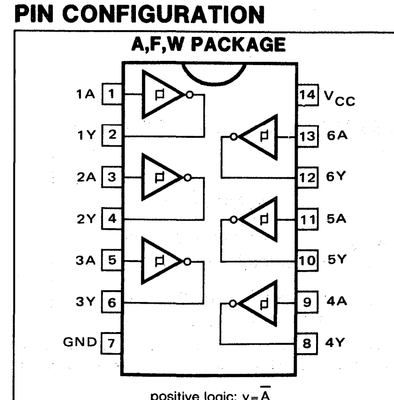
SPEED/PACKAGE AVAILABILITY

54	F,W	74	A,F
54LS	F,W	74LS	A,F

OUTPUT VOLTAGE vs. INPUT VOLTAGE



PIN CONFIGURATION



HYSTERESIS VS. TEMPERATURE-TYPICAL VALUES

PARAMETER	54/74LS -55°C	54/74LS +25°C	54/74LS +125°C	UNIT
V_{T+} Positive going threshold	1.75	1.71	1.68	V
V_{T-} Negative going threshold	.91	.88	.86	V
Hysteresis	.84	.83	.82	V

HYSTERESIS THRESHOLDS

	54/74			54/74LS			
	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
V_{T+}	1.5	1.7	2.0	1.5	1.7	1.9	V
V_{T-}	0.6	0.9	1.1	0.6	0.8	1.0	
Hysteresis	0.4	0.8					

SWITCHING CHARACTERISTICS $V_{CC} = 5V$, $T_A = 25°C$

TEST CONDITIONS	54/74 $C_L = 15pF$ $R_L = 400\Omega$			54/74LS $C_L = 15pF$ $R_L = 2k\Omega$			
PARAMETER	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
Propagation delay time t_{PLH} Low-to-high		15	22		15	22	ns
t_{PHL} High-to-low		15	22		15	22	ns

Load circuit and typical waveforms are shown at the front of section.

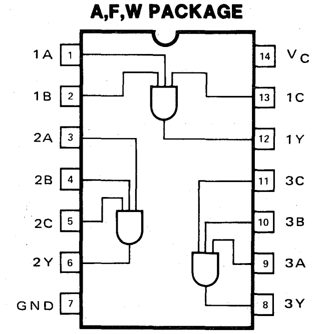
TRIPLE 3-INPUT AND GATE W/OPEN COLLECTOR OUTPUTS 54/7415

SPEED/PACKAGE AVAILABILITY

54LS F,W 74LS A,F
54S F,W 74S A,F

PIN CONFIGURATION

A,F,W PACKAGE



Positive logic: Y=AB

SWITCHING CHARACTERISTICS $V_{CC} = 5V$, $T_A = 25°C$

TEST CONDITIONS	54/74LS $C_L = 15pF$ $R_L = 2k\Omega$			54/74S $C_L = 15pF$ $R_L = 280\Omega$			
PARAMETER	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
Propagation delay time t_{PLH} Low-to-high		20	35	2.5	5.5 $C_L = 50pF$ 8.5	8.5	ns
t_{PHL} High-to-low		20	35	2.5	6 $C_L = 50pF$ 8	9	ns

Load circuit and typical waveforms are shown at the front of section.

HEX INVERTER/BUFFER 54/7416

SPEED/PACKAGE AVAILABILITY

54 F,W 74 A,F

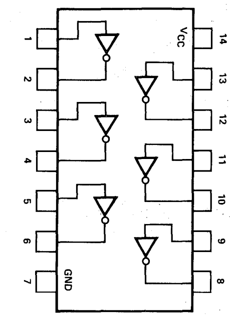
SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

TEST CONDITIONS	54/74 C_L=15pF R_L=110Ω			
PARAMETER	MIN	TYP	MAX	UNIT
Propagation delay time t_{PLH} Low-to-high		10	15	ns
t_{PHL} High-to-low		15	23	ns

Load circuit and typical waveforms are shown at the front of section.

PIN CONFIGURATION

A,F,W PACKAGE



HEX BUFFER/DRIVER 54/7417

SPEED/PACKAGE AVAILABILITY

54 F,W 74 A,F

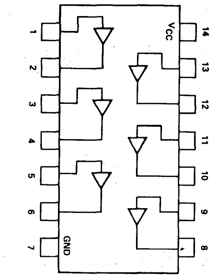
SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

TEST CONDITIONS	54/74 C_L=15pF R_L=110Ω			
PARAMETER	MIN	TYP	MAX	UNIT
Propagation delay time t_{PLH} Low-to-high		6	10	ns
t_{PHL} High-to-low		20	30	ns

Load circuit and typical waveforms are shown at the front of section.

PIN CONFIGURATION

A,F,W PACKAGE



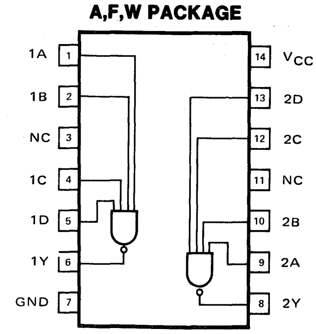
DUAL 4-INPUT NAND GATE 54/7420

SPEED/PACKAGE AVAILABILITY

54	F,W	74	A,F
54H	F,W	74H	A,F
54LS	F,W	74LS	A,F
54S	F,W	75S	A,F

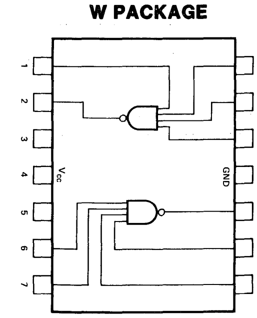
PIN CONFIGURATION

74,74H,54/74LS,54/74S
A,F,W PACKAGE



Positive logic: $Y=\overline{ABCD}$

54,54H
W PACKAGE



DUAL 4-INPUT NAND GATE 54/7420

SWITCHING CHARACTERISTICS $V_{CC} = 5V$, $T_A = 25°C$

TEST CONDITIONS	54/74 $C_L=15pF$ $R_L=400\Omega$			54/74H $C_L=25pF$ $R_L=280\Omega$			54/74LS $C_L=15pF$ $R_L=2k\Omega$			54/74S $C_L=15pF$ $R_L=280\Omega$			
PARAMETER	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
Propagation delay time t_{PLH} Low-to-high		12	22		6	10		5	15	2	3	4.5	ns
											$C_L=50pF$ 4.5		
t_{PHL} High-to-low		8	15		7	10		9	15	2	3	5	ns
											$C_L=50pF$ 5		

Load circuit and typical waveforms are shown at the front of section.

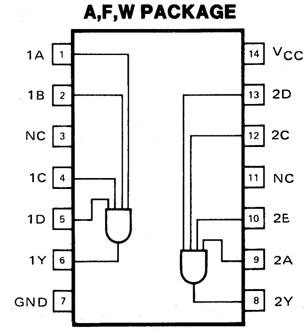
DUAL 4-INPUT AND GATE 54/7421

SPEED/PACKAGE AVAILABILITY

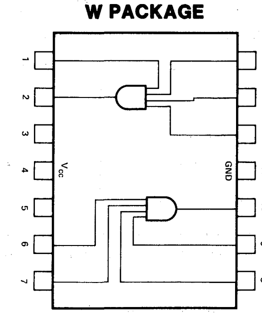
54	F,W	74	A,F
54H	F,W	74H	A,F
54LS	F,W	74LS	A,F

PIN CONFIGURATION

74,74H,54/74LS
A,F,W PACKAGE



54,54H
W PACKAGE



SWITCHING CHARACTERISTICS $V_{CC} = 5V$, $T_A = 25°C$

TEST CONDITIONS	54/74 $C_L=15pF$ $R_L=400\Omega$			54/74H $C_L=25pF$ $R_L=280\Omega$			54/74LS $C_L=15pF$ $R_L=2k\Omega$			
PARAMETER	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
Propagation delay time t_{PLH} Low-to-high		17.5	27		7.6	12		9	15	ns
t_{PHL} High-to-low		12	19		8.8	12		9	20	ns

Load circuit and typical waveforms are shown at the front of section.

LOGIC

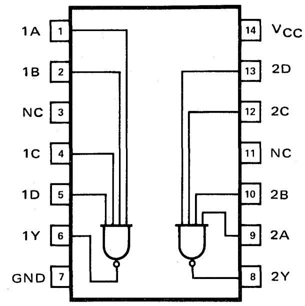
DUAL 4-INPUT NAND GATE W/OPEN COLLECTOR OUTPUTS — 54/7422

SPEED/PACKAGE AVAILABILITY

54H	F,W	74H	A,F
54LS	F,W	74LS	A,F
54S	F,W	74S	A,F

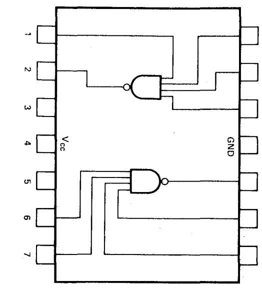
PIN CONFIGURATION

74H,54/74LS,54/74S
A,F,W PACKAGE



Positive logic: Y=$\overline{ABCD}$
NC-No internal connection

54H
W PACKAGE



SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

	54/74H			54/74LS			54/74S			
TEST CONDITIONS	C_L=25pF R_L=280Ω			C_L=15pF R_L=2kΩ			C_L=15pF R_L=280Ω			
PARAMETER	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
Propagation delay time t_{PLH} Low-to-high		10	15		17	32	2	5	7.5	ns
								C_L=50pF 7.5		
t_{PHL} High-to-low		7.5	12		15	28	2	4.5	7	ns
								C_L=50pF 7		

Load circuit and typical waveforms are shown at the front of section.

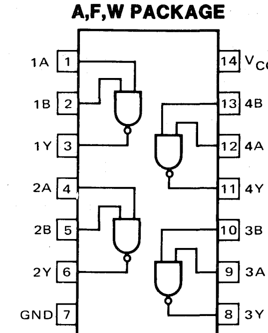
QUAD 2-INPUT NAND GATE W/OPEN COLLECTOR OUTPUTS — 54/7426

SPEED/PACKAGE AVAILABILITY

54	F	74	A,F
54LS	F,W	74LS	A,F

PIN CONFIGURATION

A,F,W PACKAGE



SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

	54/74			54/74LS			
TEST CONDITIONS	C_L=15pF R_L=1kΩ			C_L=15pF R_L=2kΩ			
PARAMETER	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
Propagation delay time t_{PLH} Low-to-high		16	24		17	32	ns
t_{PHL} High-to-low		11	17		15	28	ns

Load circuit and typical waveforms are shown at the front of section.

TRIPLE 3-INPUT NOR GATE — 54/7427

SPEED/PACKAGE AVAILABILITY

54 F,W — 74 A,F
54LS F,W — 74LS A,F

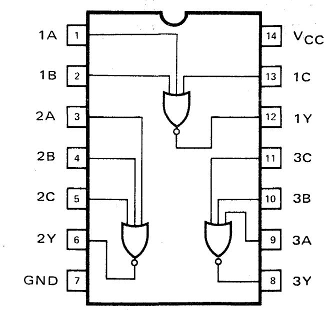
SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

TEST CONDITIONS	54/74 C_L=15pF R_L=400Ω			54/74LS C_L=15pF R_L=2kΩ			
PARAMETER	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
Propagation delay time t_{PLH} Low-to-high		7	11		5	15	ns
t_{PHL} High-to-low		10	15		9	15	ns

Load circuit and typical waveforms are shown at the front of section.

PIN CONFIGURATION

A,F,W PACKAGE



Positive logic: $Y=\overline{A+B+C}$

QUAD 2-INPUT NOR BUFFER — 54/7428

SPEED/PACKAGE AVAILABILITY

54 F,W — 74 A,F
54LS F,W — 74LS A,F

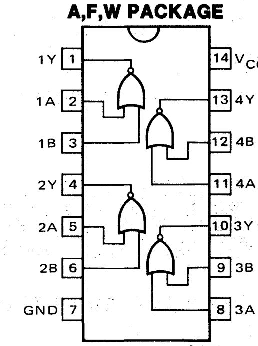
SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

TEST CONDITIONS	54/74 C_L=50pF R_L=133Ω			54/74LS C_L=45pF R_L=667Ω			
PARAMETER	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
Propagation delay time t_{PLH} Low-to-high		6	9		12	24	ns
	C_L=150pF	10	15				
t_{PHL} High-to-low		8	12		12	24	ns
	C_L=150pF	12	18				

Load circuit and typical waveforms are shown at the front of section.

PIN CONFIGURATION

A,F,W PACKAGE



Positive logic: $Y=\overline{A+B}$

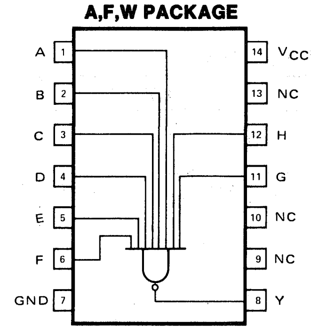
8-INPUT NAND GATE — 54/7430

SPEED/PACKAGE AVAILABILITY

54	F,W	74	A,F
54H	F,W	74H	A,F
54LS	F,W	74LS	A,F

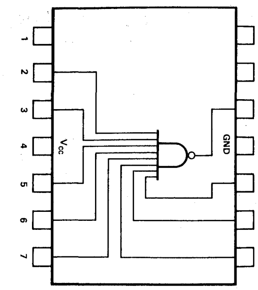
PIN CONFIGURATION

74, 74H, 54/74LS
A,F,W PACKAGE



Positive logic: $y = \overline{ABCDEFGH}$

54, 54H
W PACKAGE



SWITCHING CHARACTERISTICS $V_{CC} = 5V$, $T_A = 25°C$

TEST CONDITIONS	54/74 $C_L=15pF$ $R_L=400\Omega$			54/74H $C_L=25pF$ $R_L=280\Omega$			54/74LS $C_L=15pF$ $R_L=2k\Omega$			
PARAMETER	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNIT**
Propagation delay time t_{PLH} Low-to-high		13	22		6.8	10		5	15	ns
t_{PHL} High-to-low		8	15		8.9	12		9	20	ns

Load circuit and typical waveforms are shown at the front of section.

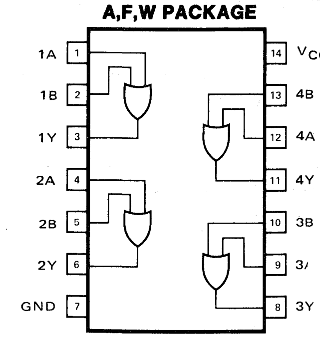
QUAD 2-INPUT OR GATE — 54/7432

SPEED/PACKAGE AVAILABILITY

54	F,W	74	A,F
54LS	F,W	74LS	A,F

PIN CONFIGURATION

A,F,W PACKAGE



Positive logic: $y = A+B$

SWITCHING CHARACTERISTICS $V_{CC} = 5V$, $T_A = 25°C$

TEST CONDITIONS	54/74 $C_L=15pF$ $R_L=400\Omega$			54/74LS $C_L=15pF$ $R_L=2k\Omega$			
PARAMETER	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNIT**
Propagation delay time t_{PLH} Low-to-high		10	15		9	22	ns
t_{PHL} High-to-low		14	22		9	22	ns

Load circuit and typical waveforms are shown at the front of section.

QUAD 2-INPUT NOR BUFFER W/OPEN COLLECTOR OUTPUTS 54/7433

SPEED/PACKAGE AVAILABILITY

54	F,W	74	A,F
54LS	F,W	74LS	A,F

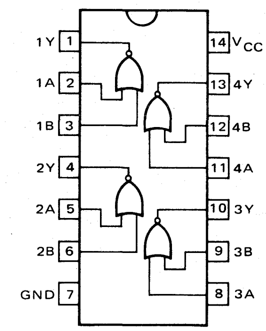
SWITCHING CHARACTERISTICS $V_{CC} = 5V$, $T_A = 25°C$

TEST CONDITIONS	54/74 $C_L=50pF$ $R_L=133\Omega$			54/74LS $C_L=45pF$ $R_L=667\Omega$			
PARAMETER	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNIT**
Propagation delay time							
t_{PLH} Low-to-high		10	15		20	32	ns
	$C_L=150pF$						
		15	22				
t_{PHL} High-to-low		12	18		18	28	ns
	$C_L=150pF$						
		16	24				

Load circuit and typical waveforms are shown at the front of section.

PIN CONFIGURATION

A,F,W PACKAGE



Positive logic: $y = \overline{A+B}$

QUAD 2-INPUT NAND BUFFER 54/7437

SPEED/PACKAGE AVAILABILITY

54	F,W	74	A,F
54LS	F,W	74LS	A,F
54S	F,W	74S	A,F

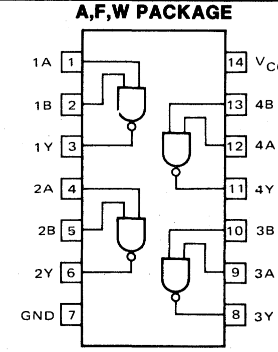
SWITCHING CHARACTERISTICS $V_{CC} = 5V$, $T_A = 25°C$

TEST CONDITIONS	54/74 $C_L=45pF$ $R_L=133\Omega$			54/74LS $C_L=45pF$ $R_L=667\Omega$			54/74S $C_L=15pF$ $R_L=93\Omega$			
PARAMETER	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNIT**
Propagation delay time										
t_{PLH} Low-to-high		13	22		12	24		4	6.5	ns
							$C_L=50pF$			
								6		
t_{PHL} High-to-low		8	15		12	24		4	6.5	ns
							$C_L=50pF$			
								6		

Load circuit and typical waveforms are shown at the front of section.

PIN CONFIGURATION

A,F,W PACKAGE



Positive logic: $y = \overline{AB}$

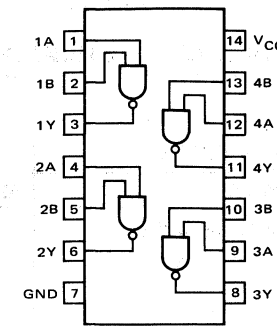
QUAD 2-INPUT NAND BUFFER W/OPEN COLLECTOR OUTPUTS 54/7438

SPEED/PACKAGE AVAILABILITY

54	F,W	74	A,F
54LS	F,W	74LS	A,F
54S	F,W	74S	A,F

PIN CONFIGURATION

A,F,W PACKAGE



Positive logic: $Y = \overline{AB}$

SWITCHING CHARACTERISTICS $V_{CC} = 5V$, $T_A = 25°C$

TEST CONDITIONS	54/74 $C_L = 45pF$ $R_L = 133\Omega$			54/74LS $C_L = 45pF$ $R_L = 667\Omega$			54/74S $C_L = 15pF$ $R_L = 93\Omega$			
PARAMETER	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNIT**
Propagation delay time t_{PLH} Low-to-high		14	22		20	32		6.5 $C_L = 50pF$ 9	10	ns
t_{PHL} High-to-low		11	18		18	28		6.5 $C_L = 50pF$ 8.5	10	ns

Load circuit and typical waveforms are shown at the front of section.

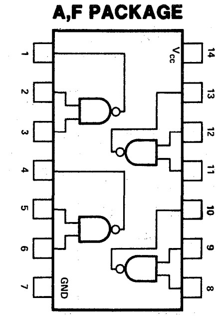
QUAD 2-INPUT NAND BUFFER 54/7439

SPEED/PACKAGE AVAILABILITY

54	F	74	A,F

PIN CONFIGURATION

A,F PACKAGE



SWITCHING CHARACTERISTICS $V_{CC} = 5V$, $T_A = 25°C$

TEST CONDITIONS	54/74 $C_L = 45pF$ $R_L = 133\Omega$			
PARAMETER	**MIN**	**TYP**	**MAX**	**UNIT**
Propagation delay time t_{PLH} Low-to-high		14	22	ns
t_{PHL} High-to-low		11	18	ns

Load circuit and typical waveforms are shown at the front of section.

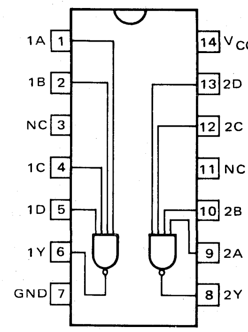
DUAL 4-INPUT NAND BUFFER — 54/7440

SPEED/PACKAGE AVAILABILITY

54	F,W	74	A,F
54H	F,W	74H	A,F
54LS	F,W	74LS	A,F
54S	F,W	74S	A,F

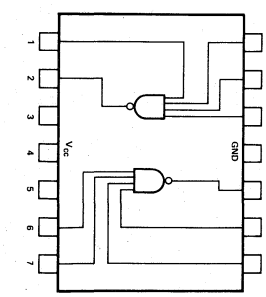
PIN CONFIGURATION

74,74H, 54/74LS, 54/74S
A,F,W PACKAGE



Positive logic: $Y = \overline{ABCD}$

54,54H
W PACKAGE



SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

TEST CONDITIONS	54/74 C_L=15pF R_L=133Ω			54/74H C_L=25pF R_L=93Ω			54/74LS C_L=45pF R_L=667Ω			54/74S C_L=50pF R_L=93Ω			
PARAMETER	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNIT**
Propagation delay time t_{PLH} Low-to-high		13	22		8.5	12		12	24	2	4 (C_L=150pF: 6)	6.5	ns
t_{PHL} High-to-low		8	15		6.5	12		12	24	2	4 (C_L=150pF: 6)	6.5	ns

Load circuit and typical waveforms are shown at the front of section.

BCD-TO-DECIMAL DECODER (1-of-10) — 54/7442

SPEED/PACKAGE AVAILABILITY

54	F,W	74	B,F
54LS	F,W	74LS	B,F

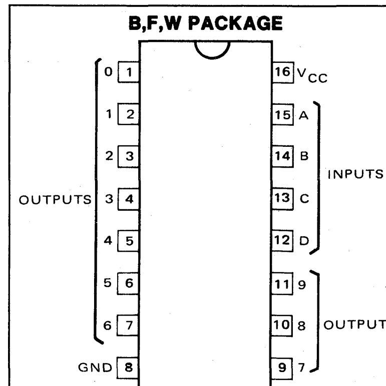
SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

TEST CONDITIONS			54/74 C_L=15pF R_L=400Ω			54/74LS C_L=15pF R_L=2KΩ			
PARAMETER	**FROM INPUT**	**TO OUTPUT**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNIT**
Propagation delay time t_{PLH} Low-to-high	A,B,C,D	through 2 logic levels		10	25		10	25	ns
t_{PHL} High-to-low				14	25		14	25	
t_{PLH} Low-to-high	A,B,C,D	through 3 logic levels		17	30		17	30	ns
t_{PHL} High-to-low				17	30		17	30	

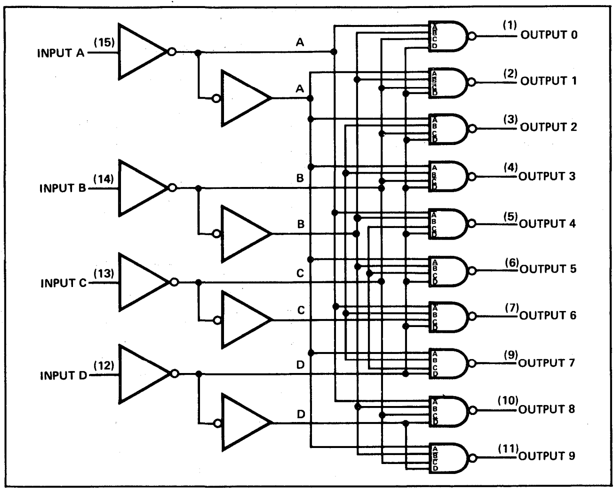
Load circuit and waveforms shown at front of section (totem pole outputs).

PIN CONFIGURATION

B,F,W PACKAGE



FUNCTIONAL BLOCK DIAGRAM



FUNCTION TABLE

NO.	BCD INPUT				DECIMAL OUTPUT									
	D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	L	L	L	L	L	H	H	H	H	H	H	H	H	H
1	L	L	L	H	H	L	H	H	H	H	H	H	H	H
2	L	L	H	L	H	H	L	H	H	H	H	H	H	H
3	L	L	H	H	H	H	H	L	H	H	H	H	H	H
4	L	H	L	L	H	H	H	H	L	H	H	H	H	H
5	L	H	L	H	H	H	H	H	H	L	H	H	H	H
6	L	H	H	L	H	H	H	H	H	H	L	H	H	H
7	L	H	H	H	H	H	H	H	H	H	H	L	H	H
8	H	L	L	L	H	H	H	H	H	H	H	H	L	H
9	H	L	L	H	H	H	H	H	H	H	H	H	H	L
INVALID	H	L	H	L	H	H	H	H	H	H	H	H	H	H
	H	L	H	H	H	H	H	H	H	H	H	H	H	H
	H	H	L	L	H	H	H	H	H	H	H	H	H	H
	H	H	L	H	H	H	H	H	H	H	H	H	H	H
	H	H	H	L	H	H	H	H	H	H	H	H	H	H
	H	H	H	H	H	H	H	H	H	H	H	H	H	H

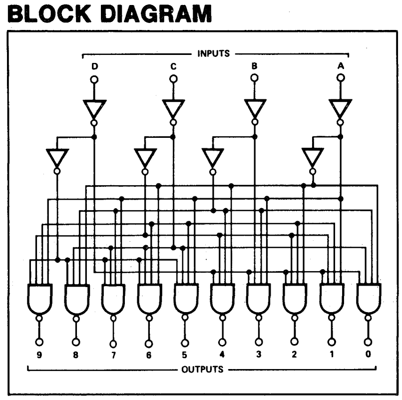
H = high level, L = low level

EXCESS 3-TO-DECIMAL DECODER 54/7443

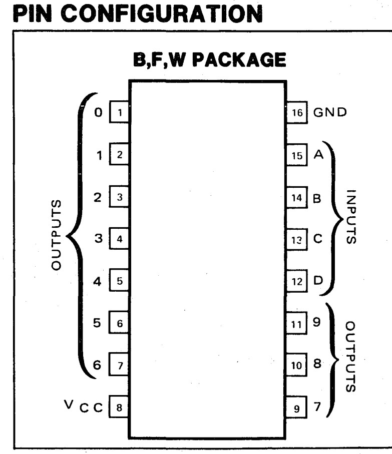
SPEED/PACKAGE AVAILABILITY

54 F,W, 74 B,F

BLOCK DIAGRAM



PIN CONFIGURATION



SWITCHING CHARACTERISTICS $V_{CC} = 5V$, $T_A = 25°C$

TEST CONDITIONS			54/74 $C_L = 15pF$ $R_L = 400\Omega$			
PARAMETER	FROM INPUT	TO OUTPUT	MIN	TYP	MAX	UNIT
Propagation delay time t_{PLH} Low-to-high		through 2 logic levels	10	17	25	ns
t_{PHL} High-to-low			10	22	30	
t_{PLH} Low-to-high		through 3 logic levels		26	35	ns
t_{PHL} High-to-low				23	35	

Load circuit and typical waveforms are shown at the front of section.

TRUTH TABLE-EXCESS INPUT / DECIMAL OUTPUT

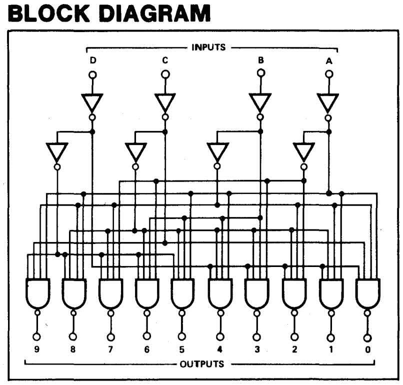
D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	0	1	1	0	1	1	1	1	1	1	1	1	1
0	1	0	0	1	0	1	1	1	1	1	1	1	1
0	1	0	1	1	1	0	1	1	1	1	1	1	1
0	1	1	0	1	1	1	0	1	1	1	1	1	1
0	1	1	1	1	1	1	1	0	1	1	1	1	1
1	0	0	0	1	1	1	1	1	0	1	1	1	1
1	0	0	1	1	1	1	1	1	1	0	1	1	1
1	0	1	0	1	1	1	1	1	1	1	0	1	1
1	0	1	1	1	1	1	1	1	1	1	1	0	1
1	1	0	0	1	1	1	1	1	1	1	1	1	0
1	1	0	1	1	1	1	1	1	1	1	1	1	1
1	1	1	0	1	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1	1	1	1	1
0	0	0	0	1	1	1	1	1	1	1	1	1	1
0	0	0	1	1	1	1	1	1	1	1	1	1	1
0	0	1	0	1	1	1	1	1	1	1	1	1	1

EXCESS 3-GRAY-TO-DECIMAL DECODER 54/7444

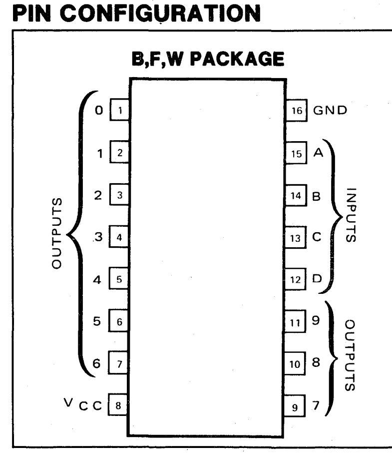
SPEED/PACKAGE AVAILABILITY

54 F,W 74 B,F

BLOCK DIAGRAM



PIN CONFIGURATION



SWITCHING CHARACTERISTICS V_{CC}=5V,T_A=25°C

TEST CONDITIONS			54/74 C_L=15pF R_L=400Ω			
PARAMETER	FROM INPUT	TO OUTPUT	MIN	TYP	MAX	UNIT
Propagation delay time						
t_{PLH} Low-to-high		through 2 logic levels	10	17	25	ns
t_{PHL} High-to-low			10	22	30	
t_{PLH} Low-to-high		through 3 logic levels		26	35	ns
t_{PHL} High-to-low				23	35	

Load circuit and typical waveforms are shown at the front of section.

TRUTH TABLE-EXCESS INPUT / DECIMAL OUTPUT

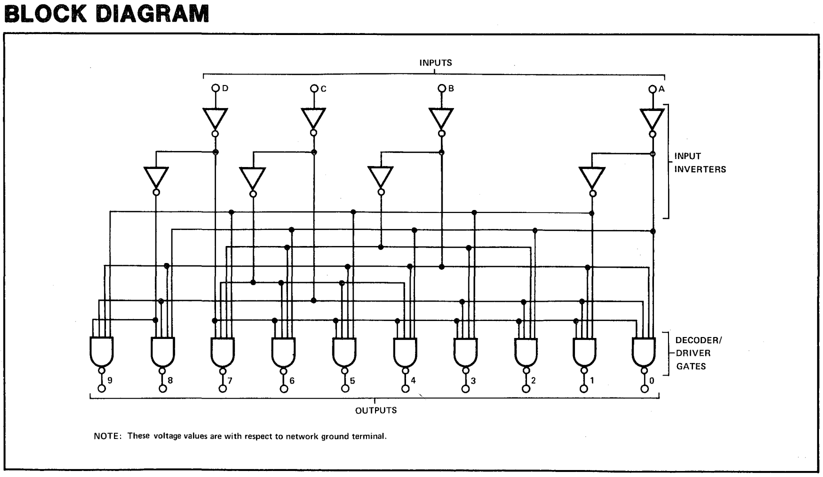
D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	0	1	0	0	1	1	1	1	1	1	1	1	1
0	1	1	0	1	0	1	1	1	1	1	1	1	1
0	1	1	1	1	1	0	1	1	1	1	1	1	1
0	1	0	1	1	1	1	0	1	1	1	1	1	1
0	1	0	0	1	1	1	1	0	1	1	1	1	1
1	1	0	0	1	1	1	1	1	0	1	1	1	1
1	1	0	1	1	1	1	1	1	1	0	1	1	1
1	1	1	1	1	1	1	1	1	1	1	0	1	1
1	1	1	0	1	1	1	1	1	1	1	1	0	1
1	0	1	0	1	1	1	1	1	1	1	1	1	0
1	0	1	1	1	1	1	1	1	1	1	1	1	1
1	0	0	1	1	1	1	1	1	1	1	1	1	1
1	0	0	0	1	1	1	1	1	1	1	1	1	1
0	0	0	0	1	1	1	1	1	1	1	1	1	1
0	0	0	1	1	1	1	1	1	1	1	1	1	1
0	0	1	1	1	1	1	1	1	1	1	1	1	1

BCD-TO-DECIMAL DECODER/DRIVER 54/7445

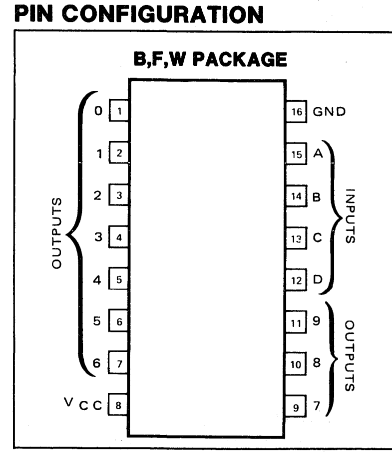
SPEED/PACKAGE AVAILABILITY

54 F,W, 74 B,F

BLOCK DIAGRAM



PIN CONFIGURATION



SWITCHING CHARACTERISTICS V_{CC}=5V, T_A=25°C

TEST CONDITIONS	54/74 C_L=15pF R_L=100Ω			
PARAMETER	**MIN**	**TYP**	**MAX**	**UNIT**
Propagation delay time t_{PLH} Low-to-high			50	ns
t_{PHL} High-to-low			50	

Load circuit and typical waveforms are shown at the front of section.

TRUTH TABLE-INPUTS

D	C	B	A
0	0	0	0
0	0	0	1
0	0	1	0
0	0	1	1
0	1	0	0
0	1	0	1
0	1	1	0
0	1	1	1
1	0	0	0
1	0	0	1
1	0	1	0
1	0	1	1
1	1	0	0
1	1	0	1
1	1	1	0
1	1	1	1

TRUTH TABLE-OUTPUTS

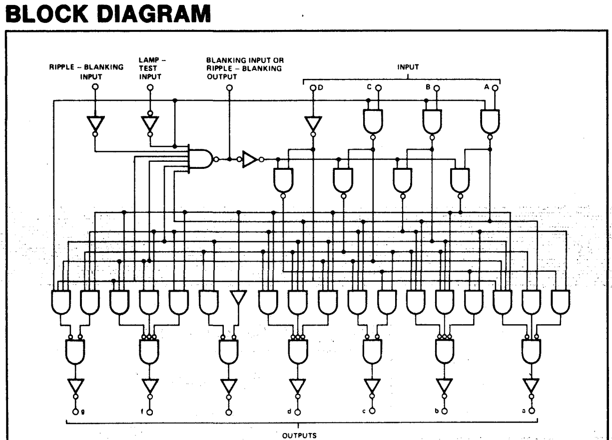
0	1	2	3	4	5	6	7	8	9
0	1	1	1	1	1	1	1	1	1
1	0	1	1	1	1	1	1	1	1
1	1	0	1	1	1	1	1	1	1
1	1	1	0	1	1	1	1	1	1
1	1	1	1	0	1	1	1	1	1
1	1	1	1	1	0	1	1	1	1
1	1	1	1	1	1	0	1	1	1
1	1	1	1	1	1	1	0	1	1
1	1	1	1	1	1	1	1	0	1
1	1	1	1	1	1	1	1	1	0
1	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1

BCD-TO SEVEN SEGMENT DECODER/DRIVER 54/7446A

SPEED/PACKAGE AVAILABILITY

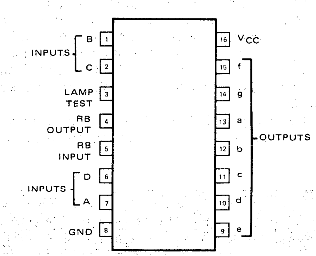
54 F 74 B,F

BLOCK DIAGRAM



PIN CONFIGURATION

B,F PACKAGE



SWITCHING CHARACTERISTICS $V_{CC} = 5V$, $T_A = 25°C$

TEST CONDITIONS			54/74 $C_L = 15pF$ $R_L = 120\Omega$			
PARAMETER	**FROM INPUT**	**TO OUTPUT**	**MIN**	**TYP**	**MAX**	**UNIT**
Propagation delay time t_{PLH} Low-to-high	A,RBI	Any			100	ns
t_{PHL} High-to-low	A or RBi				100	

Load circuit and typical waveforms are shown at the front of section.

TRUTH TABLE

	INPUTS							OUTPUTS							
DECIMAL OR FUNCTION	LT	RBI	D	C	B	A	B1/RBO	a	b	c	d	e	f	g	NOTE
0	1	1	0	0	0	0	1	0	0	0	0	0	0	1	1
1	1	x	0	0	0	1	1	1	0	0	1	1	1	1	1
2	1	x	0	0	1	0	1	0	0	1	0	0	1	0	
3	1	x	0	0	1	1	1	0	0	0	0	1	1	0	
4	1	x	0	1	0	0	1	1	0	0	1	1	0	0	
5	1	x	0	1	0	1	1	0	1	0	0	1	0	0	
6	1	x	0	1	1	0	1	1	1	0	0	0	0	0	
7	1	x	0	1	1	1	1	0	0	0	1	1	1	1	
8	1	x	1	0	0	0	1	0	0	0	0	0	0	0	
9	1	x	1	0	0	1	1	0	0	0	1	1	0	0	
10	1	x	1	0	1	0	1	1	1	1	0	0	1	0	
11	1	x	1	0	1	1	1	1	0	0	1	1	0	0	
12	1	x	1	1	0	0	1	1	0	1	1	1	0	0	
13	1	x	1	1	0	1	1	0	1	1	0	1	0	0	
14	1	x	1	1	1	0	1	1	1	1	0	0	0	0	
15	1	x	1	1	1	1	1	1	1	1	1	1	1	1	
BI	x	x	x	x	x	x	0	1	1	1	1	1	1	1	2
RBI	1	0	0	0	0	0	0	1	1	1	1	1	1	1	3
LT	0	x	x	x	x	x	1	0	0	0	0	0	0	0	4

NOTES:
1. BI/BRO is wire-OR logic serving as blanking input (BI) and/or ripple-blanking output (RBO). The blanking input must be open or held at a logical 1 when output functions 0 through 15 are desired and ripple-blanking input (RBI) must be open or at a logical 1 during the decimal 0 input. X = input may be high or low.
2. When a logical 0 is applied to the blanking input (forced condition) all segment outputs go to a logical 1 regardless of the state of any other input condition.
3. When ripple-blanking input (RBI) is at a logical 0 and A = B = C = D = logical 0, all segment outputs go to a logical 1 and the ripple-blanking output goes to a logcial 0 (response condition).
4. When blanking input/ripple-blanking output is open or held at a logical 1, and a logical 0 is applied to lamp-test input, all segment outputs go to a logical 0.

BCD-TO-SEVEN SEGMENT DECODER/DRIVER 54/7447A

SPEED/PACKAGE AVAILABILITY

54 F 74 B,F

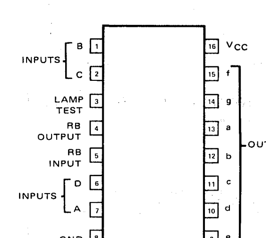
SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

TEST CONDITIONS			54/74 C_L=15pF R_L=120Ω			
PARAMETER	FROM INPUT	TO OUTPUT	MIN	TYP	MAX	UNIT
Propagation delay time t_{PLH} Low-to-high	A,RBI	Any			100	ns
t_{PHL} High-to-low					100	ns

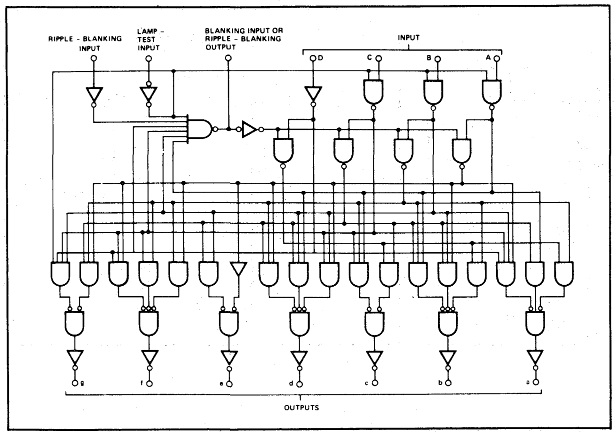
Load circuit and typical waveforms are shown at the front of section.

PIN CONFIGURATION

B,F PACKAGE



LOGIC DIAGRAM



TRUTH TABLE

	INPUTS							OUTPUTS							
DECIMAL OR FUNCTION	LT	RBI	D	C	B	A	BI/RBO	a	b	c	d	e	f	g	NOTE
0	1	1	0	0	0	0	1	0	0	0	0	0	0	1	1
1	1	x	0	0	0	1	1	1	0	0	1	1	1	1	1
2	1	x	0	0	1	0	1	0	0	1	0	0	1	0	
3	1	x	0	0	1	1	1	0	0	0	0	1	1	0	
4	1	x	0	1	0	0	1	1	0	0	1	1	0	0	
5	1	x	0	1	0	1	1	0	1	0	0	1	0	0	
6	1	x	0	1	1	0	1	1	1	0	0	0	0	0	
7	1	x	0	1	1	1	1	0	0	0	1	1	1	1	
8	1	x	1	0	0	0	1	0	0	0	0	0	0	0	
9	1	x	1	0	0	1	1	0	0	0	1	1	0	0	
10	1	x	1	0	1	0	1	1	1	1	0	0	1	0	
11	1	x	1	0	1	1	1	1	1	0	0	1	1	0	
12	1	x	1	1	0	0	1	1	0	1	1	1	0	0	
13	1	x	1	1	0	1	1	0	1	1	0	1	0	0	
14	1	x	1	1	1	0	1	1	1	1	0	0	0	0	
15	1	x	1	1	1	1	1	1	1	1	1	1	1	1	
BI	x	x	x	x	x	x	0	1	1	1	1	1	1	1	2
RBI	1	0	0	0	0	0	0	1	1	1	1	1	1	1	3
LT	0	x	x	x	x	x	1	0	0	0	0	0	0	0	4

NOTES:
1. BI/BRO is wire-OR logic serving as blanking input (BI) and/or ripple-blanking output (RBO). The blanking input must be open or held at a logical 1 when output functions 0 through 15 are desired and ripple-blanking input (RBI) must be open or at a logical 1 during the decimal o input. X = input may be high or low.
2. When a logical 0 is applied to the blanking input (forced condition) all segment outputs go to a logical 1 regardless of the state of any other input condition.
3. When ripple-blanking input (RBI) is at a logical 0 and A = B = C = D = logical 0, all segment outputs go to a logical 1 and the ripple-blanking output goes to a logical 0 (response condition).
4. When blanking input/ripple-blanking output is open or held at a logical 1, and a logical 0 is applied to lamp-test input, all segment outputs go to a logical 0.

SPEED/PACKAGE AVAILABILITY

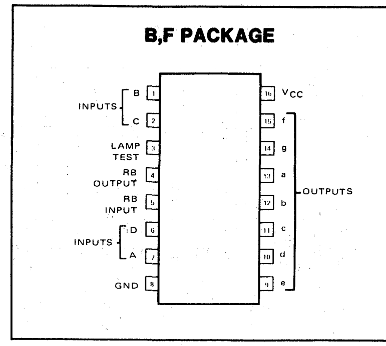
54 F 74 B,F

SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

TEST CONDITIONS			54/74 C_L=15pF (54)R_L=1kΩ (74)R_L=667Ω			
PARAMETER	**FROM INPUT**	**TO OUTPUT**	**MIN**	**TYP**	**MAX**	**UNIT**
Propagation delay time						
t_{PLH} Low-to-high	A,RBI	Any			100	ns
t_{PHL} High-to-low					100	ns

Load circuit and typical waveforms are shown at the front of section.

PIN CONFIGURATION



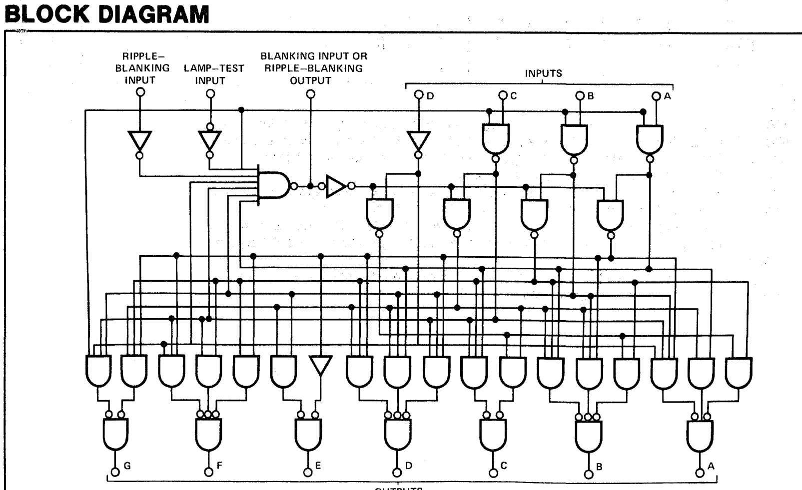
TRUTH TABLE

FUNCTION	LT	RBI	D	C	B	A	BI/RBO	a	b	c	d	e	f	g	NOTE
	INPUTS							OUTPUTS							
0	1	1	0	0	0	0	1	1	1	1	1	1	1	0	1
1	1	x	0	0	0	1	1	0	1	1	0	0	0	0	1
2	1	x	0	0	1	0	1	1	1	0	1	1	0	1	
3	1	x	0	0	1	1	1	1	1	1	1	0	0	1	
4	1	x	0	1	0	0	1	0	1	1	0	0	1	1	
5	1	x	0	1	0	1	1	1	0	1	1	0	1	1	
6	1	x	0	1	1	0	1	0	0	1	1	1	1	1	
7	1	x	0	1	1	1	1	1	1	1	0	0	0	0	
8	1	x	1	0	0	0	1	1	1	1	1	1	1	1	
9	1	x	1	0	0	1	1	1	1	1	0	0	1	1	
10	1	x	1	0	1	0	1	0	0	0	1	1	0	1	
11	1	x	1	0	1	1	1	0	0	1	1	0	0	1	
12	1	x	1	1	0	0	1	0	1	0	0	0	1	1	
13	1	x	1	1	0	1	1	1	0	0	1	0	1	1	
14	1	x	1	1	1	0	1	0	0	0	1	1	1	1	
15	1	x	1	1	1	1	1	0	0	0	0	0	0	0	
BI	x	x	x	x	x	x	0	0	0	0	0	0	0	0	2
RBI	1	0	0	0	0	0	0	0	0	0	0	0	0	0	3
LT	0	x	x	x	x	x	1	1	1	1	1	1	1	1	4

NOTES:

1. BI/BRO is wire-OR logic serving as blanking input (BI) and/or ripple-blanking output (RBO). The blanking input must be open or held at a logical 1 when output functions 0 through 15 are desired and ripple-blanking input (RBI) must be open or at a logical 1 during the decimal 0 input. X = input may be high or low.
2. When a logical 0 is applied to the blanking input (forced condition) all segment outputs go to a logical 1 regardless of the state of any other input condition.
3. When ripple-blanking input (RBI) is at a logical 0 and A = B = C = D= logical 0, all segment outputs go to a logical 1 and the ripple-blanking output goes to a logical 0 (response condition).
4. When blanking input/ripple-blanking output is open or held at a logical 1, and a logical 0 is applied to lamp-test input, all segmant outputs go to a logical 1.

BLOCK DIAGRAM

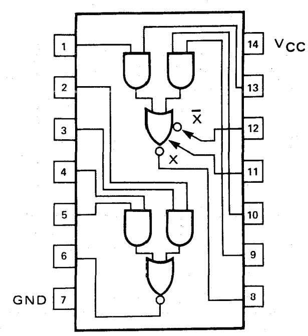


SPEED/PACKAGE AVAILABILITY

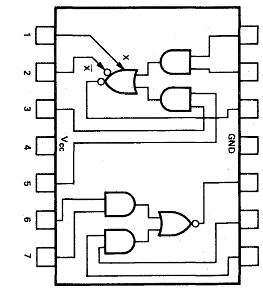
54	F,W	74	A,F
54H	F,W,	74H	A,F

PIN CONFIGURATION

A,F PACKAGE



W PACKAGE



SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°CC

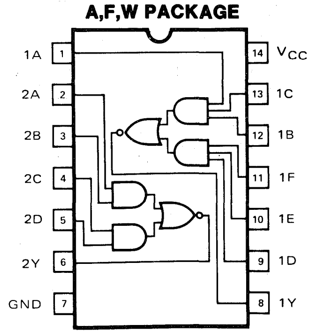
TEST CONDITIONS	54/74 C_L=15pF R_L=400Ω			54/74H C_L=25pF R_L=280Ω Expander pins are open			
PARAMETER	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNIT**
Propagation delay time t_{PLH} Low-to-high		13	22		6.8 C_X=15pF 11	11	ns
t_{PHL} High-to-low		8	15		6.2 C_X=15pF 7.4	11	ns

Load circuit and typical waveforms are shown at the front of section.

DUAL 2-WIDE 2-INPUT AND-OR-INVERT GATE 54/7451

PIN CONFIGURATION

54/74LS
A,F,W PACKAGE

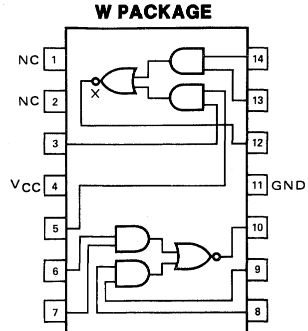


positive logic:
1Y = $\overline{(1A \cdot 1B \cdot 1C) + (1D \cdot 1E \cdot 1F)}$
2Y = $\overline{(2A \cdot 2B) + (2C \cdot 2D)}$

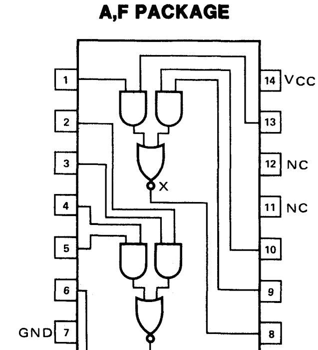
SPEED/PACKAGE AVAILABILITY

54	F,W	74	A,F
54H	F,W	74H	A,F
54LS	F,W	74LS	A,F

54,54H
W PACKAGE



OTHERS
A,F PACKAGE



DUAL 2-WIDE 2-INPUT AND-OR-INVERT GATE 54/7451

SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

TEST CONDITIONS	54/74 C_L=15pF R_L=400Ω			54/74H C_L=25pF R_L=280Ω			54/74LS C_L=15pF R_L=2kΩ			54/74S C_L=15pF R_L=280Ω			
PARAMETER	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNIT**
Propagation delay time t_{PLH} Low-to-high		13	22		6.8	11		9	15	2	3.5 C_L=50pF 5	5.5	ns
t_{PHL} High-to-low		8	15		6.2	11		9.5	15	2	3.5 C_L=50pF 5.5	5.5	ns

Make no external connection to X and $\overline{X}$ pins of the 54/7451 and the 54/74H51.
Load circuit and typical waveforms are shown at the front of section.

4-WIDE 2-2-2-3-INPUT AND-OR GATE 54/7452

SPEED/PACKAGE AVAILABILITY

54H F,W 74H A,F

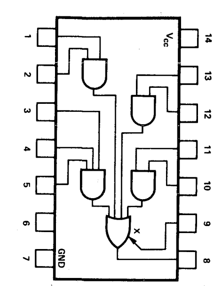
SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

TEST CONDITIONS	54/74H C_L=25pF R_L=280Ω EXPANDER PIN IS OPEN			
PARAMETER	**MIN**	**TYP**	**MAX**	**UNIT**
Propagation delay time t_{PLH} Low-to-high		10.6 C_X = 15pF 14.8	15	ns
t_{PHL} High-to-low		9.2 C_X = 15pF 9.8	15	ns

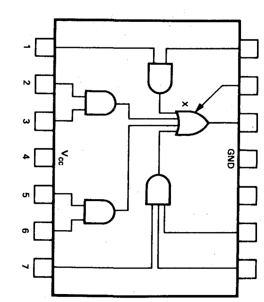
Load circuit and typical waveforms are shown at the front of section.

PIN CONFIGURATION

A,F PACKAGE



W PACKAGE

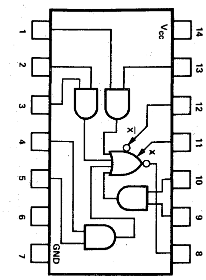


SPEED/PACKAGE AVAILABILITY

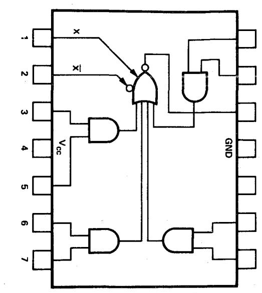
54	F,W	74	A,F
54H	F,W	74H	A,F

PIN CONFIGURATION

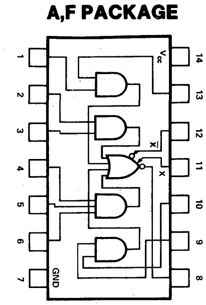
74
A,F PACKAGE



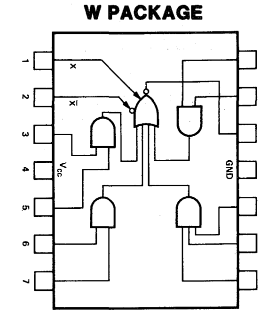
54
W PACKAGE



54/74H
A,F PACKAGE



54H
W PACKAGE



SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

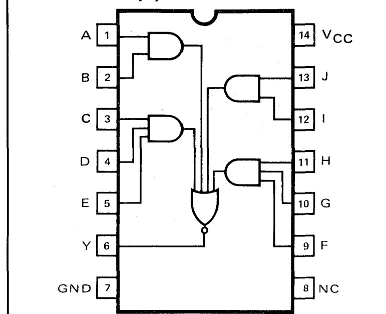
TEST CONDITIONS	54/74 C_L=15pF R_L=400Ω			54/74H C_L=25pF R_L=280Ω EXPANDER PINS ARE OPEN			
PARAMETER	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNIT**
Propagation delay time t_{PLH} Low-to-high		13	22		7 C_X=15pF 11.4	11	ns
t_{PHL} High-to-low		8	15		6.2 C_X=15pF 7.4	11	ns

Load circuit and typical waveforms are shown at the front of section.

SPEED/PACKAGE AVAILABILITY

54	F,W	74	A,F
54H	F,W	74H	A,F
54LS	F,W	74LS	A,F

PIN CONFIGURATION

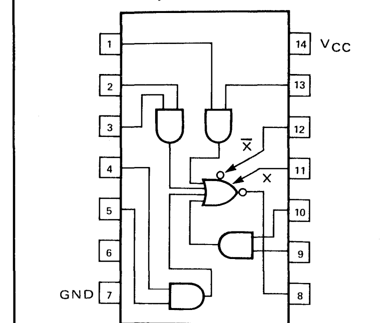


54/74LS A,F,W PACKAGE

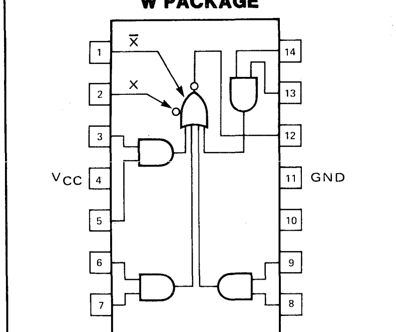
positive logic:

$Y = \overline{(AB) + (CDE) + (FGH) + (IJ)}$

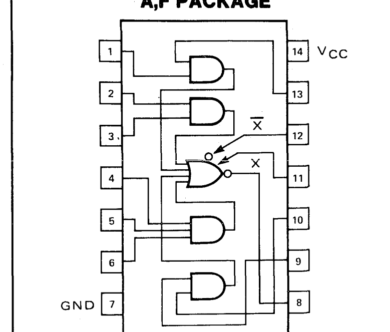
NC – No internal connection



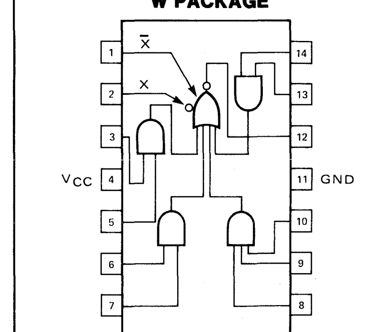
54/74 A,F PACKAGE



54 W PACKAGE



54H/74H A,F PACKAGE



54H W PACKAGE

SWITCHING CHARACTERISTICS $V_{CC} = 5V$, $T_A = 25°C$

	54/74			54/74H			54/74LS			
TEST CONDITIONS	C_L=15pF R_L=400Ω			C_L=25pF R_L=280Ω			C_L=15pF R_L=2kΩ			
PARAMETER	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
Propagation delay time t_{PLH} Low-to-high		13	22		7	11		7	20	ns
t_{PHL} High-to-low		8	15		6.2	11		11.5	20	ns

Load circuit and typical waveforms are shown at the front of section.
Make no external connection to X and X̄ pins of the 54/7454 and 54/74H54.

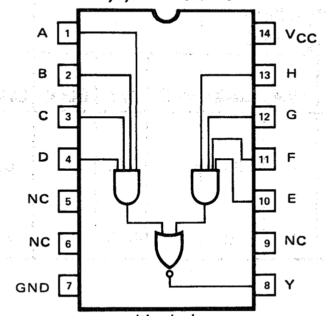
2-WIDE 4-INPUT AND-OR-INVERT GATE — 54/7455

SPEED/PACKAGE AVAILABILITY

54H	F,W	74H	A,F
54LS	F,W	74LS	A,F

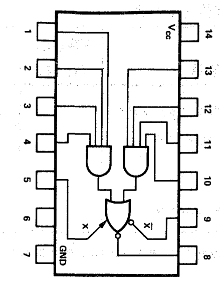
PIN CONFIGURATION

54/74LS
A,F,W PACKAGE



positive logic:
$Y = \overline{(ABCD) + (EFGH)}$

54,74H
A,F PACKAGE

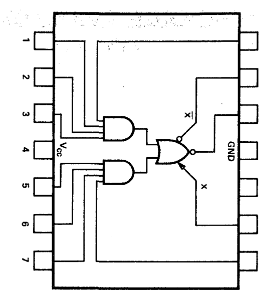


SWITCHING CHARACTERISTICS $V_{CC} = 5V$, $T_A = 25°C$

TEST CONDITIONS	54/74H C_L=25pF R_L=280Ω EXPANDER PINS ARE OPEN			54/74LS C_L=15pF R_L=2kΩ			
PARAMETER	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
Propagation delay time t_{PLH} Low-to-high		7 C_X=15pF 11.4	11		12	20	ns
t_{PHL} High-to-low		6.5 C_X=15pF 7.7	11		11.5	20	ns

Load circuit and typical waveforms are shown at the front of section.

54H
W PACKAGE



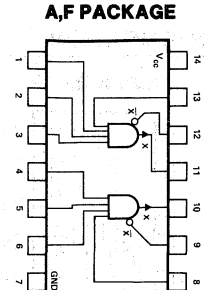
DUAL 4-INPUT EXPANDER — 54/7460

SPEED/PACKAGE AVAILABILITY

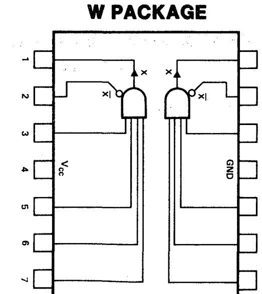
54	F,W	74	A,F
54H	F,W	74H	A,F

PIN CONFIGURATION

A,F PACKAGE



W PACKAGE



DUAL 4-INPUT EXPANDER 54/7460

SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

TEST CONDITIONS			54/74 C_L=15pF R_L=400Ω			54/74H			
PARAMETER	**FROM INPUT**	**TO OUTPUT**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNIT**
Propagation delay time									
t_{PLH} Low-to-high		through 54/7450, 54/7453		15	30		N/A		ns
t_{PHL} High-to-low				10	20		N/A		ns

Load circuit and typical waveforms are shown at the front of section.

TRIPLE 3-INPUT EXPANDER 54/7461

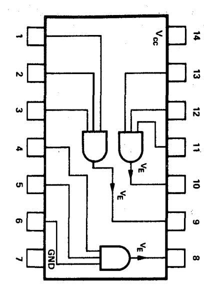
(FOR USE WITH 54/74H52)

SPEED/PACKAGE AVAILABILITY

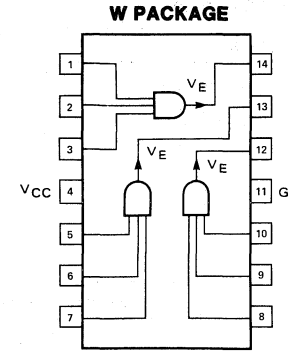
54H F,W 74H A,F

PIN CONFIGURATION

A,F PACKAGE



W PACKAGE



3-2-2-3-INPUT AND-OR EXPANDER 54/7462

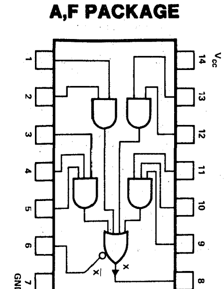
(FOR USE WITH 54/74H50, 54/74H53, 54/74H55)

SPEED/PACKAGE AVAILABILITY

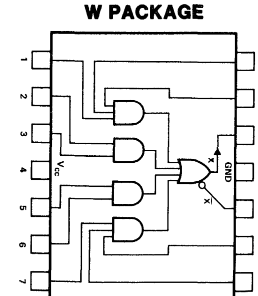
54H F,W 74H A,F

PIN CONFIGURATION

A,F PACKAGE



W PACKAGE



4-2-3-2-INPUT AND-OR GATE 54/7464

SPEED/PACKAGE AVAILABILITY

54S F,W 74S A,F

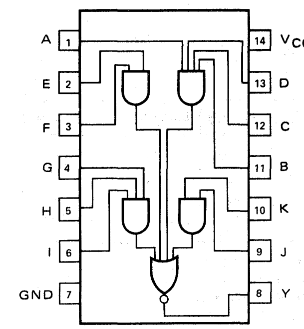
SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

TEST CONDITIONS	54/74S C_L=15pF R_L=280Ω			
PARAMETER	**MIN**	**TYP**	**MAX**	**UNIT**
Propagation delay time t_{PLH} Low-to-high	2	3.5 C_L=50pF 5	5.5	ns
t_{PHL} High-to-low	2	3.5 C_L=50pF 5.5	5.5	ns

Load circuit and typical waveforms are shown at the front of section.

PIN CONFIGURATION

A,F,W PACKAGE



positive logic: $\overline{ABCD + EF + GHI + JK}$

4-2-3-2-INPUT AND-OR GATE 54/7465

SPEED/PACKAGE AVAILABILITY

54S F,W 74S A,F

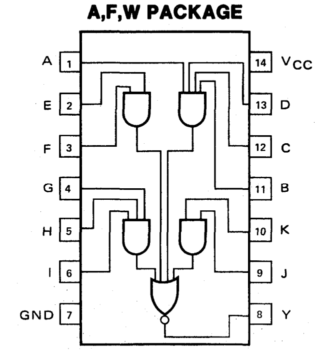
SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

TEST CONDITIONS	54/74S C_L=15pF R_L=280Ω			
PARAMETER	**MIN**	**TYP**	**MAX**	**UNIT**
Propagation delay time t_{PLH} Low-to-high	2	5 C_L=50pF 8	7.5	ns
t_{PHL} High-to-low	2	5.5 C_L=50pF 6.5	8.5	ns

Load circuit and typical waveforms are shown at the front of section.

PIN CONFIGURATION

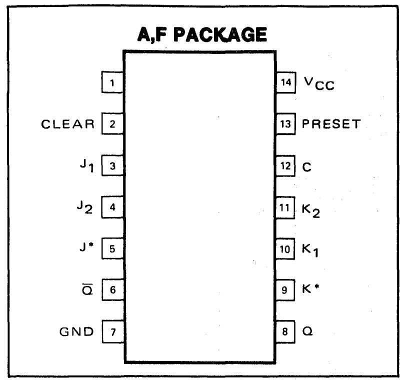
A,F,W PACKAGE

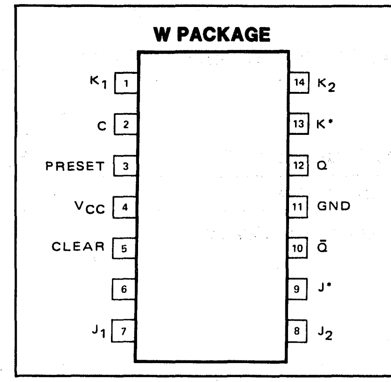


SPEED/PACKAGE AVAILABILITY

54 F,W 74 A,F

PIN CONFIGURATION





TRUTH TABLE

LOGIC

J_n	K_n	Q_{n+1}	PRESET	CLEAR	Q
0	0	Q_n	0	0	†
1	0	1	1	0	0
0	1	0	0	1	1
1	1	$\overline{Q}_n$	1	1	0

$J = J_1 J_2 J^*$ $K = K_1 K_2 K^*$
n is time prior to clock
n+1 is time following clock
† both outputs in 0 state

SWITCHING CHARACTERISTICS $V_{CC} = 5V$, $T_A = 25°C$

TEST CONDITIONS				54/74 C_L=15pF R_L=400Ω			
PARAMETER		FROM INPUT	TO OUTPUT	MIN	TYP	MAX	UNIT
f_{Clock}	Clock frequency			15	35		MHz
t_{Setup}	Input setup time				10	20	ns
t_{Hold}	Input hold time				0	5	ns
Propagation delay time							
t_{PLH}	Low-to-high	Clear, Preset				50	ns
t_{PHL}	High-to-low					50	
t_{PLH}	Low-to-high	Clock		10	27	50	ns
t_{PHL}	High-to-low			10	18	50	

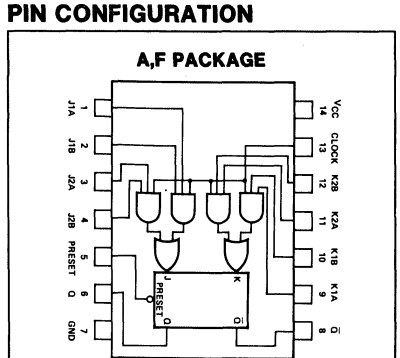
Load circuit and typical waveforms are shown at the front of section.

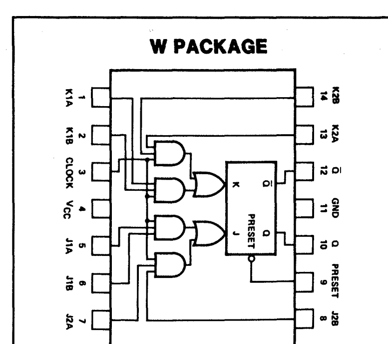
J-K MASTER-SLAVE FLIP-FLOP 54/7471

SPEED/PACKAGE AVAILABILITY

54H F,W 74H A,F

PIN CONFIGURATION





TRUTH TABLE

t_n		t_{n+1}
J	K	Q
0	0	Q_n
0	1	0
1	0	1
1	1	$\overline{Q}_n$

NOTES:
1. J = (J1A•J1B)+ (J2A•J2B)
2. K = (K1A•K1B) + (K2A•K2B)
3. t_n = bit time before clock pulse.
4. t_{n+1} = bit time after clock pulse.

SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

TEST CONDITIONS				54/74H C_L=15pF R_L=280Ω		
PARAMETER	**FROM INPUT**	**TO OUTPUT**	**MIN**	**TYP**	**MAX**	**UNIT**
f_{Clock} Clock frequency			25	30		MHz
Propagation delay time						
t_{PLH} Low-to-high	Preset			6	13	ns
t_{PHL} High-to-low				12	24	
t_{PLH} Low-to-high	Clock		6	14	21	ns
t_{PHL} High-to-low			10	22	27	

Load circuit and typical waveforms are shown at the front of section.

J-K MASTER-SLAVE FLIP-FLOP 54/7472

SPEED/PACKAGE AVAILABILITY

54	F,W	74	A,F
54H	F,W	74H	A,F

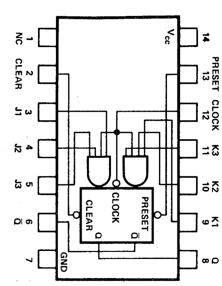
TRUTH TABLE

t_n		t_{n+1}
J	K	Q
0	0	Q_n
0	1	0
1	0	1
1	1	$\overline{Q}_n$

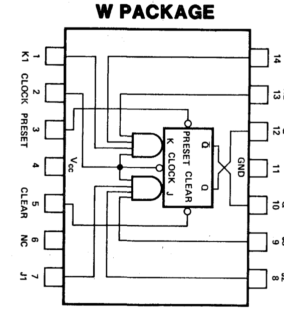
NOTES:
1. J = J1 • J2 • J3
2. K = K1 • K2 • K3
3. t_n = bit time before clock pulse.
4. t_{n+1} = bit time after clock pulse.
5. NC = no internal connection.

PIN CONFIGURATION

A,F PACKAGE



W PACKAGE



SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

TEST CONDITIONS				54/74 C_L=15pF R_L=400Ω			54/74H C_L=25pF R_L=280Ω			
PARAMETER		**FROM INPUT**	**TO OUTPUT**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNIT**
f_{Clock}	Clock frequency			15	20		25	30		MHz
$t_{w(Clock)}$	Width of clock input pulse									
	Clock high			20			12			ns
	Clock low			47			28			
$t_{w(Clear)}$	Width of clear input pulse			25			16			ns
t_{Setup}	Input setup time			0↑			0↑			ns
t_{Hold}	Input hold time			0↓			0↓			ns
Propagation delay time										
t_{PLH}	Low-to-high	Clear			16	25		6	13	ns
t_{PHL}	High-to-low				25	40		12	24	
t_{PLH}	Low-to-high	Clock		10	16	25		16	21	ns
t_{PHL}	High-to-low			10	25	40		22	27	

Load circuit and typical waveforms are shown at the front of section.

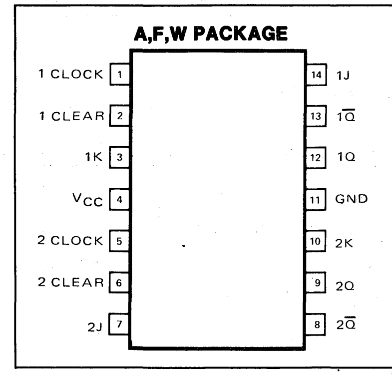
SPEED/PACKAGE AVAILABILITY

54	F,W	74	A,F
54H	F,W	74H	A,F
54LS	F,W	74LS	A,F

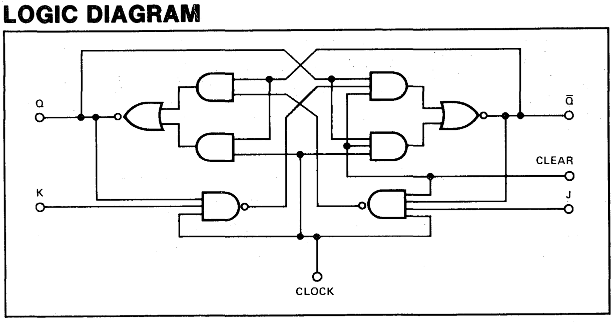
DESCRIPTION

This monolithic edge-triggered dual J-K flip-flop features individual J, K, clock, and clear inputs to each flip-flop. A low logic level at the clear input resets the Q output to a low level regardless of the levels at the other inputs. With clear inactive (high), a high level at the clock input enables the J and K inputs and data will be accepted. The logic levels at the J and K inputs may be allowed to change when the clock pulse is high and the bistable will perform according to the function table, as long as minimum setup and hold times are observed. Input data is transferred to the outputs on the negative-going edge of the clock pulse.

PIN CONFIGURATION



LOGIC DIAGRAM



FUNCTION TABLE (Each Flip-Flop)

54/74, 54/74H

INPUTS				OUTPUTS	
CLEAR	CLOCK	J	K	Q	Q̄
L	X	X	X	L	H
H	⎍	L	L	Q_0	$\overline{Q}_0$
H	⎍	H	L	H	L
H	⎍	L	H	L	H
H	⎍	H	H	TOGGLE	

54/74LS73

INPUTS				OUTPUTS	
CLEAR	CLOCK	J	K	Q	Q̄
L	X	X	X	L	H
H	↓	L	L	Q_0	$\overline{Q}_0$
H	↓	H	L	H	L
H	↓	L	H	L	H
H	↓	H	H	TOGGLE	
H	H	X	X	Q_0	$\overline{Q}_0$

H = high level (steady state)
L = low level (steady state)
X = irrelevant
↓ = transition from high to low level
Q_0 = the level of Q before the indicated input conditions were established.
TOGGLE: Each output changes to the complement of its previous level on each ↓ clock transition.

SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

TEST CONDITIONS				54/74 C_L=15pF R_L=400Ω			54/74H C_L=25pF R_L=280Ω			54/74LS C_L=15pF R_L=2kΩ			
PARAMETER		FROM INPUT	TO OUTPUT	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
f_{Clock}	Clock frequency			15	20		25	30		30	45		MHz
$t_{w(Clock)}$	Width of clock input pulse									20			ns
	Clock high			20			12						
	Clock low			47			28						
$t_{w(Clear)}$	Width of clear input pulse			25			16			25			ns
t_{Setup}	Input setup time			0↑			0↑			20			ns
t_{Hold}	Input hold time			0↓			0↓			0			ns
Propagation delay time													
t_{PLH}	Low-to-high	Clear			16	25		6	13		11	20	ns
t_{PHL}	High-to-low				25	40		12	24		15	30	ns
t_{PLH}	Low-to-high	Clock		10	16	25		16	21		11	20	ns
t_{PHL}	High-to-low			10	25	40		22	27		15	30	ns

Load circuit and typical waveforms are shown at the front of section.

SPEED/PACKAGE AVAILABILITY

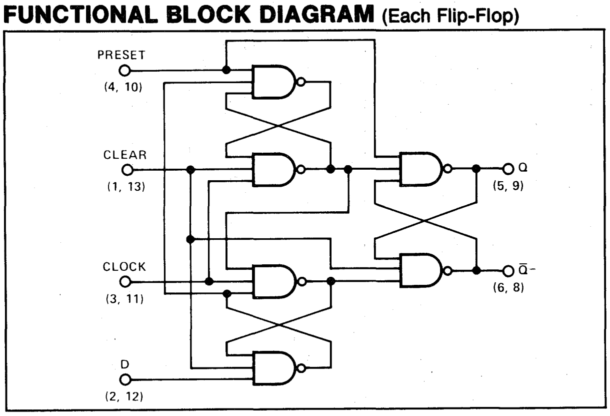
54	F,W	74	A,F
54H	F,W	74H	A,F
54LS	F,W	74LS	A,F
54S	F,W	74S	A,F

DESCRIPTION

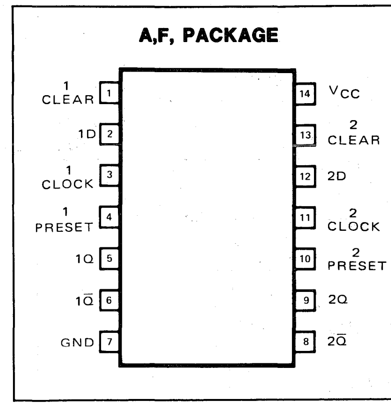
These monolithic dual edge-triggered D-type flip-flops feature individual D, clock, preset, and clear inputs.

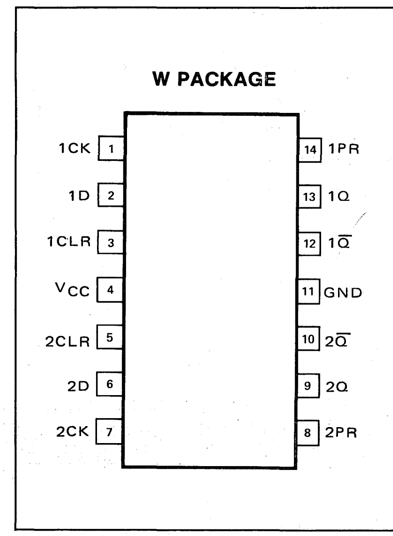
Preset and clear inputs are active-low and operate independently of the clock input. When preset and clear are inactive (high), information at the D input is transferred to the Q output on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D-input signal has no effect at the output.

FUNCTIONAL BLOCK DIAGRAM (Each Flip-Flop)



PIN CONFIGURATION





TRUTH TABLE (Each Flip-Flop)

	Inputs			Outputs	
Preset	**Clear**	**Clock**	**D**	**Q**	**Q̄**
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\bar{Q}_0$

H = high level (steady state) L= low level (steady state)
*This condition is nonstable. It will not remain after clear and preset return to their inactive (high) state.

SWITCHING CHARACTERISTICS V_{CC}= 5V, T_A = 25°C

TEST CONDITIONS				54/74 C_L=15pF R_L=400Ω			54/74H C_L=25pF R_L=280Ω			54/74LS C_L=15pF R_L=2kΩ			54/74S C_L=15pF R_L=280Ω			
PARAMETER		FROM INPUT	TO OUTPUT	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
f_{Clock}	Clock frequency			15	25		35	43		25	33		75	90		MHz
$t_{w(Clock)}$	Width of clock input pulse									25						
	Clock high			30			15						6			ns
	Clock low			37			13.5						7.3			
$t_{w(Clear}$	Width of clear input pulse			30			25			25			7			ns
$t_{w(Preset)}$	Width of preset input pulse			30			25			25			7			ns
t_{Setup}	Input setup time			20↑	15								3↓			ns
	High level						10↑			25						
	Low level						15↑			20						
t_{Hold}	Input hold time			5↑	2		5↑			5			2↓			ns
Propagation delay time																
t_{PLH}	Low-to-high	Clear, Preset				25			20		8	25		5	6 CLK=1	ns
														8	13.5 CLK=0	
t_{PHL}	High-to-low					40			30		16	40		5	8	
t_{PHL}	Low-to-high	Clock		10	14	25	4	8.5	15		8	25		7	9	ns
t_{PHL}	High-to-low			10	20	40		13	20		16	40		7	9	

Load circuit and typical waveforms are shown at the front of section.

QUAD BISTABLE LATCH 54/7475

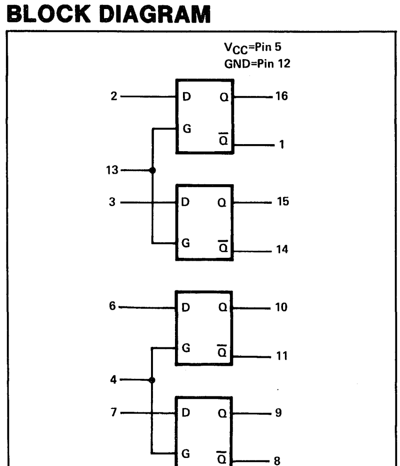
SPEED/PACKAGE AVAILABILITY

54	F	74	B,F
54LS	F,W	74LS	B,F

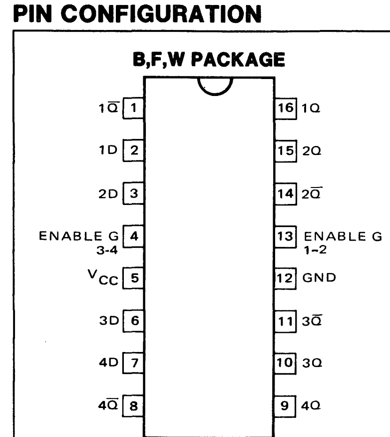
DESCRIPTION

This latch is ideally suited for use as temporary storage for binary information between processing units and input/output or indicator units. Information present at a data (D) input is transferred to the Q output when the enable (G) is high and the Q output will follow the data input as long as the enable remains high. When the enable goes low, the information (that was present at the data input at the time the transition occurred) is retained at the Q output until the enable is permitted to go high.

BLOCK DIAGRAM



PIN CONFIGURATION

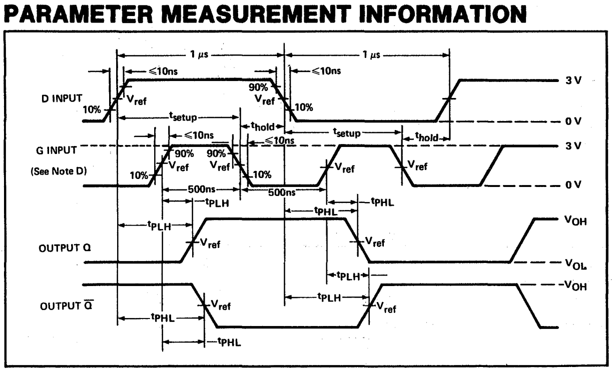


SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

TEST CONDITIONS			54/74 C_L=15pF R_L=400Ω			54/74LS C_L=15pF R_L=2kΩ			
PARAMETER	**FROM INPUT**	**TO OUTPUT**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNIT**
t_W Width of enabling pulse						20			
t_{Setup} Input setup time						20			
High level				7	20				
Low level				14	20				
t_{Hold} Input hold time						0			
High Level			0	15					
Low level			0	6					
Propagation delay time									
t_{PLH} Low-to-high	D	Q		16	30		15	27	ns
t_{PHL} High-to-low				14	25		9	17	
t_{PLH} Low-to-high	D	$\overline{Q}$		24	40		12	20	ns
t_{PHL} High-to-low				7	15		7	15	
t_{PHL} Low-to-high	G	Q		16	30		15	27	ns
t_{PHL} High-to-low				7	15		14	25	
t_{PLH} Low-to-high	G	$\overline{Q}$		16	30		16	30	ns
t_{PHL} High-to-low				7	15		7	15	

Load circuit and typical waveforms are shown at the front of section

PARAMETER MEASUREMENT INFORMATION



VOLTAGE WAVEFORMS

NOTES:
A. The pulse generators have the following characteristics: Z_{out} = 50 Ω; for pulse generator A, PRR ≤ 500 kHz; for pulse generator B, PRR ≤ 1 MHz. Positions of D and G input pulses are varied with respect to each other to verify setup times.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N3064.
D. When measuring propagation delay times from the D input, the corresponding G input must be held high.
E. V_{ref} = 1.3V.

TRUTH TABLE (Each Latch)

LOGIC **54/74**

(Each Latch)		
t_n	t_n+1	
D	Q	$\overline{Q}$
1	1	0
0	0	1

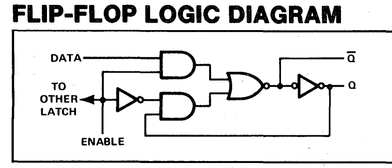
NOTES:
1. t_n = bit time before clock pulse
2. t_n+1 = bit time after clock pulse.
3. These voltages are with respect to network ground terminal.

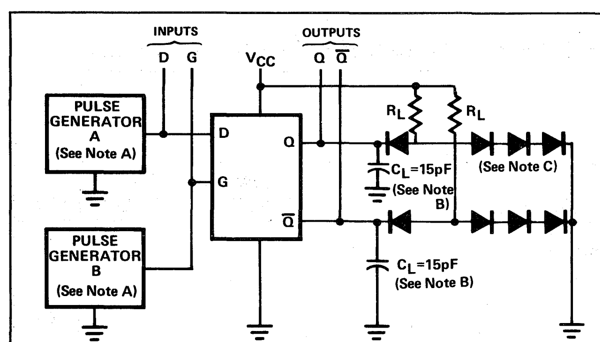
54/74LS

INPUTS		OUTPUTS	
D	G	Q	$\overline{Q}$
L	H	L	H
H	H	H	L
X	L	Q_0	$\overline{Q}_0$

H = high level, L = low level,
X = irrelevant
Q_0 = the level of Q before the high-to-low transition of G

FLIP-FLOP LOGIC DIAGRAM





TEST CIRCUIT

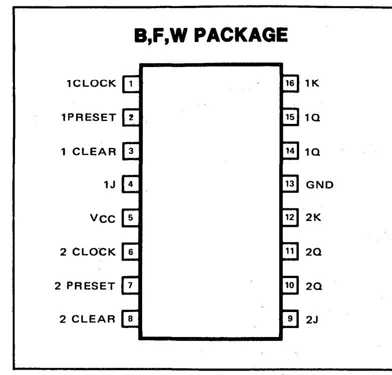
SPEED/PACKAGE AVAILABILITY

54	F,W	74	B,F
54H	F,W	74H	B,F
54LS	F,W	74LS	B,F

DESCRIPTION

This monolithic dual J-K flip-flop features individual J, K, clock, and asynchronous preset and clear inputs to each flip-flop. The preset or clear inputs, when low, set or reset the outputs regardless of the levels at the other inputs. When preset and clear inputs are inactive (high), a high level at the clock input enables the J and K inputs and data will be accepted. The logic levels at the J and K inputs may be allowed to change when the clock pulse is high and the bistable will perform according to the function table as long as minimum setup and hold times are observed. Input data is transferred to the outputs on the negative-going edge of the clock pulse.

PIN CONFIGURATION



FUNCTION TABLE (Each Flip Flop)

54/74,54/74H

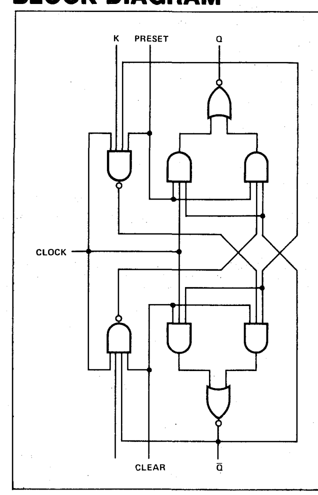
INPUTS					OUTPUTS	
PRESET	CLEAR	CLOCK	J	K	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	⎍	L	L	Q_0	$\overline{Q}_0$
H	H	⎍	H	L	H	L
H	H	⎍	L	H	L	H
H	H	⎍	H	H	TOGGLE	

54/74LS

INPUTS					OUTPUTS	
PRESET	CLEAR	CLOCK	J	K	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	L	Q_0	$\overline{Q}_0$
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	
H	H	H	X	X	Q_0	Q_0

H = high level (steady state)
L = low level (steady state)
X = irrelevant
↓ = transition from high to low level
Q_0 = the level of Q before the indicated steady-state input conditions were established.
TOGGLE: Each output changes to the complement of its previous level on each ↓ clock transition.
*This configuration is nonstable, that is, it will not persist when preset and clear inputs return to their inactive (high) level.

FUNCTIONAL BLOCK DIAGRAM



SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

TEST CONDITIONS				54/74 C_L=15pF R_L=400Ω			54/74H C_L=25pF R_L=280Ω			54/74LS C_L=15pF R_L=2kΩ			
PARAMETER		FROM INPUT	TO OUTPUT	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
f_{Clock}	Clock frequency			15	20		25	30		30	45		MHz
$t_{w(Clock)}$	Width of clock pulse									20			ns
	Clock high			20			12						
	Clock low			47			28						
t_w(Preset)	Width of preset pulse			25			16			25			ns
t_w(Clear)	Width of clear pulse			25			16			25			ns
t_{Setup}	Input setup time			0↑			0↑			20↓			ns
t_{Hold}	Input hold time			0↓			0↓			0↓			ns
Propagation delay time													
t_{PLH}	Low-to-high	Clear, Preset			16	25		6	13		11	20	ns
t_{PHL}	High-to-low				25	40		12	24		15	30	
t_{PLH}	Low-to-high	Clock		10	16	25		16	21		11	20	
t_{PHL}	High-to-low			10	25	40		22	27		15	30	

Load circuit and typical waveforms are shown at the front of section.

QUAD BISTABLE LATCH — 5477

SPEED/PACKAGE AVAILABILITY
54 W

SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

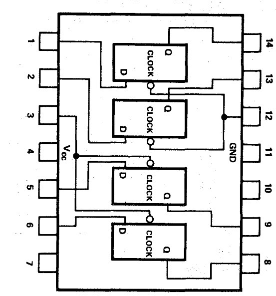
TEST CONDITIONS				54 C_L=15pF R_L=400Ω			
PARAMETER		**FROM INPUT**	**TO OUTPUT**	**MIN**	**TYP**	**MAX**	**UNIT**
t_{Setup}	Input setup time						
	High level				7	20	ns
	Low level				14	20	
t_{Hold}	Input hold time						ns
	High level			0	15*		
	Low level			0	6*		
Propagation delay time							
t_{PLH}	Low-to-high	D	Q		16	30	ns
t_{PHL}	High-to-low				14	25	
t_{PLH}	Low-to-high	C	Q		16	30	
t_{PHL}	High-to-low				7	15	

Load circuit and typical waveforms are shown on 54/7475 data sheet.

*These typical times indicate that period occurring prior to the fall of clock pulse (to) below 1.5V when data at the D input will still be recognized and stored.

PIN CONFIGURATION

W PACKAGE



TRUTH TABLE
LOGIC

(Each Latch)	
t_n	t_n+1
D	Q
1	1
0	0

NOTES:
1. t_n = bit time before clock pulse.
2. t_n+1 = bit time after clock pulse
3. These voltages are with respect to network ground terminal.

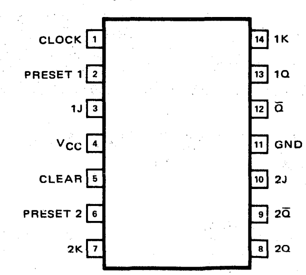
DUAL J-K NEGATIVE EDGE-TRIGGERED FLIP-FLOP — 54/7478

SPEED/PACKAGE AVAILABILITY
54LS F,W 74LS A,F

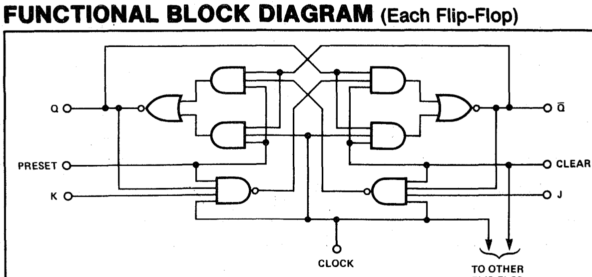
DESCRIPTION
This monolithic dual J-K edge-triggered flip-flop features individual J, K, and preset inputs plus common clock and common clear inputs. The preset or clear inputs, when low, set or reset the outputs regardless of the levels at the other inputs. When preset and clear inputs are inactive (high), a high level at the clock input enables the J and K inputs and data will be accepted. The logic levels at the J and K inputs may be allowed to change when the clock pulse is high and the bistable will perform according to the function table as long as minimum setup and hold times are observed. Input data is transferred to the outputs on the negative-going edge of the clock pulse.

PIN CONFIGURATION

A,F,W PACKAGE



FUNCTIONAL BLOCK DIAGRAM (Each Flip-Flop)



FUNCTION TABLE (Each Flip-Flop)

INPUTS					OUTPUTS	
PRESET	CLEAR	CLOCK	J	K	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	L	Q_0	$\overline{Q}_0$
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	
H	H	H	X	X	Q_0	$\overline{Q}_0$

H = high level (steady state)
L = low level (steady state)
X = irrelevant
↓ = transition from high to low level
Q_0= the level of Q before the indicated steady-state input conditions were established
TOGGLE: Each output changes to the complement of its previous level on each ↓ clock transition.
*This configuration is nonstable, that is, it will not persist when preset and clear inputs return to their inactive (high) level.

SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

PARAMETER		TEST CONDITIONS	LIMITS			
			MIN	TYP	MAX	UNIT
f_{Clock}	Clock frequency	C_L = 15pF, R_L = 2kΩ	30	45		MHz
$t_{w(Clock)}$	Width of clock pulse (high)		20			ns
$t_{w(Preset)}$	Width of preset pulse (low)		25			ns
$t_{w(Clear)}$	Width of clear pulse (low)		25			ns
t_{Setup}	Input setup time		20↓			ns
t_{Hold}	Input hold time		0↓			ns
t_{PLH}	Propagation delay time, low-to-high-level output from clear, preset or clock (as appropriate)			11	20	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clear, preset or clock (as appropriate)			15	30	ns

Load circuit and typical waveforms are shown at the front of book.

GATED FULL ADDER 54/7480

SPEED/PACKAGE AVAILABILITY

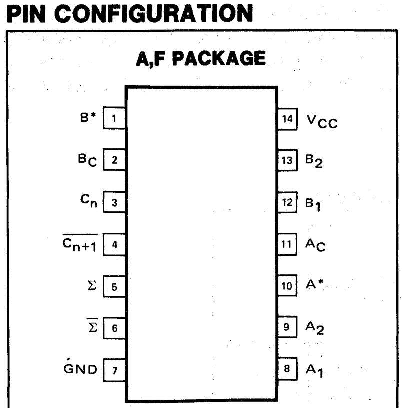
54 F,W 74 A,F

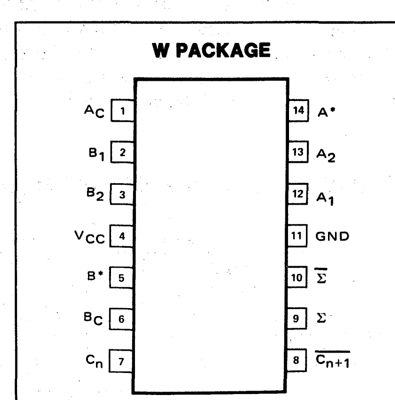
TRUTH TABLE

C_N	B	A	$\overline{C_{n+1}}$	$\overline{\Sigma}$	Σ
0	0	0	1	1	0
0	0	1	1	0	1
0	1	0	1	0	1
0	1	1	0	1	0
1	0	0	1	0	1
1	0	1	0	1	0
1	1	0	0	1	0
1	1	1	0	0	1

NOTES:
1. $A = \overline{A^* \cdot A_C}$, $B = \overline{B^* \cdot B_C}$ where $A^* = \overline{A_1 \cdot A_2}$, $B^* = \overline{B_1 \cdot B_2}$.
2. When A* or B* are used as inputs, A_1 and B_2 respectively, must be connected to GND.

PIN CONFIGURATION





SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

TEST CONDITIONS			54/74 C_L=15pF R_L=780Ω			
PARAMETER	**FROM INPUT**	**TO OUTPUT**	**MIN**	**TYP**	**MAX**	**UNIT**
Propagation delay time						
t_{PLH} Low-to-high	C_n	$\overline{C_{n+1}}$		13	17	ns
t_{PHL} High-to-low				8	12	
t_{PLH} Low-to-high	B_C	$\overline{C_{n+1}}$		18	25	
t_{PHL} High-to-low				38	55	
TEST CONDITIONS				C_L=15pF R_L = 400Ω		
t_{PLH} Low-to-high	A_C	Σ		52	70	
t_{PHL} High-to-low				62	80	
t_{PLH} Low-to-high	B_C	$\overline{\Sigma}$		38	55	
t_{PHL} High-to-low				56	75	
TEST CONDITIONS				C_L=15pF		
t_{PLH} Low-to-high	A_1	A*		48	65	
t_{PHL} High-to-low				17	25	
t_{PLH} Low-to-high	B_1	B*		48	65	
t_{PHL} High-to-low				17	25	

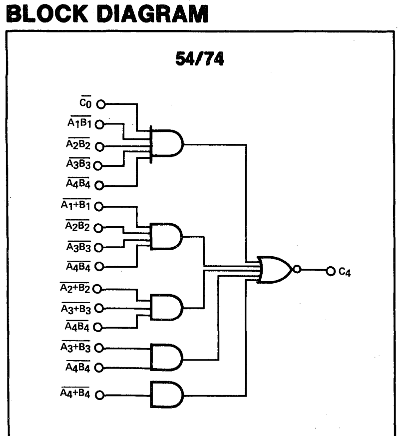
Load circuit and typical waveforms are shown at the front of section.

4-BIT BINARY FULL ADDER 54/7483/83A

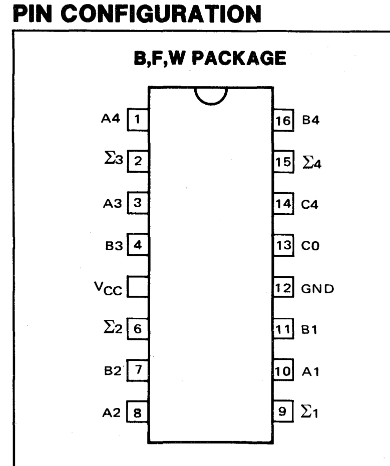
SPEED/PACKAGE AVAILABILITY

54	F,W	74	B,F
54LS	F,W	74LS	B,F

BLOCK DIAGRAM



PIN CONFIGURATION



LOGIC

SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

TEST CONDITIONS			54/74 C_L=50pF R_L=400			54/74LS C_L=15pF R_L=2k			
PARAMETER	FROM INPUT	TO OUTPUT	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
Propagation delay time									
t_{PLH} Low-to-high	C_0	1		23	34				ns
t_{PHL} High-to-low				20	34				
t_{PLH} Low-to-high	C_0	2		24	35				
t_{PHL} High-to-low				22	35				
t_{PLH} Low-to-high	C_0	3		30	50				
t_{PHL} High-to-low				24	40				
t_{PLH} Low-to-high	C_0	4		30	50				
t_{PHL} High-to-low				28	50				
t_{PLH} Low-to-high	A_2,B_2	2			40				
t_{PHL} High-to-low					35				
t_{PLH} Low-to-high	A_4,B_4	4			40				
t_{PHL} High-to-low					35				
TEST CONDITIONS			C_L = 50pF R_L = 780						
t_{PLH} Low-to-high	C_0	C_4		12	20		11	17	
t_{PHL} High-to-low				12	20		11	17	
t_{PLH} Low-to-high	C_0	Any Σ					16	24	
t_{PHL} High-to-low							15	24	
t_{PLH} Low-to-high	A_i,B_i	Σ i					15	24	
t_{PHL} High-to-low							15	24	
t_{PLH} Low-to-high	A_i,B_i	C_4					11	17	
t_{PHL} High-to-low							12	17	

Load circuit and typical waveforms are shown at the front of section.

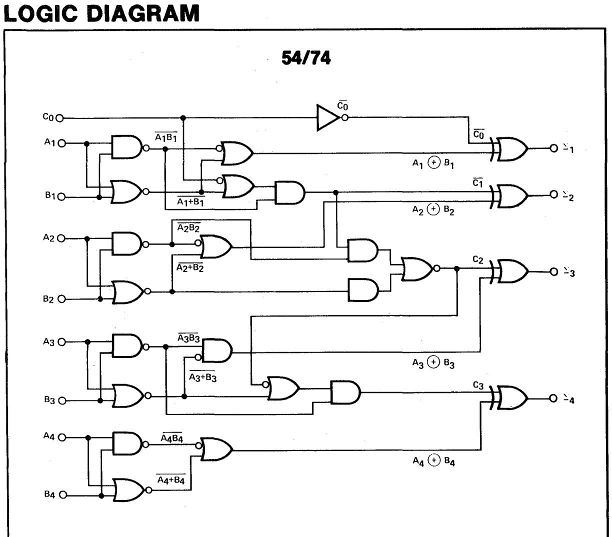
FUNCTION TABLE

INPUT				OUTPUT WHEN CO=L			OUTPUT WHEN CO=H		
				WHEN C2=L			WHEN C2=H		
A1 A3	B1 B3	A2 A4	B2 B4	Σ1 Σ3	Σ2 Σ4	C2 C4	Σ1 Σ3	Σ2 Σ4	C2 C4
L	L	L	L	L	L	L	H	L	L
H	L	L	L	H	L	L	L	H	L
L	H	L	L	H	L	L	L	H	L
H	H	L	L	L	H	L	H	H	L
L	L	H	L	L	H	L	H	H	L
H	L	H	L	H	H	L	L	L	H
L	H	H	L	H	H	L	L	L	H
H	H	H	L	L	L	H	H	L	H
L	L	L	H	L	H	L	H	H	L
H	L	L	H	H	H	L	L	L	H
L	H	L	H	H	H	L	L	L	H
H	H	L	H	L	L	H	H	L	H
L	L	H	H	L	L	H	H	L	H
H	L	H	H	H	L	H	L	H	H
L	H	H	H	H	L	H	L	H	H
H	H	H	H	L	H	H	H	H	H

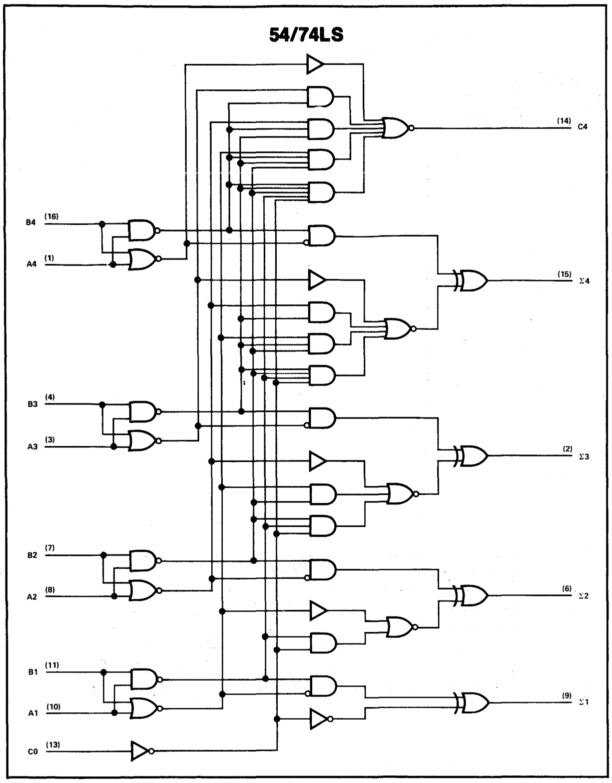
H = high level, L = low level

NOTE: Input conditions at A1, B1, A, B2, and CO are used to determine outputs Σ1 and Σ2 and the value of the internal carry C2. The values at C2, A3, B3, A4, and B4, are then used to determine outputs Σ3, Σ4, and C4.

LOGIC DIAGRAM



LOGIC DIAGRAM



4-BIT MAGNITUDE COMPARATOR 54/7485

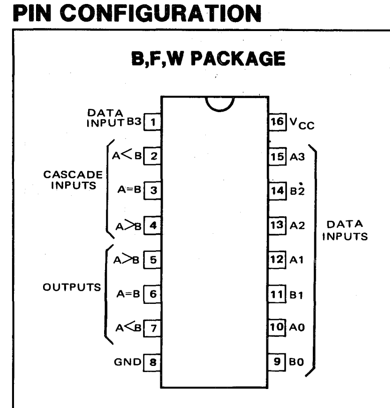
SPEED/PACKAGE AVAILABILITY

54	F,W	74	B,F
54LS	F,W	74LS	B,F
54S	F,W	74S	B,F

DESCRIPTION

This four-bit magnitude comparator performs comparison of straight binary and straight BCD (8-4-2-1) codes. Three fully decoded decisions about two 4-bit words (A, B) are made and are externally available at three outputs. These devices are fully expandable to any number of bits without external gates. Words of greater length may be compared by connecting comparators in cascade. The A > B, A < B and A = B outputs of a stage handling less-significant bits are connected to the corresponding A > B, A < B, and A = B inputs of the next stage handling more-significant bits. The stage handling the least-significant bits must have a high-level voltage applied to the A = B input. The cascading path is implemented with only a two-gate-level delay to reduce overall comparison times for long words. An alternate method of cascading which further reduces the comparison time is shown in the typical application data.

PIN CONFIGURATION



FUNCTION TABLE

COMPARING INPUTS				CASCADING INPUTS			OUTPUTS		
A3, B3	A2, B2	A1, B1	A0, B0	A > B	A < B	A = B	A > B	A < B	A = B
A3 > B3	X	X	X	X	X	X	H	L	L
A3 < B3	X	X	X	X	X	X	L	H	L
A3 = B3	A2 > B2	X	X	X	X	X	H	L	L
A3 = B3	A2 < B2	X	X	X	X	X	L	H	L
A3 = B2	A2 = B2	A1 > B1	X	X	X	X	H	L	L
A3 = B3	A2 = B2	A1 < B1	X	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 > B0	X	X	X	H	L	L
A3 = B3	A2 = B2	A1 = B1	A0 < B0	X	X	x	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	H	L	L	H	L	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	H	L	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	L	H	L	L	H
A3 = B3	A2 = B2	A1 = B1	A0 = B0	X	X	H	L	L	H
A3 = B3	A2 = B2	A1 = B1	A0 = B0	H	H	L	L	L	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	L	L	H	H	L

H = high level, L = low level, X = irrelevant

SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

TEST CONDITIONS				54/74 C_L=15pF R_L=400Ω			54/74LS C_L=15pF R_L=2kΩ			54/74S C_L = 15pF R_L=280Ω				
PARAMETER		FROM INPUT	TO OUTPUT	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	NUMBER OF GATE LEVELS	UNIT
Propagation delay time														
t_{PLH}	Low-to-high	Any A,B	A>B,A<B		7			14			5		1	ns
t_{PHL}	High-to-low				11			11			5.5			
t_{PLH}	Low-to-high				12			19			7.5		2	
t_{PHL}	High-to-low				15			15			7			
t_{PLH}	Low-to-high				17	26		24	36		10.5	16	3	
t_{PHL}	High-to-low				20	30		20	30		11	16.5		
t_{PLH}	Low-to-high	Any A,B	A=B		23	35		23	40		12	18	4	
t_{PHL}	High-to-low				20	30		20	30		11	16.5		
t_{PLH}	Low-to-high	A<B,A=B	A>B		7	11		14	22		5	7.5	1	
t_{PHL}	High-to-low				11	17		11	17		5.5	8.5		
t_{PLH}	Low-to-high	A=B	A=B		13	20		13	20		7	10.5	1	
t_{PHL}	High-to-low				11	17		11	17		5	7.5		
t_{PLH}	Low-to-high	A>B,A=B	A<B		7	11		14	22		5	7.5	1	
t_{PHL}	High-to-low				11	17		11	17		5.5	8.5		

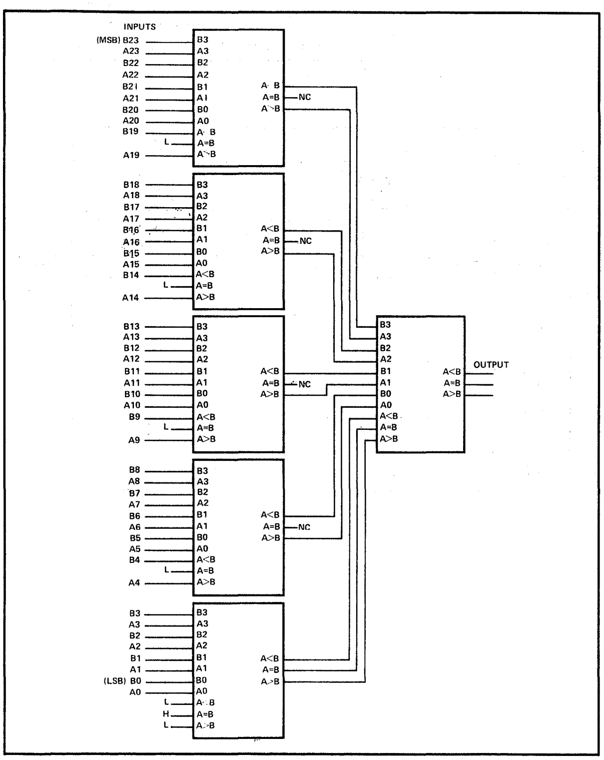
Load circuit and typical waveforms are shown at the front of section.

TYPICAL APPLICATION DATA

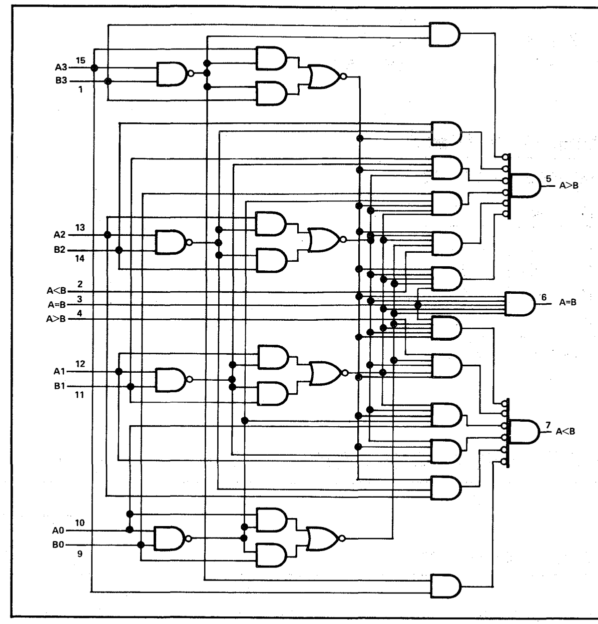
COMPARISON OF TWO N-BIT WORDS

This application demonstrates how these magnitude comparators can be cascaded to compare longer words. The example illustrated shows the comparison of two 24-bit words; however, the design is expandable to n-bits. As an example, one comparator can be used with five of the 24-bit comparators illustrated to expand the word length to 120-bits. Typical comparison times for various word lengths using the 54/74LS85 are:

WORD LENGTH	NUMBER OF PKGS	
1-4 bits	1	24 ns
5-24 bits	2-6	48 ns
25-120 bits	8-31	72 ns



BLOCK DIAGRAM

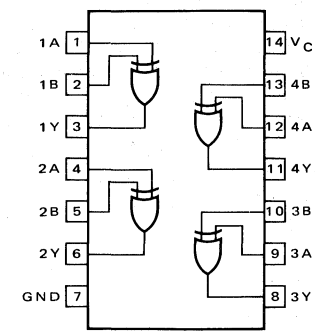


SPEED/PACKAGE AVAILABILITY

54	F,W	74	A,F
54LS	F,W	74LS	A,F
54S	F,W	74S	A,F

PIN CONFIGURATION

A,F,W PACKAGE



positive logic: Y = A ⊕ B = $\overline{A}B + A\overline{B}$

FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

H= high level, L = low level

SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

TEST CONDITIONS			54/74 C_L=15pF R_L=400Ω			54/74LS C_L=15pF R_L=2k			54/74S C_L=15pF R_L=280			
PARAMETER	FROM INPUT	TO OUTPUT	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
Propagation delay time t_{PLH} Low-to-high	A or B Other input low			15	23		12	23		7	10.5	ns
t_{PHL} High-to-low	A or B			11	17		10	17		6.5	10	
t_{PLH} Low-to-high	Other input high			18	30		10	30		7	10.5	
t_{PHL} High-to-low				13	22		18	22		6.5	10	

Load circuit and typical waveforms are shown at the front of section.

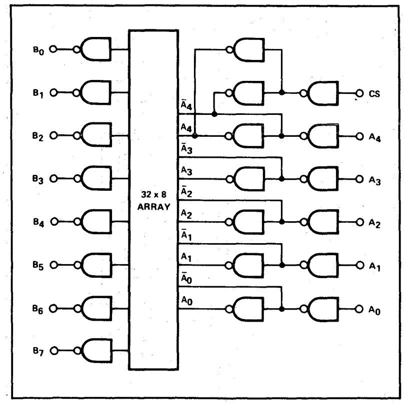
256-BIT READ-ONLY MEMORY 7488

SPEED/PACKAGE AVAILABILITY

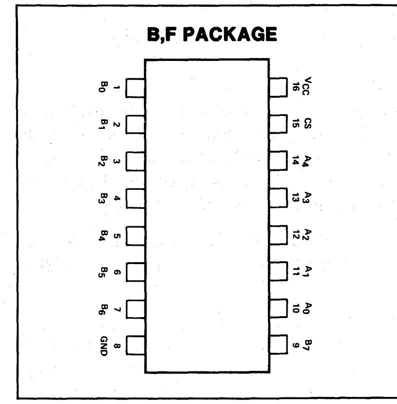
74 B,F

NOTE: For specific electrical data, refer to 82S23/123 data sheet in Memories section.

LOGIC DIAGRAM



PIN CONFIGURATION



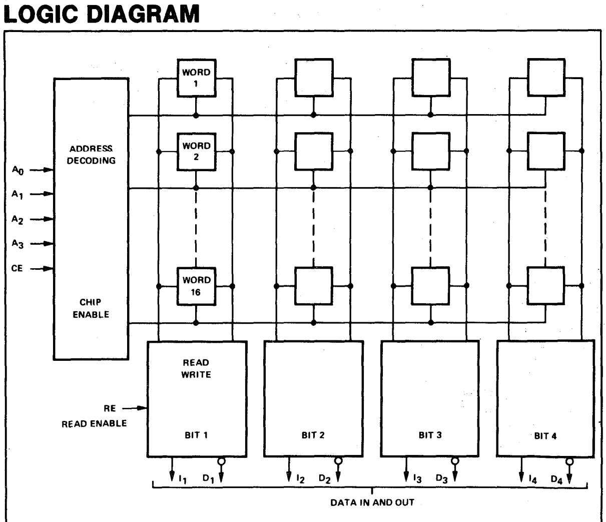
64-BIT READ/WRITE MEMORY (RAM) 7489

SPEED/PACKAGE AVAILABILITY

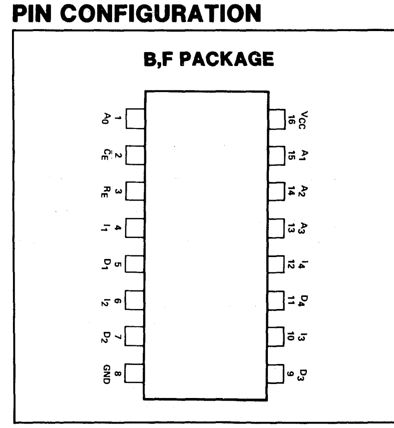
74 B,F

NOTE: For specific electrical data, refer to 82S23/123 in Bipolar Memories section.

LOGIC DIAGRAM



PIN CONFIGURATION



SPEED/PACKAGE AVAILABILITY

54	F,W	74	A,F
54LS	F,W	74LS	A,F

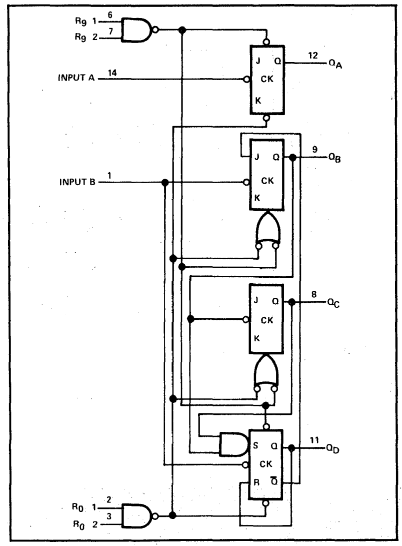
DESCRIPTION

This monolithic counter contains four master-slave flip-flops and additional gating to provide a divide-by-two counter and a three-stage binary counter for which the count cycle length is divide-by-five.

The 54/74LS90 also has a gated zero reset and gated set-to-nine inputs for use in BCD nine's complement applications.

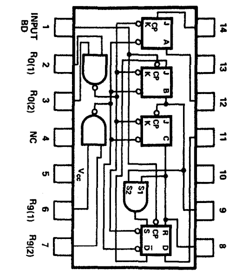
To use its maximum count length of this counter, the B input is connected to the Q_A output. The input count pulses are applied to input A and the outputs are as described in the function table. A symmetrical divide-by-ten count can be obtained by connecting the Q_D output to the A input and applying the input count to the B input which gives a divide-by-ten square wave at output Q_A.

BLOCK DIAGRAM 54LS/74LS

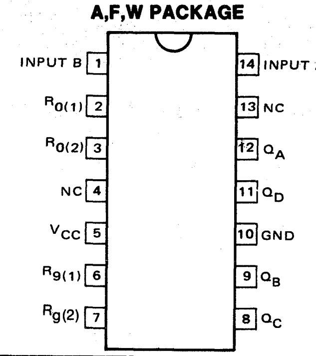


PIN CONFIGURATION

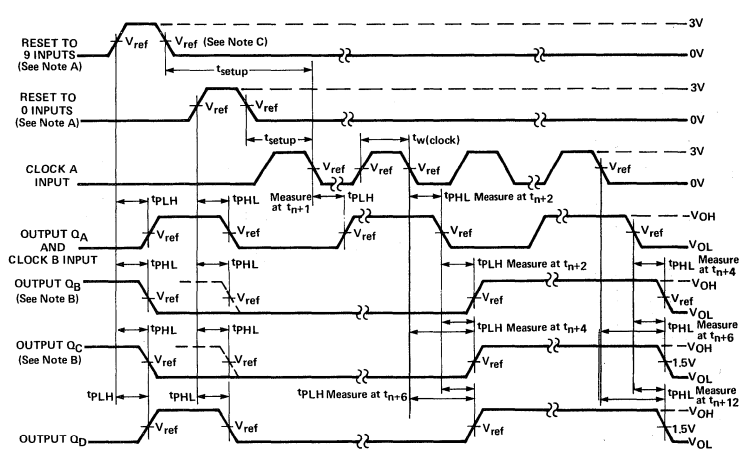
54/74
A,F,W PACKAGE



54LS/74LS
A,F,W PACKAGE



PARAMETER MEASUREMENT INFORMATION



VOLTAGE WAVEFORMS

A. Each reset input is tested separately with the other reset at 4.5 V.
B. Reference waveforms are shown with dashed lines.
C. V_{ref} = 1.3 V.
Load circuit is shown at front of section (for totem pole outputs).

SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

TEST CONDITIONS				54/74 C_L=15pF R_L=400Ω			54/74LS C_L=15pF R_L=2kΩ			
PARAMETER		FROM INPUT	TO OUTPUT	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
f_{Count}	Count frequency			10	18					MHz
		A	Q_A				32	42		
		B	Q_B				16			
$t_{w(Clock)}$	Width of			50						ns
	clock pulse	A	Q				15			
		B	Q				30			
		Reset	Q				15			
$t_{w(Reset)}$	Width of reset pulse			50			25			ns
Propagation delay time										
t_{PLH}	Low-to-high	Input Count Pulse	Q_C		60	100				ns
t_{PHL}	High-to-low				60	100				
t_{PLH}	Low-to-high	A	Q_A					10	16	
t_{PHL}	High-to-low							12	18	
t_{PLH}	Low-to-high	A	Q_D					32	48	
t_{PHL}	High-to-low							34	50	
t_{PLH}	Low-to-high	B	Q_B					10	16	
t_{PHL}	High-to-low							14	21	
t_{PLH}	Low-to-high	B	Q_C					21	32	
t_{PHL}	High-to-low							23	35	
t_{PLH}	Low-to-high	B	Q_D					21	32	
t_{PHL}	High-to-low							23	35	
t_{PHL}	High-to-low	Set-to-0	Any					26	40	
t_{PLH}	Low-to-high	Set-to-9	Q_A,Q_D					20	30	
t_{PHL}	High-to-low	Set-to-9	Q_B,Q_C					26	40	

Load circuit and typical waveforms shown at front of section .

BCD COUNT SEQUENCE (See Note A)

COUNT	OUTPUT Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

BI-QUINARY (5-2) (See Note B)

COUNT	OUTPUT Q_A	Q_D	Q_C	Q_B
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	H	L	L	L
6	H	L	L	H
7	H	L	H	L
8	H	L	H	H
9	H	H	L	L

RESET/COUNT FUNCTION TABLE

RESET INPUTS $R_{0(1)}$	$R_{0(2)}$	$R_{9(1)}$	$R_{9(2)}$	OUTPUT Q_D	Q_C	Q_B	Q_A
H	H	L	X	L	L	L	L
H	H	X	L	L	L	L	L
X	X	H	H	H	L	L	H
X	L	X	L	COUNT			
L	X	L	X	COUNT			
L	X	X	L	COUNT			
X	L	L	X	COUNT			

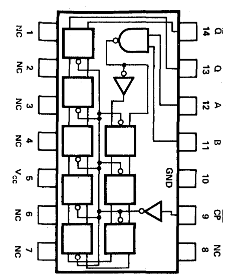
NOTES:
A. Output Q_A is connected to input B for BCD count.
B. Output Q_D is connected to input A for bi-quinary count.
C. Output Q_A is connected to input B.
D. H = high level, L = low level, X = irrelevant

SPEED/PACKAGE AVAILABILITY

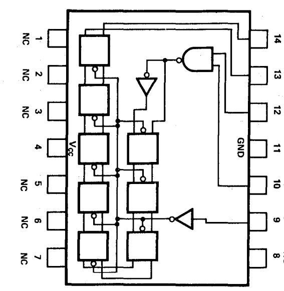
54 F,W 74 A,F

PIN CONFIGURATION

A,F PACKAGE



W PACKAGE



SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

TEST CONDITIONS	54/74 C_L=15pF R_L=400Ω			
PARAMETER	**MIN**	**TYP**	**MAX**	**UNIT**
f_{Max}	10	18		MHz
Propagation delay time				
t_{PLH} Low-to-high		24	40	ns
t_{PHL} High-to-low		27	40	

Load circuit and typical waveforms are shown at the front of section.

TRUTH TABLE

t_n		t_n+8
A	B	Q
0	0	0
0	1	0
1	0	0
1	1	1

NOTES:
1. t_n = bit time before clock pulse.
2. t_n+8 = bit time after 8 clock pulse.

DIVIDE-BY-TWELVE COUNTER 54/7492

SPEED/PACKAGE AVAILABILITY

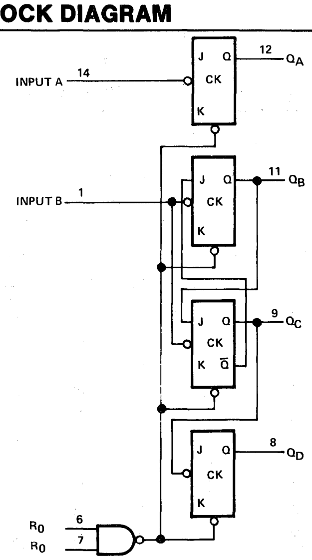
54 F,W 74 A,F

DESCRIPTION

This monolithic counter contains four master-slave flip-flops and additional gating to provide a divide-by-two counter and a three stage binary counter for which the count cycle length is divide-by-six.

To use its maximum count length of this counter, the B input is connected to the Q_A output. The input count pulses are applied to input A and the outputs are as described in the function table.

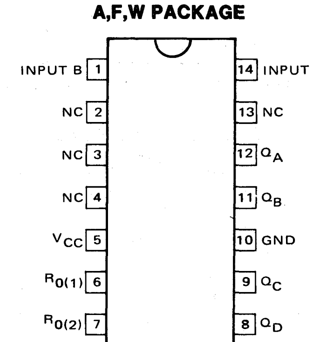
BLOCK DIAGRAM



The J and K inputs shown without connection for reference only and are functionally at a high level.

PIN CONFIGURATION

A,F,W PACKAGE



SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

TEST CONDITIONS				54/74 C_L=15pF R_L=400			54/74LS C_L=15pF R_L=2k			
PARAMETER		FROM INPUT	TO OUTPUT	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
f_{Count}	Count frequency			10	18					MHz
		A	Q_A				32	42		
		B	Q_B				16			
t_W	Width of pulse	A	Q				15			ns
		B	Q				30			
		Reset	Q				15			
t_{Setup}	Input setup time						25			ns
Propagation delay time										
t_{PLH}	Low-to-high	Input Count Pulse	Q_D		60	100				ns
t_{PHL}	High-to-low				60	100				
t_{PLH}	Low-to-high	A	Q_A					10	16	
t_{PHL}	High-to-low							12	18	
t_{PLH}	Low-to-high	A	Q_D					32	48	
t_{PHL}	High-to-low							34	50	
t_{PLH}	Low-to-high	B	Q_B					10	16	
t_{PHL}	High-to-low							14	21	
t_{PLH}	Low-to-high	B	Q_C					10	16	
t_{PHL}	High-to-low							14	21	
t_{PLH}	Low-to-high	B	Q_D					21	32	
t_{PHL}	High-to-low							23	35	
t_{PHL}	High-to-low	Set-to-0	Any					26	40	

RESET/COUNT FUNCTION TABLE

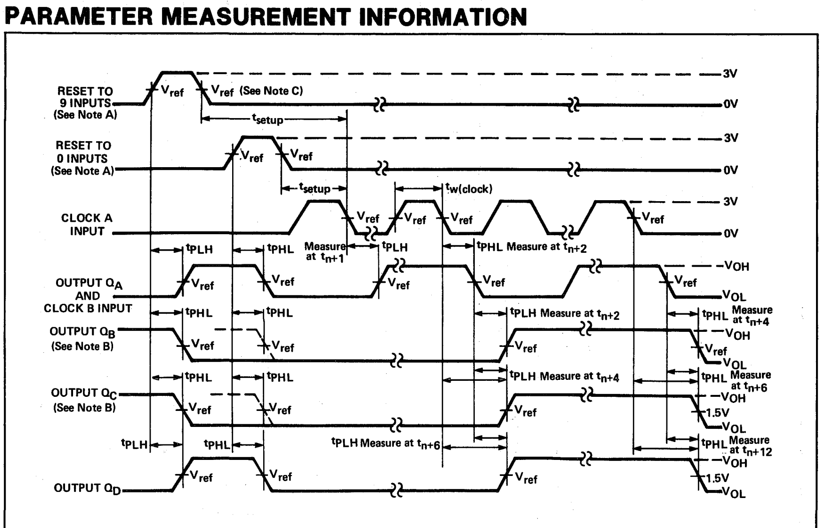
RESET INPUTS		OUTPUT			
$R_{0(1)}$	$R_{0(2)}$	Q_D	Q_C	Q_B	Q_A
H	H	L	L	L	L
L	X	COUNT			
X	L	COUNT			

COUNT SEQUENCE

COUNT	OUTPUT			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	H	L	L	L
7	H	L	L	H
8	H	L	H	L
9	H	L	H	H
10	H	H	L	L
11	H	H	L	H

Output Q_A is connected to Input B.

PARAMETER MEASUREMENT INFORMATION



VOLTAGE WAVEFORMS

NOTES:
A. Each reset input is tested separately with the other reset at 4.5 V.
B. Reference waveforms are shown with dashed lines.
C. V_{ref} = 1.8 V.
Load circuit shown at front of book (for totem pole outputs).

SPEED/PACKAGE AVAILABILITY

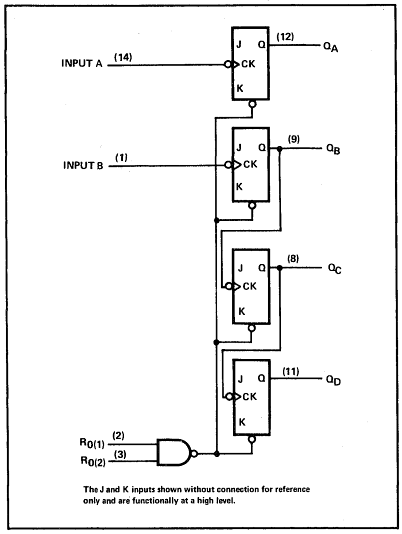
54	A,F,W	74	A,F
54LS	F,W	74LS	A,F

DESCRIPTION

This monolithic counter contains four master-slave flip-flops and additional gating to provide a divide-by-two counter and a three stage binary counter for which the count cycle length is divide-by-eight.

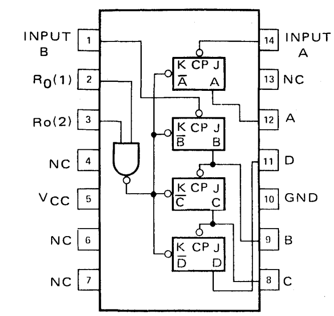
To use its maximum count length of this counter, the B input is connected to the Q_A output. The input count pulses are applied to input A and the outputs are as described in the function table.

BLOCK DIAGRAM

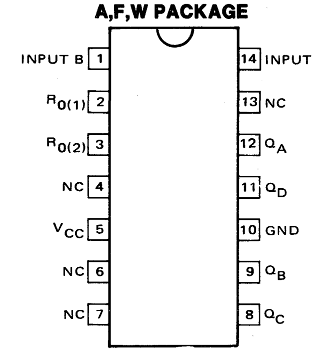


PIN CONFIGURATION

54/74
A,F,W PACKAGE



54/74LS
A,F,W PACKAGE



SWITCHING CHARACTERISTICS $V_{CC} = 5V$, $T_A = 25°C$

TEST CONDITIONS				54/74 $C_L=15pF$ $R_L=400\Omega$			54/74LS $C_L=15pF$ $R_L=2k\Omega$			
PARAMETER		**FROM INPUT**	**TO OUTPUT**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNIT**
f_{Count}	Count frequency			10	18					MHz
		A	Q_A				32	42		
		B	Q_B				16			
t_W	Width of pulse			50						ns
		A	Q				15			
		B	Q				30			
		Reset	Q	50			15			
t_{Setup}	Input setup time						25			ns
Propagation delay time										
t_{PLH}	Low-to-high	Input Count Pulse	Q_D		75	135				ns
t_{PHL}	High-to-low				75	135				
t_{PLH}	Low-to-high	A	Q_A					10	16	
t_{PHL}	High-to-low							12	18	
t_{PLH}	Low-to-high	A	Q_D					46	70	
t_{PHL}	High-to-low							46	70	
t_{PLH}	Low-to-high	B	Q_B					10	16	
t_{PHL}	High-to-low							14	21	
t_{PLH}	Low-to-high	B	Q_C					21	32	
t_{PHL}	High-to-low							23	35	
t_{PLH}	Low-to-high	B	Q_D					34	51	
t_{PHL}	High-to-low							34	51	
t_{PHL}	High-to-low	Set-to-0	Any					26	40	

COUNT SEQUENCE

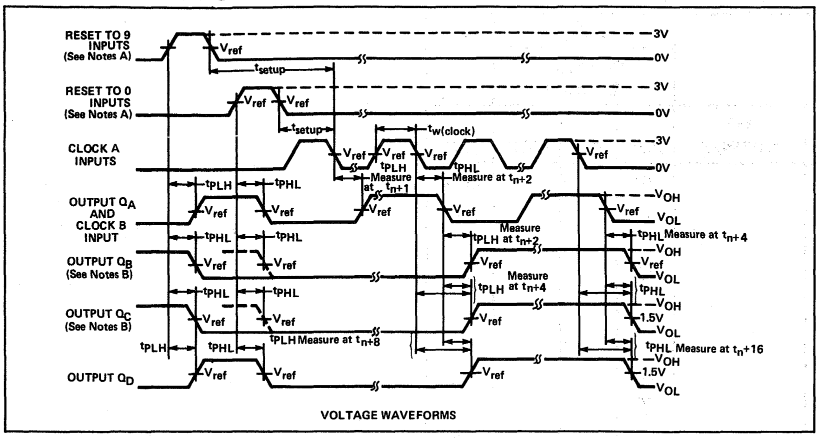
COUNT	OUTPUT Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

Output Q_A is connected to input B.

RESET/COUNT FUNCTION TABLE

RESET INPUTS		OUTPUT			
$R_{0(1)}$	$R_{0(2)}$	Q_D	Q_C	Q_B	Q_A
H	H	L	L	L	L
L	X	COUNT			
X	L	COUNT			

PARAMETER MEASUREMENT INFORMATION



VOLTAGE WAVEFORMS

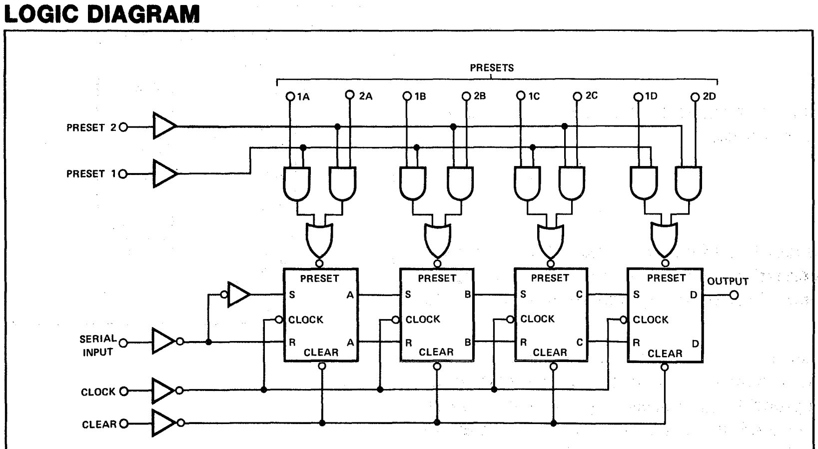
NOTES:
A. Each reset input is tested separately with the other reset at 4.5 V.
B. Reference waveforms are shown with dashed lines.
C. V_{ref} = 1.8 V.
Load circuit shown at front of book (for totem pole outputs).

4-BIT SHIFT REGISTER 54/7494

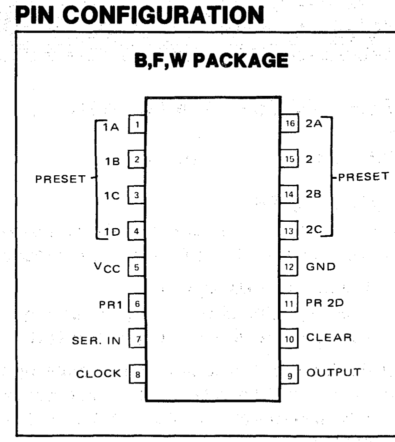
SPEED/PACKAGE AVAILABILITY

54 F,W 74 B,F

LOGIC DIAGRAM



PIN CONFIGURATION



LOGIC

SWITCHING CHARACTERISTICS $V_{CC} = 5V$, $T_A = 25°C$

TEST CONDITIONS				54/74 $C_L = 15pF$ $R_L = 400\Omega$			
PARAMETER		FROM INPUT	TO OUTPUT	MIN	TYP	MAX	UNIT
f_{Clock}	Clock frequency			10			MHz
$t_{w(Clock)}$	Width of clock pulse			35			ns
$t_{w(Clear \ \& \ Preset)}$	Width of clear and preset pulse			30			ns
t_{Setup}	Input setup time						
	High level			35			ns
	Low level			25			
t_{Hold}	Input hold time			0			ns
Propagation delay time							
t_{PLH}	Low-to-high	Clock			25	40	ns
t_{PHL}	High-to-low				25	40	
t_{PLH}	Low-to-high	Preset				35	
t_{PHL}	High-to-low	Clear				40	

Load circuit and typical waveforms are shown at the front of section.

4-BIT PARALLEL-ACCESS SHIFT REGISTER 54/7495/95B

SPEED/PACKAGE AVAILABILITY

54	F	74	A,F
54LS	F,W	74LS	A,F

DESCRIPTION

This 4-bit register features parallel and serial inputs, parallel outputs, mode control, and two clock inputs. The register has three modes of operation:

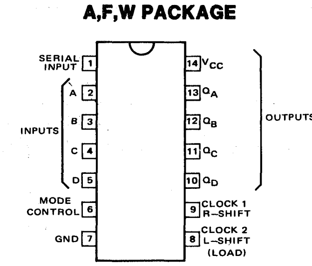
Parallel (broadside) load
Shift right (the direction Q_A toward Q_D)
Shift left (the direction Q_D toward Q_A)

Parallel loading is accomplished by applying the four bits of data and taking the mode control input high. The data is loaded into the associated flip-flops and appears at the outputs after the high-to-low transition of the clock-2 input. During loading, the entry of serial data is inhibited.

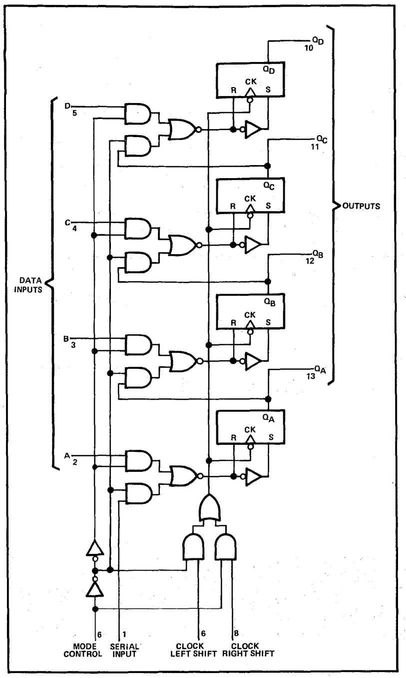
Shift right is accomplished on the high-to-low transition of clock 1 when the mode control is low; shift left is accomplished on the high-to-low transition of clock 2 when the mode control is high by connecting the output of each flip-flop to the parallel input of the previous flip-flop (Q_D to input C, etc.) and serial data is entered at input D. The clock input may be applied commonly to clock 1 and clock 2 if both modes can be clocked from the same source. Changes at the mode control input should normally be made while both clock inputs are low; however, conditions described in the last three lines of the function table will also ensure that register contents are protected.

PIN CONFIGURATION

A,F,W PACKAGE



BLOCK DIAGRAM



FUNCTION TABLE

INPUTS								OUTPUTS			
MODE CONTROL	CLOCKS 2(L)	CLOCKS 1(R)	SERIAL	PARALLEL A	B	C	D	Q_A	Q_B	Q_C	Q_D
H	H	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
H	↓	X	X	a	b	c	d	a	b	c	d
H	↓	X	X	Q_B*	Q_C*	Q_D*	d	Q_{Bn}	Q_{Cn}	Q_{Dn}	d
L	L	H	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
L	X	↓	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}
L	X	↓	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}
↑	L	L	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
↓	L	L	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
↓	L	H	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
↑	H	L	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
↑	H	H	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}

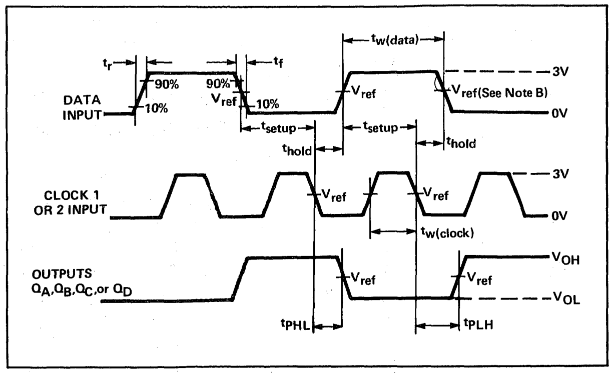
*Shifting left requires external connection of Q_B to A, Q_C to B, and Q_D to C. Serial data is entered at input D,
H = high level (steady state), L = low level (steady state), X = irrelevant (any input, including transitions)
↓ = transition from high to low level, ↑ = transition from low to high level
a, b, c, d = the level of steady-state input at Inputs A, B, C, or D, respectively.
Q_{A0}, Q_{B0} Q_{C0}, Q_{D0} = the level of Q_A, Q_B, Q_C, or Q_D, respectively, before the indicated steady state input conditions were established.
Q_{An}, Q_{Bn}, Q_{Cn}, Q_{Dn} = the level of Q_A, Q_B, Q_C, or Q_D, respectively, before the most-recent ↓ transition of the clock.

SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

TEST CONDITIONS		54/74 C_L=15pF R_L=400Ω			54/74LS C_L=15pF R_L=2kΩ			
PARAMETER		MIN	TYP	MAX	MIN	TYP	MAX	UNIT
f_{Max}		25	36		25	36		MHz
$t_{w(Clock)}$	Width of clock pulse	(54)			25			ns
		20	10					
		(74)						
		15	10					
t_{Setup}	Input setup time	10			20↓			ns
t_{Hold}	Input hold time	0			10↓			ns
$t_{Enable\ 1}$	Time to enable clock 1	15			20↓			ns
$t_{Enable\ 2}$	Time to enable clock 2	15			20↓			ns
$t_{Inhibit\ 1}$	Time to enable clock 1	5			20↑			ns
$t_{Inhibit\ 2}$	Time to inhibit clock 2	5			20↑			ns
Propagation delay time								
t_{PLH}	Low-to-high (CLK)		18	27		18	27	ns
t_{PHL}	High-to-low (CLK)		21	32		21	32	

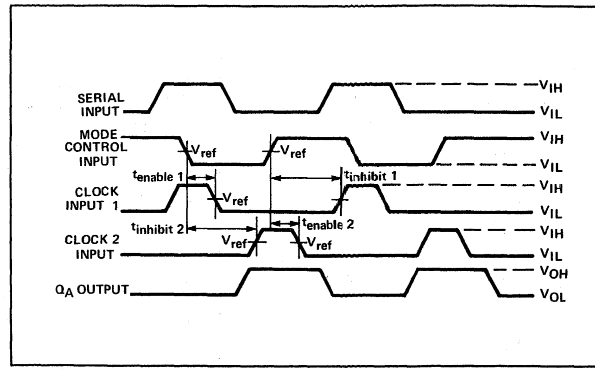
LOGIC

PARAMETER MEASUREMENT INFORMATION



SWITCHING TIMES

NOTES:
A. When testing f_{Clock} vary PRR. $t_{w(Data)} \geq 20$ ns. $t_{w(Clock)} \geq 15$ ns.
B. $V_{ref} = 1.3v$
Load circuit shown at front of book (totem pole outputs).



CLOCK ENABLE/INHIBIT TIMES

NOTES:
A. Input A is at a low level.
B. $V_{ref} = 1.3$ V.

5-BIT SHIFT REGISTER 54/7496

SPEED/PACKAGE AVAILABILITY

54	F,W	74	B,F
54LS	F,W	74LS	B,F

DESCRIPTION

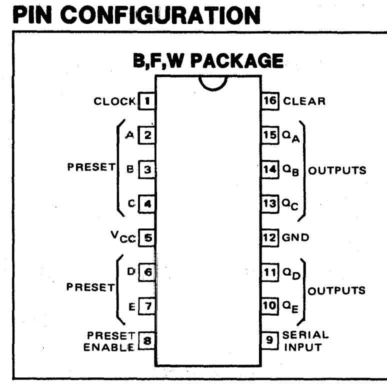
This shift register consists of five R-S master-slave flip-flops connected to perform parallel-to-serial or serial-to-parallel conversion of binary data. Since both inputs and outputs for all flip-flops are accessible, parallel-in/parallel-out or serial-in/serial-out operation may be performed.

All flip-flops are simultaneously set to a low output level by applying a low-level voltage to the clear input while the preset is inactive (low). Clearing is independent of the level of the clock input.

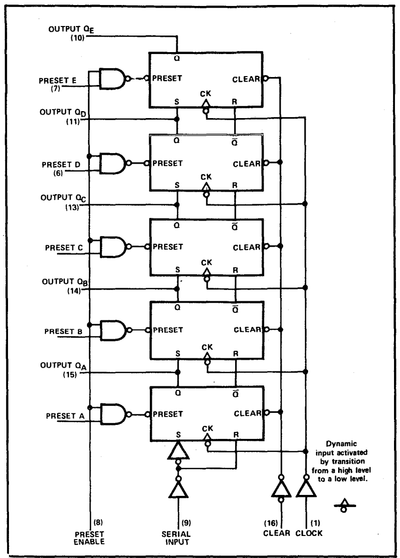
The register may be parallel loaded by using the clear input in conjunction with the preset inputs. After clearing all stages to low output levels, data to be loaded is applied to the individual preset inputs (A, B, C, D, and E) and a high-level load pulse is applied to the preset enable input. Presetting like clearing is independent of the level of the clock input.

Transfer of information to the outputs occurs on the positive-going edge of the clock pulse. The proper information must be set up at the R-S inputs of each flip-flop prior to the rising edge of the clock input waveform. The serial input provides this information to the first flip-flop, while the outputs of the subsequent flip-flops provide information for the remaining R-S inputs. The clear input must be high and the preset or preset enable inputs must be low when clocking occurs.

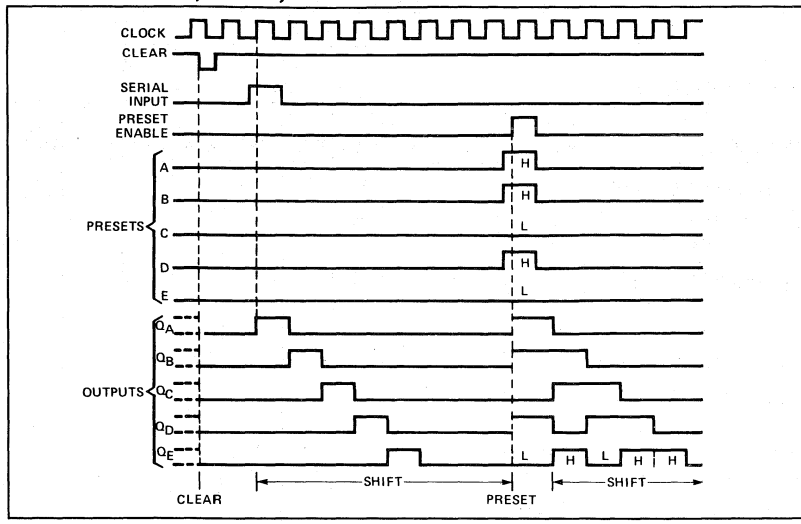
PIN CONFIGURATION



FUNCTIONAL BLOCK DIAGRAM



TYPICAL CLEAR, SHIFT, PRESET AND SHIFT SEQUENCES

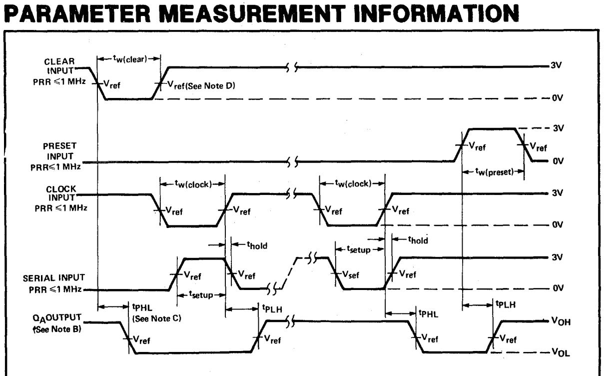


FUNCTION TABLE

INPUTS									OUTPUTS				
		PRESET											
CLEAR	PRESET ENABLE	A	B	C	D	E	CLOCK	SERIAL	Q_A	Q_B	Q_C	Q_D	Q_E
L	L	X	X	X	X	X	X	X	L	L	L	L	L
L	X	L	L	L	L	L	X	X	L	L	L	L	L
H	H	H	H	H	H	H	X	X	H	H	H	H	H
H	H	L	L	L	L	L	L	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	Q_{E0}
H	H	H	L	H	L	H	L	X	H	Q_{B0}	H	Q_{D0}	H
H	L	X	X	X	X	X	L	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	Q_{E0}
H	L	X	X	X	X	X	↑	H	H	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{Dn}
H	L	X	X	X	X	X	↑	L	L	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{Dn}

H = high level (steady state), L = low level (steady state)
X = irrelevant (any input, including transitions)
↑ = transition from low to high level
Q_{A0}, Q_{B0}, etc = the level of Q_A, Q_B, etc, respectively before the indicated steady-state input conditions were established.
Q_{An}, Q_{Bn}, etc = the level of Q_A, Q_B, etc, respectively before the most recent ↑ transition of the clock.

PARAMETER MEASUREMENT INFORMATION



VOLTAGE WAVEFORMS

NOTES:
A. Preset may be tested by applying a high-level voltage to the individual preset inputs and pulsing the preset enable or by applying a high-level voltage to the preset enable and pulsing the individual preset inputs.
B. Q_A output is illustrated. Relationship of serial input to other Q outputs is illustrated in the typical shift squence.
C. Outputs are set to the high level prior to the measurement of t_{PHL} from the clear input.
D. V_{ref} = 1.3V
Load circuit shown at front of book (totem pole outputs.)

SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

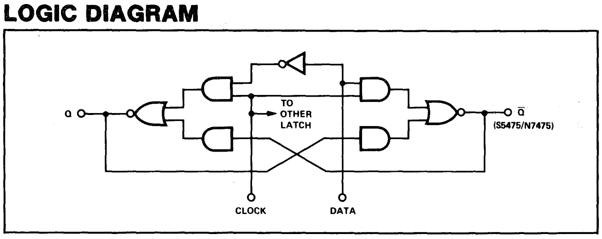
TEST CONDITIONS			54/74 C_L=15pF R_L=400Ω			54/74LS C_L=15pF R_L=2kΩ			
PARAMETER	FROM INPUT	TO OUTPUT	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
f_{Clock} Clock frequency			10			10			MHz
$t_{w(Clock)}$ Width of clock pulse			35			35			ns
$t_{w(Preset \& Clear)}$ Width preset & clear pulse			30			30			ns
t_{Setup} Input setup time			30			30†			ns
t_{Hold} Input hold time			0			0†			ns
Propagation delay time									
t_{PLH} Low-to-high	Clock			25	40		25	40	ns
t_{PHL} High-to-low				25	40		25	40	
t_{PLH} Low-to-high	Preset				35				
t_{PHL} High-to-low				28	40				
t_{PLH} Low-to-high	Preset, Preset Enable						28	35	
t_{PHL} High-to-low	Clear				55			55	

4-BIT BISTABLE LATCH 54/74100

SPEED/PACKAGE AVAILABILITY

54 Q,F 74 N,F

LOGIC DIAGRAM



TRUTH TABLE

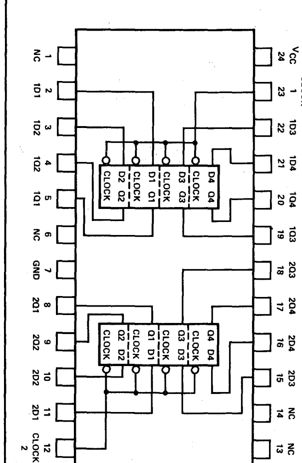
(Each Latch)	
t_n	t_n+1
D	Q
1	1
0	0

NOTES:
1. t_n=bit time before clock negative going transition.
2. t_n+1=bit time after clock negative-going transition.

NC — No internal connection.

PIN CONFIGURATION

F,Q,N PACKAGE



SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

TEST CONDITIONS				54/74 C_L=15pF R_L=400Ω			
PARAMETER		FROM INPUT	TO OUTPUT	MIN	TYP	MAX	UNIT
t_W	Width of Pulse			20			ns
t_{Setup}	Input setup time			20			ns
Propagation delay time							
t_{PLH}	Low-to-high	D	Q		16	30	ns
t_{PHL}	High-to-low				14	25	
t_{PLH}	Low-to-high	C	Q		16	30	
t_{PHL}	High-to-low				7	15	

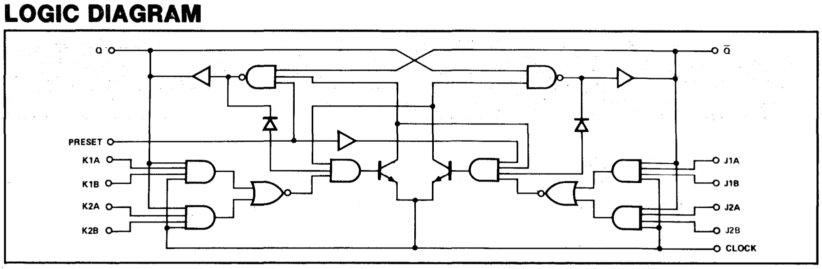
Load circuit and typical waveforms are shown at the front of section.

J-K EDGE-TRIGGERED FLIP-FLOP 54/74101

SPEED/PACKAGE AVAILABILITY

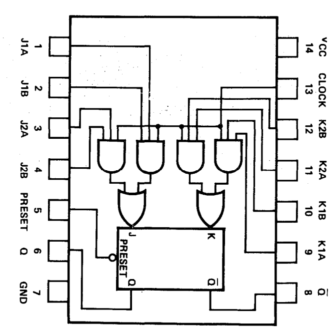
54H F,W 74H A,F

LOGIC DIAGRAM

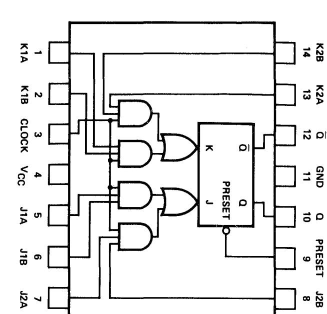


PIN CONFIGURATION

AF PACKAGE



W PACKAGE



TRUTH TABLE

t_n		t_{n+1}
J	K	Q
0	0	Q_n
0	1	0
1	0	1
1	1	$\overline{Q}_n$

NOTES:
1. J=(J1A•J1B)+(J2A•J2B)
2. K=(K1A•K1B)+(K2A•K2B)
3. t_n=Bit time before clock pulse
4. t_{n+1}=Bit time after clock pulse

SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

TEST CONDITIONS				54/74H C_L=25pF R_L=280Ω			
PARAMETER		FROM INPUT	TO OUTPUT	MIN	TYP	MAX	UNIT
t_{Clock}	Clock frequency			40	50		MHz
$t_{w(Clock)}$	Width of clock pulse High level Low level			 10 15			 ns
$t_{w(Clear)}$	Width of clear pulse			16			ns
t_{Setup}	Input setup time Data high Data low			 10 13			 ns
t_{Hold}	Input hold time			0			ns
Propagation delay time							
t_{PLH}	Low-to-high	Preset			8	12	ns
t_{PHL}	High-to-low						
t_{PHL}	Clock low Clock high				23 15	35 20	
t_{PLH}	Low-to-high	Clock		5	10	15	
t_{PHL}	High-to-low			8	16	20	

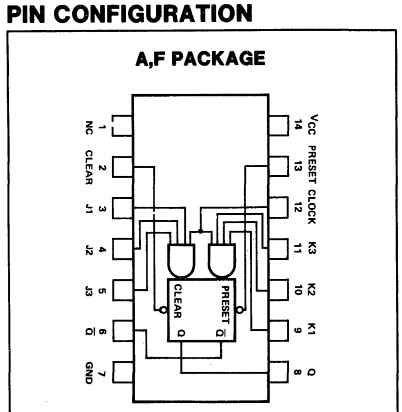
Load circuit and typical waveforms are shown at the front of section.

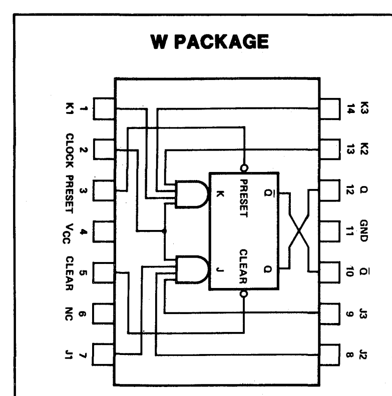
J-K EDGE-TRIGGERED FLIP-FLOP WITH AND INPUTS 54/74102

SPEED/PACKAGE AVAILABILITY

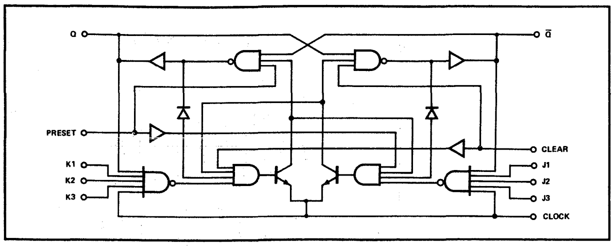
54H F,W 74H A,F

PIN CONFIGURATION





LOGIC DIAGRAM



TRUTH TABLE

t_n J	t_n K	t_n+1 Q
0	0	Q_n
0	1	0
1	0	1
1	1	$\overline{Q}_n$

NOTES:
1. J = J1 • J2 • J3
2. K = K1 • K2 • K3
3. t_n = bit time before clock pulse.
4. t_n+1 = bit time after clock pulse.
5. NC—no internal connection.

SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

TEST CONDITIONS			54/74H C_L=25pF R_L=280Ω			
PARAMETER	FROM INPUT	TO OUTPUT	MIN	TYP	MAX	UNIT
f_{Clock} Clock frequency			40	50		MHz
$t_{w(Clock)}$ Width of clock pulse						
High level			10			ns
Low level			15			
$t_{w(Clear)}$ Width of clear pulse			15			ns
t_{Setup} Input setup time						
Data high			10			ns
Data low			13			
t_{Hold} Input hold time			0			ns
Propagation delay time						
t_{PLH} Low-to-high	Preset			8	12	ns
t_{PHL} High-to-low						
Clock Low				23	35	
Clock high				15	20	
t_{PLH} Low-to-high	Clock		5	10	15	
t_{PHL} High-to-low			8	16	20	

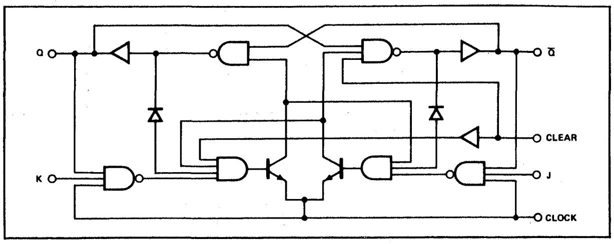
Load circuit and typical waveforms are shown at the front of section.

LOGIC

SPEED/PACKAGE AVAILABILITY

54H F,W 74H A,F

LOGIC DIAGRAM



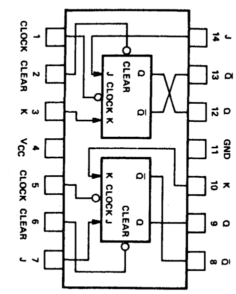
SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

TEST CONDITIONS				54/74H C_L=25pF R_L=280Ω			
PARAMETER		FROM INPUT	TO OUTPUT	MIN	TYP	MAX	UNIT
f_{Clock}	Clock frequency			40	50		MHz
$t_{w(Clock)}$	Width of clock pulse						
	High level			10			ns
	Low level			15			
$t_{w(Clear)}$	Width of clear pulse			16			ns
t_{Setup}	Input setup time Data High			10			ns
	Data low			13			
t_{Hold}	Input hold time			0			ns
Propagation delay time							
t_{PLH}	Low-to-high	Preset			8	12	ns
t_{PHL}	High-to-low				23	35	
	Clock high				15	20	
t_{PLH}	Low-to-high	Clock		5	10	15	
t_{PHL}	High-to-low			8	16	20	

Load circuit and typical waveforms are shown at the front of section.

PIN CONFIGURATION

A,F,W PACKAGE



TRUTH TABLE

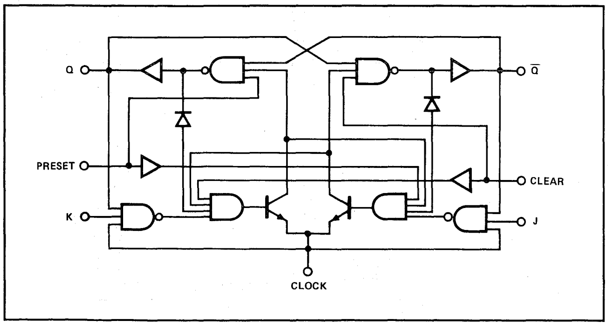
t_n		t_n+1
J	K	Q
0	0	Q_n
0	1	0
1	0	1
1	1	$\overline{Q}_n$

NOTES:
1. t_n = bit time before clock pulse
2. t_n+1 = bit time after clock pulse

SPEED/PACKAGE AVAILABILITY

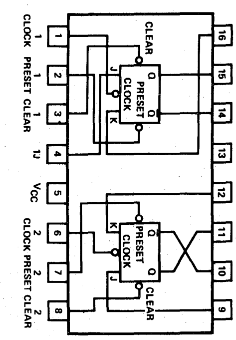
54H F,W   74H B,F

BLOCK DIAGRAM



PIN CONFIGURATION

B,F,W PACKAGE



SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

TEST CONDITIONS				54/74H C_L=25pF R_L=280Ω			
PARAMETER		**FROM INPUT**	**TO OUTPUT**	**MIN**	**TYP**	**MAX**	**UNIT**
f_{Clock}	Clock frequency			40	50		MHz
$t_{w(Clock)}$	Width of clock pulse						
	High level			10			ns
	Low Level			15			
$t_{w(Clear)}$	Width of clear pulse			16			ns
t_{Setup}	Input setup time						
	Data high			10			ns
	Data low			13			
t_{Hold}	Input hold time			0			ns
Propagation delay time							
t_{PLH}	Low-to-high	Preset			8	12	ns
t_{PHL}	High-to-low						
	Clock low				23	35	
	Clock high				15	20	
t_{PLH}	Low-to-high	Clock		5	10	15	
t_{PHL}	High-to-low			8	16	20	

Load circuit and typical waveforms are shown at the front of section.

TRUTH TABLE

t_n		t_n+1
J	K	Q
0	0	Q_n
0	1	0
1	0	1
1	1	$\overline{Q}_n$

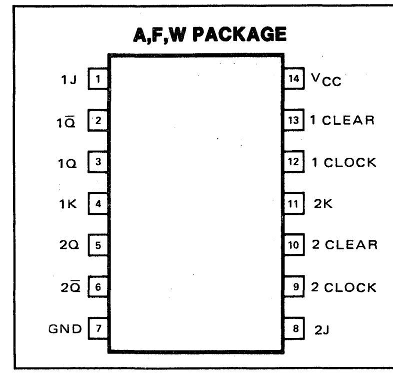
NOTES:
1. t_n=bit time before clock pulse.
2. t_n+1=bit time after clock pulse.

DUAL J-K MASTER-SLAVE FLIP-FLOP 54/74107

SPEED/PACKAGE AVAILABILITY

54	F	74	A,F
54LS	F,W	74LS	A,F

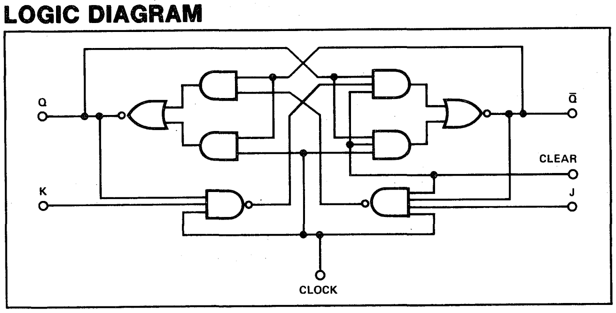
PIN CONFIGURATION



DESCRIPTION

A low logic level at the clear input resets the Q output to a low level regardless of the levels at the other inputs. With clear inactive (high), a high level at the clock input enables the J and K inputs and data will be accepted. The logic levels at the J and K inputs may be allowed to change when the clock pulse is high and the bistable will perform according to the function table, as long as minimum setup and hold times are observed. Input data is transferred to the outputs on the negative-going edge of the clock pulse.

LOGIC DIAGRAM



TRUTH TABLE (Each Flip-Flop)

INPUTS				OUTPUTS	
CLEAR	CLOCK	J	K	Q	$\overline{Q}$
L	X	X	X	L	H
H	↓	L	L	Q_0	$\overline{Q}_0$
H	↓	H	L	H	L
H	↓	L	H	L	H
H	↓	H	H	TOGGLE	
H	H	X	X	Q_0	$\overline{Q}_0$

H = high level (steady state)
L = low level (steady state)
X = irrelevant
↓ = transition from high to low level
Q_0 = the level of Q before the indicated input conditions were established.
TOGGLE: each output changes to the complement of its previous level on each ↓ clock transition.

SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

TEST CONDITIONS			54/74 C_L=15pF R_L=400Ω			54/74LS C_L=15pF R_L=2KΩ			
PARAMETER	FROM INPUT	TO OUTPUT	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
f_{Clock} Clock frequency			15	20		30	45		MHz
$t_{w\,(Clock)}$ Width of clock pulse						20			ns
Clock high			20						
Clock low			47						
$t_{w\,(Clear)}$ Width of clear pulse			25			25			ns
t_{Setup} Input setup time			0			20↓			ns
t_{Hold} Input hold time			0			0↓			ns
Propagation delay time									
t_{PLH} Low-to-high	Clear			16	25		11	20	ns
t_{PHL} High-to-low				25	40		15	30	
t_{PLH} Low-to-high	Clock		10	16	25		11	20	
t_{PHL} High-to-low			10	25	40		15	30	

Load circuit and typical waveforms are shown at the front of section.

SPEED/PACKAGE AVAILABILITY

54H F,W 74H A,F

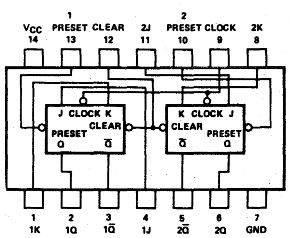
TRUTH TABLE

t_n		t_n+1
J	K	Q
0	0	Q_n
0	1	0
1	0	1
1	1	$\overline{Q}_n$

NOTES:
1. t_n = bit time before clock pulse
2. t_n+1 = bit time after clock pulse

PIN CONFIGURATION

A,F,W PACKAGE



SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

TEST CONDITIONS			54/74H C_L=25pF R_L=280Ω			
PARAMETER	FROM INPUT	TO OUTPUT	MIN	TYP	MAX	UNIT
f_{Clock} Clock frequency			40	50		MHz
$t_{w\ (Clock)}$ Width of clock pulse						
High level			10			ns
Low level			15			
$t_{w\ (Clear)}$ Width of clear pulse			16			ns
t_{Setup} Input setup time						
Data high			10			ns
Data low			13			
t_{Hold} Input hold time			0			ns
Propagation delay time						
t_{PLH} Low-to-high	Preset			8	12	ns
t_{PHL} High-to-low						
Clock low				23	35	
Clock high				15	20	
t_{PLH} Low-to-high	Clock		5	10	15	
t_{PHL} High-to-low			8	16	20	

Load circuit and typical waveforms are shown at the front of section.

SPEED/PACKAGE AVAILABILITY

54	F,W	74	B,F
54LS	F,W	74LS	B,F

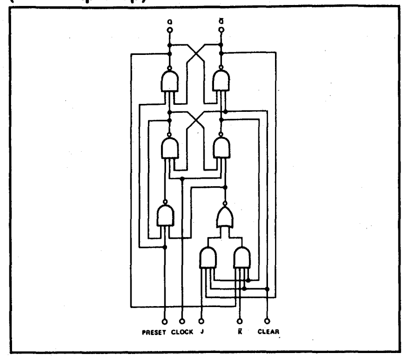
DESCRIPTION

A low level at preset or clear sets or resets the outputs regardless of the levels of the other inputs. When preset and clear are inactive (high), data at the J and $\overline{K}$ inputs meeting the setup time requirements are transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive-going pulse. Following the hold time interval, data at the J and $\overline{K}$ inputs may be changed without affecting the levels at the outputs.

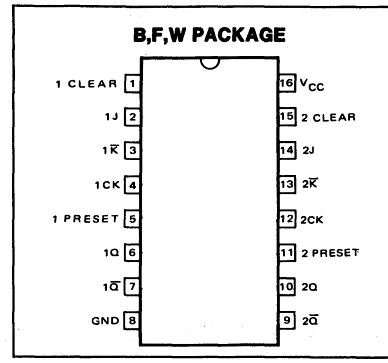
The J and $\overline{K}$ data inputs simplify hardware design as a D-type flip-flop can be implemented by simply tying the J and $\overline{K}$ inputs together.

FUNCTIONAL BLOCK DIAGRAM

(Each Flip-Flop)



PIN CONFIGURATION



TRUTH TABLE (Each Flip-Flop)

INPUTS					OUTPUTS	
PRESET	CLEAR	CLOCK	J	$\overline{K}$	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↑	L	L	L	H
H	H	↑	H	L	TOGGLE	
H	H	↑	L	H	Q_0	$\overline{Q}_0$
H	H	↑	H	H	H	L
H	H	L	X	X	Q_0	$\overline{Q}_0$

H = high level (steady state)
L = low level (steady state)
X = irrelevant
↑ = transition from low to high level
Q_0 = the level of Q before the indicated steady-state input conditions were established
TOGGLE: each output changes to the complement of its previous level on each ↑ clock transition.
*This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level.

SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

TEST CONDITIONS			54/74 C_L=15pF R_L=400Ω			54/74LS C_L=15pF R_L=2KΩ			
PARAMETER	FROM INPUT	TO OUTPUT	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
f_{Clock} Clock frequency			25	33		25	33		MHz
$t_{w\ (Clock)}$ Width of clock pulse			20			25			ns
$t_{w\ (Preset)}$ Width of preset pulse			20			25			ns
$t_{w\ (CLear)}$ Width of clear pulse			20			25			ns
t_{Setup} Input setup time			10↑			20↑			ns
t_{Hold} Input hold time			6↑			5↑			ns
Propagation delay time									
t_{PLH} Low-to-high	Clock	Q,Q̄	4	10	16				ns
t_{PHL} High-to-low			9	18	28				
t_{PLH} Low-to-high	Preset	Q		10	15				
t_{PHL} High-to-low	Preset	Q̄		23	35				
t_{PLH} Low-to-high	Clear	Q̄		10	15				
t_{PHL} High-to-low	Clear	Q		17	25				
t_{PLH} Low-to-high	CLR, PRE or CLK (as appropriate)						8	25	
t_{PHL} High-to-low							16	40	

Load circuit and typical waveforms are shown at the front of section.

DUAL J-K NEGATIVE EDGE-TRIGGERED FLIP-FLOP 54/74112

(Separate clock, preset and clear inputs)

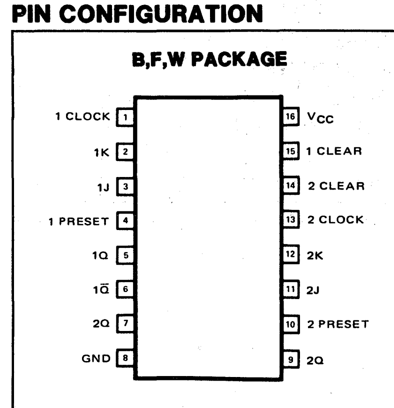
SPEED/PACKAGE AVAILABILITY

54LS F,W 74LS B,F
54S F,W 74S B,F

DESCRIPTION

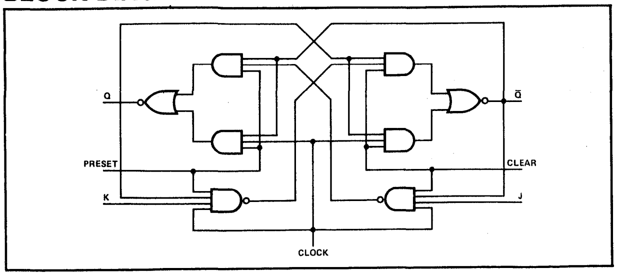
The preset or clear inputs, when low, set or reset the outputs regardless of the levels at the other inputs. When preset and clear inputs are inactive (high), a high level at the clock input enables the J and K inputs and data will be accepted. The logic levels at the J and K inputs may be allowed to change when the clock pulse is high and the bistable will perform according to the function table as long as minimum setup and hold times are observed. Input data is transferred to the outputs on the negative-going edge of the clock pulse.

PIN CONFIGURATION



LOGIC

BLOCK DIAGRAM



FUNCTIONAL TABLE (Each Flip-Flop)

INPUTS					OUTPUTS	
PRESET	CLEAR	CLOCK	J	K	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	L	Q_0	$\overline{Q_0}$
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	
H	H	H	X	X	Q_0	$\overline{Q_0}$

H = high level (steady state)
L = low level (steady state)
X = irrelevant
↓= transition from high to low level
Q_0 = the level of Q before the indicated steady-state input conditions were established.
TOGGLE: Each output changes to the complement of its previous level on each ↓ clock transition.
*This configuration is nonstable, that is, it will not persist when preset and clear inputs return to their inactive (high) level.

SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

TEST CONDITIONS			54/74LS C_L=15pF R_L=2kΩ			54/74S C_L=15pF R_L=280Ω			
PARAMETER	FROM INPUT	TO OUTPUT	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
f_{Clock} Clock frequency			30	45		80	125		MHz
$t_{w(Clock)}$ Width of clock pulse			20						ns
Clock high						6			
Clock low						6.5			
$t_{w(Preset)}$ Width of preset pulse			25			8			ns
$t_{w(Clear)}$ Width of clear pulse			25			8			ns
t_{Setup} Input setup time			20↓			3↓			ns
t_{Hold} Input hold time			0↓			0↓			ns
Propagation delay time									
t_{PLH} Low-to-high	CLR, PRE or CLK (as appropriate)			11	20	2	4	7	ns
t_{PHL} High-to-low				15	30	2	5	7	

Load circuit and typical waveforms are shown at the front of section.

DUAL J-K NEGATIVE EDGE-TRIGGERED FLIP-FLOP

(Separate clock and preset inputs)

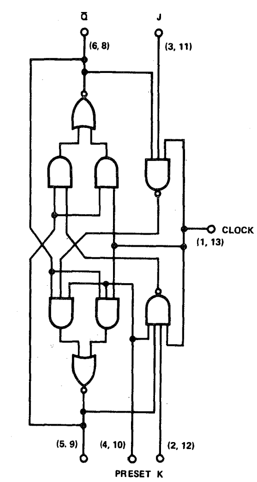
SPEED/PACKAGE AVAILABILITY

54LS F,W	74LS A,F
54S A,F,W	74S A,F

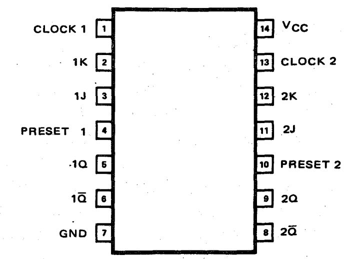
DESCRIPTION

A low level at the preset input sets the Q output high regardless of the levels at the other inputs. When preset is inactive (high), a high level at the clock input enables the J and K inputs and data will be accepted. The logic levels at the J and K inputs may be allowed to change when the clock pulse is high and the bistable will perform according to the function table as long as minimum setup and hold times are observed. Input data is transferred to the outputs on the negative-going edge of the clock pulse.

BLOCK DIAGRAM (Each Flip-Flop)



PIN CONFIGURATION



TRUTH TABLE (Each Flip-Flop)

Inputs				Outputs	
Preset	Clock	J	K	Q	Q̄
L	X	X	X	H	L
H	↓	L	L	Q_0	$\bar{Q}_0$
H	↓	H	L	H	L
H	↓	L	H	L	H
H	↓	H	H	Toggle	
H	H	X	X	Q_0	$\bar{Q}_0$

SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

TEST CONDITIONS			54/74LS C_L=15pF R_L=2kΩ			54/74S C_L=15pF R_L=280Ω			
PARAMETER	FROM INPUT	TO OUTPUT	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
f_{Clock} Clock frequency			30	45		80	125		MHz
$t_{w(Clock)}$ Width of Clock pulse			20						ns
Clock high						6			
Clock low						6.5			
$t_{w(Preset)}$ Width of preset pulse			25			8			ns
$t_{w(Clear)}$ Width of clear pulse			25						ns
t_{Setup} Input setup time			20↓			8			ns
t_{Hold} Input hold time			0↓			3↓			ns
Propagation delay time									
t_{PLH} Low-to-high	CLR, PRE or CLK (as appropriate)			11	20	2	4	7	ns
t_{PHL} High-to-low				15	30	2	5	7	

Load circuit and typical waveforms are shown at the front of section.

DUAL J-K NEGATIVE EDGE-TRIGGERED FLIP-FLOP — 54/74114

(Separate preset, common clock and clear)

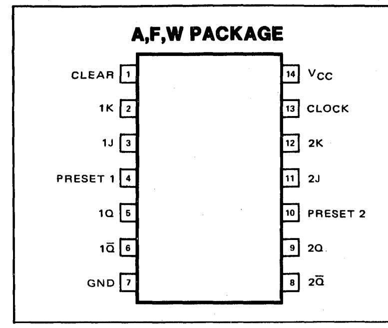
SPEED/PACKAGE AVAILABILITY

54LS F,W — 74LS A,F
54S A,F,W — 74S A,F

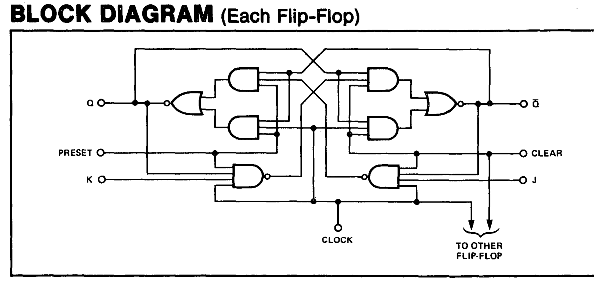
DESCRIPTION

The preset or clear inputs, when low, set or reset the outputs regardless of the levels at the other inputs. When preset and clear inputs are inactive (high), a high level at the clock input enables the J and K inputs and data will be accepted. The logic levels at the J and K inputs may be allowed to change when the clock pulse is high and the bistable will perform according to the function table as long as minimum setup and hold times are observed. Input data is transferred to the outputs on the negative-going edge of the clock pulse.

PIN CONFIGURATION



BLOCK DIAGRAM (Each Flip-Flop)



SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

TEST CONDITIONS			54/74LS C_L=15pF R_L=2kΩ			54/74S C_L=15pF R_L=280Ω			
PARAMETER	FROM INPUT	TO OUTPUT	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
f_{Clock} Clock frequency			30	45		80	125		MHz
$t_{w(Clock)}$ Width of clock pulse			20						ns
Clock high						6			
Clock low						6.5			
$t_{w(Preset)}$ Width of preset pulse			25			8			ns
$t_{w(Clear)}$ Width of clear pulse			25			8			ns
t_{Setup} Input setup time			20↓			3↓			ns
t_{Hold} Input hold time			0↓			0↓			ns
Propagation delay time									
t_{PLH} Low-to-high	CLR, PRE or CLK (as appropriate)			11	20	2	4	7	ns
t_{PHL} High-to-low				15	30	2	5	7	

Load circuit and typical waveforms are shown at the front of section.

TRUTH TABLE (Each Flip-Flop)

Inputs					Outputs	
Preset	Clear	Clock	J	K	Q	Q̄
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	L	Q_0	$\overline{Q}_0$
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	Toggle	
H	H	H	X	X	Q_0	$\overline{Q}_0$

H = high level (steady state)
L = low level (steady state)
X = irrelevant
↓ = transition from high to low level
Q0 = the level of Q before the indicated steady-state input conditions were established
TOGGLE: = Each output changes to the complement of its previous level on each clock transition.
*This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level.

SPEED/PACKAGE AVAILABILITY

54 F,Q 74 N,F

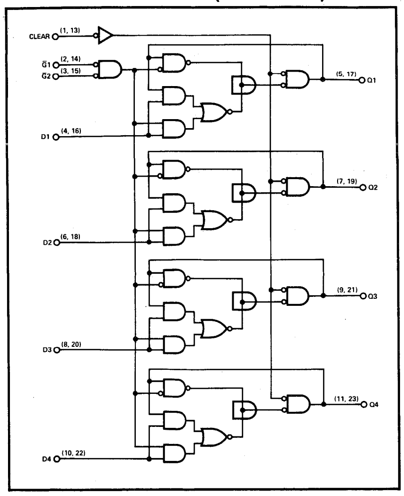
TRUTH TABLE (Each Latch)

INPUTS				OUTPUT
CLEAR	ENABLE $\overline{G1}$	ENABLE $\overline{G2}$	DATA	Q
H	L	L	L	L
H	L	L	H	H
H	X	H	X	Q_0
H	H	X	X	Q_0
L	X	X	X	L

H = high level, L = low level, X = irrelevant

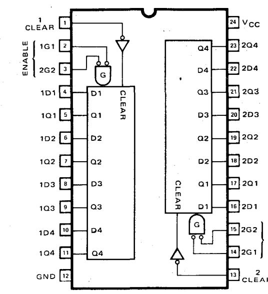
Q_0 = the level of Q before these input conditions were established.

BLOCK DIAGRAM (Each Latch)



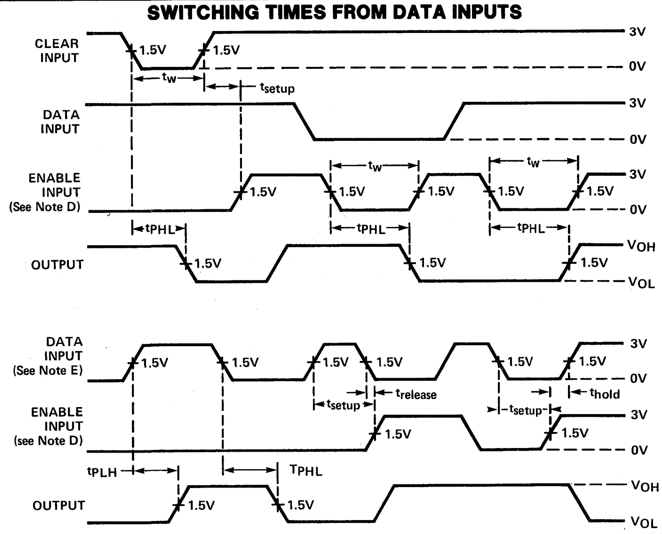
PIN CONFIGURATION

F,N,Q PACKAGE



PARAMETER MEASUREMENT INFORMATION

SWITCHING TIMES FROM DATA INPUTS



NOTES:

A. Input pulses are supplied by generators having the following characteristics: t ≤ 10ns, t_f ≤ 10ns, PRR = 1 MHz, duty cycle ≤ 50%, $Z_{out} \approx 50\ \Omega$.

B. C_L includes probe and jig capacitance.

C. All diodes are 1N3064.

D. The other enable input is low.

E. Clear input is high.

SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

TEST CONDITIONS			54/74 C_L=15pF R_L=400Ω			
PARAMETER	FROM INPUT	TO OUTPUT	MIN	TYP	MAX	UNIT
$t_{w(Enable\ \&\ Clear)}$ Width of enable & clear pulse			18			ns
$t_{Setup\ (Data)}$ Data input setup time						
High level			8			ns
Low level			44			
$t_{Setup\ (Clear)}$ Clear input setup time			8			ns
$t_{Release}$ Shift/load release time					2	ns
t_{Hold} Input hold time			8			ns
Propagation delay time						
t_{PLH} Low-to-high	Enable	Any Q		19	30	ns
t_{PHL} High-to-low				15	22	
t_{PLH} Low-to-high	Data	Q		10	15	
t_{PHL} High-to-low				12	18	
t_{PHL} High-to-low	Clear	Any Q		15	22	

MONOSTABLE MULTIVIBRATOR 54/74121

SPEED/PACKAGE AVAILABILITY

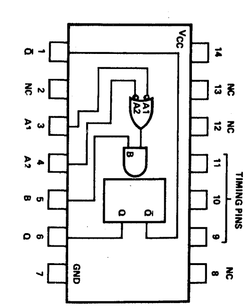
54 F,W 74 A,F

THRESHOLD VOLTAGE V_{CC} = Min

PARAMETER	INPUT	MIN	TYP	MAX	UNIT
V_{T+} Positive Going Threshold	A		1.4	2	V
	B		1.55	2	V
V_{T-} Negative Going Threshold	A	0.8	1.4		V
	B	0.8	1.35		V

PIN CONFIGURATION

A,F,W PACKAGE

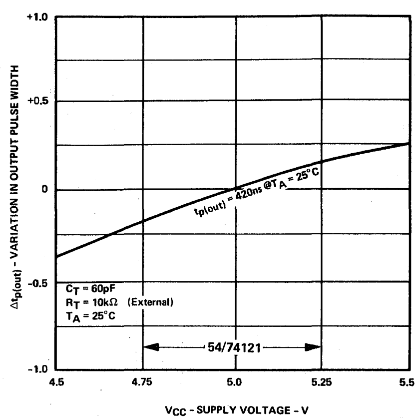


SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

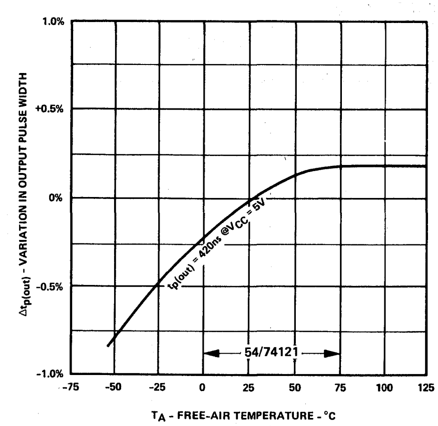
TEST CONDITIONS				54/74 C_L=15pF C_T=80pF			
PARAMETER		FROM INPUT	TO OUTPUT	MIN	TYP	MAX	UNIT
$t_{w(in)}$				50			ns
$t_{w(out)}$				R_T=Open pin 9 to V_{CC}			
				70	110	150	ns
				C_T=0			
				20	30	50	
				C_T=100pF R_T=10kΩ Pin 9 open			
				600	700	800	
				C_T=1μF			
				6	7	8	ns
t_{Hold}	Input hold time			R_T=Open pin 9 to V_{CC}			
					30	50	ns
dv/dt	Input slope	B		1			V/s
		A_1,A_2		1			V/μs
R_{ext}	External timing resistance			(54) 1.4		30	kΩ
				(74) 1.4		40	
C_{ext}	External timing			0		1000	μf
	Duty cycle (%)			R_T=2k			
						67	kΩ
				R_T=Max R_{ext}			
						90	
Propagation delay time							
t_{PLH}	Low-to-high	B	Q	15	35	55	ns
t_{PHL}	High-to-low	B	Q	20	40	65	
t_{PLH}	Low-to-high	A_1,A_2	Q	25	45	70	
t_{PHL}	High-to-low	A_1,A_2	Q	30	50	80	

TYPICAL CHARACTERISTICS

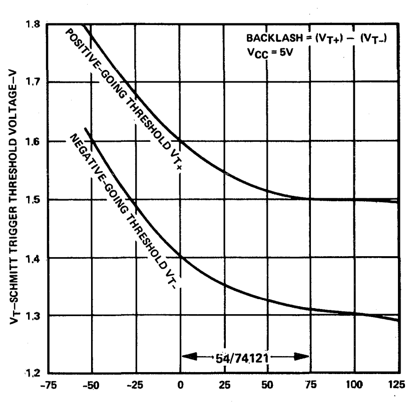
VARIATION IN OUTPUT PULSE WIDTH VERSUS SUPPLY VOLTAGE



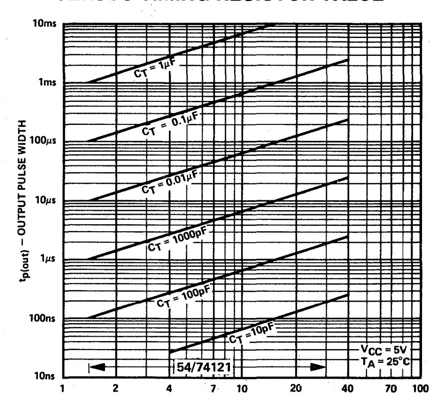
VARIATION IN OUTPUT PULSE WIDTH VERSUS FREE-AIR TEMPERATURE



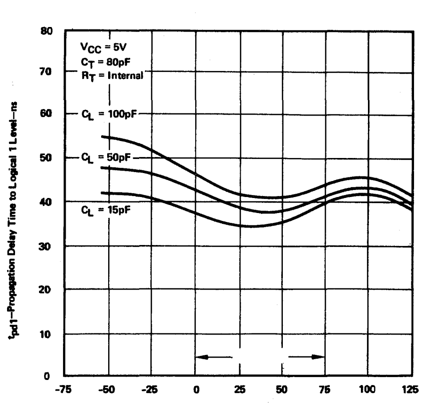
SCHMITT TRIGGER THRESHOLD VOLTAGE VERSUS FREE-AIR TEMPERATURE



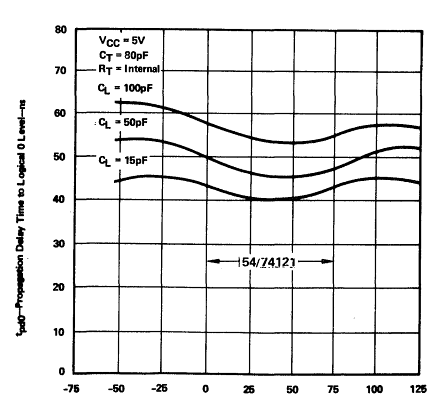
OUTPUT PULSE WIDTH VERSUS TIMING RESISTOR VALUE



PROPAGATION DELAY TIME TO LOGICAL 1 LEVEL (B INPUT TO Q INPUT) VERSUS FREE-AIR TEMPERATURE

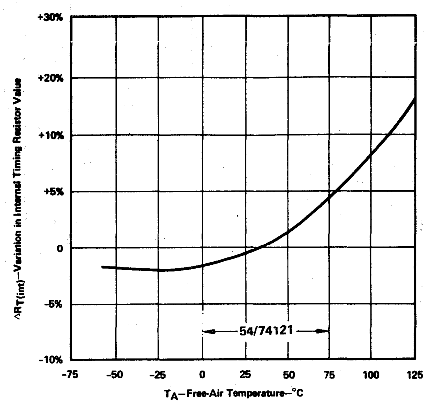


PROPAGATION DELAY TIME TO LOGICAL 0 LEVEL (B INPUT TO Q OUTPUT) VERSUS FREE-AIR TEMPERATURE



TYPICAL CHARACTERISTICS, (Continued)

VARIATION IN INTERNAL TIMING RESISTOR VALUE VERSUS FREE-AIR TEMPERATURE



TRUTH TABLE

t_n INPUT			t_n+1 INPUT			OUTPUT
A1	A2	B	A1	A2	B	
1	1	0	1	1	1	Inhibit
0	x	1	0	x	0	Inhibit
x	0	1	x	0	0	Inhibit
0	x	0	0	x	1	One Shot
x	0	0	x	0	1	One Shot
1	1	1	x	0	1	One Shot
1	1	1	0	x	1	One Shot
x	0	0	x	1	0	Inhibit
0	x	0	1	x	0	Inhibit
x	0	1	1	1	1	Inhibit
0	x	1	1	1	1	Inhibit
1	1	0	x	0	0	Inhibit
1	1	0	0	x	0	Inhibit

1 = $V_{in(1)} \geq 2V$ 0 = $V_{in(0)} \leq 0.8V$

1. A1 and A2 are negative-edge-triggered logic inputs, and will trigger the one shot when either or both go to logical 0 with B at logical 1.
2. B is a positive Schmitt-trigger input for slow edges or level detection, and will trigger the one shot when B goes to logical 1 with either A1 or A2 at logical 0. (See Truth Table)
3. External timing capacitor may be connected between pin (positive) and pin With no external capacitance, an output pulse width of 30ns is obtained typically.
4. To use the internal timing resistor (2kΩ nominal), connect pin to pin
5. To obtain variable pulse width connect external variable resistance between pin and pin . No external current limiting is needed.
6. For accurate repeatable pulse widths connect an external resistor between pin and pin with pin open-circuit.
7. t_n = time before input transition.
8. t_n+1 = time after input transition.
9. x indicates that either a logical 0 or 1, may be present.

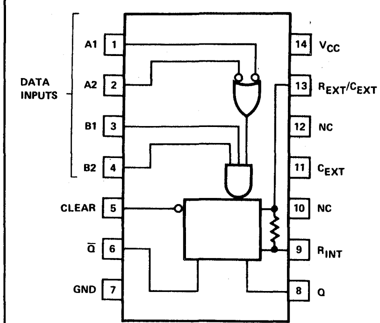
LOGIC

SPEED/PACKAGE AVAILABILITY

74 A,F

PIN CONFIGURATION

A,F PACKAGE



SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

TEST CONDITIONS				74 C_L=15pF R_L=400Ω			
PARAMETER		**FROM INPUT**	**TO OUTPUT**	**MIN**	**TYP**	**MAX**	**UNIT**
$t_{wq(min)}$					45	65	ns
t_{wq}				C_{ext} = 1000pF R_{ext} = 10kΩ			
				3.08	3.42	3.76	ns
$t_{w(in)}$				40			ns
R_{ext}	External timing resistance			(54) 5		25	kΩ
				(74) 5		50	
C_{ext}	External timing capacitance			No restriction			µf
	Wiring cap. at R_{ext}/C_{ext} terminal					50	pF
				C_{ext} = 0 R_{ext} = 5kΩ			
Propagation delay time							
t_{PLH}	Low-to-high	Either A	Q		22	33	ns
t_{PHL}	High-to-low	Either A	$\overline{Q}$		30	40	
t_{PLH}	Low-to-high	Either B	Q		19	28	
t_{PHL}	High-to-low	Either B	$\overline{Q}$		27	36	
t_{PLH}	Low-to-high	Clear	$\overline{Q}$		30	40	
t_{PHL}	High-to-low	Clear	Q		18	27	

Load circuit and typical waveforms are shown at the front of section.

$t_W = 0.32\, R_T C_{ext} \left(1 + \frac{0.7}{R_T}\right)$

TRUTH TABLE

INPUTS				OUTPUTS	
A_1	A_2	B_1	B_2	Q	Q
H	H	X	X	L	H
X	X	L	X	L	H
X	X	X	L	L	H
L	X	H	H	L	H
L	X	↑	H	⊓	⊔
L	X	H	↑	⊓	⊔
X	L	H	H	L	H
X	L	↑	H	⊓	⊔
X	L	H	↑	⊓	⊔
H	↓	H	H	⊓	⊔
↓	↓	H	H	⊓	⊔
	H	H	H	⊓	⊔

NOTES:

A. H = high level (steady state), L = low level (steady state), ↑ = transition from low to high level, ↓ = transition from high to low level, = one high-level pulse, = one low-level pulse, X = irrelevant (any input, including transitions).

B. NC = no internal connection.

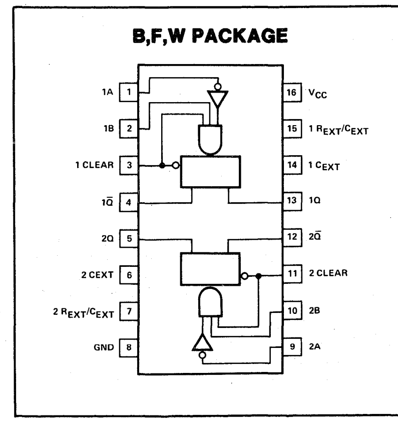
C. To use the internal timing resistor of N74122 (10kΩ nominal), connect R_{int} to V_{CC}.

D. An external timing capacitor may be connected between C_{ext} and R_{ext}/C_{ext} (positive).

SPEED/PACKAGE AVAILABILITY

54 F,W 74 B,F

PIN CONFIGURATION



DESCRIPTION

These monolithic TTL retriggerable monostable multivibrators feature dc triggering from gated low-level-active (A) and high-level-active (B) inputs, and also provide overriding direct clear inputs. Complementary outputs are provided. A full fan-out to 10 normalized Series 54/74 loads is available from each of the outputs at the low logic level, and in the high-level state, a fan-out of 20 is available. The retrigger capability simplifies the generation of output pulses of extremely long duration. By triggering the input before the output pulse is terminated, the output pulse may be extended. The overriding clear capability permits any output pulse to be terminated at a predetermined time independently of the timing components R and C.

Figure A illustrates triggering the one-shot with the high-level-active (B) inputs.

SWITCHING CHARACTERISTICS $V_{CC} = 5V$, $T_A = 25°C$

TEST CONDITIONS				54/74 $C_L = 15pF$ $R_L = 400\Omega$			
PARAMETER		FROM INPUT	TO OUTPUT	MIN	TYP	MAX	UNIT
$t_{w(min)}$							
t_w	Width of pulse			C_{ext} = 1000pF R_{ext} = 10KΩ 54/74123			
				3.08	3.42	3.76	µs
				54/74123A			
				2.76	3.03	3.37	
$t_{w(in)}$				40			ns
R_{ext}	External timing resistance			(54) 5		25	kΩ
				(74) 5		50	
C_{ext}	External timing			No restriction			µf
	Wiring cap. at R_{ext}/C_{ext} terminal					50	pF
Propagation delay time				C_{ext} = 0 R_{ext} = 5kΩ			
t_{PLH}	Low-to-high	Either A	Q		22	33	ns
t_{PHL}	High-to-low	Either A	$\overline{Q}$		30	40	
t_{PLH}	Low-to-high	Either B	Q		19	28	
t_{PHL}	High-to-low	Either B	$\overline{Q}$		27	36	
t_{PLH}	Low-to-high	Clear	$\overline{Q}$		30	40	
t_{PHL}	High-to-low	Clear	Q		18	27	

Load circuit and typical waveforms are shown at the front of section.

54/74123: $t_w = 0.32 R_T C_{ext} (1 + \frac{0.7}{R_T})$

54/74123A: $t_w = 0.25 R_T C_{ext} (1 + \frac{0.7}{R_T})$

TRUTH TABLE

INPUTS		OUTPUTS	
A	B	Q	$\overline{Q}$
H	X	L	H
X	L	L	H
L	↑	⊓	⊔
↓	H	⊓	⊔

NOTES:

A. H = high level (steady-state), ↑ = low level (steady state), ↑ = transition from low to high level, ↓ = transition from high to low level, = one high-level pulse, = one low-level pulse, X = irrelevant (any input, including transitions).

B. NC = no internal connection.

C. To use the internal timing resistor of N74122 (10kΩ nominal), connect R_{int} to V_{CC}.

D. An external timing capacitor may be connected between C_{ext} and R_{ext}/C_{ext} (positive).

TYPICAL CHARACTERISTICS

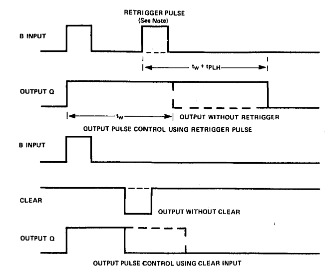


Figure A — typical input/output pulses

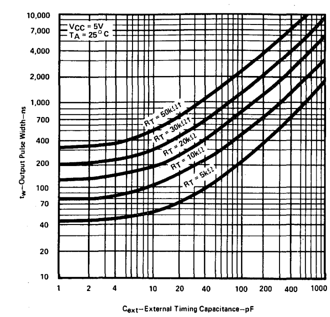


Figure B — output pulse width vs. external timing capacitance

† These values of resistance exceed the maximums recommended for use over the full temperature range of the S54122 and S54123.

NOTE:

When using electrolytic capacitor, insure that minimum rating is 20 volts so that 5% reverse voltage rating is 1.0 volt or greater.

QUAD BUS BUFFER GATE 54/74125

SPEED/PACKAGE AVAILABILITY

54 F,W 74 A,F

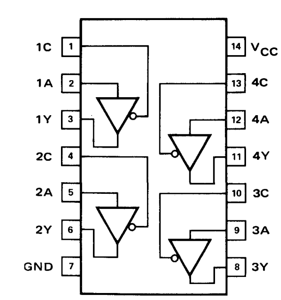
SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

TEST CONDITIONS	54/74 C_L=50pF R_L=400Ω			
PARAMETER	**MIN**	**TYP**	**MAX**	**UNIT**
Propagation delay time				
t_{PLH} Low-to-high		8	13	ns
t_{PHL} High-to-low		12	18	
Output enable time				
t_{ZH} To high level		11	17	ns
t_{ZL} To low level		16	25	
Output disable time	C_L=5pF			
t_{HZ} From high level		5	8	ns
t_{LZ} From low level		7	12	

Load circuit and typical waveforms are shown at the front of section.

PIN CONFIGURATION

A,F,W PACKAGE



QUAD BUS BUFFER GATE — 54/74126

SPEED/PACKAGE AVAILABILITY

54 F,W   74 A,F

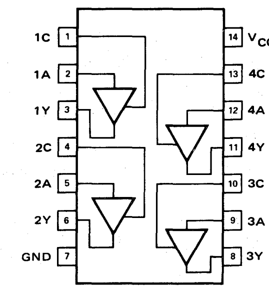
SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

TEST CONDITIONS	54/74 C_L=50pF R_L=400Ω			
PARAMETER	**MIN**	**TYP**	**MAX**	**UNIT**
Propagation delay time				
t_{PLH} Low-to-high		8	13	ns
t_{PHL} High-to-low		12	18	
Output enable time				
t_{ZH} To high level		11	18	ns
t_{ZL} To low level		16	25	
Output disable time	C_L=5pF			
t_{HZ} From high level		10	16	ns
t_{LZ} From low level		12	18	

Load circuit and typical waveforms are shown at the front of section.

PIN CONFIGURATION

A,F,W PACKAGE



QUAD 2-INPUT NOR BUFFER — 54/74128

SPEED/PACKAGE AVAILABILITY

54 F,W   74 A,F

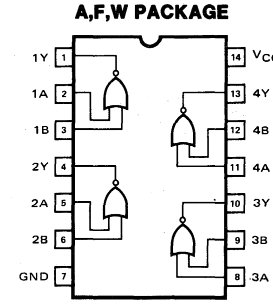
SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

TEST CONDITIONS	54/74 C_L = 50pF R_L = 133Ω			
PARAMETER	**MIN**	**TYP**	**MAX**	**UNIT**
Propagation delay time				
t_{PLH} Low-to-high		6	9	ns
t_{PHL} High-to-low		8	12	
	C_L = 150pF			
t_{PHL} Low-to-high		10	15	ns
t_{PHL} High-to-low		12	18	

Load circuit and typical waveforms are shown at the front of section.

PIN CONFIGURATION

A,F,W PACKAGE



Positive logic: $Y=\overline{A+B}$

SPEED/PACKAGE AVAILABILITY

54	F,W	74	A,F
54LS	F,W	74LS	A,F

DESCRIPTION

Each circuit functions as a NAND gate, but because of the Schmitt action, it has different input threshold levels for positive- and negative-going signals. The hysteresis or backlash, which is the difference between the two threshold levels, is typically 800 millivolts.

These circuits are temperature compensated and can be triggered from the slowest of input ramps and still give clean, jitter-free output signals.

SWITCHING CHARACTERISTICS $V_{CC} = 5V$, $T_A = 25°C$

TEST CONTITIONS	54/74 $C_L = 15pF$ $R_L = 400\Omega$			54/74LS $C_L = 15pF$ $R_L = 2k\Omega$			
PARAMETER	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
Propagation delay time t_{PLH} Low-to-high		15	22		15	22	ns
t_{PHL} High-to-low		15	22		15	22	

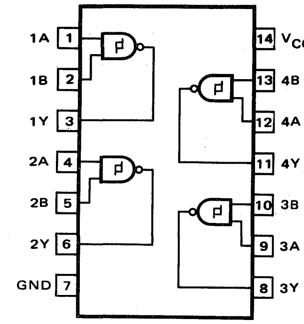
Load circuit and typical waveforms are shown at the front of section.

HYSTERESIS THRESHOLDS

	54/74			54/74LS			
	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
VT+ Positive going threshold	1.5	1.7	2.0	1.5	1.7	1.9	
VT- Negative going threshold	0.6	0.9	1.1	0.6	0.8	1.0	

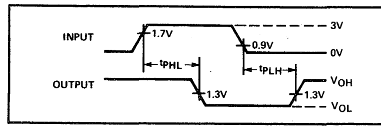
PIN CONFIGURATION

A,F,W PACKAGE



positive logic: $Y=\overline{AB}$

PARAMETER MEASUREMENT INFORMATION



NOTES:

A. The input waveform is supplied by a generator with the following characteristics: $Z_{out} = 50\ \Omega$ and PRR ≤ 1 MHz, $t_r \le 15$ ns, $t_f \le 6$ ns.

SPEED/PACKAGE AVAILABILITY

54S	F,W	74S	B,F

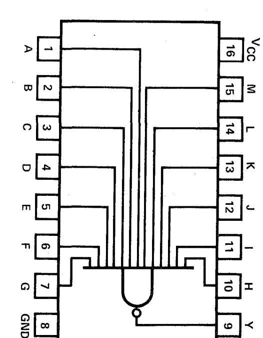
SWITCHING CHARACTERISTICS $V_{CC} = 5V$, $T_A = 25°C$

TEST CONDITIONS	54/74s $C_L=15pF$ $R_L=280\Omega$			
PARAMETER	MIN	TYP	MAX	UNIT
Propagation delay time t_{PLH} Low-to-high	2	4	6	ns
t_{PHL} High-to-low	2	4.5	7	
		$C_L=50pF$		
t_{PLH} Low-to-high		5.5		
t_{PHL} High-to-low		6.5		

Load circuit and typical waveforms are shown at the front of section.

PIN CONFIGURATION

B,F,W PACKAGE



Positive logic: $Y=\overline{ABCDEFGHIJKLM}$

12-INPUT NAND GATE — 54/74134

SPEED/PACKAGE AVAILABILITY

54S F,W   74S B,F

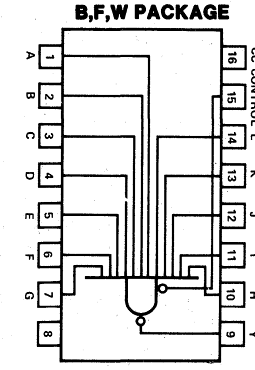
SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

TEST CONDITIONS	54/74S C_L=15pF R_L=280Ω			
PARAMETER	MIN	TYP	MAX	UNIT
Propagation delay time				
t_{PLH} Low-to-high	2	4	6	ns
t_{PHL} High-to-low	2	5	7.5	
		C_L=50pF		
t_{PLH} Low-to-high		5.5		
t_{PHL} High-to-low		7		
Output enable time		C_L=50pF		
t_{ZH} To High level		13	19.5	ns
t_{ZL} To low level		14	21	
Output disable time		C_L=5pF		
t_{HZ} From high level		5.5	8.5	ns
t_{LZ} From low level		9	14	

Load circuit and typical waveforms are shown at the front of section.

PIN CONFIGURATION

B,F,W PACKAGE



TRUTH TABLE

INPUTS												OUTPUT	OUTPUT
A	B	C	D	E	F	G	H	I	J	K	L	CONTROL	Y
H	H	H	H	H	H	H	H	H	H	H	H	L	H
ANY NUMBER OF INPUTS LOW												L	H
X	X	X	X	X	X	X	X	X	X	X	X	H	Z

H = high logic level, L = low logic level, X = irrelevant
Z = high-impedance (output off)

QUAD EXCLUSIVE-OR/NOR GATE — 54/74135

SPEED/PACKAGE AVAILABILITY

54S W,F   74S B,F

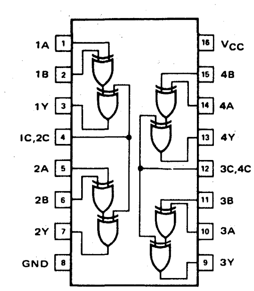
SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

TEST CONDITIONS			54/74S C_L=15pF R_L=280Ω			
PARAMETER	FROM INPUT	TO OUTPUT	MIN	TYP	MAX	UNIT
Propagation delay time						
t_{PLH} Low-to-high	A,B	B,A = L, C = L		8.5	13	ns
t_{PHL} High-to-low				11	15	
t_{PLH} Low-to-high	A,B	B,A = H, C = L		8	12	
t_{PHL} High-to-low				9	13.5	
t_{PLH} Low-to-high	A,B	B,A = L, C = H		10	15	
t_{PHL} High-to-low				6.5	10	
t_{PLH} Low-to-high	A,B	B,A = H, C = H		8.5	12	
t_{PHL} High-to-low				7	11	
t_{PLH} Low-to-high	C	A = B		8	12	
t_{PHL} High-to-low				9.5	14.5	
t_{PLH} Low-to-high	C	A ≠ B		7.5	11.5	
T_{PHL} High-to-low				8	12	

Load circuit and typical waveforms are shown at the front of section.

PIN CONFIGURATION

B,F,W PACKAGE



TRUTH TABLE

INPUTS			OUTPUT
A	B	C	Y
L	L	L	L
L	H	L	H
H	L	L	H
H	H	L	L
L	L	H	H
L	H	H	L
H	L	H	L
H	H	H	H

H = high level, L = low level

SPEED/PACKAGE AVAILABILITY

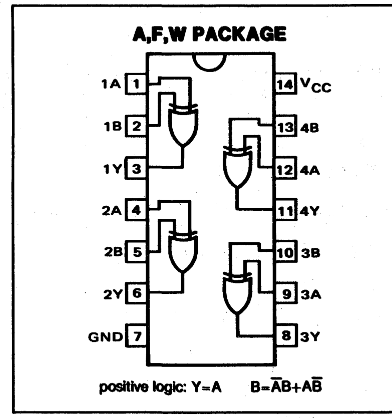
54LS F,W 74LS A,F

FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

H = high level, L = low level

PIN CONFIGURATION



SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

PARAMETER★	FROM (INPUT)	TEST CONDITIONS		LIMITS MIN	TYP	MAX	UNIT
t_{PLH}	A or B	Other input low	C_L = 15pF,		18	30	ns
t_{PHL}			R_L = 2kΩ		18	30	
t_{PLH}	A or B	Other input high			18	30	ns
t_{PHL}					18	30	

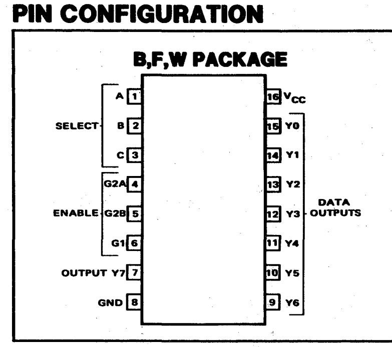
★t_{PLH} = propagation delay time, low-to-high level output
t_{PHL} = propagation delay time, high-to-low-level output
Load circuit and typical waveforms shown in front of book.

3-TO-8 LINE DECODER/DEMULTIPLEXER 54/74138

SPEED/PACKAGE AVAILABILITY

54LS F,W 74LS B,F
54S F,W 74S B,F

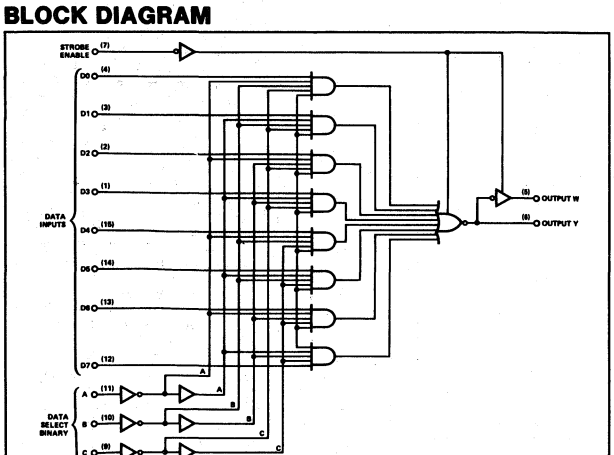
PIN CONFIGURATION



DESCRIPTION

The S54LS138 and N74LS138 decode one-of-eight lines dependent on the conditions at the three binary select inputs and the three enable inputs. Two active-low and one active-high enable inputs reduce the need for external gates or inverters when expanding. A 24-line decoder can be implemented without external inverters and a 32-line decoder requires only one inverter. An enable input can be used as a data input for demultiplexing applications. Typical delay time through the three-level address circuitry is 22 nanoseconds. Typical power dissipation is 32 milliwatts.

BLOCK DIAGRAM



TRUTH TABLE

INPUTS					OUTPUTS							
ENABLE		SELECT										
G1	G2*	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	H	H	H	H	H	L	H	H	H	H
H	L	H	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	H	L	H	H
H	L	H	H	L	H	H	H	H	H	H	L	H
H	L	H	H	H	H	H	H	H	H	H	H	L

*G2 = G2A + G2B
H = high level, L = low level, X = irrelevant

SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

TEST CONDITIONS			54/74LS C_L=15pF R_L=2KΩ			54/74S C_L=15pF R_L=280Ω				
PARAMETER	FROM INPUT	TO OUTPUT	MIN	TYP	MAX	MIN	TYP	MAX	LEVELS OF DELAY	UNIT
Propagation delay time										
t_{PLH} Low-to-high	Binary Select	Any		13	20		4.5	7	2	ns
t_{PHL} High-to-low				27	41		7	10.5		
t_{PLH} Low-to-high				18	27		7.5	12	3	
t_{PHL} High-to-low				26	39		8	12		
t_{PLH} Low-to-high	Enable	Any		12	18		5	8	2	
t_{PHL} High-to-low				21	32		7	11		
t_{PLH} Low-to-high				17	26		7	11	3	
t_{PHL} High-to-low				25	38		7	11		

Load circuit and typical waveforms are shown at the front of section.

DUAL 2-TO-4 LINE DECODER/DEMULTIPLEXER 54/74139

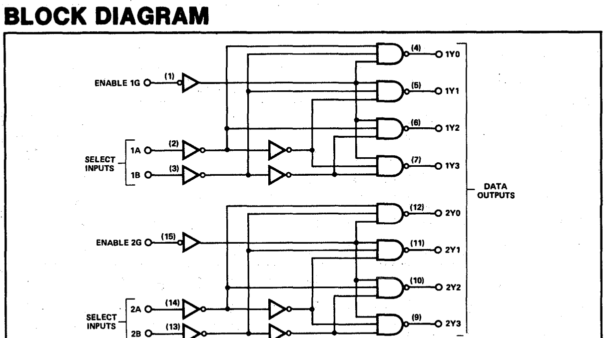
SPEED/PACKAGE AVAILABILITY

54LS F,W 74LS B,F
54S F,W 74S B,F

DESCRIPTION

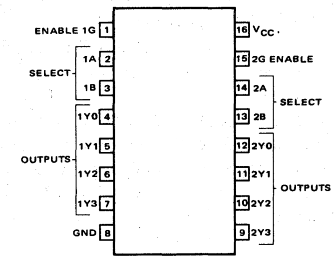
The S54LS139 and N74LS139 comprise two individual two-line-to-four-line decoders in a single package. The active-low enable input can be used as a data line in demultiplexing applications. Typical total delay time is 22 nanoseconds through the three-gate-level address circuitry and power consumption is typically 34 milliwatts total.

BLOCK DIAGRAM



PIN CONFIGURATION

B,F,W PACKAGE



TRUTH TABLE (Each Decoder/Demultiplexer)

INPUTS			OUTPUTS			
ENABLE	SELECT					
G	B	A	Y0	Y1	Y2	Y3
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	L	H	H	L	H	H
L	H	L	H	H	L	H
L	H	H	H	H	H	L

H=high level, L=low level, X=irrelevant

LOGIC

SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

TEST CONDITIONS			54/74LS C_L=15pF R_L=2KΩ			54/74S C_L=15pF R_L=280Ω				
PARAMETER	**FROM INPUT**	**TO OUTPUT**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**LEVELS OF DELAY**	**UNIT**
Propagation delay time										
t_{PLH} Low-to-high	Binary	Any		13	20		5	7.5	2	ns
t_{PHL} High-to-low	Select			22	33		6.5	10		
t_{PLH} Low-to-high				18	29		7	12	3	
t_{PHL} High-to-low				25	38		8	12		
t_{PLH} Low-to-high	Enable	Any		16	24		5	8	2	
t_{PHL} High-to-low				21	32		6.5	10		

Load circuit and typical waveforms shown at the front of section.

BCD-TO-DECIMAL DECODER/DRIVER 54/74145

SPEED/PACKAGE AVAILABILITY

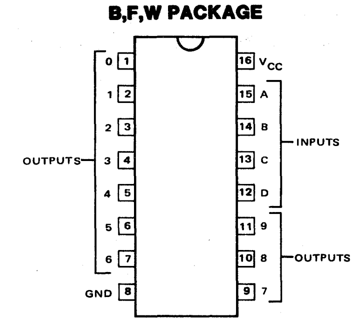
54 F,W 74 B,F
54LS F,W 74LS B,F

DESCRIPTION

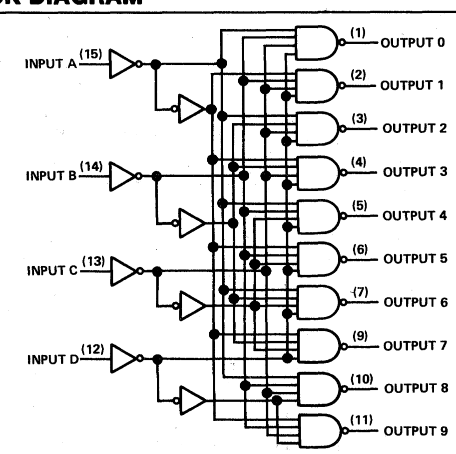
This monilithic BCD-to-decimal decoder/driver consists of eight inverters and ten four-input NAND gates. The inverters are connected in pairs to make BCD input data available for decoding by the NAND gates. Full decoding of valid BCD input logic ensures that all outputs remain off for all invalid binary input conditions. This decoder features high-performance, n-p-n output transistors designed for use as indicator/relay drivers or as open-collector logic-circuit drivers. Each of the high-breakdown output transistors (15 volts) will sink up to 80 milliamperes of current. Each input is one standard load. Inputs and outputs are entirely compatible for use with TTL or DTL logic circuits, and the outputs are compatible for interfacing with most MOS integrated circuits. Power dissipation is typically 35 milliwatts.

PIN CONFIGURATION

B,F,W PACKAGE



BLOCK DIAGRAM



FUNCTION TABLE

NO.	INPUTS				OUTPUTS									
	D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	L	L	L	L	L	H	H	H	H	H	H	H	H	H
1	L	L	L	H	H	L	H	H	H	H	H	H	H	H
2	L	L	H	L	H	H	L	H	H	H	H	H	H	H
3	L	L	H	H	H	H	H	L	H	H	H	H	H	H
4	L	H	L	L	H	H	H	H	L	H	H	H	H	H
5	L	H	L	H	H	H	H	H	H	L	H	H	H	H
6	L	H	H	L	H	H	H	H	H	H	L	H	H	H
7	L	H	H	H	H	H	H	H	H	H	H	L	H	H
8	H	L	L	L	H	H	H	H	H	H	H	H	L	H
9	H	L	L	H	H	H	H	H	H	H	H	H	H	L
	H	L	H	L	H	H	H	H	H	H	H	H	H	H
	H	L	H	H	H	H	H	H	H	H	H	H	H	H
	H	H	L	L	H	H	H	H	H	H	H	H	H	H
	H	H	L	H	H	H	H	H	H	H	H	H	H	H
	H	H	H	L	H	H	H	H	H	H	H	H	H	H
	H	H	H	H	H	H	H	H	H	H	H	H	H	H

H = high level, (off), L = low level (on)

SWITCHING CHARACTERISTICS $V_{CC} = 5V$, $T_A = 25°C$

TEST CONDITIONS	54/74 $C_L = 15pF$ $R_L = 100\Omega$			54/74LS $C_L = 45pF$ $R_L = 665\Omega$			
PARAMETER	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
Propagation delay time							
t_{PLH} Low-to-high			50			50	ns
t_{PHL} High-to-low			50			50	ns

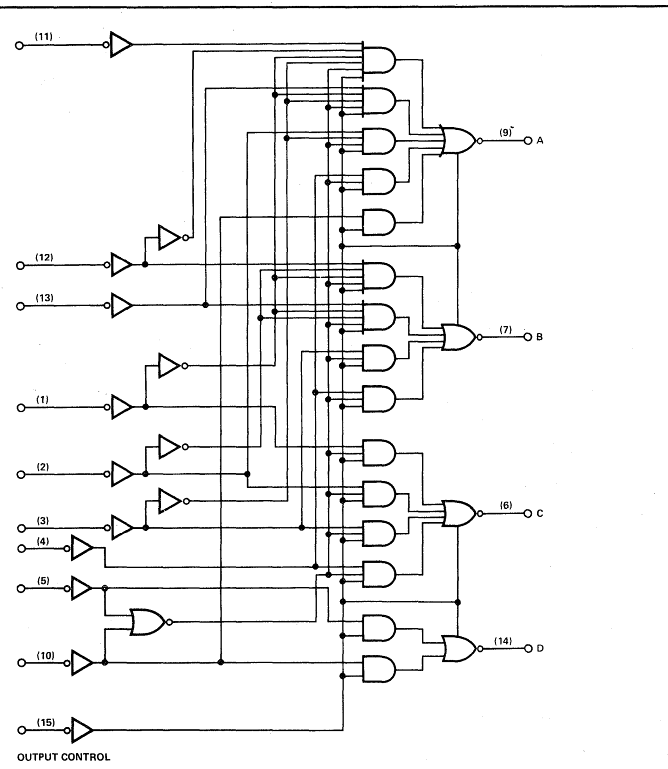
Load circuit and typical waveforms are shown at the front of section.

10-LINE TO 4-LINE PRIORITY ENCODER 54/74147

SPEED/PACKAGE AVAILABILITY

54 F,W 74 B,F

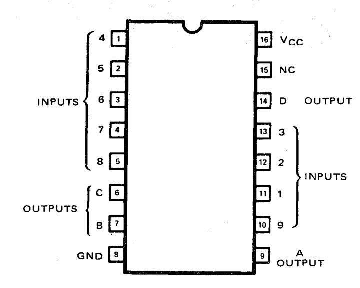
BLOCK DIAGRAM



Pin (16) = V_{CC}, Pin (8) - GND
Pin (15) = No connection

PIN CONFIGURATION

B,F,W PACKAGE



NC - no internal connection

TRUTH TABLE

INPUTS									OUTPUTS			
1	2	3	4	5	6	7	8	9	D	C	B	A
H	H	H	H	H	H	H	H	H	H	H	H	H
X	X	X	X	X	X	X	X	L	L	H	H	L
X	X	X	X	X	X	X	L	H	L	H	H	H
X	X	X	X	X	X	L	H	H	H	L	L	L
X	X	X	X	X	L	H	H	H	H	L	L	H
X	X	X	X	L	H	H	H	H	H	L	H	L
X	X	X	L	H	H	H	H	H	H	L	H	H
X	X	L	H	H	H	H	H	H	H	H	L	L
X	L	H	H	H	H	H	H	H	H	H	L	H
L	H	H	H	H	H	H	H	H	H	H	H	L

H = high logic level, L = low logic level, X = irrelevant

SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

TEST CONDITIONS			54/74 C_L = 15pF R_L=400Ω				
PARAMETER	FROM INPUT	TO OUTPUT	MIN	TYP	MAX	WAVEFORM	UNIT
Propagation delay time							
t_{PLH} Low-to-high	Any	Any		9	14	In phase output	ns
t_{PHL} High-to-low				7	11		
t_{PLH} Low-to-high				13	19	Out of phase output	
t_{PHL} High-to-low				10	15		

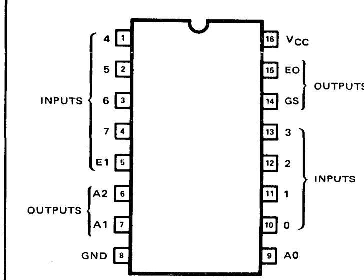
Load circuit and typical waveforms are shown at the front of section.

8-LINE TO 8-LINE PRIORITY ENCODER 54/74148

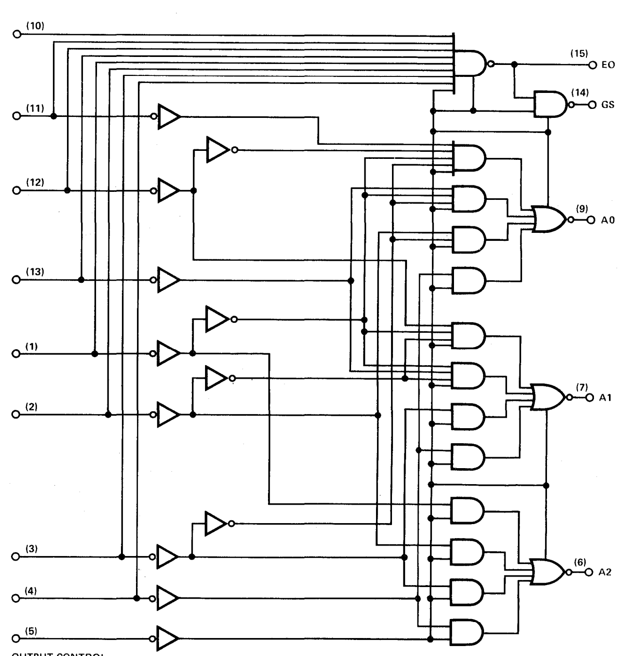
SPEED/PACKAGE AVAILABILITY

54 F,W 74 B,F

PIN CONFIGURATION



BLOCK DIAGRAM



Pin (16)=V_{CC}, pin (8)=GND

TRUTH TABLE

INPUTS									OUTPUTS				
E1	0	1	2	3	4	5	6	7	A2	A1	A0	GS	EO
H	X	X	X	X	X	X	X	X	H	H	H	H	H
L	H	H	H	H	H	H	H	H	H	H	H	H	L
L	X	X	X	X	X	X	X	L	L	L	L	L	H
L	X	X	X	X	X	X	L	H	L	L	H	L	H
L	X	X	X	X	X	L	H	H	L	H	L	L	H
L	X	X	X	X	L	H	H	H	L	H	H	L	H
L	X	X	X	L	H	H	H	H	H	L	L	L	H
L	X	X	L	H	H	H	H	H	H	L	H	L	H
L	X	L	H	H	H	H	H	H	H	H	L	L	H
L	L	H	H	H	H	H	H	H	H	H	H	L	H

SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

TEST CONDITIONS				54/74 C_L=15pF R_L=400Ω			
PARAMETER		FROM INPUT	TO OUTPUT	MIN	TYP	MAX	WAVEFORM	UNIT
Propagation delay time								
t_{PLH}	Low-to-high	0-7	A_0,A_1,A_2		10	15	In phase output	ns
t_{PHL}	High-to-low				9	14		
t_{PLH}	Low-to-high				13	19	Out of phase output	
t_{PHL}	High-to-low				10	15		
t_{PLH}	Low-to-high	0-7	E_0		6	10	Out of phase output	
t_{PHL}	High-to-low				9	14		
t_{PLH}	Low-to-high	0-7	GS		14	21	In phase output	
t_{PHL}	High-to-low				12	18		
t_{PLH}	Low-to-high	E_1	A_0,A_1,A_2		10	15	In phase output	
t_{PHL}	High-to-low				10	15		
t_{PLH}	Low-to-high	E_1	GS		8	12	In phase output	
t_{PHL}	High-to-low				10	15		
t_{PLH}	Low-to-high	E_1	E_0		8	13	In phase output	
t_{PHL}	High-to-low				13	19		

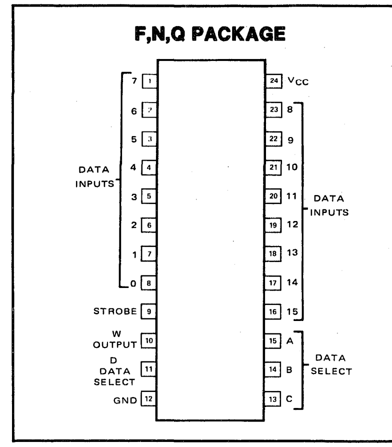
Load circuit and typical waveforms are shown at the front of section.

LOGIC

SPEED/PACKAGE AVAILABILITY

54 Q,F 74 N,F

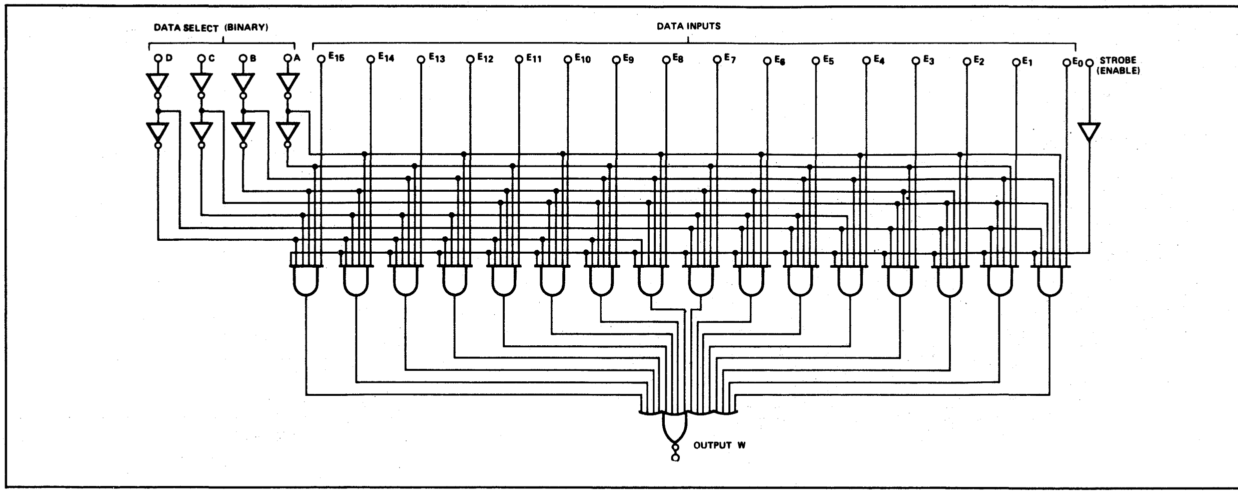
PIN CONFIGURATION



TRUTH TABLE

INPUTS																					OUTPUT
D	C	B	A	STROBE	E_0	E_1	E_2	E_3	E_4	E_5	E_6	E_7	E_8	E_9	E_{10}	E_{11}	E_{12}	E_{13}	E_{14}	E_{15}	W
X	X	X	X	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1
0	0	0	0	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1
0	0	0	0	0	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0
0	0	0	1	0	X	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1
0	0	0	1	0	X	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0
0	0	1	0	0	X	X	0	X	X	X	X	X	X	X	X	X	X	X	X	X	1
0	0	1	0	0	X	X	1	X	X	X	X	X	X	X	X	X	X	X	X	X	0
0	0	1	1	0	X	X	X	0	X	X	X	X	X	X	X	X	X	X	X	X	1
0	0	1	1	0	X	X	X	1	X	X	X	X	X	X	X	X	X	X	X	X	0
0	1	0	0	0	X	X	X	X	0	X	X	X	X	X	X	X	X	X	X	X	1
0	1	0	0	0	X	X	X	X	1	X	X	X	X	X	X	X	X	X	X	X	0
0	1	0	1	0	X	X	X	X	X	0	X	X	X	X	X	X	X	X	X	X	1
0	1	0	1	0	X	X	X	X	X	1	X	X	X	X	X	X	X	X	X	X	0
0	1	1	0	0	X	X	X	X	X	X	0	X	X	X	X	X	X	X	X	X	1
0	1	1	0	0	X	X	X	X	X	X	1	X	X	X	X	X	X	X	X	X	0
0	1	1	1	0	X	X	X	X	X	X	X	0	X	X	X	X	X	X	X	X	1
0	1	1	1	0	X	X	X	X	X	X	X	1	X	X	X	X	X	X	X	X	0
1	0	0	0	0	X	X	X	X	X	X	X	X	0	X	X	X	X	X	X	X	1
1	0	0	0	0	X	X	X	X	X	X	X	X	1	X	X	X	X	X	X	X	0
1	0	0	1	0	X	X	X	X	X	X	X	X	X	0	X	X	X	X	X	X	1
1	0	0	1	0	X	X	X	X	X	X	X	X	X	1	X	X	X	X	X	X	0
1	0	1	0	0	X	X	X	X	X	X	X	X	X	X	0	X	X	X	X	X	1
1	0	1	0	0	X	X	X	X	X	X	X	X	X	X	1	X	X	X	X	X	0
1	0	1	1	0	X	X	X	X	X	X	X	X	X	X	X	0	X	X	X	X	1
1	0	1	1	0	X	X	X	X	X	X	X	X	X	X	X	1	X	X	X	X	0
1	1	0	0	0	X	X	X	X	X	X	X	X	X	X	X	X	0	X	X	X	1
1	1	0	0	0	X	X	X	X	X	X	X	X	X	X	X	X	1	X	X	X	0
1	1	0	1	0	X	X	X	X	X	X	X	X	X	X	X	X	X	0	X	X	1
1	1	0	1	0	X	X	X	X	X	X	X	X	X	X	X	X	X	1	X	X	0
1	1	1	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0	X	1
1	1	1	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1	X	0
1	1	1	1	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0	1
1	1	1	1	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1	0

LOGIC DIAGRAM



SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

TEST CONDITIONS			54/74 C_L=15pF R_L=400Ω			
PARAMETER	FROM INPUT	TO OUTPUT	MIN	TYP	MAX	UNIT
Propagation delay time						
t_{PLH} Low-to-high	A,B,C (4 levels)	Y		35	52	ns
t_{PHL} High-to-low				20	30	
t_{PLH} Low-to-high	A,B,C,D (3 levels)	W		23	35	
t_{PHL} High-to-low				22	33	
t_{PLH} Low-to-high	Strobe	Y		35	52	
t_{PHL} High-to-low				19	30	
t_{PLH} Low-to-high	Strobe	W		15.5	24	
t_{PHL} High-to-low				21	30	
t_{PLH} Low-to-high	D_0-D_7	Y		19	29	
t_{PHL} High-to-low				16	24	
t_{PLH} Low-to-high	E_0-E_{15}	W		13	20	
t_{PHL} High-to-low				8.5	14	

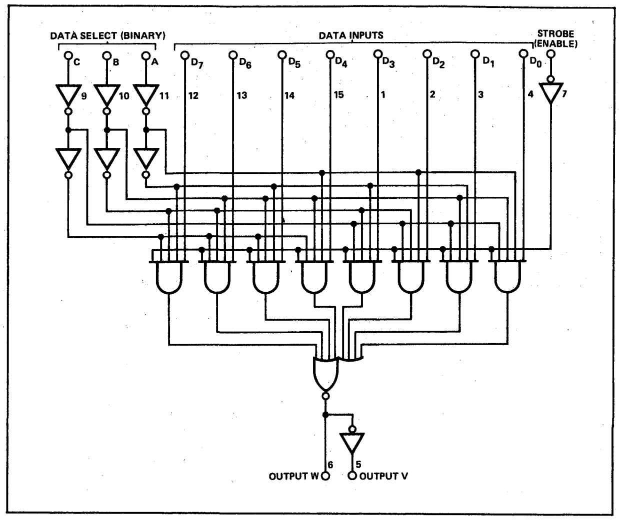
Load circuit and typical waveforms are shown at the front of section.

LOGIC

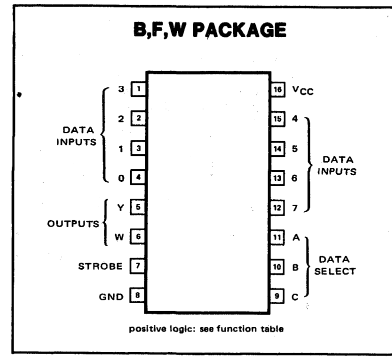
SPEED/PACKAGE AVAILABILITY

54	F,W	74	B,F
54LS	F,W	74LS	B,F
54S	F,W	74S	B,F

BLOCK DIAGRAM



PIN CONFIGURATION



TRUTH TABLE

INPUTS				OUTPUTS	
SELECT			STROBE		
C	B	A	S	Y	W
X	X	X	H	L	H
L	L	L	L	D0	$\overline{D0}$
L	L	H	L	D1	$\overline{D1}$
L	H	L	L	D2	$\overline{D2}$
L	H	H	L	D3	$\overline{D3}$
H	L	L	L	D4	$\overline{D4}$
H	L	H	L	D5	$\overline{D5}$
H	H	L	L	D6	$\overline{D6}$
H	H	H	L	D7	$\overline{D7}$

H = high level, L = low level, X = irrelevant
D0, D1 . . . D7 = the level of the D respective input

SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

TEST CONDITIONS				54/74 C_L=15pF R_L=400Ω			54/74LS C_L=15pF R_L=2kΩ			54/74S C_L=15pF R_L=280Ω			
PARAMETER		FROM INPUT	TO OUTPUT	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
Propagation delay time													
t_{PLH}	Low-to-high	A,B,C (4 levels)	Y		35	52		27	43		12	18	ns
t_{PHL}	High-to-low				20	30		31	50		12	18	
t_{PLH}	Low-to-high	A,B,C,D (3 levels)	W		23	35							
t_{PHL}	High-to-low				22	33							
t_{PLH}	Low-to-high	A,B,C	W					24	39		10	15	
		(3 levels)						20	32		9	13.5	
t_{PHL}	High-to-low												
t_{PLH}	Low-to-high	Strobe	Y		35	52		23	37		11	16.5	
t_{PHL}	High-to-low				19	30		25	42		12	18	
t_{PLH}	Low-to-high	Strobe	W		15.5	24		19	31		9	13	
t_{PHL}	High-to-low				21	30		16	26		8.5	12	
t_{PLH}	Low-to-high	D_0—D_7	Y		19	29							
t_{PHL}	High-to-low				16	24							
t_{PLH}	Low-to-high	E_0—E_{15}	W		13	20							
t_{PHL}	High-to-low				8.5	14							
t_{PLH}	Low-to-high	Any D	Y					16	26		8	12	
t_{PHL}	High-to-low							20	32		8	12	
t_{PLH}	Low-to-high	Any D	W					13	21		4.5	7	
t_{PHL}	High-to-low							9	15		4.5	7	

Load circuit and typical waveforms are shown at the front of section.

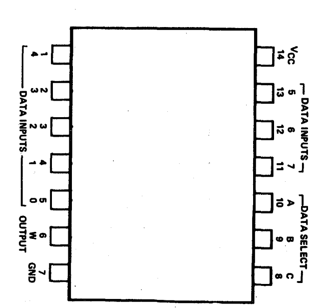
8-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER 54/74152

SPEED/PACKAGE AVAILABILITY

54 F,W 74 A,F

PIN CONFIGURATION

W PACKAGE

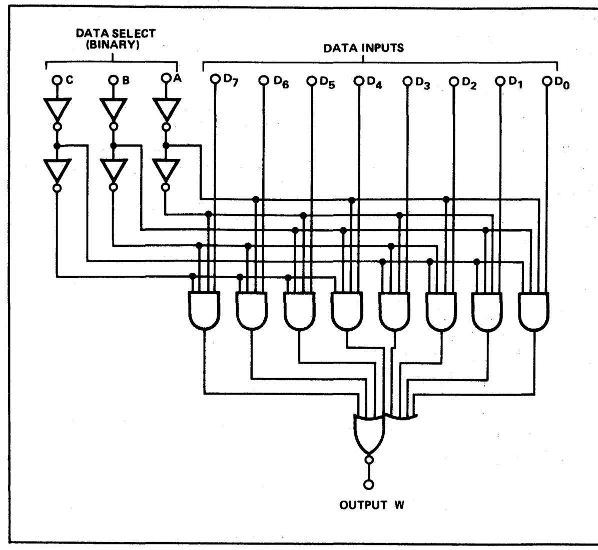


TRUTH TABLE

INPUTS											OUTPUTS
C	B	A	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	W
X	X	X	X	X	X	X	X	X	X	X	1
0	0	0	0	X	X	X	X	X	X	X	1
0	0	0	1	X	X	X	X	X	X	X	0
0	0	1	X	0	X	X	X	X	X	X	1
0	0	1	X	1	X	X	X	X	X	X	0
0	1	0	X	X	0	X	X	X	X	X	1
0	1	0	X	X	1	X	X	X	X	X	0
0	1	1	X	X	X	0	X	X	X	X	1
0	1	1	X	X	X	1	X	X	X	X	0
1	0	0	X	X	X	X	0	X	X	X	1
1	0	0	X	X	X	X	1	X	X	X	0
1	0	1	X	X	X	X	X	0	X	X	1
1	0	1	X	X	X	X	X	1	X	X	0
1	1	0	X	X	X	X	X	X	0	X	1
1	1	0	X	X	X	X	X	X	1	X	0
1	1	1	X	X	X	X	X	X	X	0	1
1	1	1	X	X	X	X	X	X	X	1	0

When used to indicate an input, X = Irrelevant.

LOGIC DIAGRAM



SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

TEST CONDITIONS			54 C_L = 15pF R_L = 400 Ω			
PARAMETER	FROM INPUT	TO OUTPUT	MIN	TYP	MAX	UNIT
Propagation delay time t_{PLH} Low-to-high	A,B,C,D (3 levels)	W		23	35	ns
t_{PHL} High-to-low				22	33	ns
t_{PLH} Low-to-high	D_0-D_7	W		13	20	ns
T_{PHL} High-to-low				8.5	14	ns

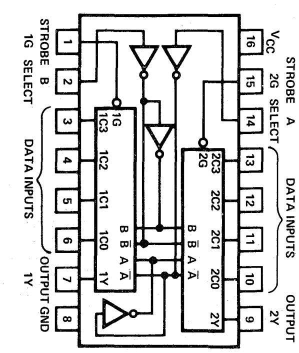
Load circuit and typical waveforms are shown at the front of section.

SPEED/PACKAGE AVAILABILITY

54	F,W	74	B,F
54LS	F,W	74LS	B,F
54S	F,W	74S	B,F

PIN CONFIGURATION

B,F,W PACKAGE

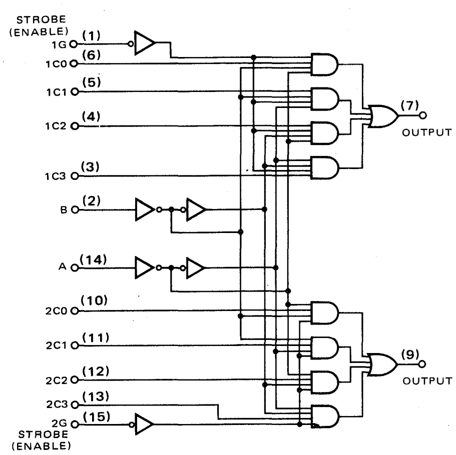


TRUTH TABLE

SELECT INPUTS		DATA INPUTS				STROBE	OUTPUT
B	A	C0	C1	C2	C3	G	Y
X	X	X	X	X	X	H	L
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

Select inputs A and B are common to both sections.
H = high level, L = low level, X = irrelevant

BLOCK DIAGRAM



SWITCHING CHARACTERISTICS $V_{CC} = 5V$, $T_A = 25°C$

TEST CONDITIONS			54/74 $C_L = 30pF$ $R_L = 400\Omega$			54/74LS $C_L = 15pF$ $R_L = 2K\Omega$			54/74S $C_L = 15pF$ $R_L = 280\Omega$			
PARAMETER	FROM INPUT	TO OUTPUT	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
Propagation delay time												
t_{PLH} Low-to-high	Data	Y		12	18		10	15		6	9	ns
t_{PHL} High-to-low				15	23		17	26		6	9	
t_{PLH} Low-to-high	Address	Y		22	34							
t_{PHL} High-to-low				22	34							
t_{PLH} Low-to-high	Strobe	Y		19	30		16	24		10	15	
t_{PHL} High-to-low				15	23		21	32		9	13.5	
t_{PLH} Low-to-high	Select	Y					19	29		11.5	18	
t_{PHL} High-to-low							25	38		12	18	

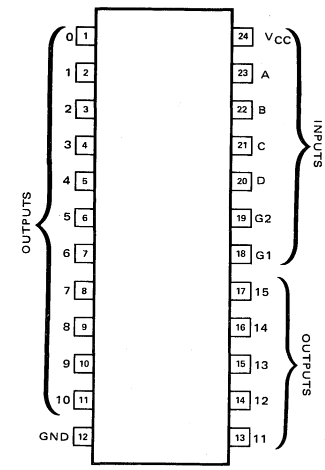
Load circuit and typical waveforms are shown at the front of section.

SPEED/PACKAGE AVAILABILITY

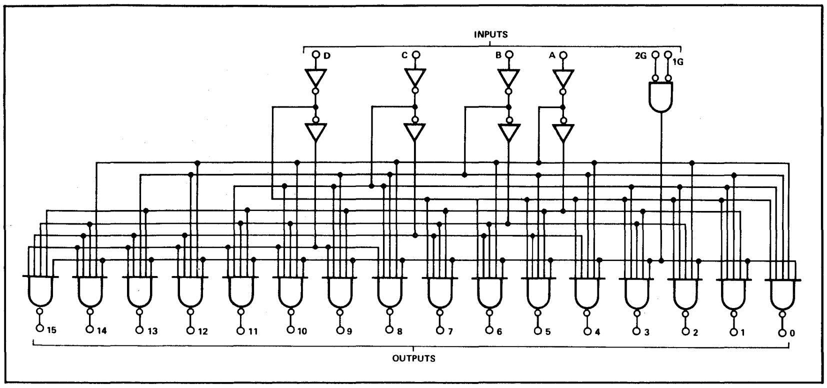
54 Q,F 74 N,F

PIN CONFIGURATION

F,N,Q PACKAGE



LOGIC DIAGRAM



TRUTH TABLE

INPUTS						OUTPUTS															
G1	G2	D	B	B	A	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	L	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H
L	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H
L	L	H	L	L	L	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H
L	L	H	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H
L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
L	L	H	H	L	L	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H
L	L	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L
L	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	L	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H

H = High, L = Low, X= Irrelevant

SWITCHING CHARACTERISTICS $V_{CC} = 5V$, $T_A = 25°C$

TEST CONDITIONS			54/74 $C_L = 15pF$ $R_L = 400$			
PARAMETER	FROM INPUT	TO OUTPUT	MIN	TYP	MAX	UNIT
Propagation delay time						
t_{PLH} Low-to-high	A,B,C,D (3 levels)			24	36	ns
t_{PHL} High-to-low				22	33	
t_{PLH} Low-to-high	Either			20	30	
t_{PHL} High-to-low	Strobe			18	27	

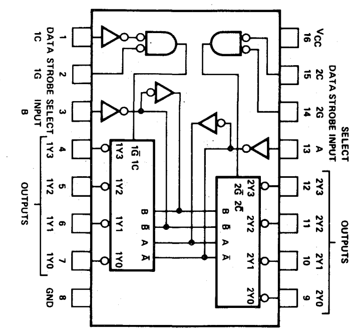
Load circuit and typical waveforms are shown at the front of section.

SPEED/PACKAGE AVAILABILITY

54 F,W 74 B,F

PIN CONFIGURATION

B,F,W PACKAGE



TRUTH TABLE

2-LINE TO 4-LINE DECODER

INPUTS				OUTPUTS			
SELECT		STROBE	DATA				
B	A	1G	1C	1Y0	1Y1	1Y2	1Y3
X	X	H	X	H	H	H	H
L	L	L	H	L	H	H	H
L	H	L	H	H	L	H	H
H	L	L	H	H	H	L	H
H	H	L	H	H	H	H	L
X	X	X	L	H	H	H	H

1-LINE TO 4-LINE DEMULTIPLEXER

INPUTS				OUTPUTS			
SELECT		STROBE	DATA				
B	A	2G	2C	2Y0	2Y1	2Y2	2Y3
X	X	H	X	H	H	H	H
L	L	L	L	L	H	H	H
L	H	L	L	H	L	H	H
H	L	L	L	H	H	L	H
H	H	L	L	H	H	H	L
X	X	X	H	H	H	H	H

†C = inputs 1C and 2C connected together
‡G = inputs 1G and 2G connected together

3-LINE TO 8-LINE DECODER TO 1-LINE TO 8-LINE DEMULTIPLEXER

INPUTS				OUTPUTS							
SELECT			STROBE OR DATA	(0)	(1)	(2)	(3)	(4)	(5)	(6)	(7)
C†	B	A	G‡	2Y0	2Y1	2Y2	2Y3	1Y0	1Y1	1Y2	1Y3
X	X	X	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	H
L	H	L	L	H	H	L	H	H	H	H	H
L	H	H	L	H	H	H	L	H	H	H	H
H	L	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	L	H	H
H	H	L	L	H	H	H	H	H	H	L	H
H	H	H	L	H	H	H	H	H	H	H	L

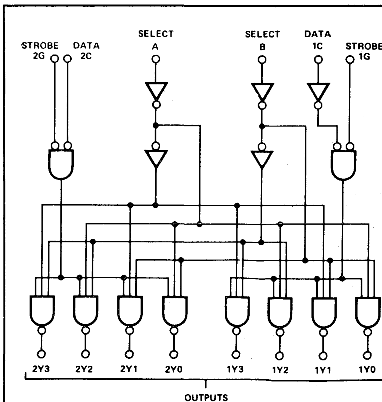
†C=inputs 1C and 2C connected together
‡G=inputs 1G and 2G connected together

SWITCHING CHARACTERISTICS $V_{CC} = 5V$, $T_A = 25°C$

TEST CONDITIONS			54/74 $C_L=15pF$ $R_L=400\Omega$				
PARAMETER	FROM INPUT	TO OUTPUT	MIN	TYP	MAX	LEVELS OF LOGIC	UNIT
Propagation delay time							
t_{PLH} Low-to-high	A,B,2C, 1G,2G	Y		13	20	2	ns
t_{PHL} High-to-low				18	27		
t_{PLH} Low-to-high	A,B	Y		21	32	3	
t_{PHL} High-to-low				21	32		
t_{PLH} Low-to-high	1C	Y		16	24	3	
t_{PHL} High-to-low				20	30		

Load circuit and typical waveforms are shown at the front of section.

LOGIC DIAGRAM



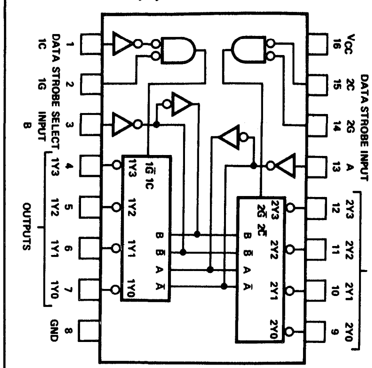
LOGIC

SPEED/PACKAGE AVAILABILITY

54 F,W 74 B,F

PIN CONFIGURATION

B,F,W PACKAGE



TRUTH TABLES

2-LINE TO 4-LINE DECODER

INPUTS				OUTPUTS			
SELECT		STROBE	DATA				
B	A	1G	1C	1Y0	1Y1	1Y2	1Y3
X	X	H	X	H	H	H	H
L	L	L	H	L	H	H	H
L	H	L	H	H	L	H	H
H	L	L	H	H	H	L	H
H	H	L	H	H	H	H	L
X	X	X	L	H	H	H	H

1-LINE TO 4-LINE DEMULTIPLEXER

INPUTS				OUTPUTS			
SELECT		STROBE	DATA				
B	A	2G	2C	2Y0	2Y1	2Y2	2Y3
X	X	H	X	H	H	H	H
L	L	L	L	L	H	H	H
L	H	L	L	H	L	H	H
H	L	L	L	H	H	L	H
H	H	L	L	H	H	H	L
X	X	X	H	H	H	H	H

3-LINE TO 8-LINE DECODER TO 1-LINE TO 8-LINE DEMULTIPLEXER

INPUTS				OUTPUTS							
SELECT			STROBE OR DATA	(0)	(1)	(2)	(3)	(4)	(5)	(6)	(7)
C†	B	A	G‡	2Y0	2Y1	2Y2	2Y3	1Y0	1Y1	1Y2	1Y3
X	X	X	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	H
L	H	L	L	H	H	L	H	H	H	H	H
L	H	H	L	H	H	H	L	H	H	H	H
H	L	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	L	H	H
H	H	L	L	H	H	H	H	H	H	L	H
H	H	H	L	H	H	H	H	H	H	H	L

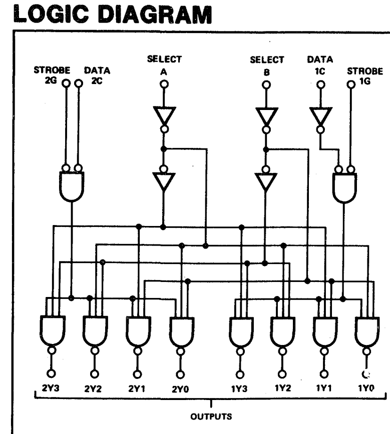
†C = inputs 1C and 2C connected together
‡G = inputs 1G and 2G connected together

SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

TEST CONDITIONS			54/74 C_L=15pF R_L=400Ω				
PARAMETER	FROM INPUT	TO OUTPUT	MIN	TYP	MAX	LEVELS OF LOGIC	UNIT
Propagation delay time							
t_{PLH} Low-to-high	A,B,2C, 1G,2G	Y		15	23	2	ns
t_{PHL} High-to-low				20	30		
t_{PLH} Low-to-high	A,B	Y		23	34	3	
t_{PHL} High-to-low				23	34		
t_{PLH} Low-to-high	1C	Y		18	27	3	
t_{PHL} High-to-low				22	33		

Load circuit and typical waveforms are shown at the front of section.

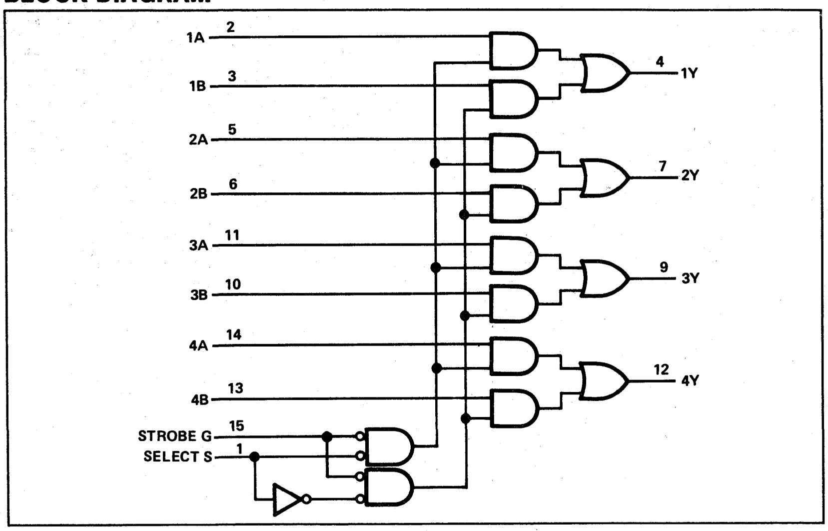
LOGIC DIAGRAM



SPEED/PACKAGE AVAILABILITY

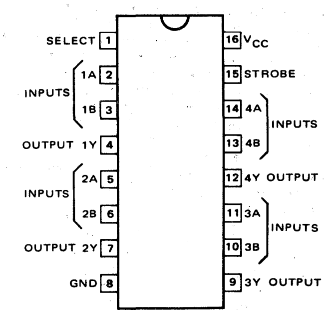
54	F,W	74	B,F
54LS	F,W	74LS	B,F
54S	F,W	74S	B,F

BLOCK DIAGRAM



PIN CONFIGURATION

B,F,W PACKAGE



positive logic: low level at S selects A inputs
high level at S selects B inputs

TRUTH TABLE

INPUTS				OUTPUT Y
STROBE	SELECT	A	B	
H	X	X	X	L
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

H = high level, L = low level, X = irrelevant

SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

TEST CONDITIONS			54/74 C_L=15pF R_L=400Ω			54/74LS C_L=15pF R_L=2kΩ			54/74S C_L=15pF R_L=280Ω			
PARAMETER	FROM INPUT	TO OUTPUT	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
Propagation delay time												
t_{PLH} Low-to-high	Data	Any		9	14		9	14		5	7.5	ns
t_{PHL} High-to-low				9	14		9	14		4.5	6.5	
t_{PLH} Low-to-high	Enable	Any		13	20							
t_{PHL} High-to-low				14	21							
t_{PLH} Low-to-high	Select	Any		15	23		15	23		9.5	15	
t_{PHL} High-to-low				18	27		8	27		9.5	15	
t_{PLH} Low-to-high	Strobe	Any					13	20		8.5	12.5	
t_{PHL} High-to-low							14	21		7.5	12	

Load circuit and typical waveforms are shown at the front of section.

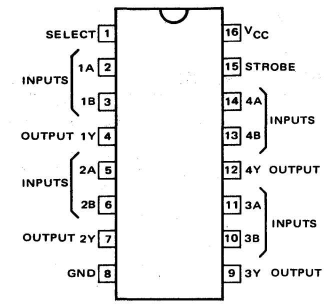
LOGIC

SPEED/PACKAGE AVAILABILITY

54	F,W	74	B,F
54LS	F,W	74LS	B,F
54S	F,W	74S	B,F

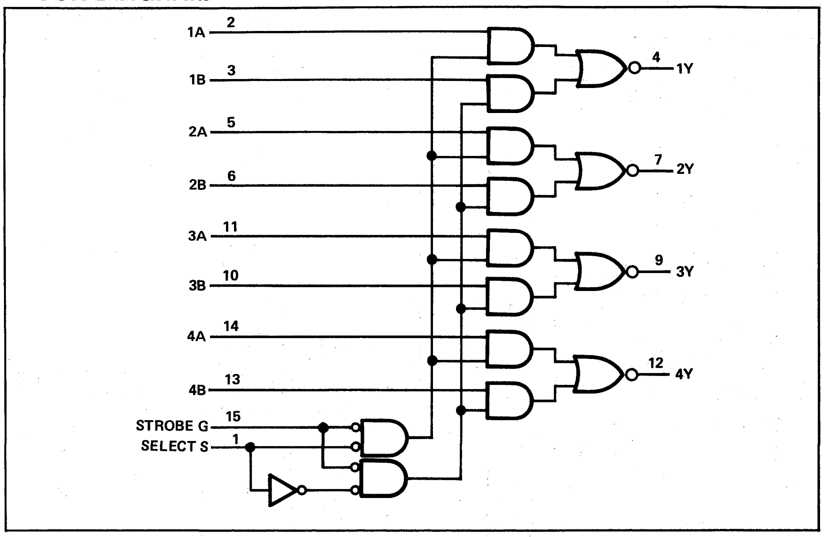
PIN CONFIGURATION

B,F,W PACKAGE



positive logic: low level at S selects A inputs
high level at S selects B inputs

BLOCK DIAGRAM



TRUTH TABLE

INPUTS				OUTPUT Y
STROBE	SELECT	A	B	
H	X	X	X	H
L	L	L	X	H
L	L	H	X	L
L	H	X	L	H
L	H	X	H	L

H = high level, L = low level, X = irrelevant

SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

TEST CONDITIONS				54/74 C_L=15pF R_L=400Ω			54/74LS C_L=15pF R_L=2kΩ			54/74S C_L=15pF R_L=280Ω			
PARAMETER		FROM INPUT	TO OUTPUT	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
Propagation delay time													
t_{PLH}	Low-to-high	Data	Any		9	14		7	12		4	6	ns
t_{PHL}	High-to-low				9	14		7	12		4	6	
t_{PLH}	Low-to-high	Enable	Any		13	20							
t_{PHL}	High-to-low				14	21							
t_{PLH}	Low-to-high	Select	Any		15	23		13	20		8	12	
t_{PHL}	High-to-low				18	27		16	24		8	12	
t_{PLH}	Low-to-high	Strobe	Any					11	17		6.5	11.5	
t_{PHL}	High-to-low							12	18		7	12	

Load circuit and typical waveforms are shown at the front of section.

SPEED/PACKAGE AVAILABILITY

54 F,W   74 B,F
54LS F,W   74LS B,F

DESCRIPTION

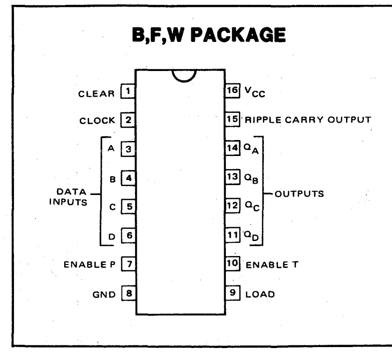
This synchronous presettable decade counter features an internal carry look-ahead for applications in high-speed counting designs. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enable inputs and internal gating. This mode of operation eliminates the output counting spikes which are normally associated with asynchronous (ripple clock) counters. A buffered clock input triggers the four flip-flops on the rising (positive-going) edge of the clock input waveform.

This counter is fully programmable; that is, the outputs may be preset to either level. As presetting is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the setup data after the next clock pulse regardless of the levels of the enable inputs. The clear function for the 54/74LS160 is asynchronous and a low level at the clear input sets all four of the flip-flop outputs low regardless of the levels of clock, load or enable inputs.

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two count-enable inputs and a ripple carry output. Both count-enable inputs (P and T) must be high to count, and input T is fed forward to enable the ripple carry output. The ripple carry output thus enabled will produce a high-level output pulse with a duration approximately equal to the high-level portion of the Q_A output. This high-level overflow ripple carry pulse can be used to enable successive cascaded stages. Transitions at the enable P or T inputs are allowed regardless of the level of the clock input.

The 54/74LS160 features a fully independent clock circuit. Changes made to control inputs (enable P or T, load or clear) that will modify the operating mode have no effect until clocking occurs. The function of the counter (whether enabled, disabled, loading or counting) will be dictated solely by the conditions meeting the stable setup and hold times.

PIN CONFIGURATION

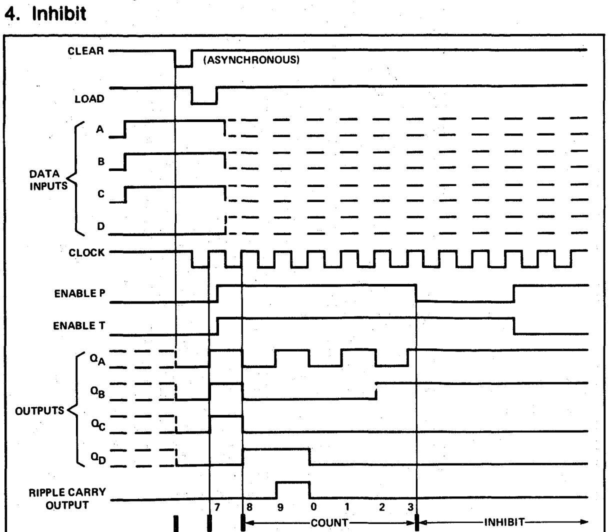


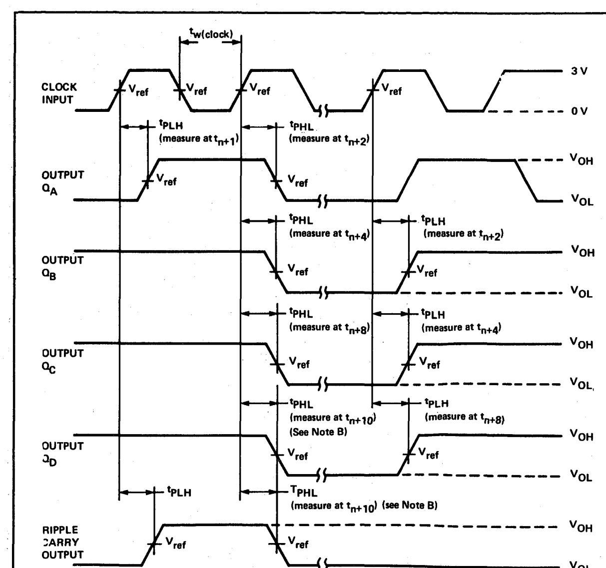
PARAMETER MEASUREMENT INFORMATION

TYPICAL CLEAR, PRESET, COUNT AND INHIBIT SEQUENCES

Illustrated below is the following sequence:

1. Clear outputs to zero
2. Preset to BCD seven
3. Count to eight, nine, zero, one, two, and three
4. Inhibit





VOLTAGE WAVEFORMS

NOTES:

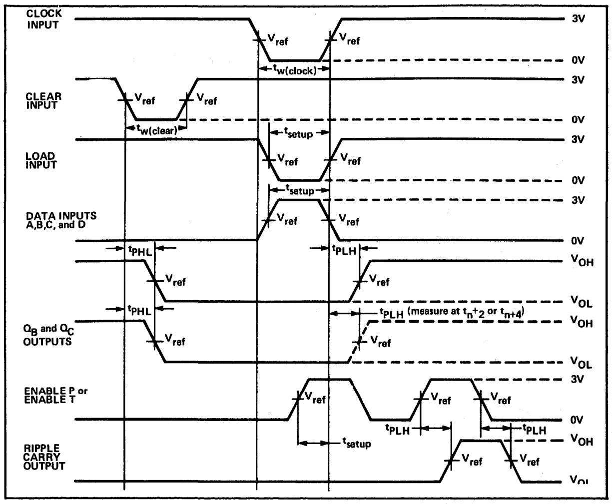
A. The input pulses are supplied by a generator having the following characteristics: PRR ≤ 1MHz, duty cycle ≤ 50%, $Z_{out} \approx 50\Omega$ $t_r \leq 15ns$, $t_f \leq 6ns$.

B. Outputs Q_D and carry are tested at t_n+10, where t_n is the bit time when all outputs are low.

C. $V_{ref} = 1.3V$.

Load circuit is shown at front of section (totem pole outputs).

FIGURE 1—SWITCHING TIMES



VOLTAGE WAVEFORMS

NOTES:

A. The input pulses are supplied by generators having the following characteristics. PRR ≤ 1MHz, duty cycle ≤ 50%, $Z_{out} \approx 50\Omega$, $t_r \leq 15ns$, $t_f \leq 6ns$.

B. Enable P and enable T setup times are measured at t_{N+0}

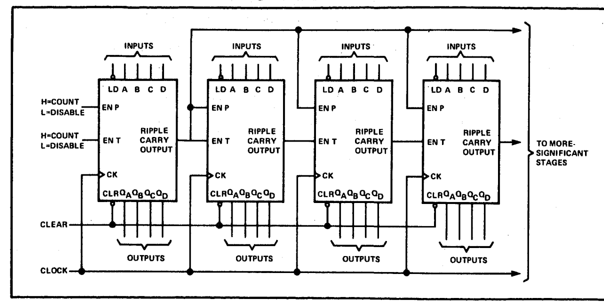
C. V_{ref} = 1.3V.

Load circuit is shown at front of book (totem pole outputs).

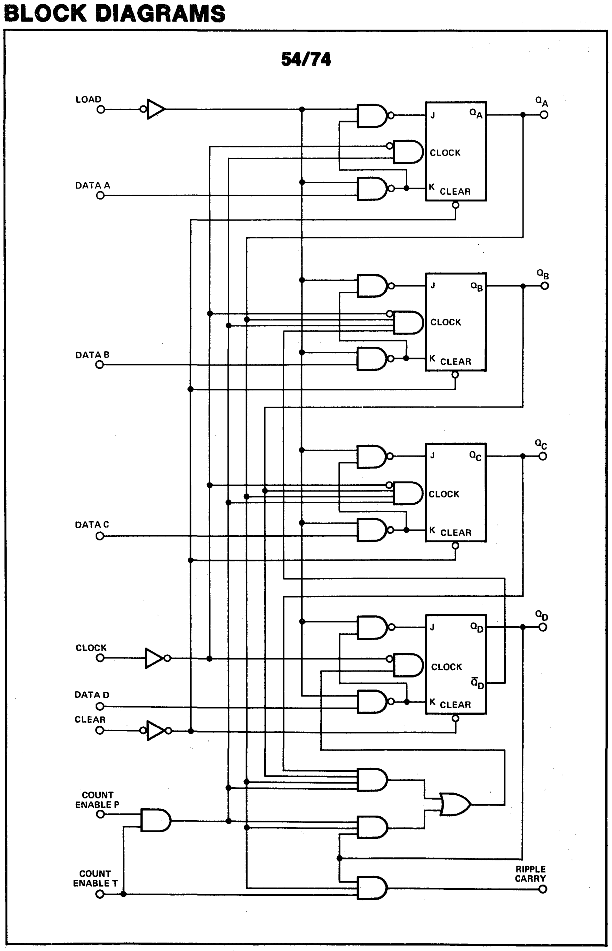
N-BIT SYNCHRONOUS COUNTERS

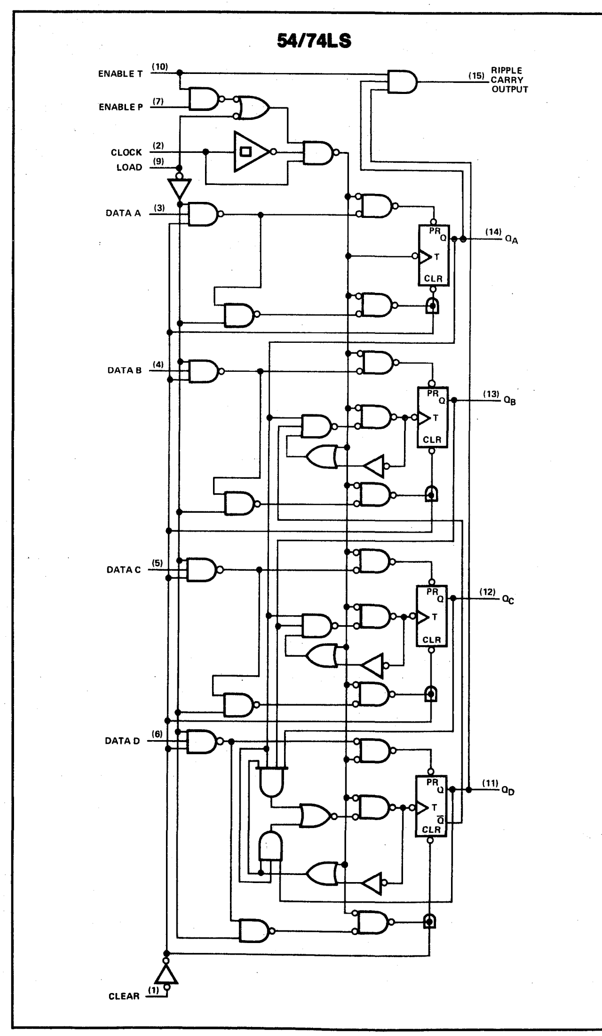
This application demonstrates how the look-ahead carry circuit can be used to implement a high-speed n-bit counter. The 54/74LS160 will count in BCD. Virtually any count mode (modulo-N, N_1-toN_2, N_1-to-maximum) can be used with this fast look-ahead circuit.

TYPICAL APPLICATION DATA



BLOCK DIAGRAMS





SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

TEST CONDITIONS				54/74 C_L=15pF R_L=400Ω			54/74LS C_L=15pF R_L=2KΩ			
PARAMETER		FROM INPUT	TO OUTPUT	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
t_{Clock}	Clock frequency			25	32		25	32		MHz
$t_{W(Clock)}$	Width of clock input pulse			25			25			ns
$t_{w(Clear)}$	Width of clear input pulse			20			20			ns
t_{Setup}	Input setup time	D_A-D_D		15						ns
		Enable P		20						
		Load		25						
		A,B,C,D	Q				0↑			
		Enable P, Enable T	Q				20↑			
		Load	Q				20↑			
t_{Hold}	Input hold time	Any		0						ns
		A,B,C,D					25↑			
		Others					10↑			
Propagation delay time										
t_{PLH}	Low-to-high	Clock	Carry		23	35		23	35	ns
t_{PHL}	High-to-low				23	35		23	35	
t_{PLH}	Low-to-high	Clock (load input high)	Q		13	20		16	24	
t_{PHL}	High-to-low				15	23		18	27	
t_{PLH}	Low-to-high	Clock (load input low)	Q		17	25		17	25	
t_{PHL}	High-to-low				19	29		19	29	
t_{PLH}	Low-to-high	Enable T	Carry		10	14		15	23	
t_{PHL}	High-to-low				10	14		15	23	
t_{PHL}	High-to-low	Clear	Q		20	30		26	38	

Load circuit and typical waveforms are shown at the front of section.

SYNCHRONOUS 4-BIT BINARY COUNTER 54/74161

SPEED/PACKAGE AVAILABILITY

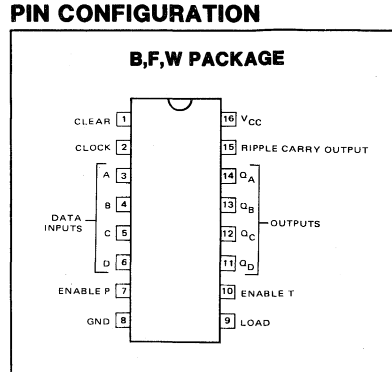
54 F,W 74 B,F
54LS F,W 74LS B,F

DESCRIPTION

This synchronous presettable binary counter features an internal carry look-ahead for applications in high-speed counting designs. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enable inputs and internal gating. This mode of operation eliminates the output counting spikes which are normally associated with asynchronous (ripple clock) counters. A buffered clock input triggers the four flip-flops on the rising (positive-going) edge of the clock input waveform.

This counter is fully programmable; that is, the outputs may be preset to either level. As presetting is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the setup data after the next clock pulse regardless of the

PIN CONFIGURATION

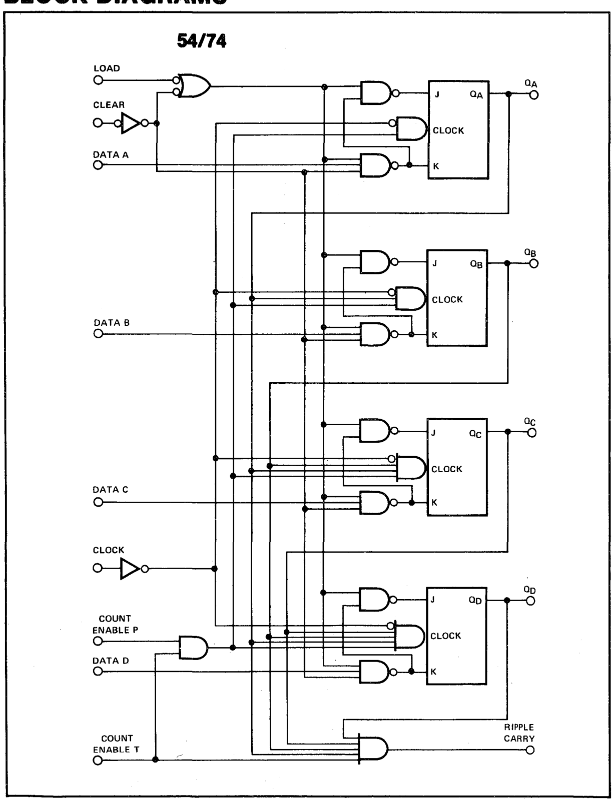


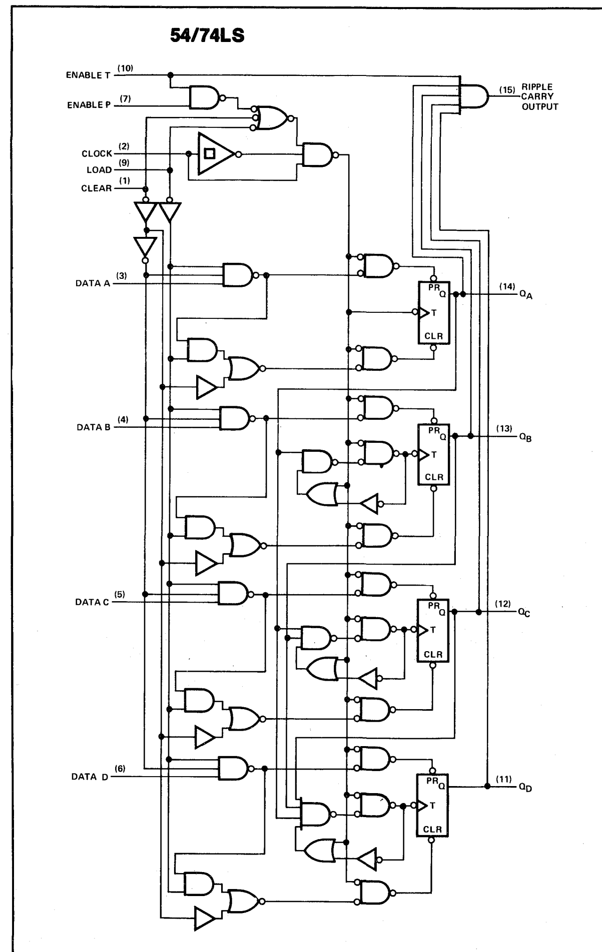
levels of the enable inputs. The clear function for the 54/74LS161 is asynchronous and a low level at the clear input sets all four of the flip-flop outputs low regardless of the levels of clock, load or enable inputs.

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two count-enable inputs and a ripple carry output. Both count-enable inputs (P and T) must be high to count, and input T is fed forward to enable the ripple carry output. The ripple carry output thus enabled will produce a high-level output pulse with a duration approximately equal to the high-level portion of the Q_A output. This high-level overflow ripple carry pulse can be used to enable successive cascaded stages. Transitions at the enable P or T inputs are allowed regardless of the level of the clock input.

The 54/74LS161 features a fully independent clock circuit. Changes made to control inputs (enable P or T, load or clear) that will modify the operating mode have no effect until clocking occurs. The function of the counter (whether enabled, disabled, loading or counting) will be dictated solely by the conditions meeting the stable setup and hold times.

BLOCK DIAGRAMS



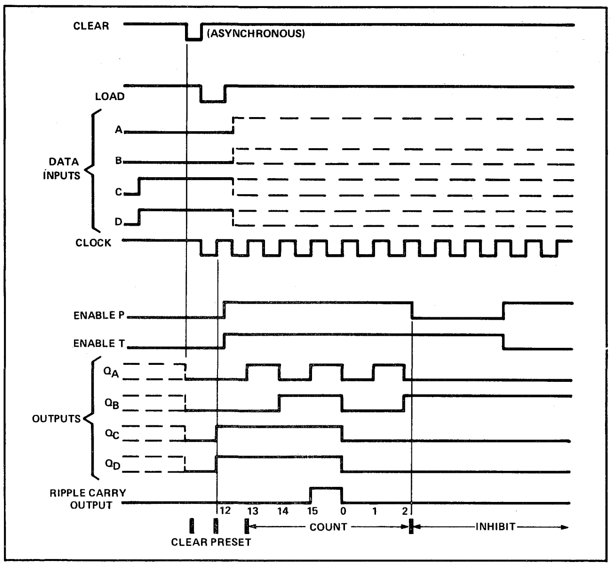


PARAMETER MEASUREMENT INFORMATION

TYPICAL CLEAR, PRESET, COUNT, AND INHIBIT SEQUENCES

Illustrated below is the following sequence:

1. Clear outputs to zero
2. Preset to binary twelve
3. Count to thirteen, fourteen, fifteen, zero, one, and two
4. Inhibit



NOTES

A. The input pulses are supplied by a generator having the following characteristics: PRR ≤ 1MHz, Duty Cycle ≤ 50%, $Z_{out} \approx 50\Omega$ $t_r \leq 15ns$, $t_f \leq 6ns$.
B. Outputs Q_D and carry are tested at t_{n+16}, where t_n is the bit time when all outputs are low.
C. $V_{ref} = 1.3V$.

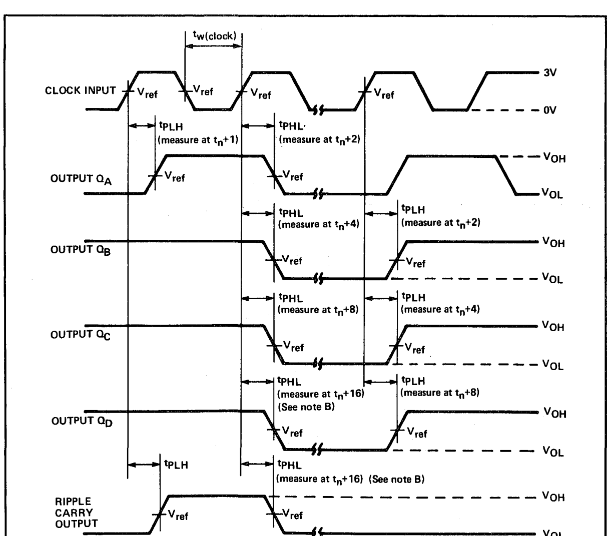


FIGURE 1—VOLTAGE WAVEFORMS

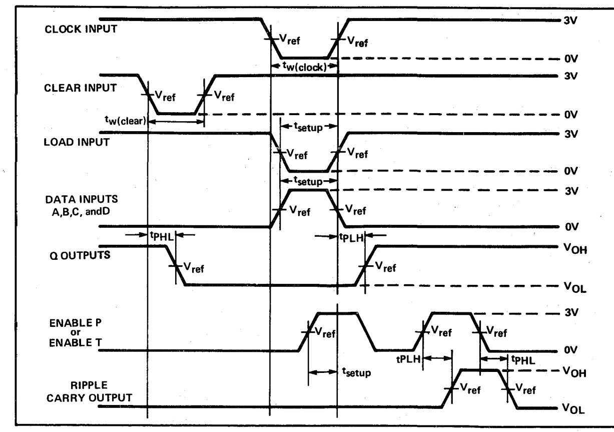


FIGURE 2—VOLTAGE WAVEFORMS

NOTES

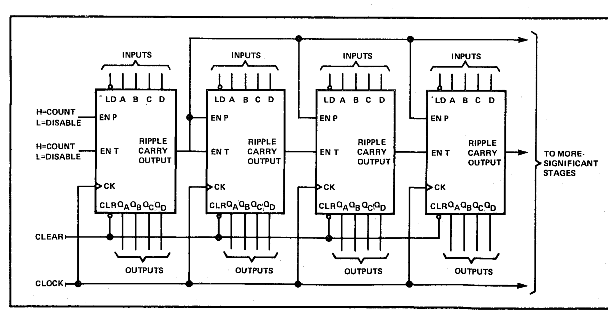
A. The input pulses are supplied by generators having the following characteristics: PRR≤1MHz, Duty cycle ≤ 50%, $Z_{out} \approx 50\Omega$, $t_r \leq 15ns$, $t_f \leq 6ns$.
B. Enable P and T setup times are measured at t_{n+0}.
C. $V_{ref} = 1.3V$.

Load circuit is shown at front of book (totem pole output).

TYPICAL APPLICATION DATA

N-BIT SYNCHRONOUS COUNTERS

This application demonstrates how the look-ahead carry circuit can be used to implement a high-speed n-bit counter.The 54/74LS161 will count in binary. Virtually any count mode (modulo-N, N_1-toN_2, N_1-to-maximum) can be used with this fast look-ahead circuit.



LOGIC

SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

TEST CONDITIONS			54/74 C_L=15pF R_L=400Ω			54/74LS C_L=15pF R_L=2kΩ			
PARAMETER	**FROM INPUT**	**TO OUTPUT**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNIT**
f_{Clock} Clock frequency			25	32		25	32		MHz
t_W (Clock) Width of clock input pulse			25			25			ns
t_W (Clear) Width of clear input pulse			20			20			ns
t_{Setup} Input setup time	$D_A - D_D$		15						ns
	Enable P		26						
	Load		25						
	A,B,C,D	Q				0†			
	Enable P, Enable T	Q				20†			
	Load	Q				20†			
t_{Hold} Input hold time	Any		0						ns
	A,B,C,D					25†			
	Others					10†			
Propagation delay time									
t_{PLH} Low-to-high	Clock	Carry		23	35		23	35	ns
t_{PHL} High-to-low				23	35		23	35	
t_{PLH} Low-to-high	Clock (load input high)	Q		13	20		16	24	
t_{PHL} High-to-low				15	23		18	27	
t_{PLH} Low-to-high	Clock (load input low)	Q		17	25		17	25	
t_{PHL} High-to-low				19	29		19	29	
t_{PLH} Low-to-high	Enable T	Carry		10	14		15	23	
t_{PHL} High-to-low				10	14		15	23	
t_{PHL} High-to-low	Clear	Q		20	30		26	38	

Load circuit and typical waveforms shown at the front of section.

SYNCHRONOUS 4-BIT DECADE COUNTER 54/74162

SPEED/PACKAGE AVAILABILITY

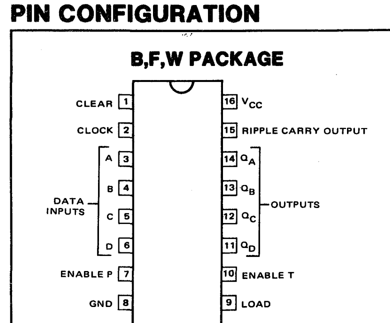
54 F,W — 74 B,F
54LS F,W — 74LS B,F

DESCRIPTION

This synchronous presettable decade counter features an internal carry look-ahead for applications in high-speed counting designs. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enable inputs and internal gating. This mode of operation eliminates the output counting spikes which are normally associated with asynchronous (ripple clock) counters. A buffered clock input triggers the four flip-flops on the rising (positive-going) edge of the clock input waveforms.

This counter is fully programmable; that is, the outputs may be preset to either level. As presetting is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the setup data after the next clock pulse regardless of

PIN CONFIGURATION



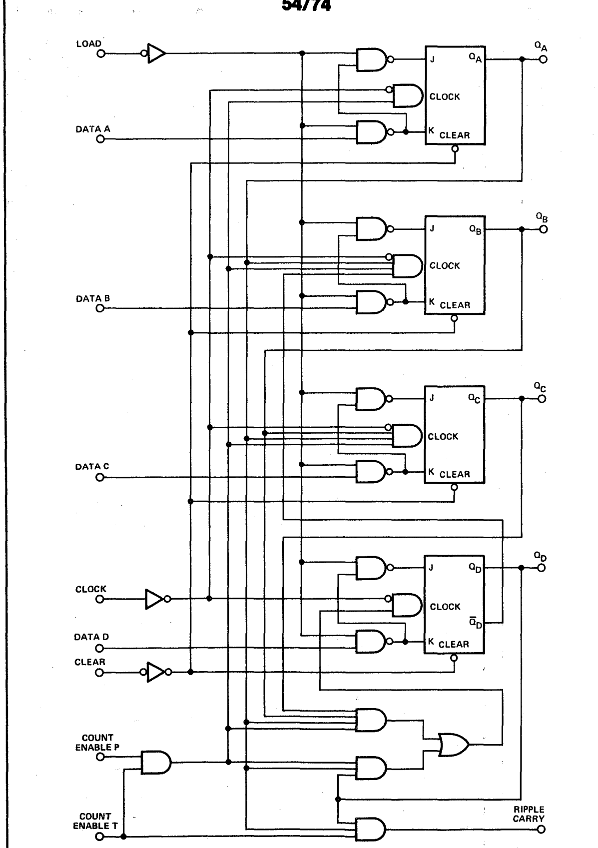
the levels of the enable inputs. The clear function for the 54/74LS162 is synchronous and a low level at the clear input sets all four of the flip-flop outputs low after the next clock pulse, regardless of the levels of the enable inputs. This synchronous clear allows the count length to be modified easily as decoding the maximum count desired can be accomplished with one external NAND gate. The gate output is connected to the clear input to synchronously clear the counter to 0000 (LLLL).

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two count-enable inputs and a ripple carry output. Both count-enable inputs (P and T) must be high to count, and input T is fed forward to enable the ripple carry output. The ripple carry output thus enabled will produce a high-level output pulse with a duration approximately equal to the high-level portion of the Q_A output. This high-level overflow ripple carry pulse can be used to enable successive cascaded stages. Transitions at the enable P or T inputs are allowed regardless of the level of the clock input.

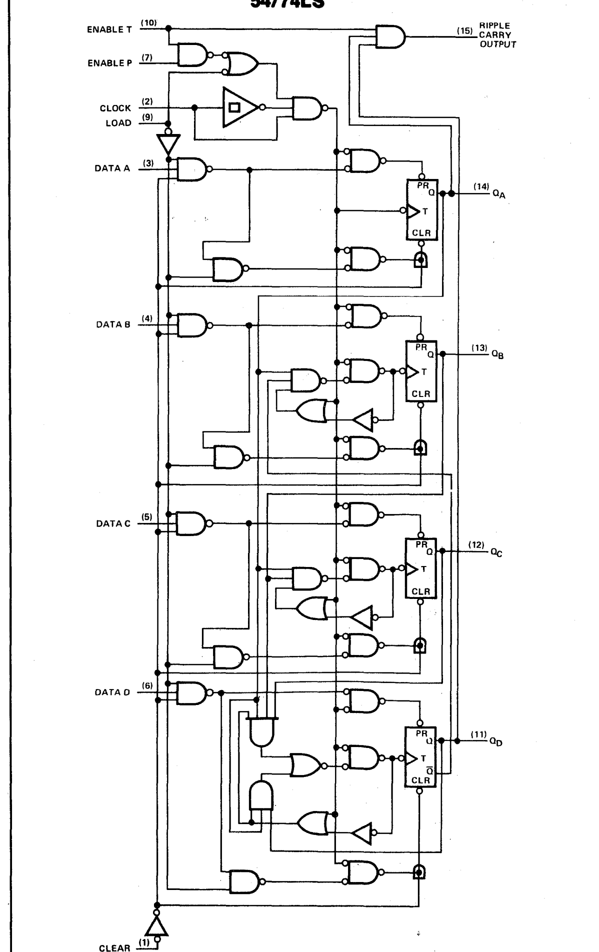
The 54/74LS162 features a fully independent clock circuit. Changes made to control inputs (enable P or T, load or clear) that will modify the operating mode have no effect until clocking occurs. The function of the counter (whether enabled, disabled, loading or counting) will be dictated solely by the conditions meeting the stable set up and hold times.

BLOCK DIAGRAMS

54/74



54/74LS



SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

TEST CONDITIONS			54/74 C_L=15pF R_L=400Ω			54/74LS C_L=15pF R_L=2KΩ			
PARAMETER	FROM INPUT	TO OUTPUT	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
f_{Clock} Clock frequency			25	32		25	32		MHz
$t_{w(Clock)}$ Width of clock input pulse			25			25			ns
$t_{w(Clear)}$ Width of clear input pulse			20			20			ns
t_{Setup} Input setup time	$D_A - D_D$		15						ns
	Enable P		20						
	Load		25						
	Clear		20						
	A,B,C,D	Q				0↑			
	Enable P, Enable T	Q				20↑			
	Load	Q				20↑			
	Clear	Q				20↑			
t_{Hold} Input hold time	Any		0						ns
	A,B,C,D					25↑			
	Others					10↑			
Propagation delay time									
t_{PLH} Low-to-high	Clock	Carry		23	35		23	35	ns
t_{PHL} High-to-low				23	35		23	35	
t_{PLH} Low-to-high	Clock	Q		13	20		16	24	
t_{PHL} High-to-low				15	23		18	27	
	(load input high)								
t_{PLH} Low-to-high	Clock	Q		17	25		17	25	
	(load input low)								
t_{PHL} High-to-low				19	29		19	29	
t_{PLH} Low-to-high	Enable T	Carry		10	14		15	23	
t_{PHL} High-to-low				10	14		15	23	
t_{PHL} High-to-low	Clear	Q		20	30		26	38	

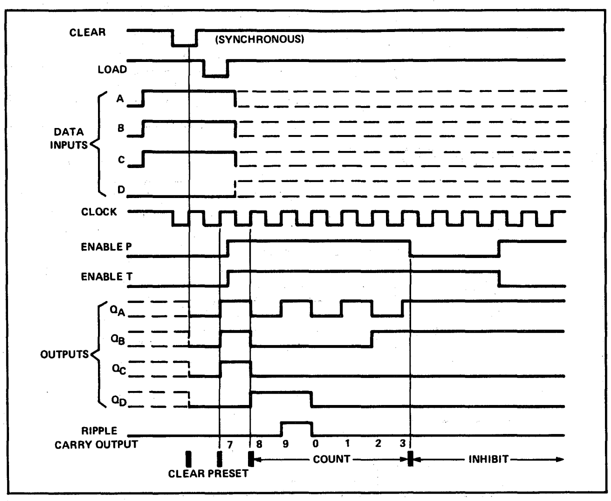
Load circuit typical and waveforms are shown at the front of section.

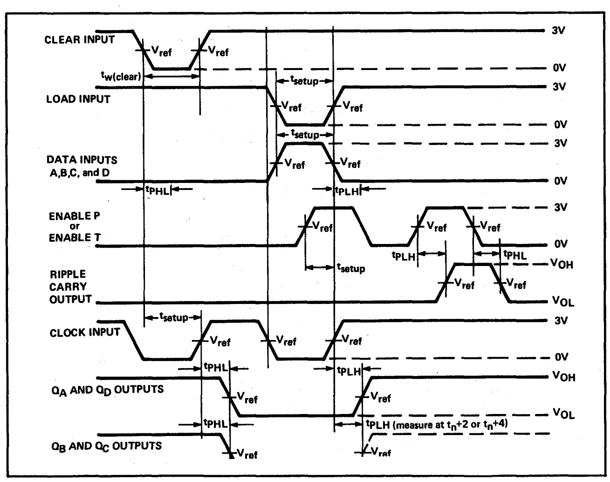
PARAMETER MEASUREMENT INFORMATION

TYPICAL CLEAR, PRESET, COUNT AND INHIBIT SEQUENCES

Illustrated below is the following sequence:

1. Clear outputs to zero
2. Preset to BCD seven
3. Count to eight, nine, zero, one, two, and three
4. Inhibit





VOLTAGE WAVEFORMS

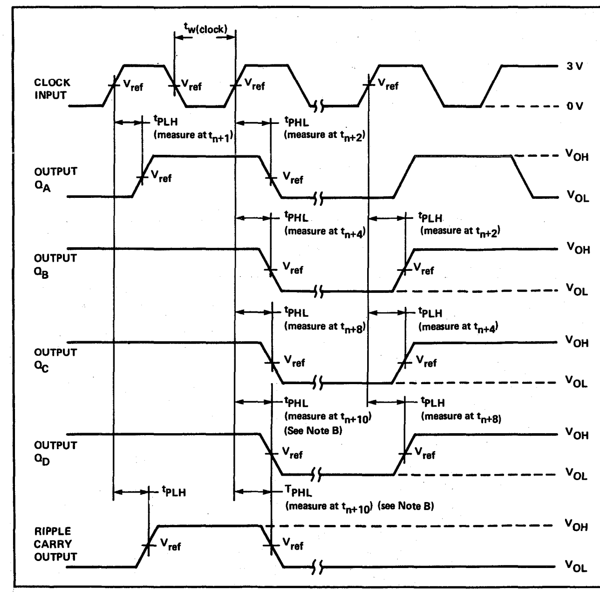
NOTES:

A. The input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, duty cycle ≤ 50%, $Z_{out} \approx 50\ \Omega$; $t_r < 15$ ns, $t_f \leq 6$ ns.

B. Enable P and enable T setup times are measured at t_{n+0}.

C. $V_{ref} = 1.3$ V.

FIGURE 2-SWITCHING TIMES



VOLTAGE WAVEFORMS

NOTES:

A. The input pulses are supplied by a generator having the following characteristics: PRR ≤ 1MHz, duty cycle ≤ 50%, $Z_{out} \approx 50\ \Omega$; $t_r \leq 15$ ns, $t_f \leq 6$ ns; vary PRR to measure f_{max}.

B. Outputs Q_D and carry are tested at t_{n+10} where t_n is the bit time when all outputs are low.

C. $V_{ref} = 1.5$ V.

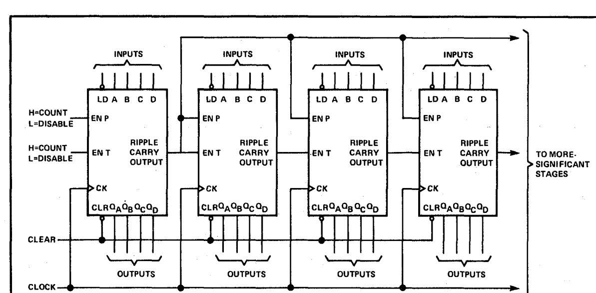
Load Circuit information is shown at the front of the book.

FIGURE 1-SWITCHING TIMES

TYPICAL APPLICATION DATA

N-BIT SYNCHRONOUS COUNTERS

This application demonstrates how the look-ahead carry circuit can be used to implement a high-speed n-bit counter. The 54/74LS162 will count in BCD. Virtually any count mode (modulo-N, N_1-toN_2, N_1-to-maximum) can be used with this fast look-ahead circuit.

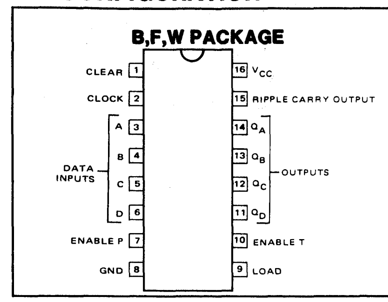


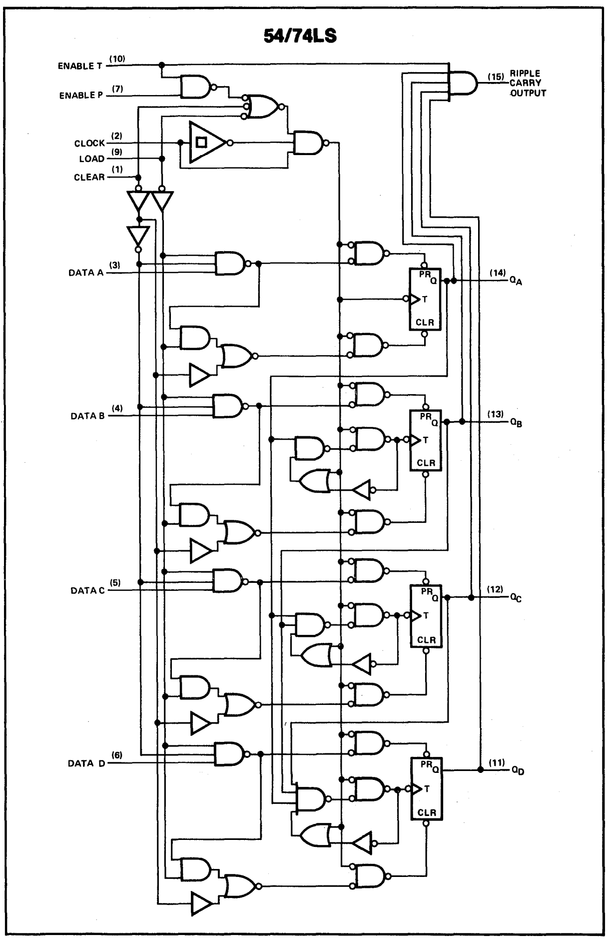
LOGIC

SPEED/PACKAGE AVAILABILITY

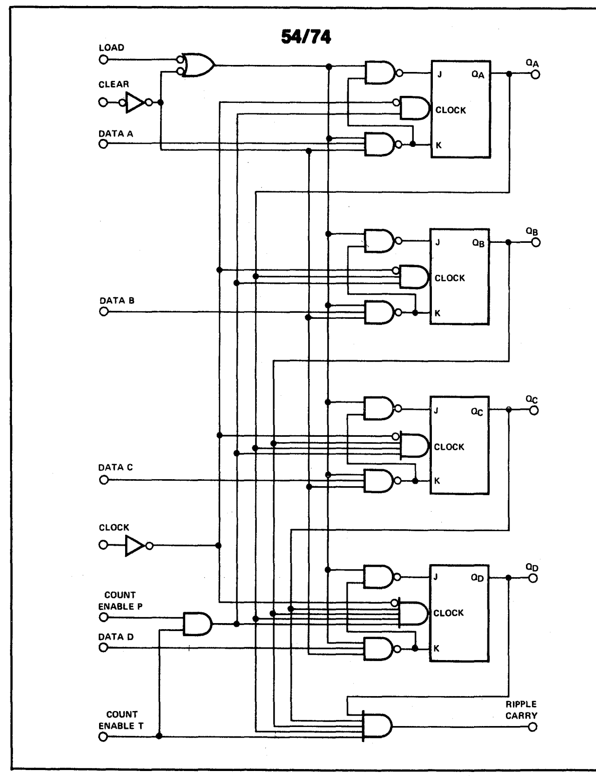
54 F,W 74 B,F
54LS F,W 74LS B,F

PIN CONFIGURATION





BLOCK DIAGRAM



DESCRIPTION

This synchronous presettable binary counter features an internal carry look-ahead for applications in high-speed counting designs. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enable inputs and internal gating. This mode of operation eliminates the output counting spikes which are normally associated with asynchronous (ripple clock) counters. A buffered clock input triggers the four flip-flops on the rising (positive-going) edge of the clock input waveforms.

This counter is fully programmable; that is, the outputs may be preset to either level. As presetting is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the setup data after the next clock pulse regardless of the levels of the enable inputs. The clear function for the 54/74LS163 is synchronous and a low level at the clear input sets all four of the flip-flop outputs low after the next clock pulse, regardless of the levels of the enable inputs. This synchronous clear allows the count length to be modified easily as decoding the maximum count desired can be accomplished with one external NAND gate. The gate output is connected to the clear input to synchronously clear the counter to 0000 (LLLL).

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two count-enable inputs and a ripple carry output. Both count-enable inputs (P and T) must be high to count, and input T is fed forward to enable the ripple carry output. The ripple carry output thus enabled will produce a high-level output pulse with a duration approximately equal to the high-level portion of the Q_A output. This high-level overflow ripple carry pulse can be used to enable successive cascaded stages. Transitions at the enable P or T inputs are allowed regardless of the level of the clock input.

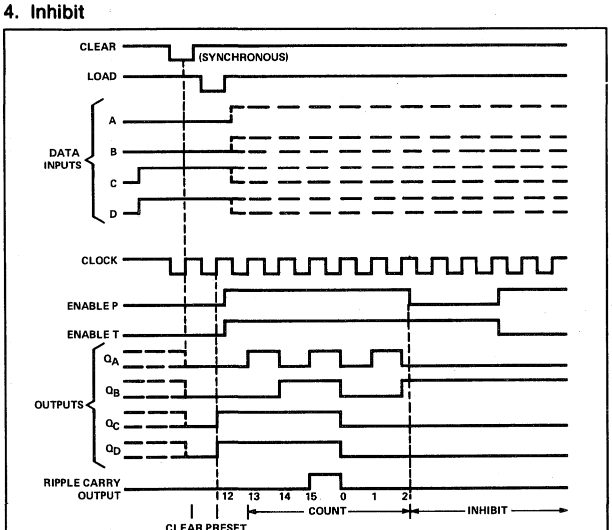
The 54/74LS163 features a fully independent clock circuit. Changes made to control inputs (enable P or T, load or clear) that will modify the operating mode have no effect until clocking occurs. The function of the counter (whether enabled, disabled, loading or counting) will be dictated solely by the conditions meeting the stable setup and hold times.

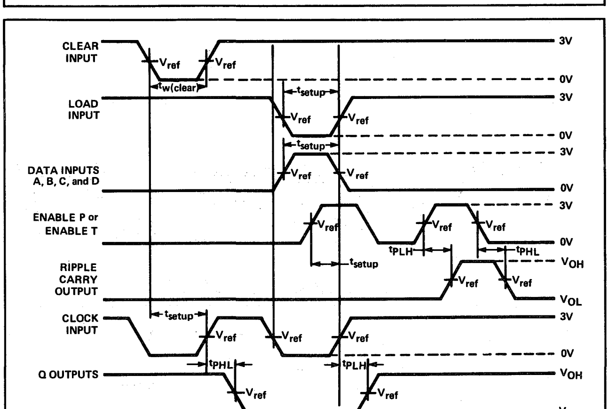
PARAMETER MEASUREMENT INFORMATION

TYPICAL CLEAR, PRESET, COUNT, AND INHIBIT SEQUENCES

Illustrated below is the following sequence:

1. Clear outputs to zero
2. Preset to binary twelve
3. Count to thirteen, fourteen, fifteen, zero, one, and two
4. Inhibit





VOLTAGE WAVEFORMS

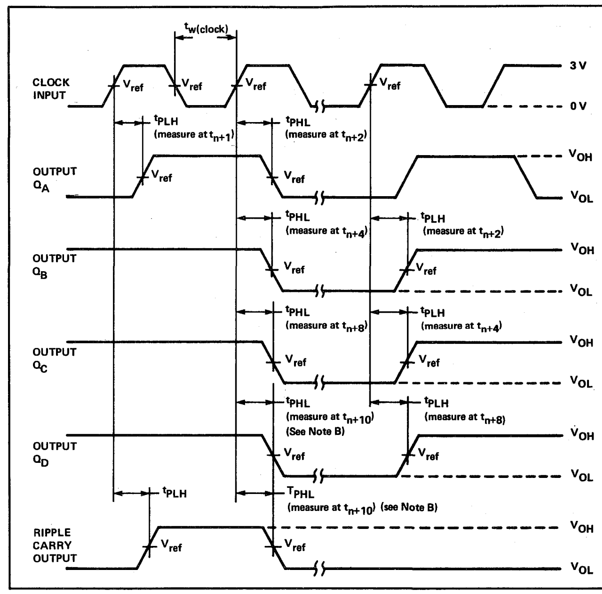
NOTES:

A. The input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, duty cycle ≤ 50%, $Z_{out} \approx 50\ \Omega$; '163, $t_r \le 10$ ns, $t_f \le 10$ ns; and for 'LS160 thru 'LS163, $t_r \le 15$ ns, $t_f \le 6$ ns.

B. Enable P and enable T setup times are measured at t_{n+0}.

C. V_{ref} = 1.3 V.

FIGURE 2—SWITCHING TIMES



VOLTAGE WAVEFORMS

NOTES:

A. The input pulses are supplied by a generator having the following characteristics: PRR ≤ 1 MHz, duty cycle ≤ 50%, $Z_{out} \approx 50\ \Omega$; $t_r \le 15$ ns, $t_f \le 6$ ns. Vary PRR to measure f_{max}.

B. Outputs Q_D and carry are tested at t_n+16 where t_n is the bit time when all outputs are low.

C. V_{ref} = 1.3 V.

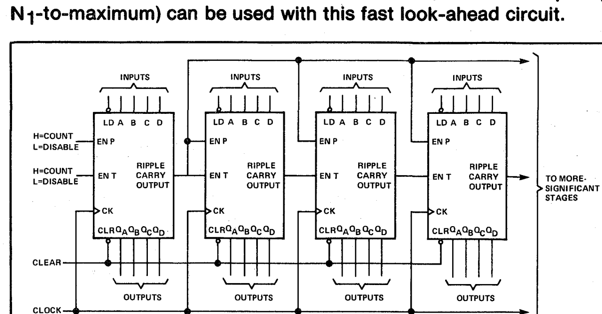
Load circuit is shown at the front of the book.

FIGURE 1—SWITCHING TIMES

TYPICAL APPLICATION DATA

N-BIT SYNCHRONOUS COUNTERS

This application demonstrates how the look-ahead carry circuit can be used to implement a high-speed n-bit counter. The 54/74LS163, will count in binary. Virtually any count mode (modulo-N, N_1-toN_2, N_1-to-maximum) can be used with this fast look-ahead circuit.



SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

TEST CONDITIONS				54/74			54/74LS			
				C_L=15pF R_L=400Ω			C_L=15pF R_L=2KΩ			
PARAMETER		FROM INPUT	TO OUTPUT	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
f_{Clock}	Clock frequency			25	32		25	32		MHz
$t_{w(Clock)}$	Width of clock input pulse			25			25			ns
$t_{w(Clear)}$	Width of clear input pulse			20			20			
t_{Setup}	Input setup time	$D_A - D_D$		15						
		Enable P		20						
		Load		25						
		Clear		20						
		A,B,C,D	Q				0↑			
		Enable P	Q				20↑			
		Enable T					20↑			
		Load	Q				20↑			
		Clear	Q				20↑			
t_{Hold}	Input hold time	Any		0						
		A,B,C,D					25↑			
		Others					10↑			
Propagation delay time										
t_{PLH}	Low-to-high	Clock	Carry		23	35		23	35	ns
t_{PHL}	High-to-low				23	35		23	35	
t_{PLH}	Low-to-high	Clock (load input high)	Q		13	20		16	24	
t_{PHL}	High-to-low				15	23		18	27	
t_{PLH}	Low-to-high	Clock (load input low)	Q		17	25		17	25	
t_{PHL}	High-to-low				19	29		19	29	
t_{PLH}	Low-to-high	Enable T	Carry		10	14		15	23	
t_{PHL}	High-to-low				10	14		15	23	
t_{PHL}	High-to-low	Clear	Q		20	30		26	38	

Load circuit and typical waveforms are shown at the front of section.

8-BIT PARALLEL-OUT SERIAL SHIFT REGISTER 54/74164

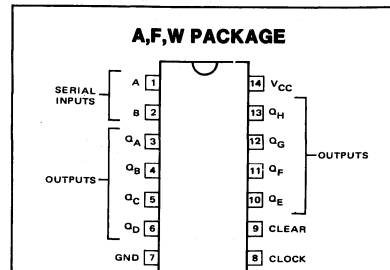
SPEED/PACKAGE AVAILABILITY

54 F,W — 74 A
54LS F,W — 74LS A

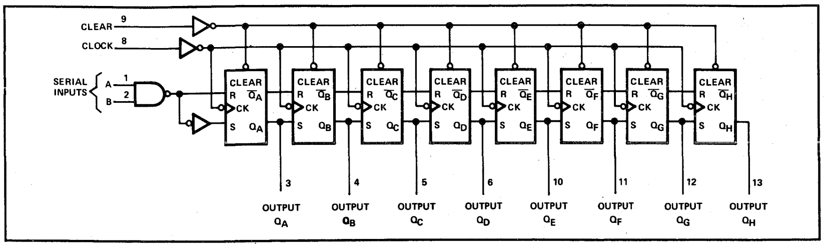
DESCRIPTION

This 8-bit shift register features gated serial inputs and an asynchronous clear. The gated serial inputs (A and B) permit complete control over incoming data as a low at either (or both) input(s) entry of the new data and resets the first flip-flop to the low level at the next clock pulse. A high-level input enables the other input which will then determine the state of the first flip-flop. Data at the serial inputs may be changed while the clock is high or low, but the only information meeting the setup requirements will be entered. Clocking occurs on the low-to-high level transition of the clock input. All inputs are diode-clamped to minimize transmission-line effects.

PIN CONFIGURATION



FUNCTIONAL BLOCK DIAGRAM



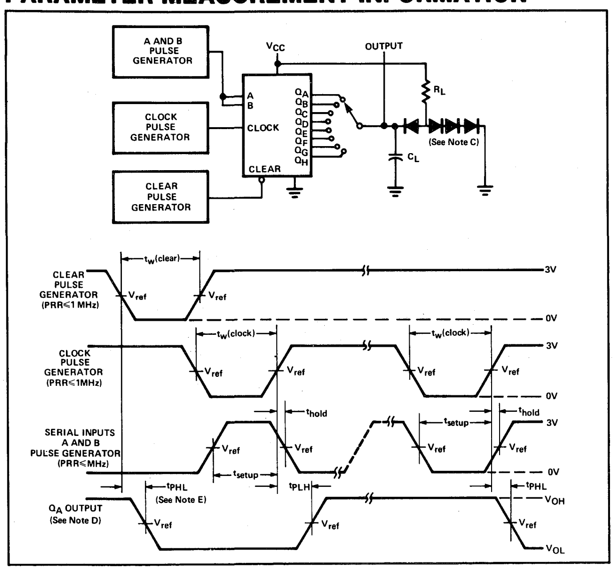
TRUTH TABLE

54/74		
SERIAL INPUTS A AND B		
INPUTS $AT t_n$		OUTPUT $AT t_{n+1}$
A	B	Q_A
H	H	H
L	H	L
H	L	L
L	L	L

54/74LS						
INPUTS				OUTPUTS		
CLEAR	CLOCK	A	B	Q_A	Q_B	Q_H
L	X	X	X	L	L	L
H	L	X	X	Q_{A0}	Q_{B0}	Q_{H0}
H	↑	H	H	H	Q_{An}	Q_{Gn}
H	↑	L	X	L	Q_{An}	Q_{Gn}
H	↑	X	L	L	Q_{An}	Q_{Gn}

H = high level (steady state), L = low level (steady state)
X = irrelevant (any input, including transitions)
↑ = transition from low to high level.
Q_{A0}, Q_{B0}, Q_{H0} = the level of Q_A, Q_B, or Q_H, respectively, before the indicated steady-state input conditions were established.
Q_{An}, Q_{Gn} = the level of Q_A or Q_G before the most-recent ↑ transition of the clock; indicates a one-bit shift.

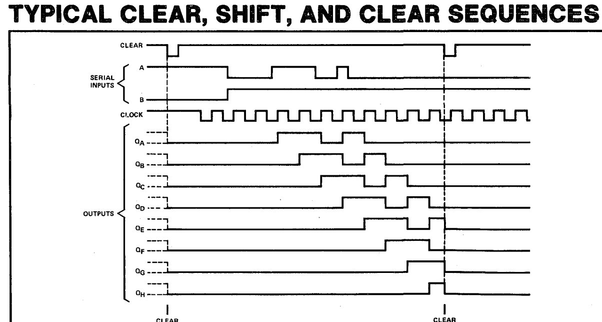
PARAMETER MEASUREMENT INFORMATION



NOTES:

A. The pulse generators have the following characteristics: duty cycle ≤50%, $Z_{out} \approx 50\Omega$; $t_r \leq 15$ ns, $t_f \leq 6$ ns.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N3064 or 1N916.
D. Q_A output is illustrated. Relationship of serial input A and B data to other Q outputs is illustrated in the typical shift sequence.
E. Outputs are set to the high level prior to the measure of t_{PHL} from the clear input.
F. $V_{ref} = 1.3V$.

TYPICAL CLEAR, SHIFT, AND CLEAR SEQUENCES



LOGIC

SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

TEST CONDITIONS			54/74 C_L=15pF R_L=800Ω			54/74LS C_L=15pF R_L=2k			
PARAMETER	FROM INPUT	TO OUTPUT	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
f_{Count} Count frequency			25	36		25	36		MHz
t_W Width of pulse			20			20			ns
t_{Setup} Input setup time			15			15†			ns
t_{Hold} Input hold time			0			5†			ns
Propagation delay time									
t_{PLH} Low-to-high	Clock		8	17	27		17	27	ns
			C_L=50pF						
			10	20	30				
t_{PHL} High-to-low			10	21	32		21	32	
			C_L=50pF						
			10	25	37				
t_{PHL} High-to-low	Clear			24	36		24	36	
			C_L=50pF						
				28	42				

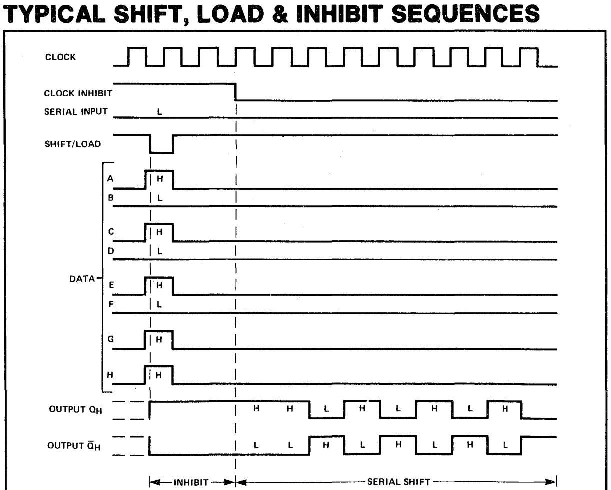
Load circuit and typical waveforms are shown at the front of section.

PARALLEL-LOAD 8-BIT SHIFT REGISTER 54/74165

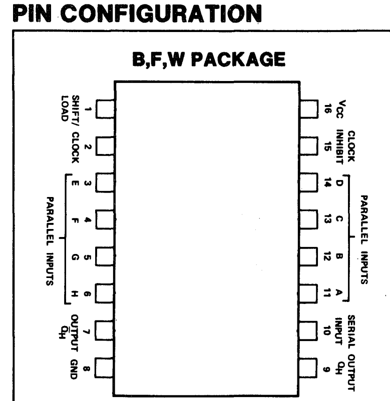
SPEED/PACKAGE AVAILABILITY

54 F,W 74 B

TYPICAL SHIFT, LOAD & INHIBIT SEQUENCES



PIN CONFIGURATION

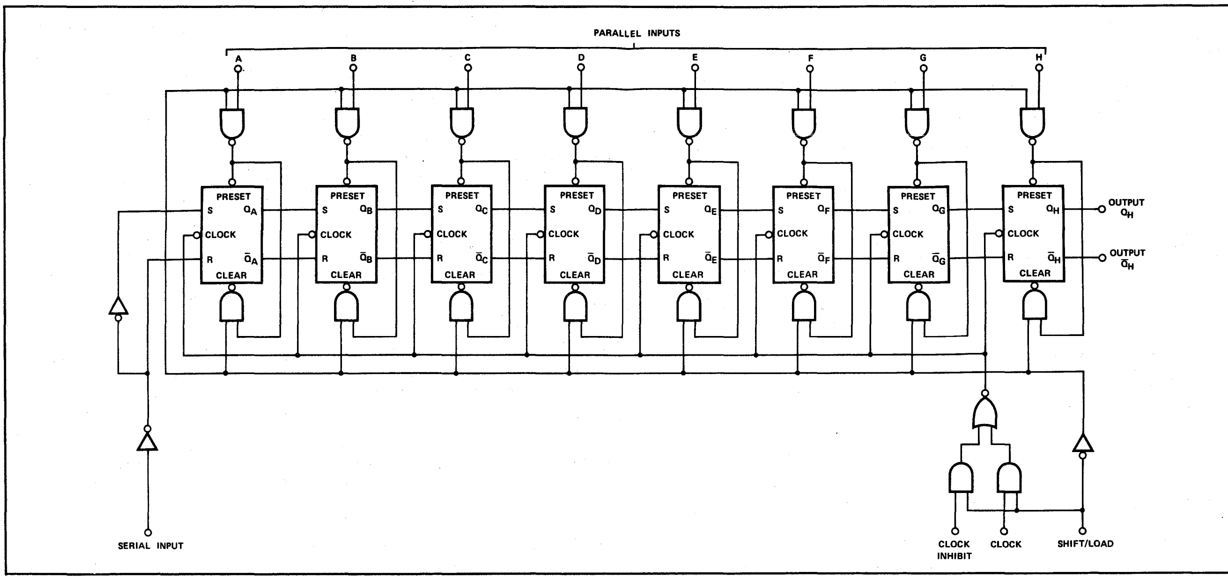


TRUTH TABLE

INPUTS					INTERNAL OUTPUTS		OUTPUT
SHIFT/LOAD	CLOCK INHIBIT	CLOCK	SERIAL	PARALLEL A...H	Q_A	Q_B	Q_H
L	X	X	X	a...h	a	b	h
H	L	L	X	X	Q_{AO}	Q_{BO}	Q_{HO}
H	L	↑	H	X	H	Q_{An}	Q_{Gn}
H	L	↑	L	X	L	Q_{An}	Q_{Gn}
H	H	↑	X	X	Q_{AO}	Q_{BO}	Q_{HO}

H = high level (steady state), L = low level (steady state)
X = irrelevant (any input, including transitions)
4 = transition from low to high level
a...h = the level of steady-state input at inputs A thru H, respectively.
Q_{AO}, Q_{BO}, Q_{HO} = the level of Q_A, A_B, or Q_H, respectively, before the indicated steady-state input conditions were established. Q_{An}, Q_{On} = the level of Q_A or Q_G, respectively, before the most recent ↑ transition of the clock.

LOGIC DIAGRAM



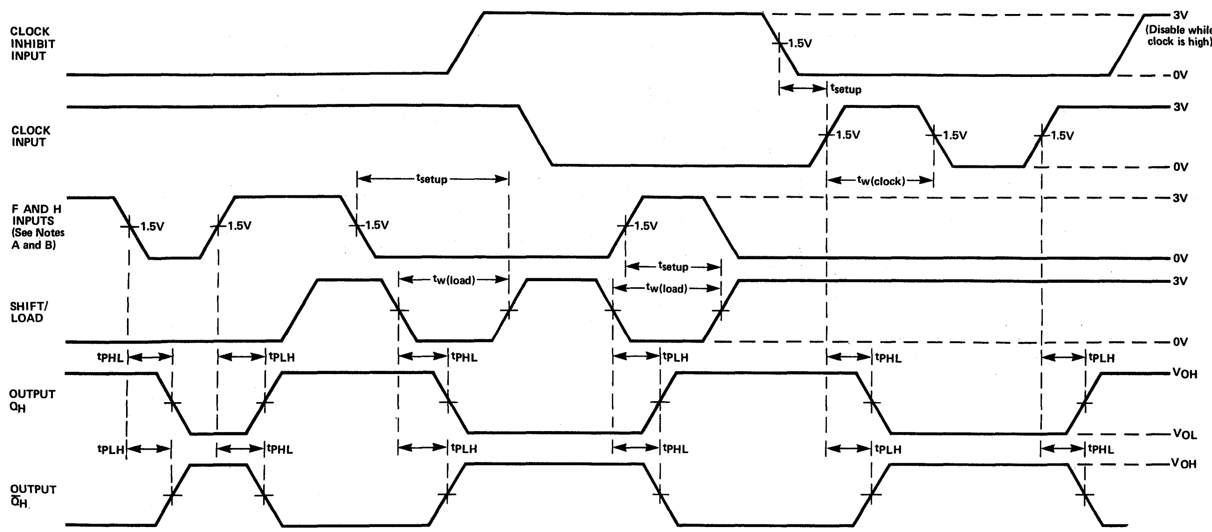
SWITCHING CHARACTERISTICS $V_{CC} = 5V$, $T_A = 25°C$

TEST CONDITIONS				54/74 C_L=15pF R_L=400Ω			
PARAMETER		FROM INPUT	TO OUTPUT	MIN	TYP	MAX	UNIT
f_{max}				20	26		MHz
t_W	Width of pulse	Clock		25			ns
		Load		15			
t_{Setup}	Input setup time						ns
		Clock		30			
		Enable					
		Parallel		10			
		Serial		20			
		Shift		45			
t_{Hold}	Input hold time			0			ns
Propagation delay time							
t_{PLH}	Low-to-high	Load	Any		21	31	ns
t_{PHL}	High-to-low				27	40	
t_{PLH}	Low-to-high	Clock	Any		16	27	
t_{PHL}	High-to-low				21	34	
t_{PLH}	Low-to-high	H	Q_H		11	20	
t_{PHL}	High-to-low				24	36	
t_{PLH}	Low-to-high	H	$\overline{Q}_H$		18	27	
t_{PHL}	High-to-low				18	27	

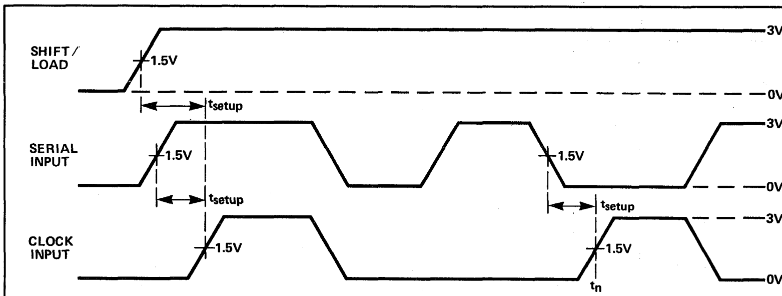
Load circuit and typical waveforms are shown at the front of section.

LOGIC

PARAMETER MEASUREMENT INFORMATION



NOTES: A. The remaining six data inputs and the serial input are low.
B. Prior to test, high-level data is loaded into H input.
C. The input pulse generators have the following characteristics: $t_r \leq 10$ ns, $t_f \leq 10$ ns, PRR $\leq$ 1 MHz, duty cycle $\leq$ 50%, $Z_{out} \approx 50\Omega$
When testing f_{max}, vary clock PRR



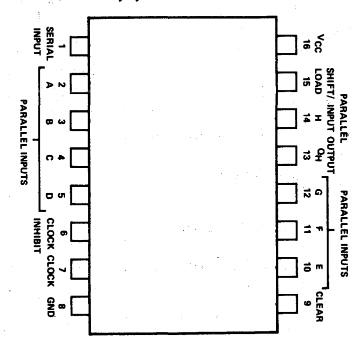
NOTES: A. The eight data inputs and the clock-inhibit input are low. Results are monitored at output Q_H at t_{n+7}.
B. The input pulse generators have the following characteristics: $t_r \leq 10$ ns, $t_f \leq 10$ ns, PRR $\leq$ 1 MHz, duty cycle $\leq$ 50%, $Z_{out} \approx 50\Omega$.

SPEED/PACKAGE AVAILABILITY

54 F,W 74 B

PIN CONFIGURATION

B,F,W PACKAGE

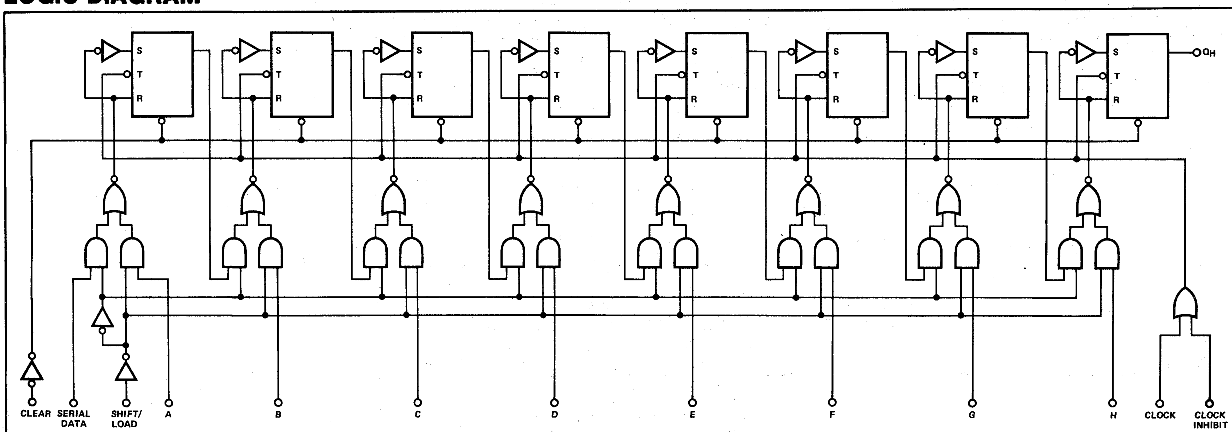


TRUTH TABLE

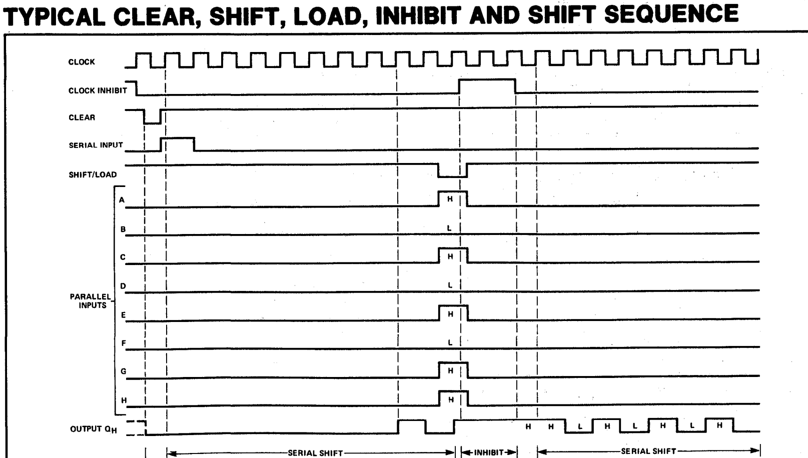
INPUTS						INTERNAL OUTPUTS		OUTPUT
CLEAR	SHIFT/ LOAD	CLOCK INHIBIT	CLOCK	SERIAL	PARALLEL A . . . H	Q_A	Q_B	Q_H
L	X	X	X	X	X	L	L	L
H	X	L	L	X	X	Q_{A0}	Q_{B0}	Q_{H0}
H	L	L	↑	X	a ... h	a	b	h
H	H	L	↑	H	X	H	Q_{An}	Q_{Gn}
H	H	L	↑	L	X	L	Q_{An}	Q_{Gn}
H	X	H	↑	X	X	Q_{A0}	Q_{B0}	Q_{H0}

H = high level (steady state), L = low level (steady state)
X = irrelevant (any input, including transitions)
↑ = transition from low to high level
a ... h = the level of steady state input at inputs A thru H, respectively.
Q_{A0}, Q_{B0}, Q_{H0} = the level of Q_A, Q_B, or Q_H, respectively, before the indicated steady-state input conditions were established.
Q_{An}, Q_{Gn} = the level of Q_A or Q_G, respectively, before the most recent ↑ transition of the clock.

LOGIC DIAGRAM



TYPICAL CLEAR, SHIFT, LOAD, INHIBIT AND SHIFT SEQUENCE



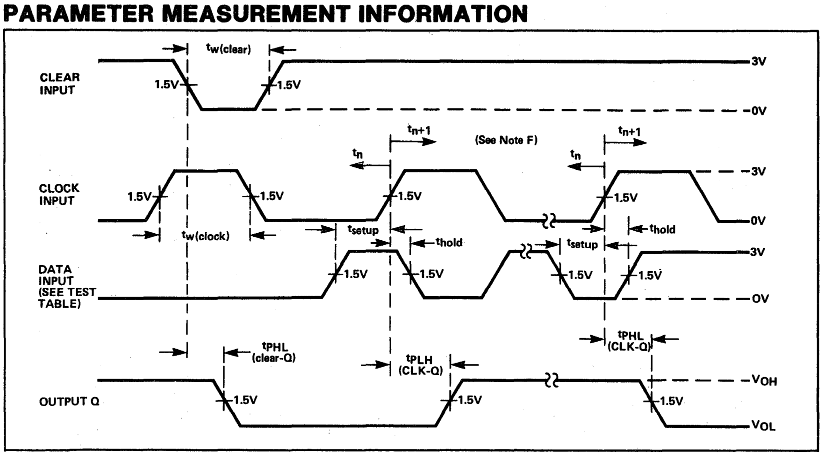
LOGIC

SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

TEST CONDITIONS				54/74 C_L=15pF R_L=400Ω			
PARAMETER		FROM INPUT	TO OUTPUT	MIN	TYP	MAX	UNIT
f_{Count}	Count frequency			25	35		MHz
$t_{w(Clock\ or\ Clear)}$	Width of clock or clear pulse			20			ns
t_{Setup}	Input setup time	Mode Control		30			ns
		Data		20			
t_{Hold}	Input hold time			0			ns
Propagation delay time							
t_{PLH}	Low-to-high	Clock		8	17	26	ns
t_{PHL}	High-to-low			8	20	30	
t_{PHL}	High-to-low	Clear			23	35	

Load circuit and typical waveforms are shown at the front of section.

PARAMETER MEASUREMENT INFORMATION



A. The clock pulse has the following characteristics: $t_{w(clock)} \geq 20$ ns and PRR = 1 MHz. The clear pulse has the following characteristics: $t_{w(clear)} \geq 20$ns and t_{hold} = 0 ns. When testing f_{max}, vary the clock PRR.

B. C_L includes probe and jig capacitance.

C. All diodes are 1N3064.

D. A clear pulse is applied prior to each test.

E. Propagation delay times (t_{PLH} and t_{PHL}) are measured at t_n+1. Proper shifting of data is verified at t_n+8 with a functional test.

F. t_n = bit time before clocking transition

t_n+1 = bit time after one clocking transition

t_n+8 = bit time after eight clocking transitions

SPEED/PACKAGE AVAILABILITY

54	F,W	74	B
54LS	F,W	74LS	B

DESCRIPTION

The register file is organized as 4 words of 4 bits each and separate on-chip decoding is provided for addressing the four word locations to either write-in or retrieve data. This permits simultaneous writing into one location and reading from another word location.

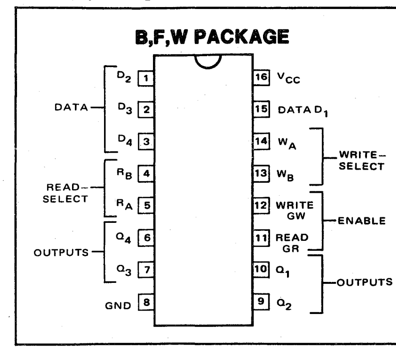
Four data inputs are available which are used to supply the 4-bit word to be stored. Location of the word is determined by the write-address inputs A and B in conjunction with a write-enable signal. Data applied at the inputs should be in its true form. That is, if a high-level signal is desired from the output, a high level is applied at the data input for that particular bit location. The latch inputs are arranged so that new data will be accepted only if both internal address gate inputs are high. When this condition exists, data at the D input is transferred to the latch output. When the write-enable input, G_W, is high, the data inputs are inhibited and their levels can cause no change in the information stored in the internal latches. When the read-enable input, G_R, is high, the data outputs are inhibited and remain high.

The individual address lines permit direct acquisition of data stored in any four of the latches. Four individual decoding gates are used to complete the address for reading a word. When the read address is made in conjunction with the read-enable signal, the word appears at the four outputs.

This arrangement—data-entry addressing separate from data read addressing and individual sense line—eliminates recovery times, permits simultaneous reading and writing, and is limited in speed only by the write time (30 nanoseconds typical) and the read time (25 nanoseconds typical). The register file has a nondestructive readout in that data is not lost when addressed.

All inputs except the read enable and write enable of the 54/74LS170 are buffered to lower the drive requirements to one Series 54LS/74LS standard load, respectively. Input-clamping diodes minimize switching transients to simplify system design. High-speed, double-ended AND-OR-INVERT gates are employed for the read-address function and drive high-sink-current, open-collector outputs. Up to 256 of these outputs may be wire-AND connected for increasing the capacity up to 1024 words. Any number of these registers may be paralleled to provide n-bit word length.

PIN CONFIGURATION



READ FUNCTION TABLE

(See Notes A and D)

READ INPUTS			OUTPUTS			
R_B	R_A	G_R	Q1	Q2	Q3	Q4
L	L	L	W0B1	W0B2	W0B3	W0B4
L	H	L	W1B1	W1B2	W1B3	W1B4
H	L	L	W2B1	W2B2	W2B3	W2B4
H	H	L	W3B1	W3B2	W3B3	W3B4
X	X	H	H	H	H	H

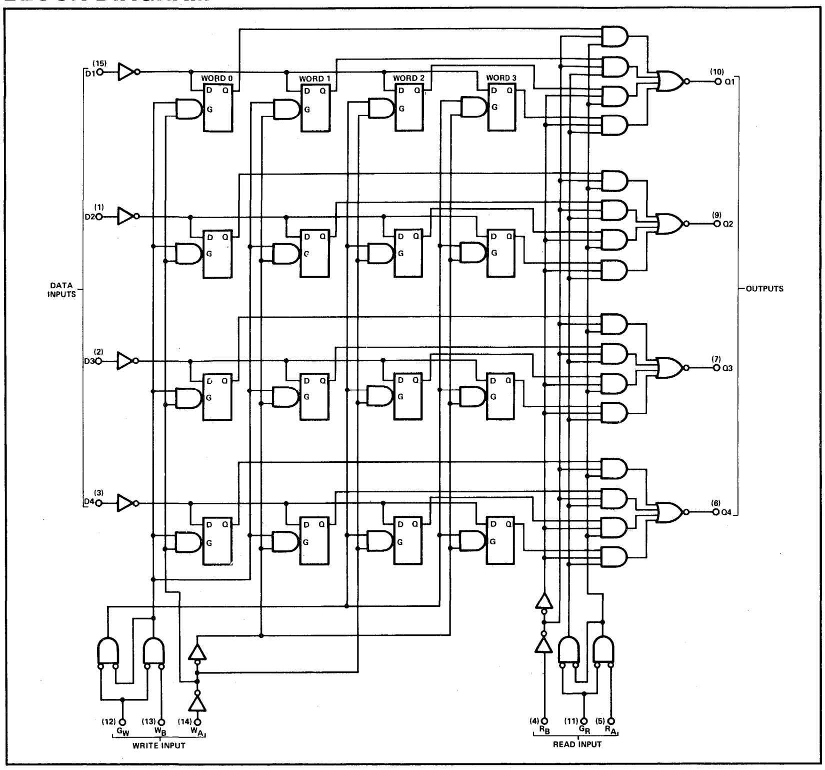
WRITE FUNCTION TABLE

(See Notes A, B, and C)

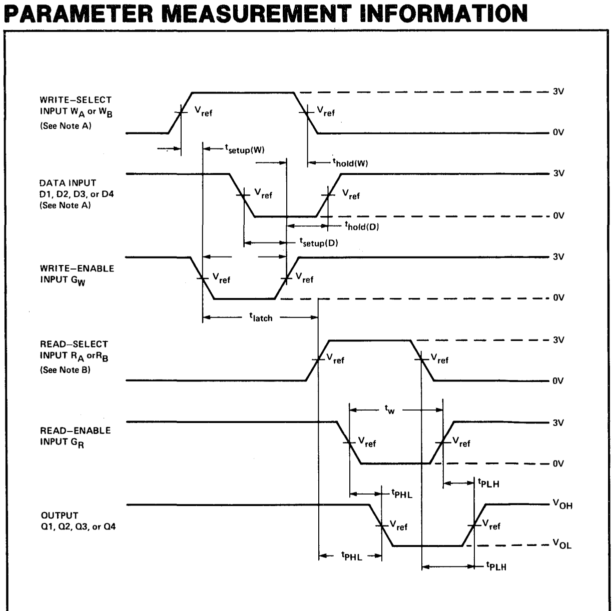
WRITE INPUTS			WORD			
W_B	W_A	G_W	0	1	2	3
L	L	L	Q=D	Q_0	Q_0	Q_0
L	H	L	Q_0	Q=D	Q_0	Q_0
H	L	L	Q_0	Q_0	Q=D	Q_0
H	H	L	Q_0	Q_0	Q_0	Q=D
X	X	H	Q_0	Q_0	Q_0	Q_0

NOTES:
A. H = high level, L = low level, X = irrelevant.
B. (Q = D) = The four selected internal flip-flop outputs will assume the states applied to the four external data inputs.
C. Q_0 = The level of Q before the indicated input conditions were established.
D. W0B1 = The first bit of word 0, etc.

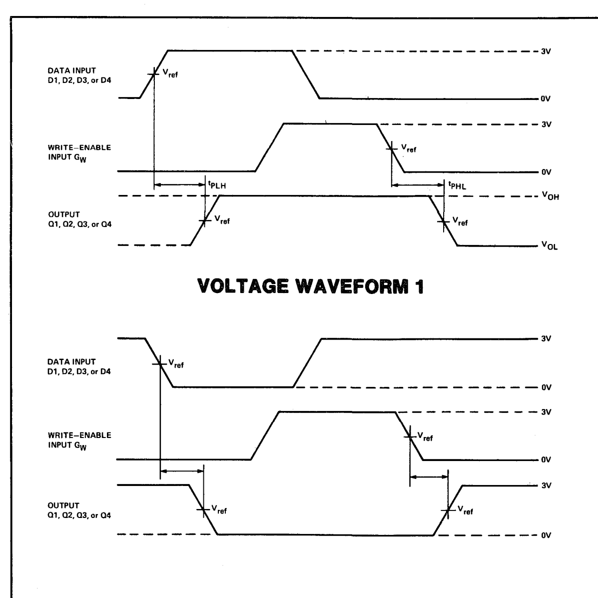
BLOCK DIAGRAM



PARAMETER MEASUREMENT INFORMATION



VOLTAGE WAVEFORMS
FIGURE 1



VOLTAGE WAVEFORM 2
FIGURE 2

NOTES:

A. High-level input pulses at the select and data inputs are illustrated in Figure 2; however, times associated with low-level pulses are measured from the same reference points.

B. When measuring delay times from a read-select input, the read-enable input is low. When measuring delay times from the read-enable input, both read-select inputs have been established at steady states.

C. In Figure 2, each select address is tested. Prior to the start of each of the above tests, both write and read address inputs are stabilized with $W_A = R_A$ and $W_B = R_B$. During the test G_R is low.

D. $V_{ref} = 1.3V$.

Load circuits are shown at the front of book (open collector outputs).

SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

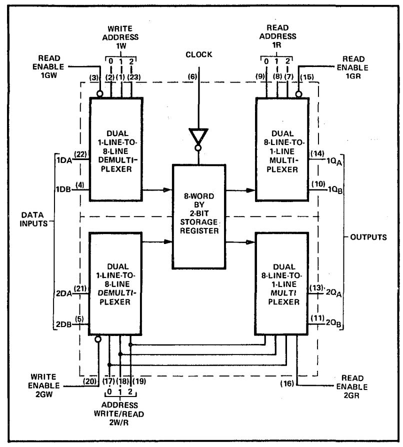
TEST CONDITIONS			54/74 C_L=15pF R_L=400Ω			54/74LS C_L=15pF R_L=2KΩ			
PARAMETER	FROM INPUT	TO OUTPUT	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
t_W Width of pulse			25			25			ns
t_{Setup} Input setup time	Data	Write Enable	10			10			ns
	Write Enable	Write Select	15			15			
t_{Hold} Input hold time	Data	Write Enable	15			15			ns
	Write Enable	Write Select	5			5			
t_{Latch}			25			25			ns
Propagation delay time									
t_{PLH} Low-to-high	Read Enable	Any Q		10	15		20	30	
t_{PHL} High-to-low				20	30		20	30	
t_{PLH} Low-to-high	Read Select	Any Q		23	35		25	40	
t_{PHL} High-to-low				30	40		24	40	
t_{PLH} Low-to-high	Write Enable	Any Q		25	40		30	45	
t_{PHL} High-to-low				34	45		26	40	
t_{PLH} Low-to-high	Data	Any Q		20	30		30	45	
t_{PHL} High-to-low				30	45		22	35	

Load circuit and typical waveforms are shown at the front of section.

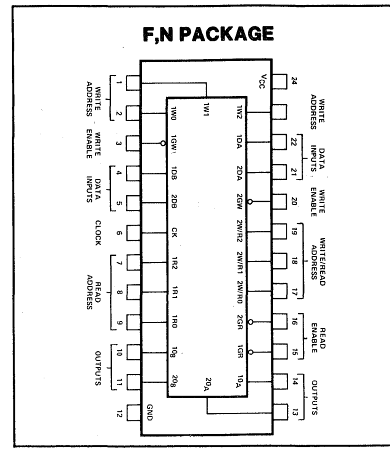
SPEED/PACKAGE AVAILABILITY

74S N

BLOCK DIAGRAM



PIN CONFIGURATION



TRUTH TABLE

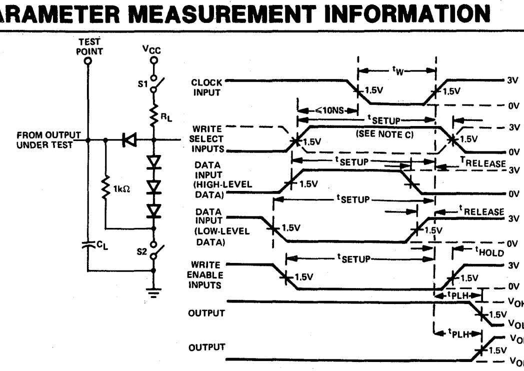
FUNCTION	SECTION 1	SECTION 2	DESCRIPTION
Write Address	1W0, 1W1, 1W2	2W/R0, 2W/R1, 2W/R2	Binary write address selects one of eight two-bit word locations.
Write Enable	1GW	2GW	When low, permits the writing of new data into the selected word location on a positive transition of the clock input.
Data Inputs	1DA, 1DB	2DA, 2DB	Data at these inputs is entered on a positive transition of the clock input into the location selected by the write address inputs if the write enable input is low. Since the two sections are independent, it is possible for both write functions to be activated with both write addresses selecting the same word location. If this occurs and the information at the data inputs is not the same for both sections (i.e., 1DA≠2DA and/or 1DB≠2DB) the low-level data will predominate in each bit and be stored.
Read Address	1R0, 1R1, 1R2	Common with write address	Binary write address selects one of eight two-bit word locations.
Read Enable	1GR	2GR	When read enable is low, the outputs assume the levels of the data stored in the location selected by read address inputs. When read enable is high, the associated outputs remain in the high-impedance state and neither significantly load nor drive the lines to which they are connected.
Data Outputs	$1Q_A$, $1Q_B$	$2Q_A$, $2Q_B$	
Clock	CK		The positive-going transition of the clock input will enter new data into the addressed location if the write enable input is low. The clock is common to both sections.

SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

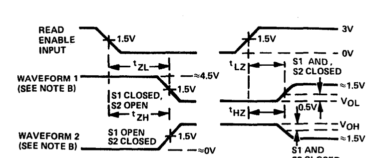
TEST CONDITIONS				54/74 C_L=50pF R_L=400Ω			
PARAMETER		FROM INPUT	TO OUTPUT	MIN	TYP	MAX	UNIT
f_{Clock}	Clock frequency			20			MHz
t_W	Width of pulse			25			ns
t_{Setup}	Input setup time	Write Select		t_W+10			ns
		High level data		30			
		Low level data		45			
		Write enable		35			
t_{Hold}	Input hold time			0			ns
$t_{Release}$	Shift/load release time					10	ns
Propagation delay time							
t_{PLH}	Low-to-high	Read select			33	45	ns
t_{PHL}	High-to-low				30	45	
t_{PLH}	Low-to-high	Clock			35	50	
t_{PHL}	High-to-low				35	50	
Output enable time							
t_{ZH}	To high level				14	30	ns
t_{ZL}	To low level				16	30	
Output disable time					C_L = 5pF		
t_{HZ}	From high level				6	20	ns
t_{LZ}	From low level				11	20	

Load circuit and typical waveforms are shown at the front of section.

PARAMETER MEASUREMENT INFORMATION



SWITCHING TIMES FROM CLOCK INPUT



ENABLE AND DISABLE TIMES FROM READ ENABLE

A. Input waveforms are supplied by pulse generators having the following characteristics: $t_r \le 7$ ns, $t_f \le 7$ ns, PRR = 1 MHz, $Z_{out} \approx 50\ \Omega$
B. Waveforms 1 is for an output with internal conditions such that the output is low except when disabled. Waveform 2 is for an output with internal conditions such that the output is high except when disabled.
C. Write select setup time, as specified, will protect data written into previous address.
D. Load circuit is shown on page 148.

LOGIC

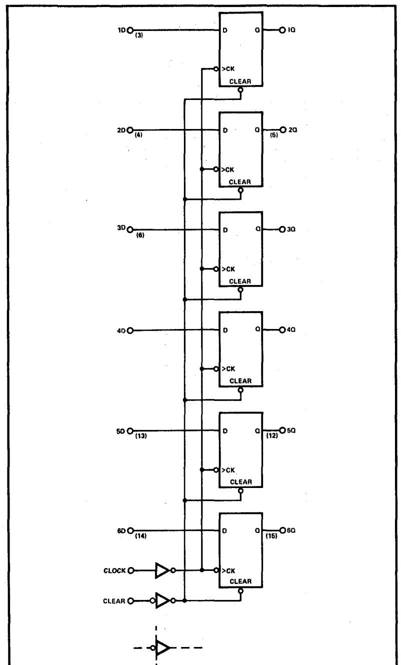
SPEED/PACKAGE AVAILABILITY

54	F,W	74	B
54LS	F,W	74LS	B
		74S	B

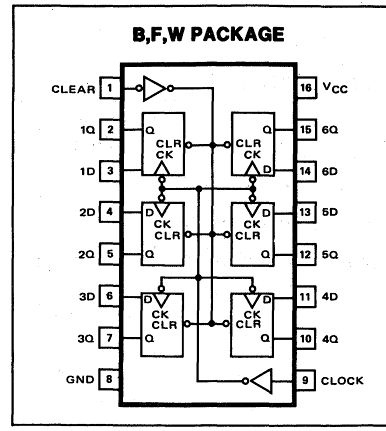
DESCRIPTION

Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the input signal has no effect at the output.

BLOCK DIAGRAM



PIN CONFIGURATION



TRUTH TABLE (Each Flip-Flop)

INPUTS			OUTPUTS
CLEAR	CLOCK	D	Q
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	Q_0

H = high level (steady state)
L = low level (steady state)
X = irrelevant
↑ = transition from low to high level
Q_0 = the level of Q before the indicated steady-state input conditions were established

SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

TEST CONDITIONS				54/74 C_L=15pF R_L=400Ω			54/74LS C_L=15pF R_L=2kΩ			54/74S C_L=15pF R_L=280Ω			
PARAMETER		FROM INPUT	TO OUTPUT	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
f_{Clock}	Clock frequency			25	35		30	40		75	110		MHz
t_W	Width of pulse Clock Clear			20			20			12			ns
t_{Setup}	Input setup time												ns
	Data			20			20↑			8			
	Clear inactive			25			25↑			15			
t_{Hold}	Input hold time			0			5↑			2			ns
Propagation delay time													
t_{PLH}	Low-to-high	Clock			20	30		20	30		9	12	ns
t_{PHL}	High-to-low				21	30		21	35		11	17	
t_{PHL}	High-to-low	Clear	Q		23	35		23	35		13	22	

Load circuit and typical waveforms are shown at the front of section.

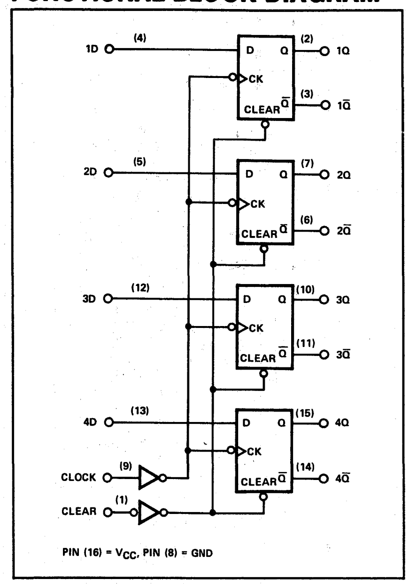
SPEED/PACKAGE AVAILABILITY

54	F,W	74	B
54LS	F,W	74LS	B
		74S	B

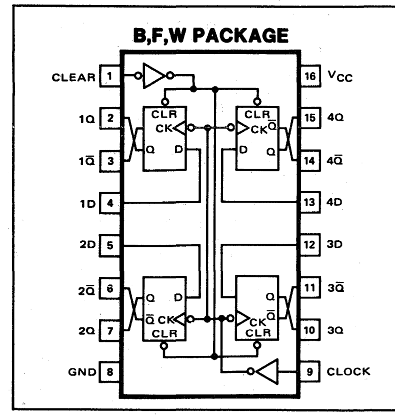
DESCRIPTION

Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



TRUTH TABLE (EACH FLIP-FLOP)

INPUTS			OUTPUTS	
CLEAR	CLOCK	D	Q	$\overline{Q}$
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	L	X	Q_0	$\overline{Q}_0$

H = high level (steady state)
L = low level (steady state)
X = irrelevant
↑ = transition from low to high level
Q_0 = the level of Q before the indicated steady-state input conditions were established

SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

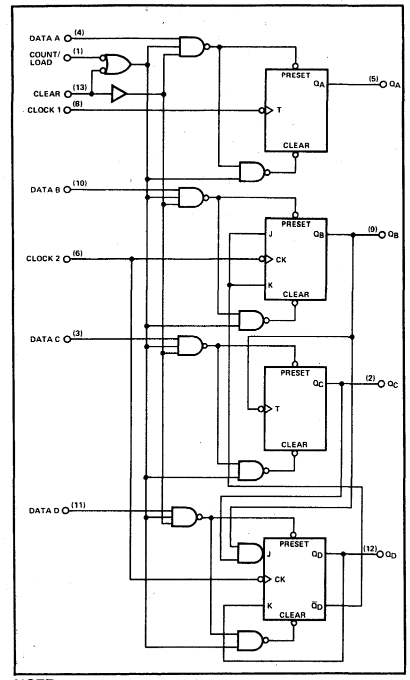
TEST CONDITIONS				54/74 C_L=15pF R_L=400Ω			54/74LS C_L=15pF R_L=2kΩ			54/74S C_L=15pF R_L=280Ω			
PARAMETER		FROM INPUT	TO OUTPUT	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
f_{Clock}	Clock frequency			25	35		30	40		75	110		MHz
t_W	Width of pulse Clock Clear			20			20			12			ns
t_{Setup}	Input setup time												ns
	Data			20			20			8			
	Clear inactive			25			25			15			
t_{Hold}	Input hold time			0			5			2			ns
Propagation delay time													
t_{PLH}	Low-to-high	Clear			16	25		16	25				ns
t_{PHL}	High-to-low				23	35		23	35				
t_{PLH}	Low-to-high	Clock			20	30		20	30		9	12	
t_{PHL}	High-to-low				21	30		21	35		11	17	
t_{PLH}	Low-to-high	Clear	$\overline{Q}$								13	15	
t_{PHL}	High-to-low	Clear	Q								13	22	

Load circuit and typical waveforms are shown at the front of section.

SPEED/PACKAGE AVAILABILITY

54 F,W 74 A

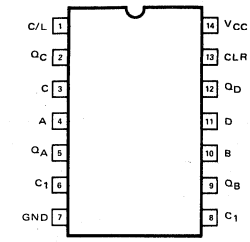
BLOCK DIAGRAM



NOTE:
For electrical specifications, refer to 8280 data sheet.

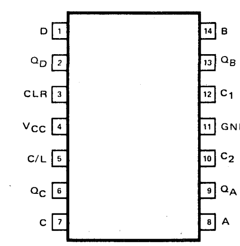
PIN CONFIGURATION

A,F PACKAGE



Asynchronous input:
low input to clear sets Q_A, Q_B, Q_C and Q_D low.

W PACKAGE



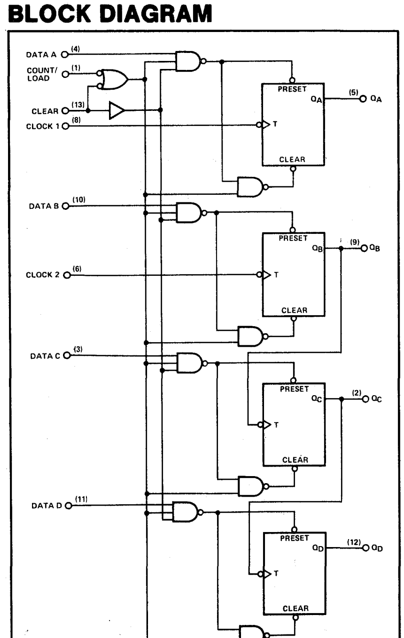
Asynchronous input:
low input to clear sets Q_A, Q_B, Q_C and Q_D low.

PRESETTABLE DECADE AND BINARY COUNTER/LATCH 54/74177

SPEED/PACKAGE AVAILABILITY

54 F,W 74 A

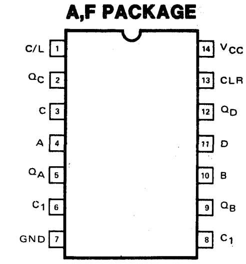
BLOCK DIAGRAM



NOTE:
For electrical specifications, refer to 8281 data sheet.

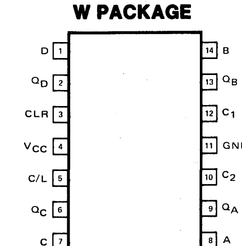
PIN CONFIGURATION

A,F PACKAGE



Asynchronous input:
low input to clear sets Q_A, Q_B, Q_C and Q_D low.

W PACKAGE



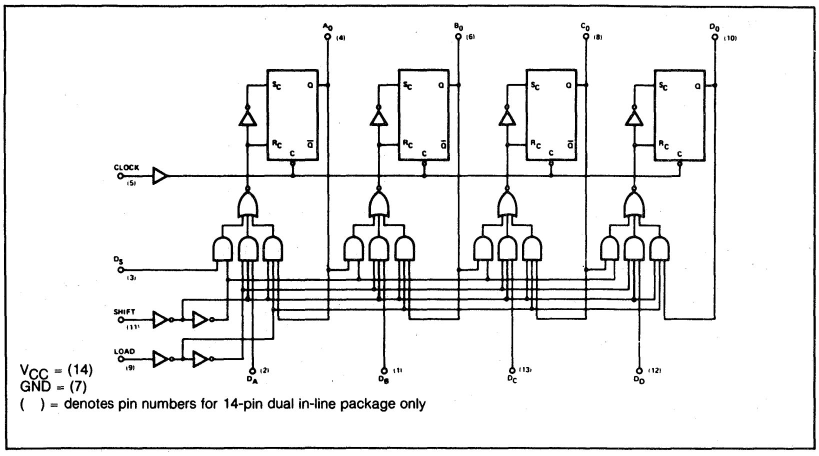
Asynchronous input:
low input to clear sets Q_A, Q_B, Q_C and Q_D low.

4-BIT PARALLEL-ACCESS SHIFT REGISTER 54/74178

SPEED/PACKAGE AVAILABILITY

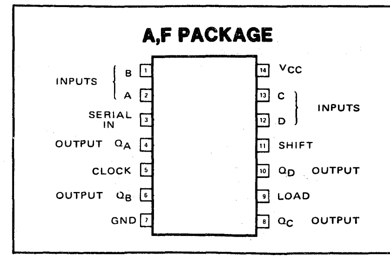
54 F,W 74 A
74S A

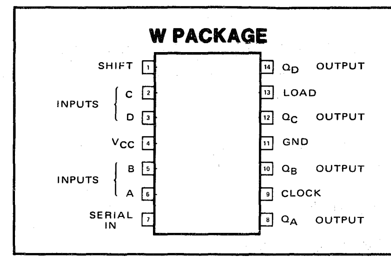
LOGIC DIAGRAM



NOTE:
For electrical specifications, refer to 8270 and 82S70 data sheets.

PIN CONFIGURATION



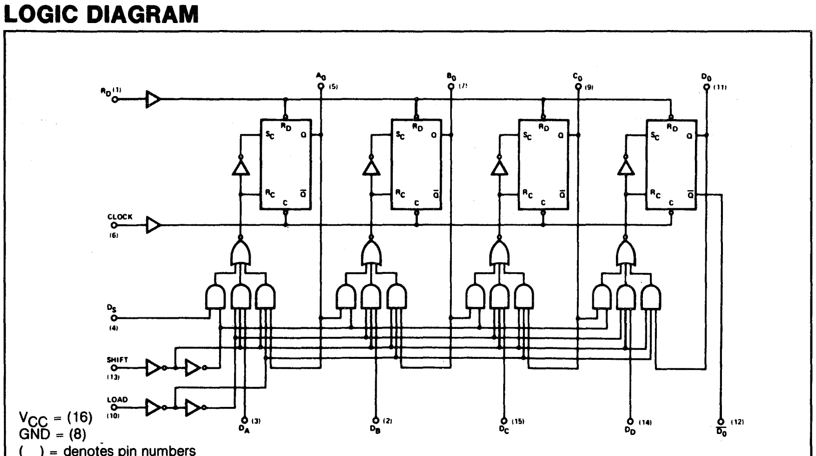


4-BIT PARALLEL-ACCESS SHIFT REGISTER 54/74179

SPEED/PACKAGE AVAILABILITY

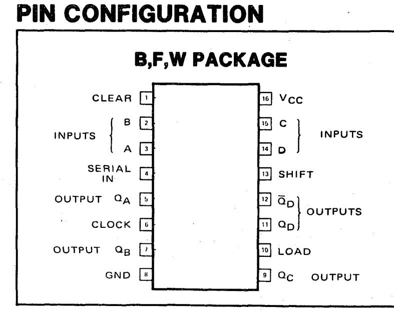
54 F,W 74 B
74S B

LOGIC DIAGRAM



NOTE:
For electrical specifications, refer to 8271 and 82S71 data sheets.

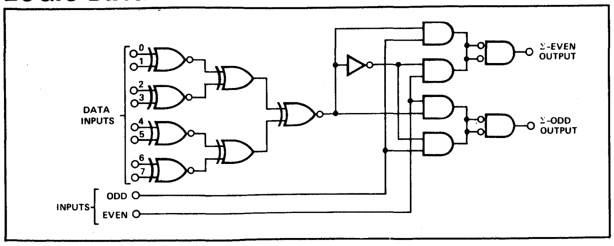
PIN CONFIGURATION



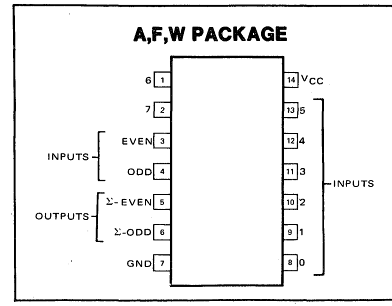
SPEED/PACKAGE AVAILABILITY

54 F,W 74 A

LOGIC DIAGRAM



PIN CONFIGURATION



SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

TEST CONDITIONS				54/74 C_L=15pF R_L=400Ω			
PARAMETER		FROM INPUT	TO OUTPUT	MIN	TYP	MAX	UNIT
Propagation delay time				Odd input = OV			
t_{PLH}	Low-to-high	Data	ΣEven		40	60	ns
t_{PHL}	High-to-low				45	68	
t_{PLH}	Low-to-high	Data	ΣOdd		32	48	
t_{PHL}	High-to-low				25	38	
				Even input = OV			
t_{PLH}	Low-to-high	Data	ΣEven		32	48	
t_{PHL}	High-to-low				25	38	
t_{PLH}	Low-to-high	Data	ΣOdd		40	60	
t_{PHL}	High-to-low				45	68	
t_{PLH}	Low-to-high	Even, Odd	ΣEven,		13	20	
t_{PHL}	High-to-low		ΣOdd		7	10	

Load circuit and typical waveforms are shown at the front of section.

TRUTH TABLE

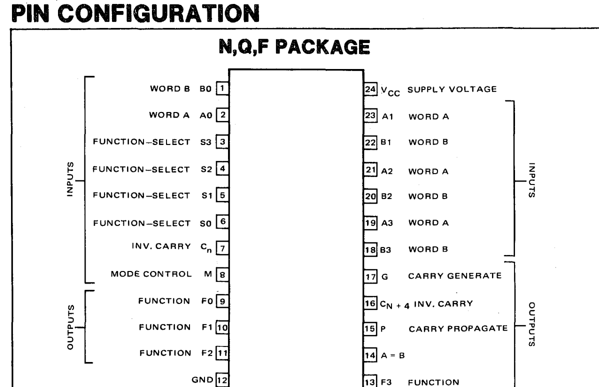
INPUTS			OUTPUTS	
Σ OF 1's AT 0 THRU 7	EVEN	ODD	Σ EVEN	Σ ODD
EVEN	1	0	1	0
ODD	1	0	0	1
EVEN	0	1	0	1
ODD	0	1	1	0
X	1	1	0	0
X	0	0	1	1

X = irrelevant

SPEED/PACKAGE AVAILABILITY

54 Q,F 74 N
54LS Q,F 74LS N
54S Q,F 74S N

PIN CONFIGURATION



TRUTH TABLE

INPUT C_n	OUTPUT C_{n+4}	ACTIVE-HIGH DATA (FIGURE1)	ACTIVE-LOW DATA (FIGURE 2)
H	H	A≤B	A≥B
H	L	A>B	A<B
L	H	A<B	A>B
L	L	A≥B	A≤B

DESCRIPTION

The S54/N74LS181 arithmetic logic unit (ALU)/function generators have a complexity of 75 equivalent gates on a monolithic chip. These circuits perform 16 binary arithmetic operations on two 4-bit words as shown in Tables 1 and 2. These operations are selected by the four function-select lines (S0, S1, S2, S3) and include addition, subtraction, decrement, and straight transfer. When performing arithmetic manipulations, the internal carries must be enabled by applying a low-level voltage to the mode control input (M). A full carry look-ahead scheme is made available in these devices for fast, simultaneous carry generation by means of two cascade-outputs (pins 15 and 17) for the four bits in the package. When used in conjunction with the 182 full carry look-ahead circuit, high-speed arithmetic operations can be performed.

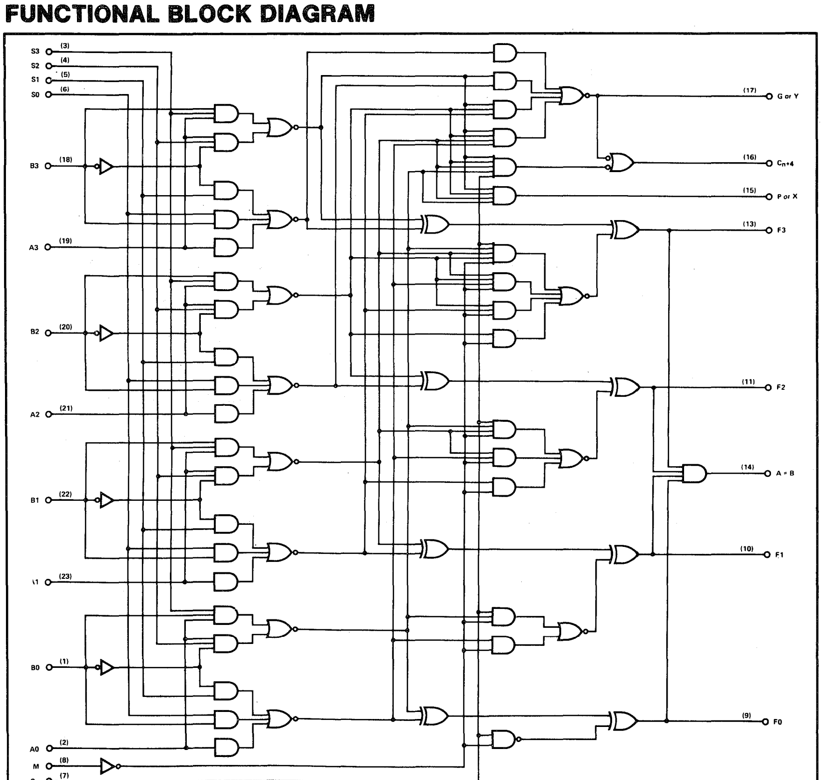
If high speed is not of importance, a ripple-carry input (C_n) and a ripple-carry output (C_n+4) are available. However, the ripple-carry delay has also been minimized so that arithmetic manipulations for small word lengths can be performed without external circuitry.

The S54/N74LS181 will accommodate active-high or active-low data if the pin designations are interpreted as follows: Subtraction is accomplished by 1's complement addition where the 1's complement of the subtrahend is generated internally. The resultant output is A—B—1 which requires an end-around or forced carry to provide A—B.

The S54/74LS181 can also be utilized as a comparator. The A = B output is internally decoded from the function outputs (F0, F1, F2, F3) so that when two words of equal magnitude are applied at the A and B inputs, it will assume a high level to indicate equality (A = B). The ALU should be in the subtract mode with C_n = H when performing this comparison. The A = B output is open-collector so that it can be wire-AND connected to give a comparison for more than four bits. The carry output (C_n+4) can also be used to supply relative magnitude information. Again, the ALU should be placed in the subtract mode by placing the function select inputs S3, S2, S1 S0 at L, H, H, L, respectively.

These circuits have been designed to not only incorporate all of the designer's requirements for arithmetic operations, but also to provide 16 possible functions of two Boolean variables without the use of external circuitry. These logic functions are selected by use of the four function-select inputs (S0, S1, S2, S3) with the mode-control input (M) at a high level to disable the internal carry. The 16 logic functions are detailed in Tables 1 and 2 and include exclusive-OR, NAND, AND, NOR, and OR functions.

FUNCTIONAL BLOCK DIAGRAM



ALU SIGNAL DESIGNATIONS

The S54/N74LS181 can be used with the signal designations of either Figure 1 or Figure 2.

The logic functions and arithmetic operations obtained with signal designations as in Figure 1 are given in Table 1; those obtained with the signal designations of Figure 2 are given in Table 2.

PIN NUMBER	2	1	23	22	21	20	19	18	9	10	11	13	7	16	15	17
Active-high data (Table 1)	A_0	B_0	A_1	B_1	A_2	B_2	A_3	B_3	F_0	F_1	F_2	F_3	$\bar{C}_n$	$\bar{C}_{n+4}$	X	Y
Active-low data (Table 2)	$\bar{A}_0$	$\bar{B}_0$	$\bar{A}_1$	$\bar{B}_1$	$\bar{A}_2$	$\bar{B}_2$	$\bar{A}_3$	$\bar{B}_3$	$\bar{F}_0$	$\bar{F}_1$	$\bar{F}_2$	$\bar{F}_3$	C_n	C_{n+4}	$\bar{P}$	$\bar{G}$

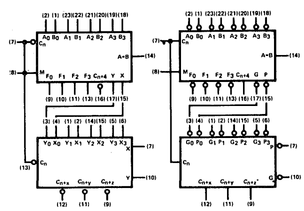


FIGURE 1 (FOR TABLE 1)

FIGURE 2 (FOR TABLE 2)

TABLE 1

SELECTION				ACTIVE-HIGH DATA		
				M=H LOGIC FUNCTIONS	M=L: ARITHMETIC OPERATIONS	
S3	S2	S1	S0		C_n=H (NO CARRY)	C_n=L (WITH CARRY)
L	L	L	L	$F=\bar{A}$	F=A	F=A PLUS 1
L	L	L	H	$F=\overline{A+B}$	F=A+B	F=(A+B) PLUS 1
L	L	H	L	$F=\bar{A}B$	$F=A+\bar{B}$	$F=(A+\bar{B})$ PLUS 1
L	L	H	H	F=0	F=MINUS 1 (2's COMPL)	F=ZERO
L	H	L	L	$F=\overline{AB}$	F=A PLUS $A\bar{B}$	F=A PLUS $A\bar{B}$ PLUS 1
L	H	L	H	$F=\bar{B}$	F=(A+B) PLUS $A\bar{B}$	F=(A-B) PLUS $A\bar{B}$ PLUS 1
L	H	H	L	$F= A \oplus B$	F=A MINUS B MINUS 1	F= A MINUS B
L	H	H	H	$F=A\bar{B}$	$F=A\bar{B}$ MINUS 1	$F=A\bar{B}$
H	L	L	L	$F=\bar{A}+B$	F=A PLUS AB	F=A PLUS AB PLUS 1
H	L	L	H	$F=\overline{A \oplus B}$	F=A PLUS B	F=A PLUS B PLUS 1
H	L	H	L	F=B	$F=(A+\bar{B})$ PLUS AB	$F=(A+\bar{B})$ PLUS AB PLUS 1
H	L	H	H	F=AB	F=AB MINUS 1	F=AB
H	H	L	L	F=1	F=A PLUS A*	F=A PLUS A PLUS 1
H	H	L	H	$F=A+\bar{B}$	F=(A+B) PLUS A	F=(A+B) PLUS A PLUS 1
H	H	H	L	F=A+B	$F=(A+\bar{B})$ PLUS A	$F=(A+\bar{B})$ PLUS A PLUS 1
H	H	H	H	F=A	F=A MINUS 1	F=A

*Each bit is shifted to the next more significant position.

TABLE 2

SELECTION				ACTIVE-LOW DATA		
				M=H LOGIC FUNCTIONS	M=L: ARITHMETIC OPERATIONS	
S3	S2	S1	S0		C_n=L (NO CARRY)	C_n=H (WITH CARRY)
L	L	L	L	$F=\overline{A}$	F=A MINUS 1	F=A
L	L	L	H	$F=\overline{AB}$	F=AB MINUS 1	F=AB
L	L	H	L	$F=\overline{A}+B$	$F=A\overline{B}$ MINUS 1	$F=A\overline{B}$
L	L	H	H	F=1	F=MINUS 1 (2's COMPL)	F=ZERO
L	H	L	L	$F=\overline{A+B}$	$F=A$ PLUS $(A+\overline{B})$	$F=A$ PLUS $(A+\overline{B})$ PLUS 1
L	H	L	H	$F=\overline{B}$	$F=AB$ PLUS $(A+\overline{B})$	$F=AB$ PLUS $(A+\overline{B})$ PLUS 1
L	H	H	L	$F=\overline{A \oplus B}$	F=A MINUS B MINUS 1	F=A MINUS B
L	H	H	H	$F=A+\overline{B}$	$F=A+\overline{B}$	$F=(A+\overline{B})$ PLUS 1
H	L	L	L	$F=\overline{A}B$	F=A PLUS (A+B)	F=A PLUS (A+B) PLUS 1
H	L	L	H	$F=A \oplus B$	F=A PLUS B	F=A PLUS B PLUS 1
H	L	H	L	F=B	$F=A\overline{B}$ PLUS (A+B)	$F=A\overline{B}$ PLUS (A+B) PLUS 1
H	L	H	H	F=A+B	F=A+B	F=(A+B) PLUS 1
H	H	L	L	F=0	F=A PLUS A*	F=A PLUS A PLUS 1
H	H	L	H	$F=A\overline{B}$	F=AB PLUS A	F=AB PLUS A PLUS 1
H	H	H	L	F=AB	$F=A\overline{B}$ PLUS A	$F=A\overline{B}$ PLUS A PLUS 1
H	H	H	H	F=A	F=A	F=A PLUS 1

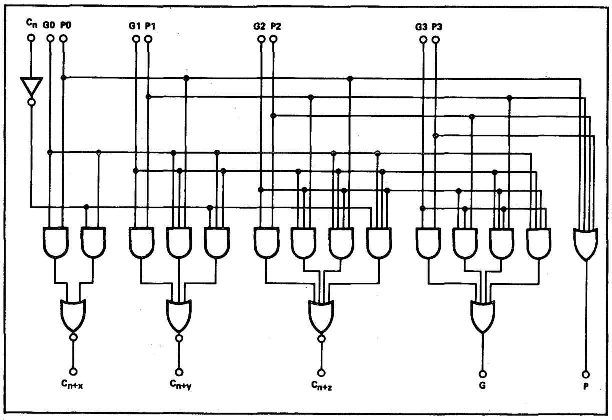
LOGIC

SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

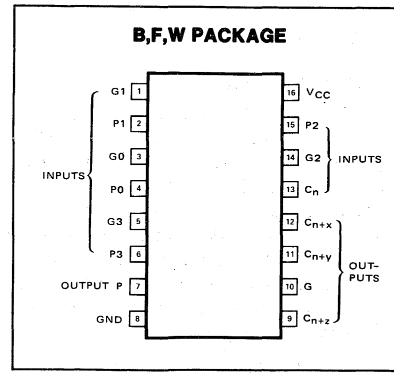
TEST CONDITIONS			54/74 M=0V S0=S3=4.5V S1=S2=0V *S0=S3=0V *S1=S2=4.5V			54/74LS M=0V S0=S3=4.5V S1=S2=0V *S0=S3=0V *S1=S2=4.5V			54/74S M=0V S0=S3=4.5V S1=S2=0V *S0=S3=0V *S1=S2=4.5V			
PARAMETER	FROM INPUT	TO OUTPUT	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
Propagation delay time												
t_{PLH} Low-to-high	C_n	C_{N+4}		12	18		18	27		7	10.5	ns
t_{PHL} High-to-low				13	19		13	20		7	10.5	
t_{PLH} Low-to-high	C_n	Any F		13	19		17	26		7	12	
t_{PHL} High-to-low	SUM or DIFF Mode			12	18		13	20		7	12	
t_{PLH} Low-to-high	Any A, B SUM Mode	G		13	19		19	29		8	12	
t_{PHL} High-to-low				13	19		15	23		7.5	12	
t_{PLH} Low-to-high	*Any A,B DIFF Mode	G		17	25		21	32		10.5	15	
t_{PHL} High-to-low				17	25		17	26		10.5	15	
t_{PLH} Low-to-high	Any A,B SUM Mode	P		13	19		20	30		7.5	12	
t_{PHL} High-to-low				17	25		20	30		7.5	12	
t_{PLH} Low-to-high	*Any A,B DIFF Mode	P		17	25		20	30		10.5	15	
t_{PHL} High-to-low				17	25		22	33		10.5	15	
t_{PLH} Low-to-high	Any A,B SUM Mode	Any F		28	42					11	16.5	
t_{PHL} High-to-low				21	32					11	16.5	
t_{PLH} Low-to-high	*Any A,B DIFF Mode	Any F		32	48					14	20	
t_{PHL} High-to-low				23	34					14	22	
t_{PLH} Low-to-high	*Any A,B DIFF Mode	A = B		35	50		33	50		15	23	
t_{PHL} High-to-low				32	48		41	62		20	30	
t_{PLH} Low-to-high	Any A,B SUM Mode	C_{n+4}					25	38		12.5	18.5	
t_{PHL} High-to-low							25	38		12.5	18.5	
t_{PLH} Low-to-high	*Any A,B DIFF Mode	C_{n+4}					27	41		15.5	23	
t_{PHL}							27	41		15.5	23	
t_{PLH} Low-to-high	A_i,B_i	F_i					21	32				
t_{PHL} High-to-low	SUM Mode						13	20				
t_{PLH} Low-to-high	*A_i,B_i	F_i					21	32				
t_{PHL} High-to-low	DIFF Mode						15	23				
			M=4.5V						M=4.5V			
t_{PLH} Low-to-high	Any A,B Logic Mode	Any F		32	48					14	20	
t_{PHL} High-to-low				23	34					14	22	
						M = 4.5V						
t_{PLH} Low-to-high	A_i,B_i	F_i					22	33				
t_{PHL} High-to-low	Logic Mode						19	29				

Load circuit and typical waveforms are shown at the front of section.

LOGIC DIAGRAM



PIN CONFIGURATION

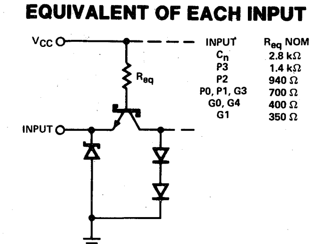


PIN DESIGNATIONS

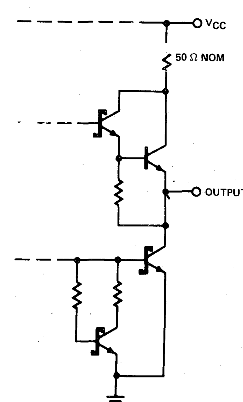
DESIGNATION	PIN NOS.	FUNCTION
G0, G1, G2, G3	3, 1, 14, 5	Active-Low Carry Generate Inputs
P0, P1, P2, P3	4, 2, 15, 6	Active-Low Carry Propagate Inputs
C_n	13	Carry Input
C_{n+x}, C_{n+y}, C_{n+z}	12, 11, 9	Carry Outputs
G	10	Active-Low Carry Generate Output
P	7	Active-Low Carry Propagate Output
V_{CC}	16	Supply Voltage
GND	8	Ground

INPUT/OUTPUT SCHEMATICS

EQUIVALENT OF EACH INPUT



TYPICAL OF ALL OUTPUTS



SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

TEST CONDITIONS			54/74 C_L=15pF R_L=400Ω			54/74S C_L=15pF R_L=280Ω			
PARAMETER	FROM INPUT	TO OUTPUT	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
Propagation delay time									
t_{PLH} Low-to-high				11	17				ns
t_{PHL} High-to-low				15	22				
t_{PLH} Low-to-high	G0,G1,G2, G3,P0,P1, P2, P3	C_{n+x}, C_{n+y}, C_{n+z}					4.5	7	
t_{PHL} High-to-low							4.5	7	
t_{PLH} Low-to-high	G0,G1,G2, G3,P1,P2, P3	G					5	7.5	
t_{PHL} High-to-low							7	10.5	
t_{PLH} Low-to-high	P0,P1,P2 P3	P					4.5	6.5	
t_{PHL} High-to-low							6.5	10	
t_{PLH} Low-to-high	C_n	C_{n+x}, C_{n+y}, C_{n+z}					6.5	10	
t_{PHL} High-to-low							7	10.5	

Load circuit and typical waveforms are shown at the front of section.

SPEED/PACKAGE RELIABILITY

54	F,W	74	B
54S	F,W	74S	B

LOGIC

SPEED/PACKAGE AVAILABILITY

54	F,W	74	B
54LS	F,W	74LS	B

DESCRIPTION

The 54/74LS190 is a synchronous, reversible up/down counter having a complexity of 58 equivalent gates. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the steering logic. This mode of operation eliminates the output counting spikes normally associated with asynchronous (ripple clock) counters.

The outputs of the four master-slave flip-flops are triggered on a low-to-high-level transition of the clock input if the enable input is low. A high at the enable input inhibits counting. Level changes at either the enable input or the down/up input should be made only when the clock input is high. The direction of the count is determined by the level of the down/up input. When low, the counter counts up and when high, it counts down.

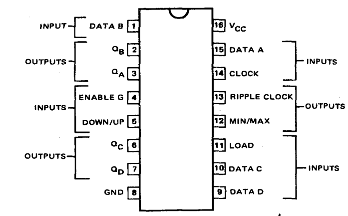
These counters are fully programmable; that is, the outputs may be preset to either level by placing a low on the load input and entering the desired data at the data inputs. The output will change to agree with the data inputs independently of the level of the clock input. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs.

The clock, down/up, and load inputs are buffered to lower the drive requirement which significantly reduces the number of clock drivers, etc., required for long parallel words.

Two outputs have been made available to perform the cascading function: ripple clock and maximum/minimum count. The latter output produces a high-level output pulse with a duration approximately equal to one complete cycle of the clock when the counter overflows or underflows. The ripple clock output produces a low-level output pulse equal in width to the low-level portion of the clock input when an overflow or underflow condition exists. The counters can be easily cascaded by feeding the ripple clock output to the enable input of the succeeding counter if parallel clocking is used, or to the clock input if parallel enabling is used. The maximum/minimum count output can be used to accomplish look-ahead for high-speed operation.

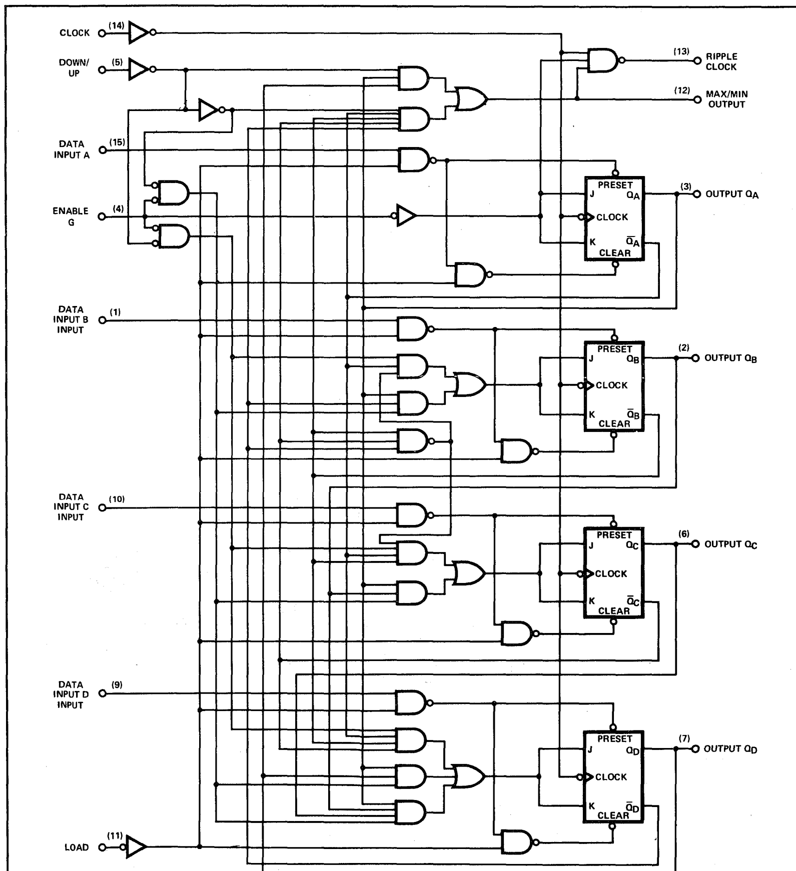
PIN CONFIGURATION

B,F,W PACKAGE



asynchronus inputs: low input to load sets Q_A=A, Q_B=B, Q_C=C, Q_D=D

BLOCK DIAGRAM



SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

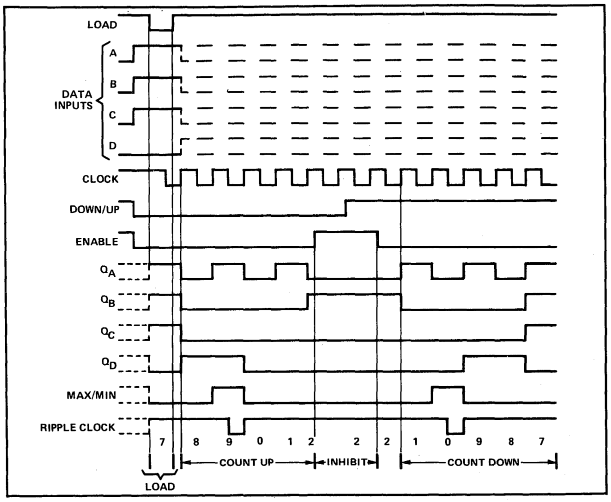
TEST CONDITIONS			54/74 C_L=15pF R_L=400Ω			54/74LS C_L=15pF R_L=2KΩ			
PARAMETER	FROM INPUT	TO OUTPUT	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
f_{Clock} Clock frequency						20	25		MHz
f_{max}			20	25					MHz
$t_{w(Clock)}$ Width of clock input pulse			25			25			ns
$t_{w(Load)}$			35			35			ns
$t_{Setup(D)}$ Input setup time			20			20↑			ns
$t_{Hold(D)}$ Input hold time			0			0↑			ns
t_{Enable} Enable time to cycle						20↑			ns
Propagation delay time									
t_{PLH} Low-to-high	Load	Q_A, Q_B, Q_C, Q_D		22	33		22	33	ns
t_{PHL} High-to-low				33	50		33	50	
t_{PLH} Low-to-high	Data A, B, C, D	Q_A, Q_B, Q_C, Q_D		14	22		14	22	
t_{PHL} High-to-low				35	50		35	50	
t_{PLH} Low-to-high	Clock	Ripple Clock		13	20		13	20	
t_{PHL} High-to-low				16	24		16	24	
t_{PLH} Low-to-high	Clock	Q_A, Q_B, Q_C, Q_D		16	24		16	24	
t_{PHL} High-to-low				24	36		24	36	
t_{PLH} Low-to-high	Clock	Max/Min		28	42		28	42	
t_{PHL} High-to-low				37	52		37	52	
t_{PLH} Low-to-high	Down/Up	Ripple Clock		30	45		30	45	
t_{PHL} High-to-low				30	45		30	45	
t_{PLH} Low-to-high	Down/Up	Max/Min		21	33		21	33	
t_{PHL} High-to-low				22	33		22	33	
t_{PLH} Low-to-high	Enable E	Ripple Clock					21	33	
t_{PHL} High-to-low							22	33	

PARAMETER MEASUREMENT INFORMATION

TYPICAL LOAD, COUNT, AND INHIBIT SEQUENCES

Illustrated below is the following sequence:

1. Load (preset) to BCD seven.
2. Count up to eight, nine (maximum), zero, one, and two.
3. Inhibit.
4. Count down to one, zero (minimum), nine, eight, and seven.



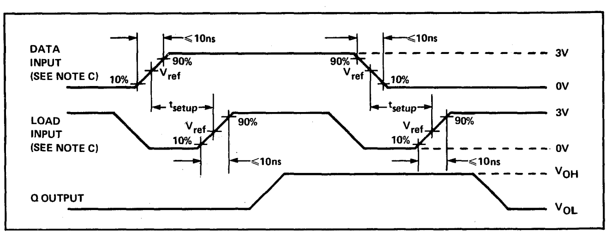
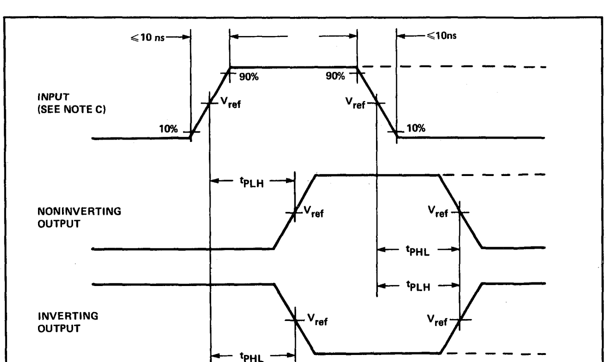


FIGURE 1 — DATA SETUP TIME VOLTAGE WAVEFORMS

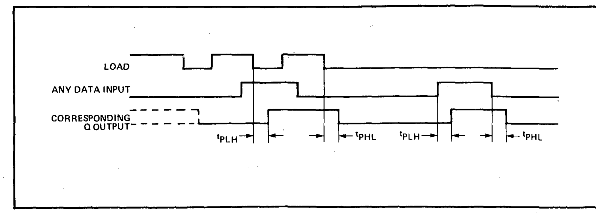
NOTES:

A. C_L includes probe and jig capacitance.
B. All diodes are 1N3064.
C. The input pulses are supplied by generators having the following characteristics: Z_{out} = 50 Ω, duty cycle ≤ 50%, PRR ≤ 1 MHz.
D. V_{ref} = 1.3V.



See waveform sequences in figures 3 through 6 for propagation times from a specific input to a specific output. For simplification, pulse rise times, reference levels, etc., have not been shown in figures 3 through 6.

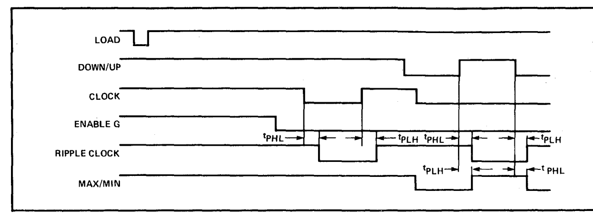
FIGURE 2 — GENERAL VOLTAGE WAVEFORMS FOR PROPAGATION TIMES



NOTE:

E. Conditions on other inputs are irrelevant.

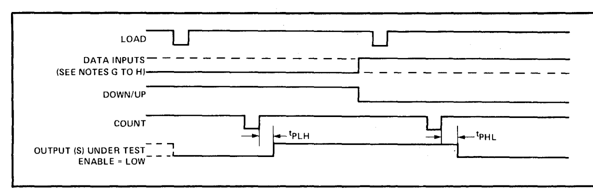
FIGURE 3 — LOAD TO OUTPUT AND DATA TO OUTPUT



NOTE:

F. All data inputs are low.

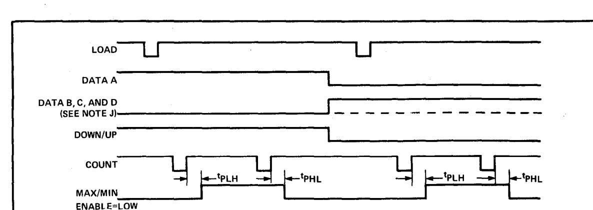
FIGURE 4 — ENABLE TO RIPPLE CLOCK, CLOCK TO RIPPLE CLOCK, DOWN/UP TO RIPPLE CLOCK, AND DOWN/UP TO MAX/MIN



NOTES:

G. To test Q_A, Q_B, and Q_C outputs: Data inputs A, B, and C are shown by the solid line. Data input D is shown by the dashed line.
H. To test Q_D output: Data inputs A and D are shown by the solid line. Data inputs B and C are held at the low logic level.

FIGURE 5 — CLOCK TO OUTPUT



NOTE:

J. Data inputs B and C are shown by the dashed line. Data input D is shown by the solid line.

FIGURE 6 — CLOCK TO MAX/MIN

SPEED/PACKAGE AVAILABILITY

54	F,W	74	B
54S	F,W	74S	B

DESCRIPTION

The 54/74LS191 is a synchronous, reversible binary up/down counter having a complexity of 58 equivalent gates. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the steering logic. This mode of operation eliminates the output counting spikes normally associated with asynchronous (ripple clock) counters.

The outputs of the four master-slave flip-flops are triggered on a low-to-high-level transition of the clock input if the enable input is low. A high at the enable input inhibits counting. Level changes at either the enable input or the down/up input should be made only when the clock input is high. The direction of the count is determined by the level of the down/up input. When low, the counter counts up and when high, it counts down.

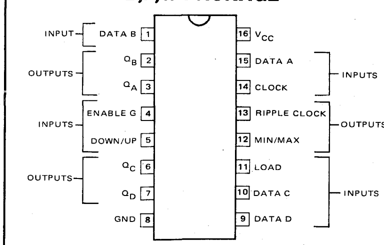
These counters are fully programmable; that is, the outputs may be preset to either level by placing a low on the load input and entering the desired data at the data inputs. The output will change to agree with the data inputs independently of the level of the clock input. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs.

The clock, down/up, and load inputs are buffered to lower the drive requirement which significantly reduces the number of clock drivers, etc., required for long parallel words.

Two outputs have been made available to perform the cascading function: ripple clock and maximum/minimum count. The latter output produces a high-level output pulse with a duration approximately equal to one complete cycle of the clock when the counter overflows or underflows. The ripple clock output produces a low-level output pulse equal in width to the low-level portion of the clock input when an overflow or underflow condition exists. The counters can be easily cascaded by feeding the ripple clock output to the enable input of the succeeding counter if parallel clocking is used, or to the clock input if parallel enabling is used. The maximum/minimum count output can be used to accomplish look-ahead for high-speed operation.

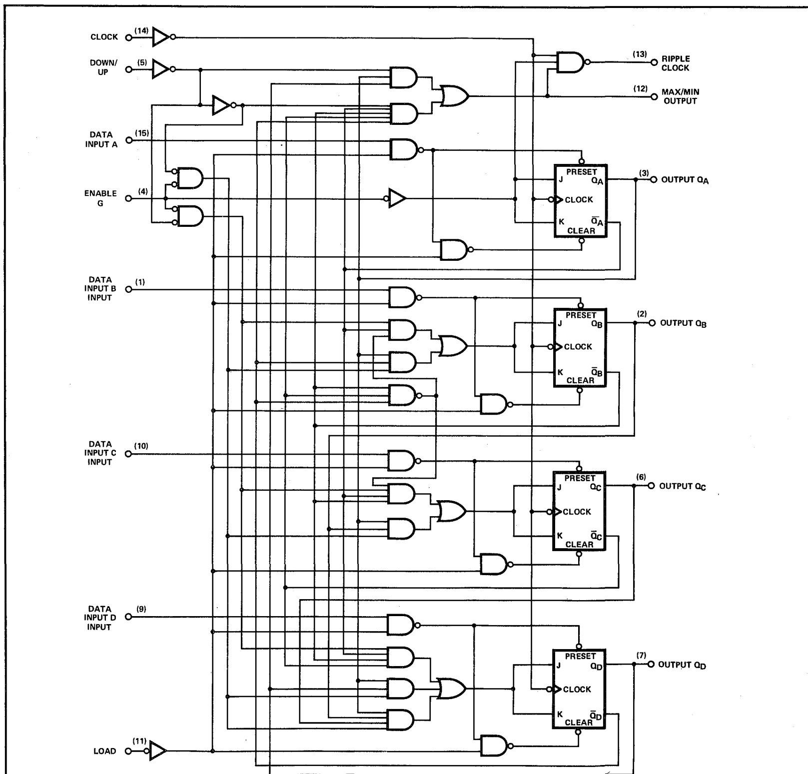
PIN CONFIGURATION

B,F,W PACKAGE



asynchronous inputs: low input to load sets Q_A=A, Q_B=B, Q_C=C, Q_D=D

BLOCK DIAGRAM



LOGIC

SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

PARAMETER		FROM INPUT	TO OUTPUT	TEST CONDITIONS	54/74 CL=15pf RL=400Ω MIN	54/74 TYP	54/74 MAX	54/74LS CL=15pf TL=2KΩ MIN	54/74LS TYP	54/74LS MAX	UNIT
f_{Clock}	Input clock frequency				20			20	25		MHz
$t_{w(Clock)}$	Width of clock input pulse				25			25			ns
$t_{w(Load)}$	Width of load input pulse				35			35			ns
t_{setup}	Input setup time				20			20↑			ns
t_{Hold}	Input hold time				0			0↑			ns
t_{Enable}	Enable time to cycle							20↑			
t_{PLH}		Load	Q_A,Q_B, Q_Q,Q_D			22	33		22	33	ns
t_{PHL}						33	50		33	50	
t_{PLH}		Data A,B, C,D	Q_A,Q_B, Q_C,Q_D			14	22		14	22	ns
t_{PHL}						35	50		35	50	
t_{PLH}		Clock	Ripple clock			13	20		13	20	ns
t_{PHL}				See Figures 1 and 3 thru 6		16	24		16	24	
t_{PLH}		Clock	Q_A,Q_B, Q_C,Q_D			16	24		16	24	ns
t_{PHL}						24	36		24	36	
t_{PLH}		Clock	Max/min			28	42		28	42	ns
t_{PHL}						37	52		37	52	
t_{PLH}		Down/up	Ripple clock			30	45		30	45	ns
t_{PHL}						30	45		30	45	
t_{PLH}		Down/up	Max/min			21	33		21	33	ns
t_{PHL}						22	33		22	33	
t_{PLH}		Enable	Ripple clock						21	33	ns
t_{PHL}		E							22	33	ns

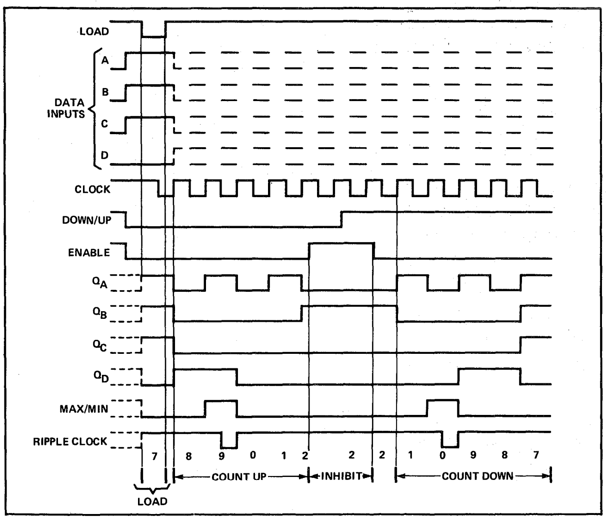
★f_{max}= maximum clock frequency
t_{PLH}= propagation delay time, low-to-high-level output
t_{PHL}= propagation delay time high-to-low-level output

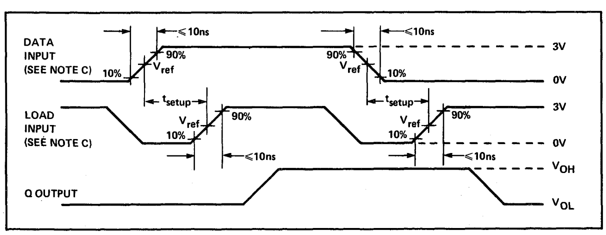
PARAMETER MEASUREMENT INFORMATION

TYPICAL LOAD, COUNT, AND INHIBIT SEQUENCES

Illustrated below is the following sequence:

1. Load (preset) to binary thirteen.
2. Count up to fourteen, fifteen (maximum), zero, one, and two.
3. Inhibit.
4. Count down to one, zero (minimum), fifteen, fourteen, and thirteen.



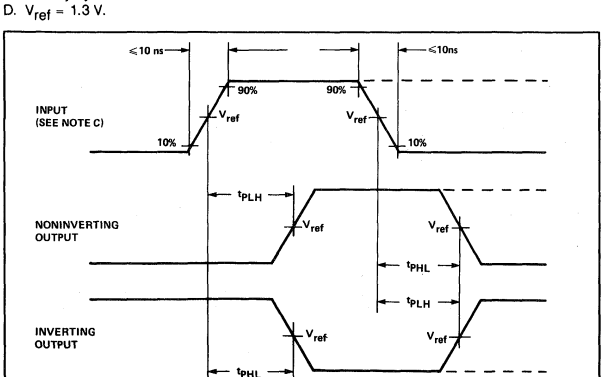


VOLTAGE WAVEFORMS

FIGURE 1 — DATA SETUP TIME VOLTAGE WAVEFORMS

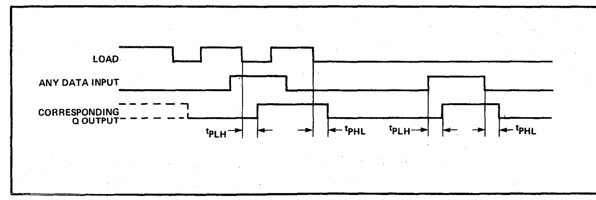
NOTES:

A. C_L includes probe and jig capacitance.
B. All diodes are 1N3064.
C. The input pulses are supplied by generators having the following characteristics: Z_{out} = 50 Ω, duty cycle ≤ 50%, PRR ≤ 1 MHz.
D. V_{ref} = 1.3 V.



See waveform sequences in figures 4 through 7 for propagation times from a specific input to a specific output. For simplification, pulse rise times, reference levels, etc., have not been shown in figures 4 through 7.

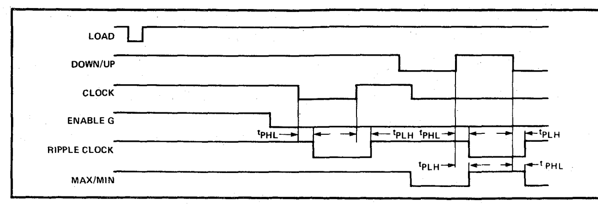
FIGURE 2 — GENERAL VOLTAGE WAVEFORMS FOR PROPAGATION TIMES



NOTE:

E. Conditions on other inputs are irrelevant.

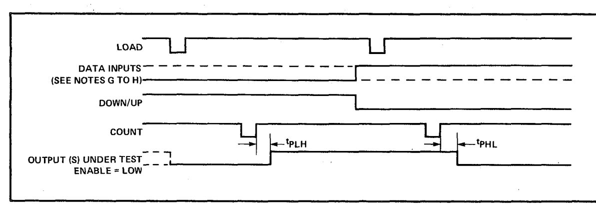
FIGURE 3 — LOAD TO OUTPUT AND DATA TO OUTPUT



NOTE:

F. All data inputs are low.

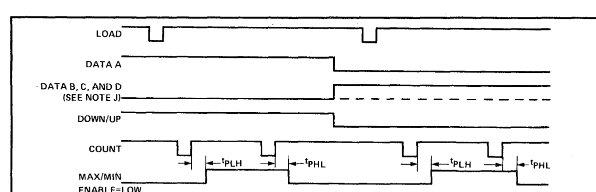
FIGURE 4 — ENABLE TO RIPPLE CLOCK, CLOCK TO RIPPLE CLOCK, DOWN/UP TO RIPPLE CLOCK,



NOTE:

G. To test Q_A, Q_B, Q_C, and Q_D outputs: All four data inputs are shown by the solid line.

FIGURE 5 — CLOCK TO OUTPUT



NOTE:

H. Data inputs B and C are shown by the dashed line for the '190 and 'LS190 and the solid line for the '191 and 'LS191: Data input D is shown by the solid line for both devices.

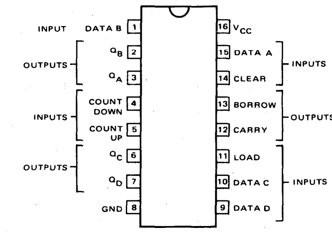
FIGURE 6 — CLOCK TO MAX/MIN

SPEED/PACKAGE AVAILABILITY

54 F,W 74 B
54LS F,W 74LS B

PIN CONFIGURATION

B,F,W PACKAGE



logic: Low input to load sets Q_A = A, Q_B = B, Q_C = C, and Q_D = D

DESCRIPTION

This monolithic circuit is a synchronous reversible (up/down) counter having a complexity of 55 equivalent gates. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincidently with each other when so instructed by the steering logic. This mode of operation eliminates the output counting spikes which are normally associated with asynchronous (ripple-clock) counters.

The outputs of the four master-slave flip-flops are triggered by a low-to-high-level transition of either count (clock) input. The direction of counting is determined by which count inputs is pulsed while the other count input is high.

All four counters are fully programmable; that is, each output may be preset to either level by entering the desired data at the data inputs while the load input is low. The output will change to agree with the data inputs independently of the count pulses. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs.

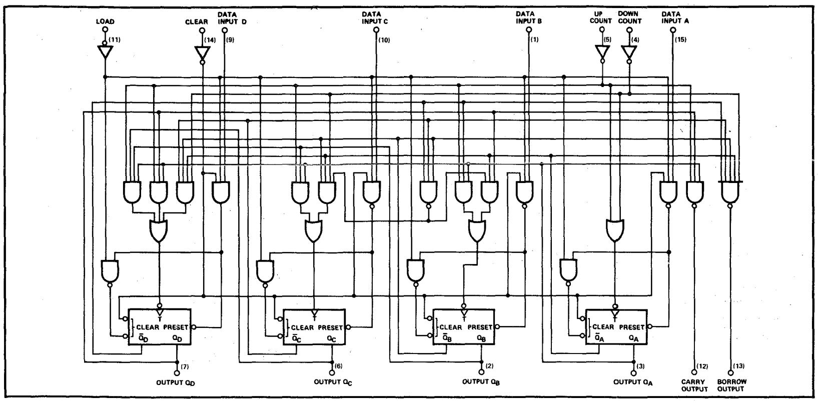
A clear input has been provided which forces all outputs to the low level when a high level is applied. The clear function is independent of the count and load inputs. The clear, count, and load inputs are buffered to lower the drive requirements. This reduces the number of clock drivers, etc., required for long words.

These counters were designed to be cascaded without the need for external circuitry. Both borrow and carry outputs are available to cascade both the up- and down-counting functions. The borrow output produces a pulse equal in width to the count-down input when the counter underflows. Similarly, the carry output produces a pulse equal in width to the count-down input when an overflow condition exists. The counters can then be easily cascaded by feeding the borrow and carry outputs to the count-down and count-up inputs respectively of the succeeding counter.

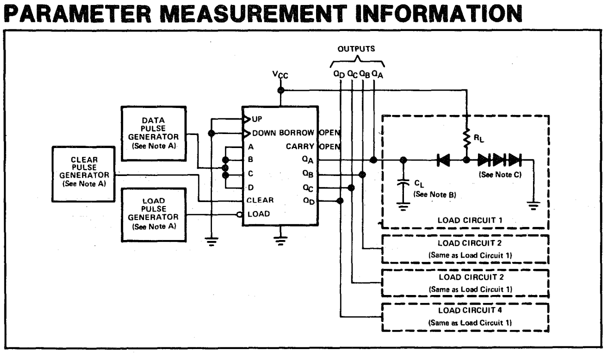
SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

TEST CONDITIONS			54/74 C_L=15pF R_L=400Ω			54/74LS C_L=15pF R_L=2k			
PARAMETER	FROM INPUT	TO OUTPUT	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
f_{Count}	Count Up	Carry	25	32		25	32		MHz
t_W Width of pulse						20			ns
t_{Setup} Input setup time						20↑			ns
t_{Hold} Input hold time						0↑			ns
Propagation delay time									
t_{PLH} Low-to-high	Count up	Carry		17	26		17	26	ns
	Count Down	Borrow		16	24		16	24	
	Either Count	Q		25	38		25	38	
	Load	Q		27	40		27	40	
t_{PHL} High-to-low	Count Up	Carry		16	24		16	24	ns
	Count Down	Borrow		16	24		16	24	
	Either Count	Q		31	47		31	47	
	Load	Q		29	40		29	40	
	Clear	Q		22	35		22	35	

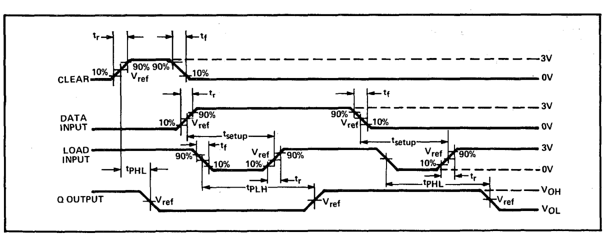
BLOCK DIAGRAM



PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES:

A. The pulse generators have the following characteristics: $Z_{out} \approx 50\ \Omega$, and for the data pulse generator PRR $\leq$ 500 kHz, duty cycle = 50%; for the load pulse generator PRR is two times data PRR, duty cycle = 50%.

B. C_L includes probe and jig capacitance.

C. Diodes are 1N3064.

D. t_r and $t_f \leq 7$ ns

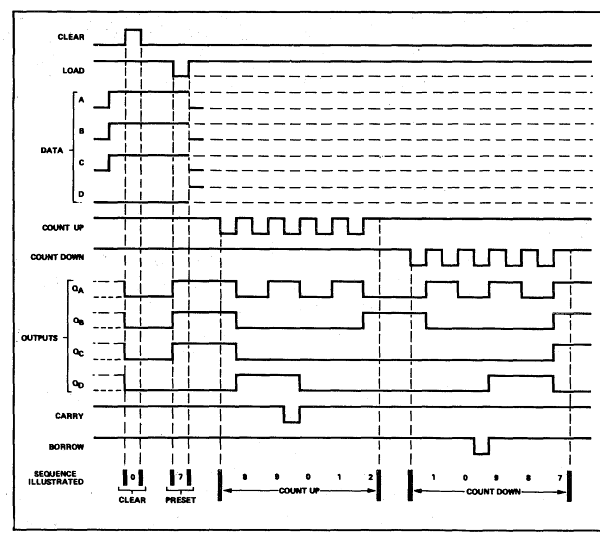
E. V_{ref} is 1.3 volts

FIGURE 1—CLEAR, SETUP, AND LOAD TIMES

TYPICAL CLEAR, LOAD, AND COUNT SEQUENCES

Illustrated below is the following sequence:

1. Clear outputs to zero.
2. Load (preset) to BCD seven.
3. Count up to eight, nine, carry, zero, one, and two.
4. Count down to one, zero, borrow, nine, eight, and seven.

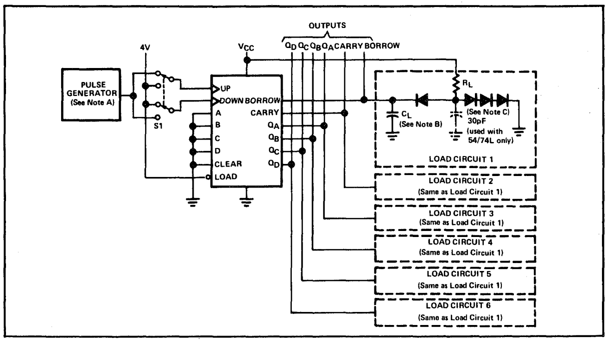


NOTES:

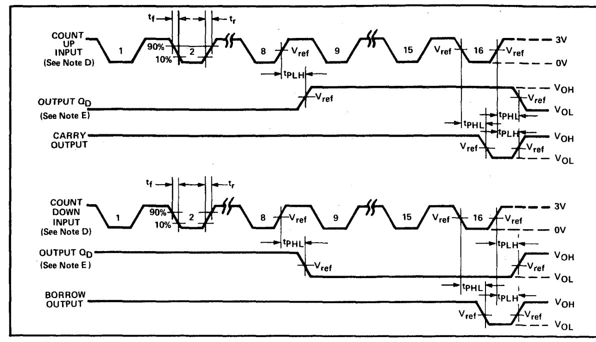
A. Clear overrides load, data, and count inputs.

B. When counting up, count-down input must be high; when counting down, count-up input must be high.

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES:

A. The pulse generator has the following characteristics: PRR ≤ 1 MHz, $Z_{out} \approx 50\ \Omega$, duty cycle = 50%.
B. C_L includes probe and jig capacitance.
C. Diodes are 1N3064
D. Count cycle is 1 through 10.
E. Waveforms for outputs Q_A, Q_B, and Q_C are omitted to simplify the drawing.
F. t_r and $t_f \leq 7$ ns
G. V_{ref} is 1.3 volts

FIGURE 2—PROPAGATION DELAY TIMES

SYNCHRONOUS 4-BIT BINARY UP/DOWN COUNTER 54/74193

SPEED/PACKAGE AVAILABILITY

54	F,W	74	B
54LS	F,W	74LS	B

DESCRIPTION

This monolithic circuit is a synchronous reversible (up/down) counter having a complexity of 55 equivalent gates. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincidently with each other when so instructed by the steering logic. This mode of operation eliminates the output counting spikes which are normally associated with asynchronous (ripple-clock) counters.

The outputs of the four master-slave flip-flops are triggered by a low-to-high-level transition of either count (clock) input. The direction of counting is determined by which count inputs is pulsed while the other count input is high.

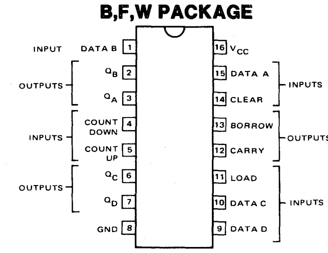
All four counters are fully programmable; that is, each output may be preset to either level by entering the desired data at the data inputs while the load input is low. The output will change to agree with the data inputs independently of the count pulses. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs.

A clear input has been provided which forces all outputs to the low level when a high level is applied. The clear function is independent of the count and load inputs. The clear, count, and load inputs are buffered to lower the drive requirements. This reduces the number of clock drivers, etc., required for long words.

These counters were designed to be cascaded without the need for external circuitry. Both borrow and carry outputs are available to cascade both the up- and down-counting functions. The borrow output produces a pulse equal in width to the count-down input when the counter underflows. Similarly, the carry output produces a pulse equal in width to the count-down input when an overflow condition exists. The counters can then be easily cascaded by feeding the borrow and carry outputs to the count-down and count-up inputs respectively of the succeeding counter.

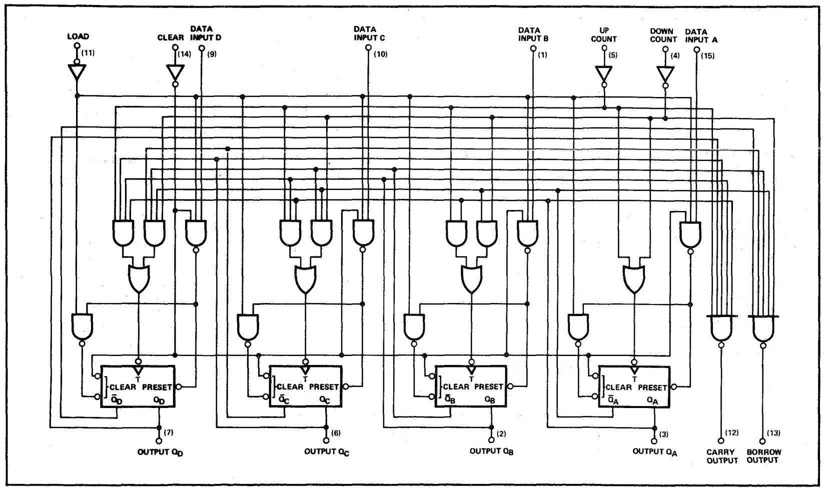
PIN CONFIGURATION

B,F,W PACKAGE



logic: Low input to load sets Q_A = A, Q_B = B, Q_C = C, and Q_D = D

BLOCK DIAGRAM

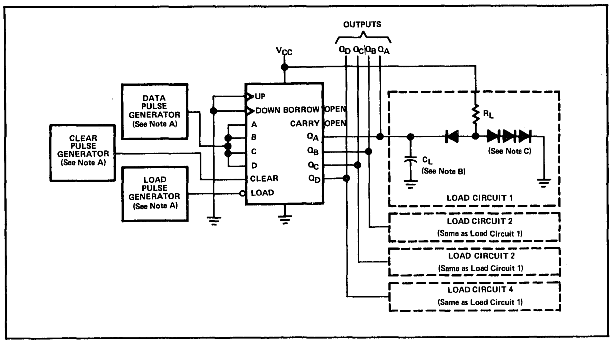


SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

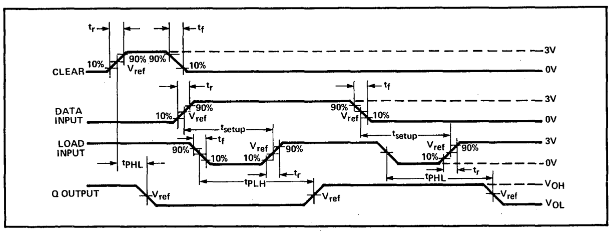
PARAMETER*		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	54/74 C_L=15pf R_L=400Ω MIN	54/74 TYP	54/74 MAX	54/74S C_L=15pf R_L=2k MIN	54/74S TYP	54/74S MAX	UNIT
f_{Count}					25	32		25	32		MHz
t_w	Input pulse width				20			20			ns
t_{Set-up}	Input setup time				20			20↑			ns
t_{Hold}	Input hold time				0			0↑			ns
t_{PLH} t_{PHL}		Count-up	Carry			17 16	26 24		17 16	26 24	ns
t_{PLH} t_{PHL}		Count-down	Borrow			16 16	24 24		16 16	24 24	ns
t_{PLH} t_{PHL}		Either-count	Q	See Figures 1 and 2		25 31	38 47		25 31	38 47	ns
t_{PLH} t_{PHL}		Load	Q			27 29	40 40		27 29	40 40	ns
t_{PHL}		Clear	Q			22	35		22	35	ns

*t_{max} = maximum clock frequency
t_{PLH} = propagation delay time, low-to-high-level output
t_{PHL} = propagation delay time, high-to-low-level output

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES:

A. The pulse generators have the following characteristics: $Z_{out} \approx 50\ \Omega$ and for the data pulse generator PRR ≤ 500 kHz, duty cycle = 50%; for the load pulse generator PRR is two times data PRR, duty cycle = 50%.

B. C_L includes probe and jig capacitance.

C. Diodes are 1N3064

D. t_r and t_f ≤ 7 ns

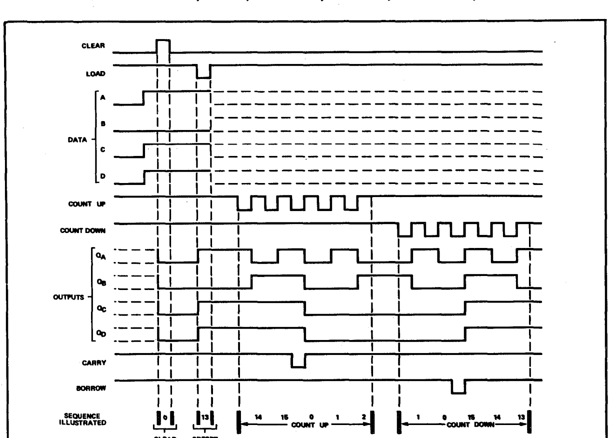
E. V_{ref} is 1.3 volts

FIGURE 1—CLEAR, SETUP, AND LOAD TIMES

TYPICAL CLEAR, LOAD, AND COUNT SEQUENCES

Illustrated below is the following sequence:

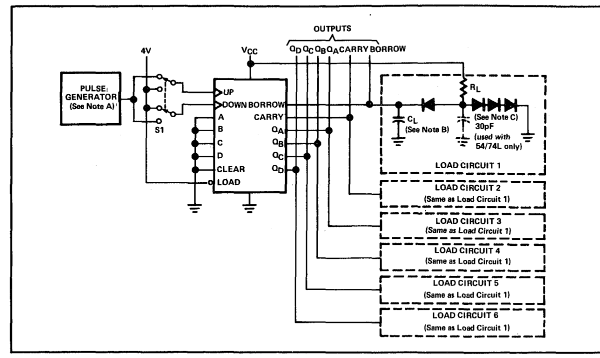
1. Clear outputs to zero.
2. Load (preset) to binary thirteen.
3. Count up to fourteen, fifteen, carry, zero, one, and two.
4. Count down to one, zero, borrow, fifteen, fourteen, and thirteen.



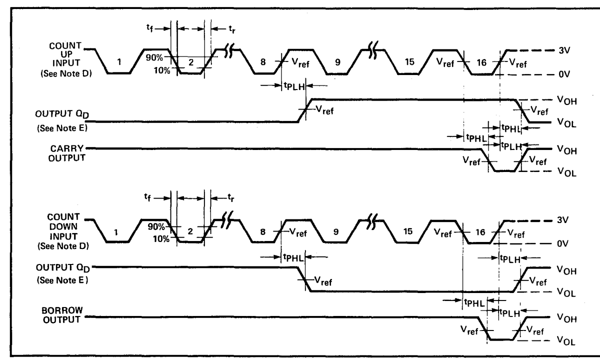
NOTES:

A. Clear overrides load, data, and count inputs.

B. When counting up, count-down input must be high; when counting down, count-up input must be high.



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES:

A. The pulse generator has the following characteristics: PRR ≤ 1 MHz, $Z_{out} \approx 50\ \Omega$, duty cycle = 50%.

B. C_L includes probe and jig capacitance.

C. Diodes are 1N3064

D. Waveforms for outputs Q_A, Q_B, and Q_C are omitted to simplify the drawing.

E. t_r and t_f ≤ 7 ns

F. V_{ref} is 1.3 volts

FIGURE 2—PROPAGATION DELAY TIMES

SPEED/PACKAGE AVAILABILITY

54	F,W	74	B
54LS	F,W	74LS	B
54S	F,W	74S	B

DESCRIPTION

This bidirectional shift register is designed to incorporate virtually all of the features a system designer may want in a shift register. The circuit contains 45 equivalent gates and features parallel inputs, parallel outputs, right-shift and left-shift serial inputs, operating-mode-control inputs, and a direct overriding clear line. The register has four distinct modes of operation, namely:

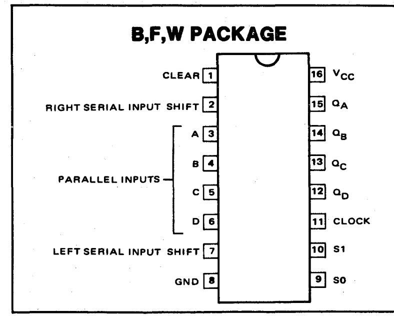
Parallel (broadside) load
Shift right (in the direction Q_A toward Q_D)
Shift left (in the direction Q_D toward Q_A)
Inhibit clock (do nothing)

Synchronous parallel loading is accomplished by applying the four bits of data and taking both mode control inputs, S0 and S1, high. The data are loaded into the associated flip-flops and appear at the outputs after the positive transistion of the clock input. During loading, serial data flow is inhibited.

Shift right is accomplished synchronously with the rising edge of the clock pulse when S0 is high and S1 is low. Serial data for this mode is entered at the shift-right data input. When S0 is low and S1 is high, data shifts left synchronously and new data is entered at the shift-left serial input.

Clocking of the flip-flop is inhibited when both mode control inputs are low. The mode controls of the S54194/N74194 should be changed only while the clock input is high.

PIN CONFIGURATION

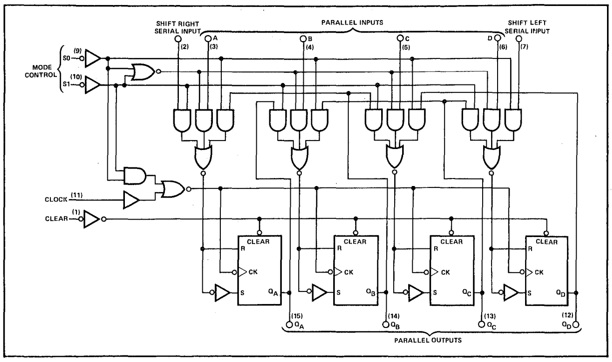


TRUTH TABLE

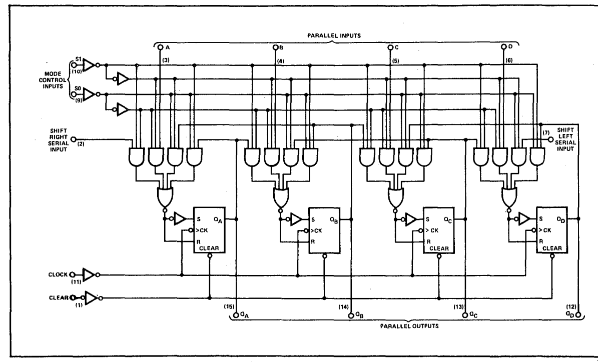
INPUTS										OUTPUTS			
	MODE			SERIAL		PARALLEL							
CLEAR	S1	S0	CLOCK	LEFT	RIGHT	A	B	C	D	Q_A	Q_B	Q_C	Q_D
L	X	X	X	X	X	X	X	X	X	L	L	L	L
H	X	X	L	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
H	H	H	↑	X	X	a	b	c	d	a	b	c	d
H	L	H	↑	X	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}
H	L	H	↑	X	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}
H	H	L	↑	H	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	H
H	H	L	↑	L	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	L
H	L	L	X	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}

H = high level (steady state)
L = low level (steady state)
X = irrelevant (any input, including transitions)
↑ = transition from low to high level
a,b,c,d, = the level of steady state input at inputs A,B,C, or D, respectively
Q_{A0}, Q_{B0}, Q_{C0}, Q_{D0} = the level of Q_A, Q_B, Q_C, or Q_D, respectively, before the indicated steady state input conditions were established
Q_{An}, Q_{Bn}, Q_{Cn}, Q_{Dn} = the level of Q_A, Q_B, Q_C, respectively, before the most recent ↑ transition of the clock

BLOCK DIAGRAM (94)



BLOCK DIAGRAM (LS194, S194)



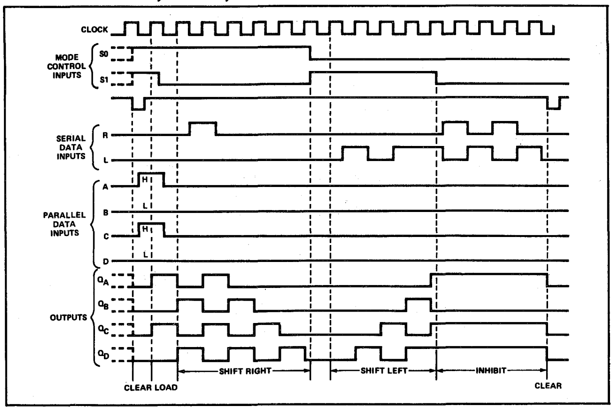
SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

TEST CONDITIONS				54/74 C_L=15pF R_L=400Ω			54/74LS C_L=15pF R_L=2kΩ			54/74S C_L=15pF R_L=280Ω			
PARAMETER		FROM INPUT	TO OUTPUT	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
f_{Clock}	Clock frequency			25	36		25	36		70	105		MHz
t_w	Width of pulse			20			20						ns
	Clock									7			
	Clear									12			
t_{Setup}	Input setup time												
	Mode control			30			30↑			8			ns
	Serial, Parallel			20			20↑			5			
	Clear inactive			25			25↑			9			
t_{Hold}	Input hold time	Any		0			0↑			3			ns
Propagation delay time													
t_{PLH}	Low-to-high	Clock		7	14	22		14	22	4	8	12	ns
t_{PHL}	High-to-low			7	17	26		17	22	4	11	16.5	
t_{PHL}	High-to-low	Clear			19	30		19	30		12.5	18.5	

Load circuit and typical waveforms are shown at the front of section.

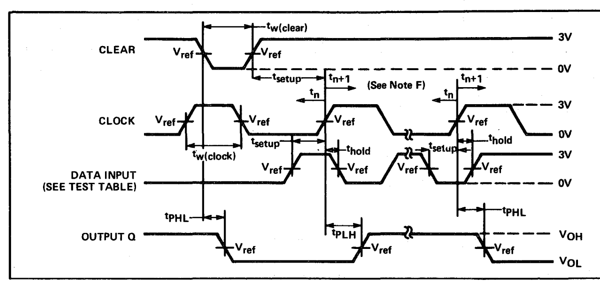
PARAMETER MEASUREMENT INFORMATION

TYPICAL CLEAR, SHIFT, AND LOAD SEQUENCES



TEST TABLE FOR SYNCHRONOUS INPUTS

DATA INPUT FOR TEST	S1	S0	OUTPUT TESTED (SEE NOTE E)
A	4.5V	4.5V	Q_A at t_n+1
B	4.5V	4.5V	Q_B at t_n+1
C	4.5V	4.5V	Q_C at t_n+1
D	4.5V	4.5V	Q_D at t_n+1
L Serial Input	4.5V	0V	Q_A at t_n+4
R Serial Input	0V	4.5V	Q_D at t_n+4



VOLTAGE WAVEFORMS

NOTES:

A. The clock pulse generator has the following characteristics: $Z_{out} \approx 50\ \Omega$ and PRR ≤ MHz, $t_r \leq 15$ ns and $t_f \leq 6$ ns. When testing f_{max}, vary PRR.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N3064 or 1N916.
D. A clear pulse is applied prior to each test.
E. $V_{ref} = 1.3V$.
F. Propagation delay times (t_{PLH} and t_{PHL}) are measured at $t_n +1$. Proper shifting of data is verified at t_n+4 with a functional test.
G. t_n = bit time before clocking transition.
t_n+1 = bit time after one clocking transition.
t_n+4 = bit time after four clocking transitions.

FIGURE 1—SWITCHING TIMES

LOGIC

4-BIT PARALLEL-ACCESS SHIFT REGISTER 54/74195

SPEED/PACKAGE AVAILABILITY

54	F,W	74	B
54LS	F,W	74LS	B
54S	F,W	74S	B

DESCRIPTION

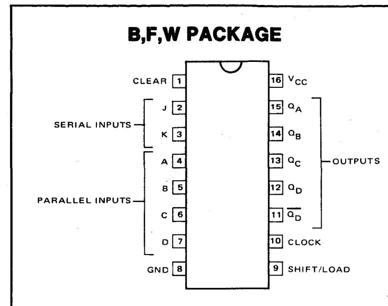
This 4-bit register features parallel inputs, parallel outputs, J-$\overline{K}$ serial inputs, shift/load control input, and a direct overriding clear. All inputs are buffered to lower the input drive requirements. The registers have two modes of operation:

Parallel (Broadside) Load
Shift (In direction Q_A toward Q_D)

Parallel loading is accomplished by applying the four bits of data and taking the shift/load control input low. The data is loaded into the associated flip-flop and appears at the outputs after the positive transition of the clock input. During loading, serial data flow is inhibited.

Shifting is accomplished synchronously when the shift/load control input is high. Serial data for this mode is entered at the J-$\overline{K}$ inputs. These inputs permit the first stage to perform as a J-$\overline{K}$, D-, or T-type flip-flop as shown in the function table.

PIN CONFIGURATION



TRUTH TABLE

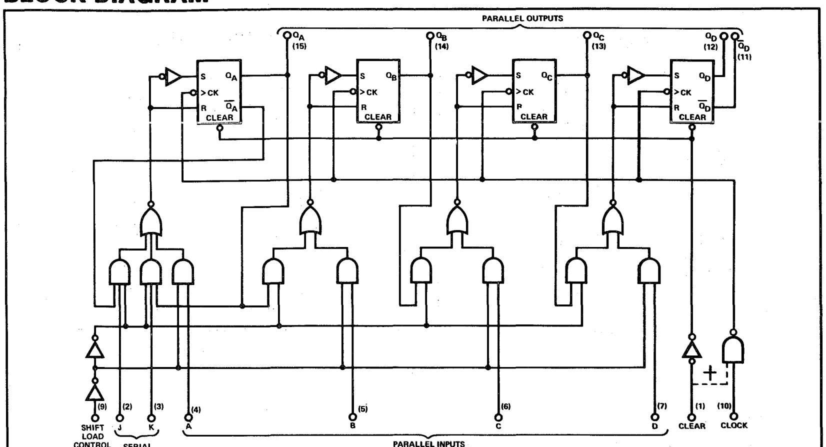
INPUTS									OUTPUTS				
			SERIAL		PARALLEL								
CLEAR	SHIFT/LOAD	CLOCK	J	$\overline{K}$	A	B	C	D	Q_A	Q_B	Q_C	Q_D	$\overline{Q}_D$
L	X	X	X	X	X	X	X	X	L	L	L	L	H
H	L	↑	X	X	a	b	c	d	a	b	c	d	$\overline{d}$
H	H	L	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	$\overline{Q}_{D0}$
H	H	↑	L	H	X	X	X	X	Q_{A0}	Q_{A0}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	H	↑	L	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	H	↑	H	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	H	↑	H	L	X	X	X	X	$\overline{Q}_{An}$	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$

H = high level (steady state)
L = low level (steady state)
X = irrelevant (any input, including transitions)
↑ = transition from low to high level
a,b,c,d = the level of steady-state input at A,B,C, or D, respectively
Q_{A0}, Q_{B0}, Q_{C0}, Q_{D0} = the level of Q_A, Q_B, Q_C, or Q_D, respectively, before the indicated steady-state input conditions were established
Q_{An}, Q_{Bn}, Q_{Cn} = the level of Q_A, Q_B, or Q_C, respectively, before the most recent transition of the clock

SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

TEST CONDITIONS				54/74 C_L=15pF R_L=400Ω			54/74LS C_L=15pF R_L=2kΩ			54/74S C_L=15pF R_L=400Ω			
PARAMETER		FROM INPUT	TO OUTPUT	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
f_{Clock}	Clock frequency			30	39		30	39		70	105		MHz
$t_{w(Clock)}$	Width of clock input pulse			16			16			7			ns
$t_{w(Clear)}$	Width of clear input pulse			12			12			12			ns
t_{Setup}	Input setup time												
	Shift/Load			25			25↑			8			ns
	Serial/Parallel			15			15↑			5			
	Clear inactive			25			25↑			9			
$t_{Release}$	Shift/Load release time					10			10↑			6	ns
T_{Hold}	Input hold time	Any		0			0↑			3			ns
Propagation delay time													
t_{PLH}	Low-to-high	Clock		6	14	22		14	22		8	12	ns
t_{PHL}	High-to-low			7	17	26		17	26		11	16.5	
t_{PHL}	High-to-low	Clear			19	30		19	30		12.5	18.5	

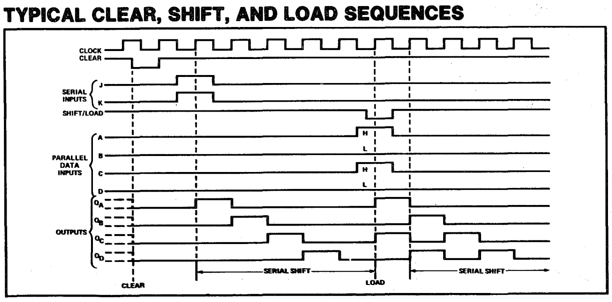
BLOCK DIAGRAM

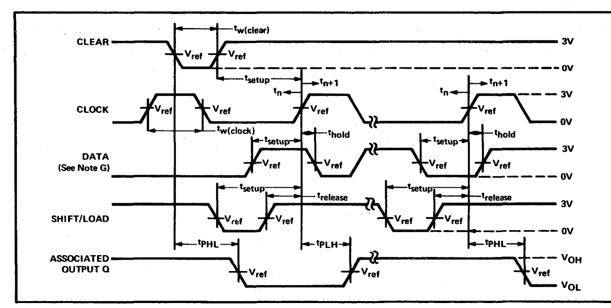


†This connection is made on '195 only.

PARAMETER MEASUREMENT INFORMATION

TYPICAL CLEAR, SHIFT, AND LOAD SEQUENCES





VOLTAGE WAVEFORMS

NOTES:

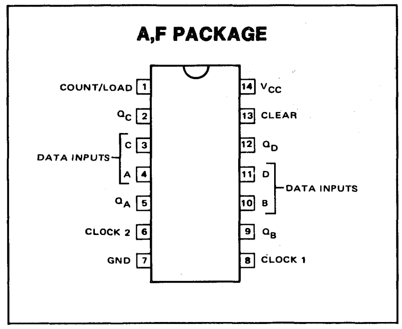
A. The clock pulse generator has the following characteristics: $Z_{out} \approx 50\ \Omega$ and PRR ≤ 1 MHz
$t_r \leq 15$ ns and $t_f \leq 6$ ns. When testing f_{max}, vary the clock PRR.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N3064.
D. A clear pulse is applied prior to each test.
E. $V_{ref} = 1.3V$.
F. Propagation delay times (t_{PLH} and t_{PHL}) are measured at t_n+1. Proper shifting of data is verified at t_n+4 with a functional test.
G. J and $\overline{K}$ inputs are tested the same as data A, B, C, and D inputs except that shift/load input remains high.
H. t_n = bit time before clocking transition.
t_n+1 = bit time after one clocking transition.
t_n+4 = bit time after four clocking transitions.

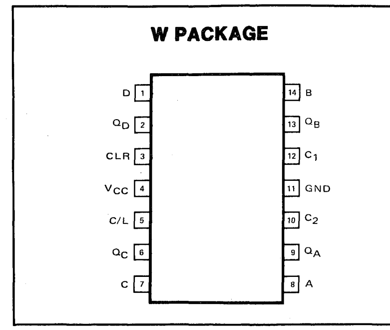
FIGURE 1—SWITCHING TIMES

SPEED/PACKAGE AVAILABILITY

54	F,W	74	A
54LS	F,W	74LS	A
54S	F,W	74S	A

PIN CONFIGURATION





DESCRIPTION

This high-speed monolithic counter consists of four DC coupled, master-slave flip-flops which are internally interconnected to provide a divide-by-two and a divide-by-five counter S54/N74LS196. This counter is fully programmable; that is, the outputs may be preset to any state by placing a low on the count/load input and entering the desired data at the data inputs. The outputs will change to agree with the data inputs independent of the state of the clocks.

During the count operation, transfer of information to the outputs occurs on the negative-going edge of the clock pulse. This counter features a direct clear which when taken low sets all outputs low regardless of the states of the clocks.

This counter may also be used as a 4-bit latch by using the count/load input as the strobe and entering data at the data inputs. The outputs will directly follow the data inputs when the count/load is low, but will remain unchanged when the count/load is high and the clock inputs are inactive.

SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

(54/74—Refer to 8290 Data Sheet, 54/74S—Refer to 82S90 Data Sheet)

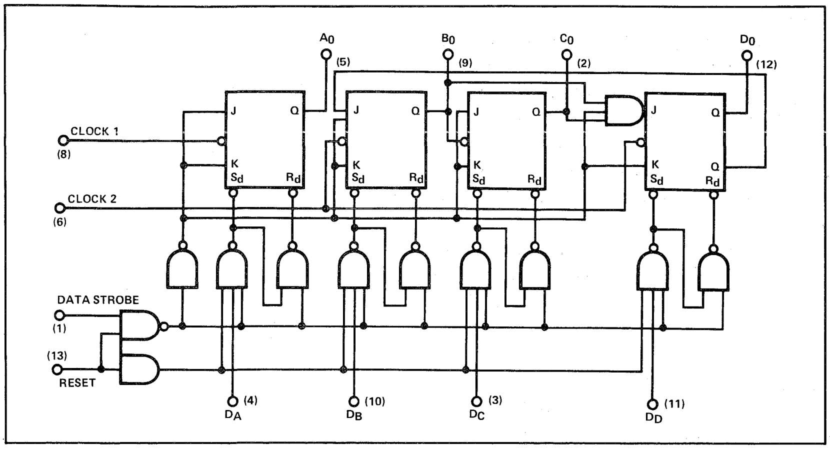
PARAMETER[1]		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	54/74LS MIN	54/74LS TYP	54/74LS MAX	UNIT
f_{Clock}		Clock 1	Q_A		30	40		MHz
		Clock 2	Q_A		15			
t_w	Input pulse-width				20			
		Clock 1			30			ns
		Clock 2						
		Clear			15			
		Load			20			
t_{Hold}	Input hold time							
		High level			$t_{w(Load)}$↓			
		Low level			$t_{w(Load)}$↓			
t_{Setup}	Input setup time	High level			10↓			ns
		Low level			15↓			ns
t_{Enable} (Note 1)	Count enable time				20↓			ns
t_{PLH}		Clock 1	Q_A	C_L = 15pF		8	15	ns
t_{PHL}				R_L = 2kΩ		13	20	
t_{PLH}		Clock 2	Q_B			16	24	ns
t_{PHL}						22	33	
t_{PLH}		Clock 2	Q_C			38	57	ns
t_{PHL}						41	62	
t_{PLH}		Clock 2	Q_D			12	18	ns
t_{PHL}						30	45	
t_{PLH}		A,B,C,D	Q_A, Q_B, Q_C, Q_D			20	30	ns
t_{PHL}						29	44	
t_{PLH}		Load	Any			27	41	ns
t_{PHL}						30	45	
t_{PHL}		Clear	Any			34	51	ns

[1] f_{max} = maximum input count frequency t_{PLH} = propagation delay time, low-to-high-level output, t_{PHL} = propagation delay time, high-to-low-level output.

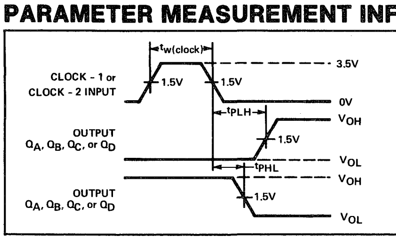
NOTE:

1. Count enable time is the internal immediately preceding the negative — going edge of the clock pulse during which internal the count/load and clear inputs must be high to ensure counting.

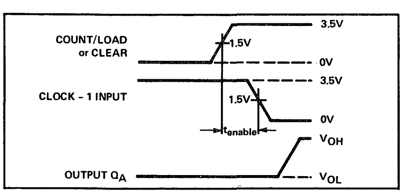
LOGIC DIAGRAM



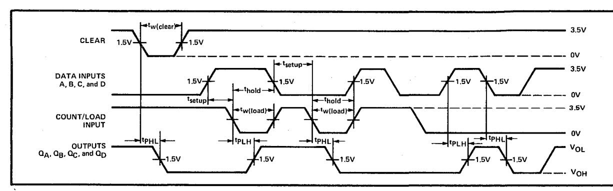
PARAMETER MEASUREMENT INFORMATION



CLOCK-MODE VOLTAGE WAVEFORMS



CLOCK ENABLE TIME VOLTAGE WAVEFORMS



CLEAR AND LOAD VOLTAGE WAVEFORMS

NOTES:

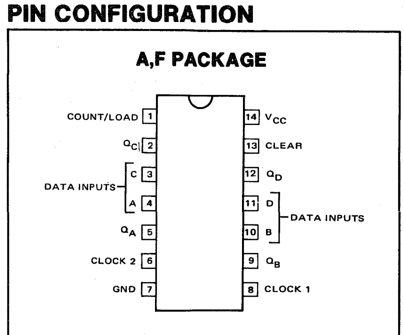
A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, duty cycle ≤ 50%, t_r ≤ 15 ns, and unless specified, t_f ≤ 15 ns. When testing f_{max}, vary PRR.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N3064.
D. Unless otherwise specified, Q_A is connected to clock 2.

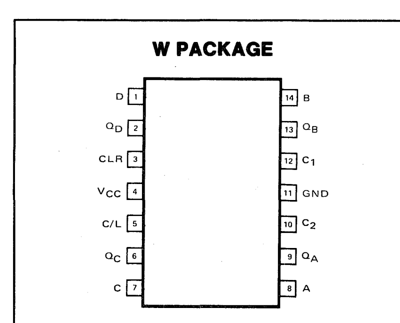
PRESETTABLE BINARY COUNTER/LATCH 54/74197

SPEED/PACKAGE AVAILABILITY

54	F,W	74	A
54LS	F,W	74LS	A
		74S	A

PIN CONFIGURATION





DESCRIPTION

This high-speed monolithic counter consists of four DC coupled, master-slave flip-flops which are internally interconnected to provide a divide-by-two and a divide-by-eight counter S54/N74LS197. These four counters are fully programmable; that is, the outputs may be preset to any state by placing a low on the count/load input and entering the desired data at the data inputs. The outputs will change to agree with the data inputs independent of the state of the clocks.

During the count operation, transfer of information to the outputs occurs on the negative-going edge of the clock pulse. These counters feature a direct clear which when taken low sets all outputs low regardless of the states of the clocks.

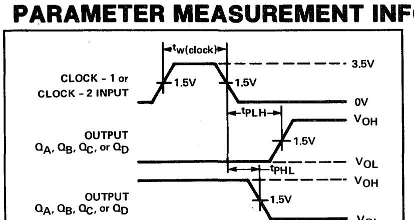
These counters may also be used as 4-bit latches by using the count/load input as the strobe and entering data at the data inputs. The outputs will directly follow the data inputs when the count/load is low, but will remain unchanged when the count/load is high and the clock inputs are inactive.

SWITCHING CHARACTERISTICS $V_{CC} = 5V$, $T_A = 25°C$

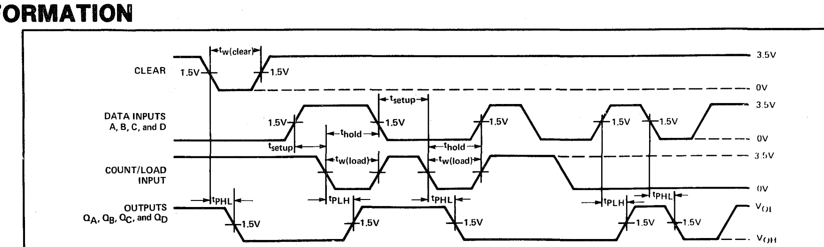
PARAMETER[1]	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	LIMITS MIN	TYP	MAX	UNIT
f_{Count}	Clock 1	Q_A	$C_L = 15pF$, $R_L = 2k\Omega$	30	40		MHz
	Clock 2	Q_A		15			
t_{PLH}	Clock 1	Q_A			8	15	ns
t_{PHL}					14	21	
t_{PLH}	Clock 2	Q_B			12	19	ns
t_{PHL}					23	35	
t_{PLH}	Clock 2	Q_C			34	51	ns
t_{PHL}					42	63	
t_{PLH}	Clock 2	Q_D			55	78	ns
t_{PHL}					63	95	
t_{PLH}	A,B,C,D	Q_A, Q_B, Q_C, Q_D			18	27	ns
t_{PHL}					29	44	
t_{PLH}	Load	Any			26	39	ns
t_{PHL}					30	45	
t_{PHL}	Clear	Any			34	51	ns

[1] f_{max} = maximum input count frequency
t_{PLH} = propagation delay time, low-to-high-level output, t_{PHL} = propagation delay time, high-to-low-level output.

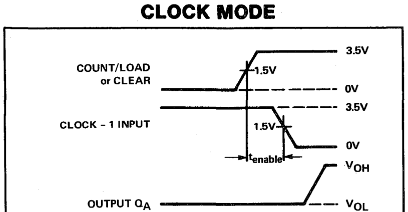
PARAMETER MEASUREMENT INFORMATION



CLOCK MODE

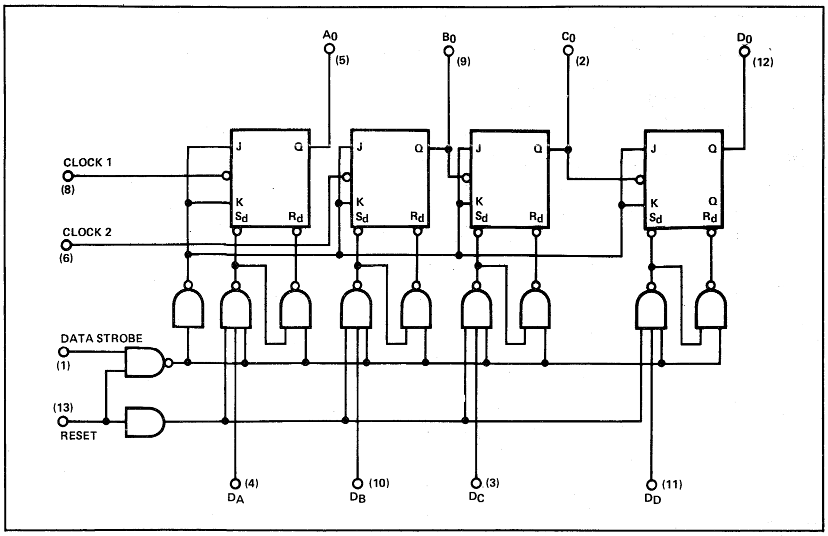


CLEAR AND LOAD



CLOCK ENABLE

LOGIC DIAGRAM



8-BIT SHIFT REGISTER 54/74198

SPEED/PACKAGE AVAILABILITY

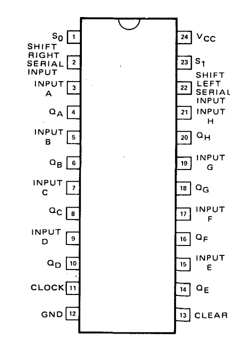
54 F,Q 74 N

TRUTH TABLE

INPUTS							OUTPUTS				
	MODE			SERIAL		PARALLEL					
CLEAR	S_1	S_0	CLOCK	LEFT	RIGHT	A...H	Q_A	Q_B	...	Q_G	Q_H
L	X	X	X	X	X	X	L	L		L	L
H	X	X	L	X	X	X	Q_{A0}	Q_{B0}		Q_{G0}	Q_{H0}
H	H	H	↑	X	X	a...h	a	b		g	h
H	L	H	↑	X	H	X	H	Q_{An}		Q_{Fn}	Q_{Gn}
H	L	H	↑	X	L	X	L	Q_{An}		Q_{Fn}	Q_{Gn}
H	H	L	↑	H	X	X	Q_{Bn}	Q_{Cn}		Q_{Hn}	H
H	H	L	↑	L	X	X	Q_{Bn}	Q_{Cn}		Q_{Hn}	L
H	L	L	X	X	X	X	Q_{A0}	Q_{B0}		Q_{G0}	Q_{H0}

H = high level (steady state), L = low level (steady state)
X = irrelevant (any input, including transitions)
↑ = transition from low to high level
a . . . h = the level of steady state input at inputs A thru H, respectively.
Q_{A0}, Q_{B0}, Q_{G0}, Q_{H0} = the level of Q_A, Q_B, Q_G, or Q_H, respectively, before the indicated steady-state input conditions were established.
Q_{An}, Q_{Bn}, etc. = the level of Q_A, Q_B, etc., respectively, before the most-recent ↑ transition of the clock.

PIN CONFIGURATION



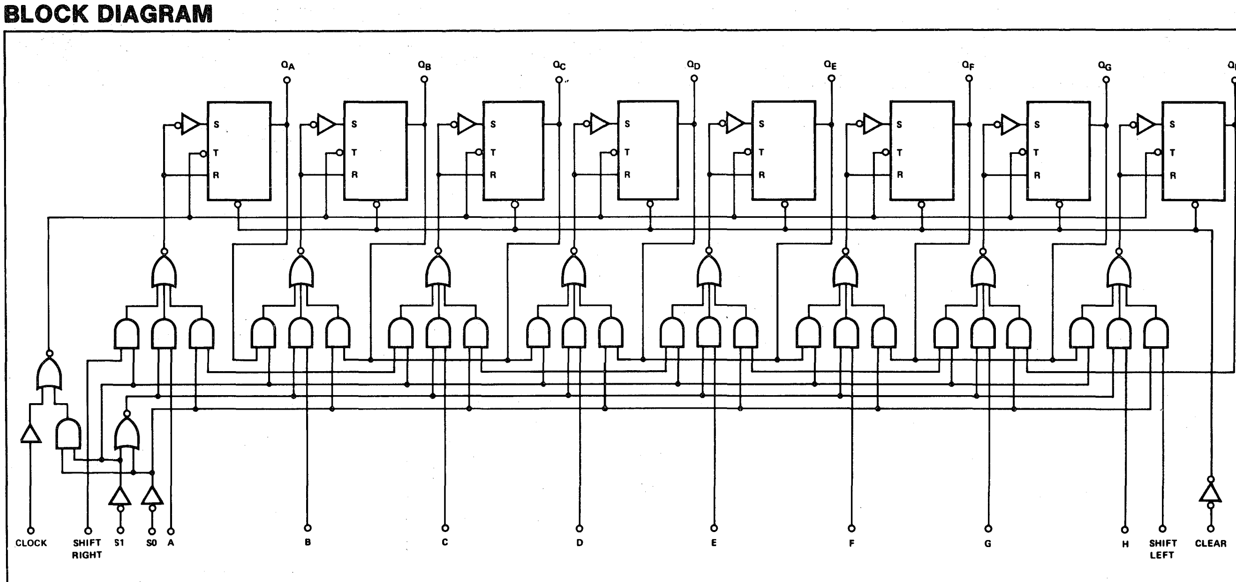
LOGIC

SWITCHING CHARACTERISTICS $V_{CC} = 5V$, $T_A = 25°C$

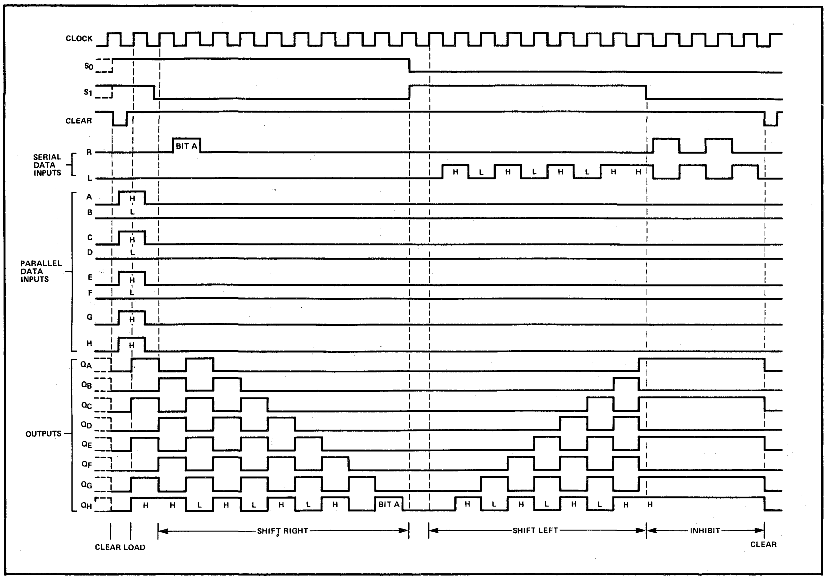
TEST CONDITIONS				54/74 $C_L = 15pF$ $R_L = 400\Omega$			
PARAMETER		FROM INPUT	TO OUTPUT	MIN	TYP	MAX	UNIT
f_{Count}	Count frequency			25	35		MHz
t_W	Width of pulse			20			ns
t_{Setup}	Input setup time			30			
	Mode control						
	Data			20			
t_{Hold}	Input hold time			0			ns
Propagation delay time							
t_{PLH}	Low-to-high	Clock		8	17	26	ns
t_{PLH}	High-to-low			8	20	30	
t_{PHL}	High-to-low	Clear			23	35	

Load circuit and typical waveforms are shown at the front of section.

BLOCK DIAGRAM



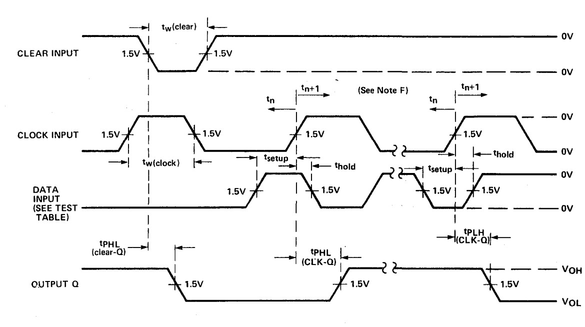
TYPICAL CLEAR, LOAD, RIGHT-SHIFT, LEFT-SHIFT, INHIBIT & CLEAR SEQUENCES



PARAMETER MEASUREMENT INFORMATION

TEST TABLE FOR SYNCHRONOUS INPUTS

DATA INPUT FOR TEST	S_1	S_0	OUTPUT TESTED (SEE NOTE E)
A	4.5V	4.5V	Q_A at t_n+1
B	4.5V	4.5V	Q_B at t_n+1
C	4.5V	4.5V	Q_C at t_n+1
D	4.5V	4.5V	Q_D at t_n+1
E	4.5V	4.5V	Q_E at t_n+1
F	4.5V	4.5V	Q_F at t_n+1
G	4.5V	4.5V	Q_G at t_n+1
H	4.5V	4.5V	Q_H at t_n+1
L Serial Input	4.5V	0V	Q_A at t_{n+8}
R Serial Input	0V	4.5V	Q_H at t_{n+8}



VOLTAGE WAVEFORMS

NOTES:

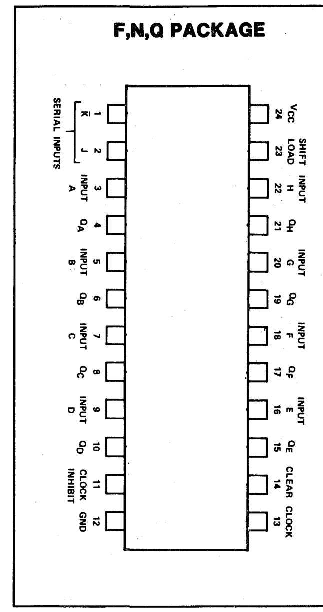
A. The clock pulse has the following characteristics: $t_{w(clock)} \geq 20$ ns and PRR = 1 MHz. The clear pulse has the following characteristics: $t_{w(clear)} \geq 20$ ns and $t_{hold} = 0$ ns. When testing f_{max}, vary the clock PRR.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N3064.
D. A clear pulse is applied prior to each test.
E. Propagation delay times (t_{PLH} and t_{PHL}) are measured at t_n+1. Proper shifting of data is verified at t_n+8 with a functional text.
t_n+1 = bit time after one clocking transition
t_n+8 = bit time after eight clocking transitions

Load circuit shown at front of section.

SPEED/PACKAGE AVAILABILITY

54 F,Q 74 N

PIN CONFIGURATION

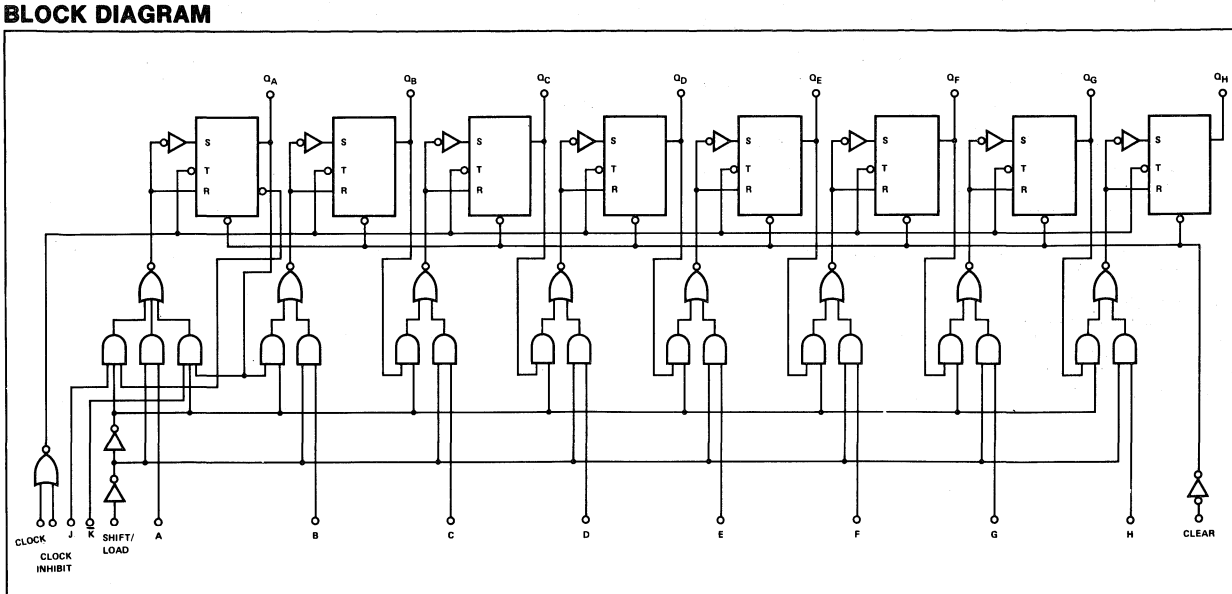


TRUTH TABLE

INPUTS							OUTPUTS				
CLEAR	SHIFT/ LOAD	CLOCK INHIBIT	CLOCK	SERIAL J	SERIAL $\overline{K}$	PARALLEL A...H	Q_A	Q_B	Q_C	...	Q_H
L	X	X	X	X	X	X	L	L	L		L
H	X	L	L	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}		Q_{H0}
H	L	L	↑	X	X	a...h	a	b	c		h
H	H	L	↑	L	H	X	Q_{A0}	Q_{A0}	Q_{Bn}		Q_{Gn}
H	H	L	↑	L	L	X	L	Q_{An}	Q_{Bn}		Q_{Gn}
H	H	L	↑	H	H	X	H	Q_{An}	Q_{Bn}		Q_{Gn}
H	H	L	↑	H	L	X	$\overline{Q}_{An}$	Q_{An}	Q_{Bn}		Q_{Gn}
H	X	H	↑	X	X	X	Q_{A0}	Q_{B0}	Q_{B0}		Q_{H0}

H = high level (steady state), L = low level (steady state)
X = irrelevant (any input, including transitions)
↑ = transition from low to high level
a . . . h = the level of steady-state input at inputs A thru H, respectively.
Q_{A0}, Q_{B0}, Q_{C0} . . . Q_{H0} = the level of Q_A, Q_B, or Q_C thru Q_H, respectively before the indicated steady state input conditions were established.
Q_{An}, Q_{Bn} . . . Q_{Gn} = the level of Q_A or Q_B thru Q_G, respectively, before the most recent ↑ transition of the clock.

BLOCK DIAGRAM

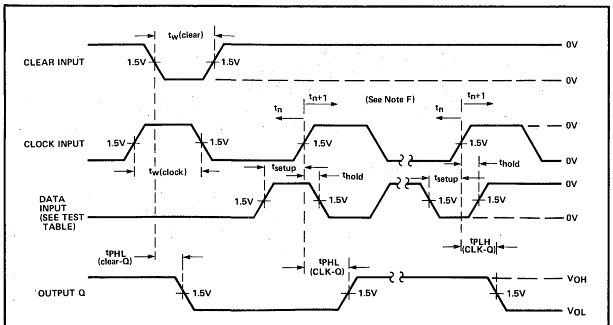


SWITCHING CHARACTERISTICS $V_{CC} = 5V$, $T_A = 25°C$

TEST CONDITIONS			54/74 C_L=15pF R_L=400Ω			
PARAMETER	FROM INPUT	TO OUTPUT	MIN	TYP	MAX	UNIT
f_{Count} Count frequency			25	35		MHz
t_W Width of pulse			20			ns
t_{Setup} Input setup time						
Mode control			30			ns
Data			20			
t_{Hold} Input hold time			0			ns
Propagation delay time						
t_{PLH} Low-to-high	Clock		8	17	26	ns
t_{PHL} High-to-low			8	20	30	
t_{PHL} High-to-low	Clear			23	35	

Load circuit and typical waveforms are shown at the front of section.

PARAMETER MEASUREMENT INFORMATION



VOLTAGE WAVEFORMS

Load circuit shown at front of section.

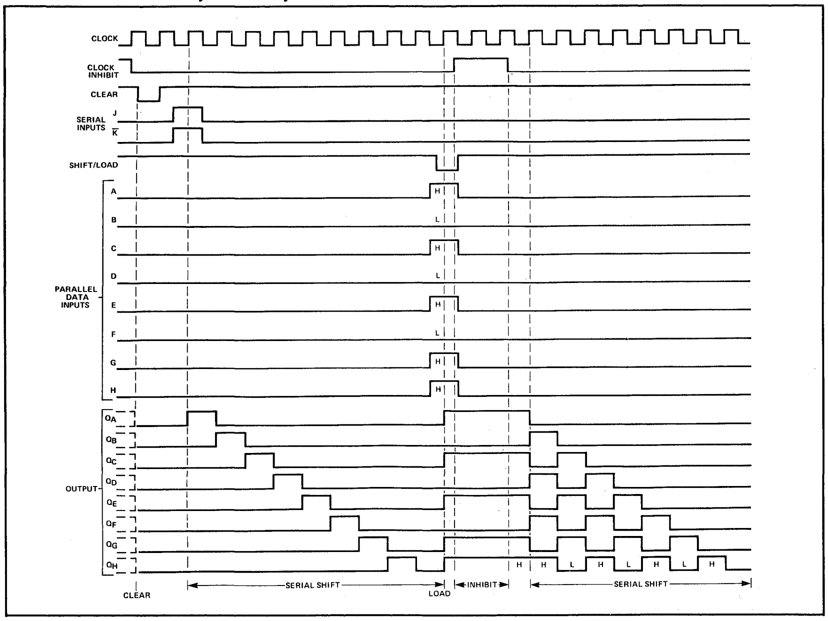
TEST TABLE FOR SYNCHRONOUS INPUTS

DATA INPUT FOR TEST	SHIFT/LOAD	OUTPUT TESTED (SEE NOTE E)
A	0V	Q_A at t_n+1
B	0V	Q_B at t_n+1
C	0V	Q_C at t_n+1
D	0V	Q_D at t_n+1
E	0V	Q_E at t_n+1
F	0V	Q_F at t_n+1
G	0V	Q_G at t_n+1
H	0V	Q_H at t_n+1
J and $\overline{K}$	4.5V	Q_H at t_n+8

NOTES:

A. The clock pulse has the following characteristics: $t_{w(clock)} \geq 20$ ns and PRR = 1 MHz. The clear pulse has the following characteristics: $t_{w(clear)} \geq 20$ ns and $t_{hold} = 0$ ns. When testing f_{max}, vary the clock PRR.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N3064.
D. A clear pulse is applied prior to each test.
E. Propagation delay times (t_{PLH} and t_{PHL}) are measured at t_n+1. Proper shifting of data is verified at t_n+8 with a functional test.
F. t_n+1 = bit time after one clock transition
t_n+8 = bit time after eight clocking transitions

TYPICAL CLEAR, SHIFT, LOAD AND INHIBIT SEQUENCES

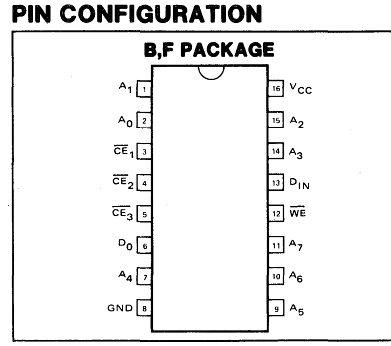


TTL 256x1 RAM — TRI-STATE 54/74200

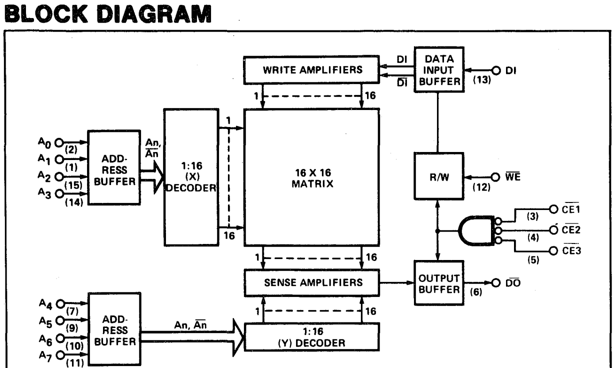
SPEED/PACKAGE AVAILABILITY AND ELECTRICAL CHARACTERISTICS

Refer to Bipolar Memory Section

PIN CONFIGURATION



BLOCK DIAGRAM



TRUTH TABLE

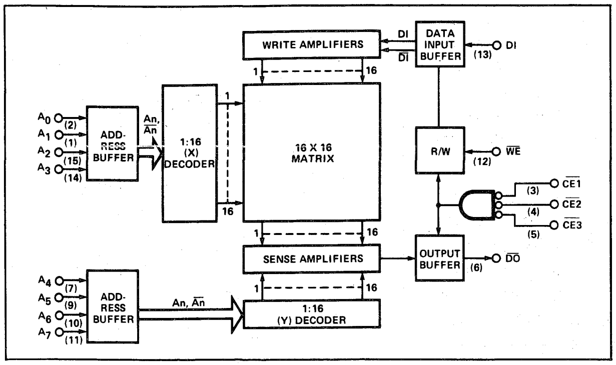
MODE	$\overline{CE}$*	$\overline{WE}$	D_{IN}	$\overline{D_{OUT}}$ 82S16/116	82S17/117	54/74S200/201	54/74S301
READ	0	1	X	STORED DATA	STORED DATA	STORED DATA	STORED DATA
WRITE "0"	0	0	0	1	1	High-Z	1
WRITE "1"	0	0	1	0	0	High-Z	1
DISABLED	1	X	X	High-Z	1	High-Z	1

*"0" = All $\overline{CE}$ inputs low; "1" = one or more $\overline{CE}$ inputs high.

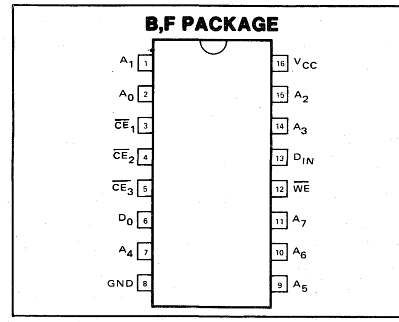
X = Don't care.

TTL 256x1 RAM — TRI-STATE 54/74201

BLOCK DIAGRAM



PIN CONFIGURATION



TRUTH TABLE

MODE	$\overline{CE}$*	$\overline{WE}$	D_{IN}	$\overline{D}_{OUT}$ 82S16/116	82S17/117	54/74S200/201	54/74S301
READ	0	1	X	STORED $\overline{DATA}$	STORED $\overline{DATA}$	STORED $\overline{DATA}$	STORED $\overline{DATA}$
WRITE "0"	0	0	0	1	1	High-Z	1
WRITE "1"	0	0	1	0	0	High-Z	1
DISABLED	1	X	X	High-Z	1	High-Z	1

*"0" = All $\overline{CE}$ inputs low; "1" = one or more $\overline{CE}$ inputs high.

SPEED/PACKAGE AVAILABILITY AND ELECTRICAL CHARACTERISTICS

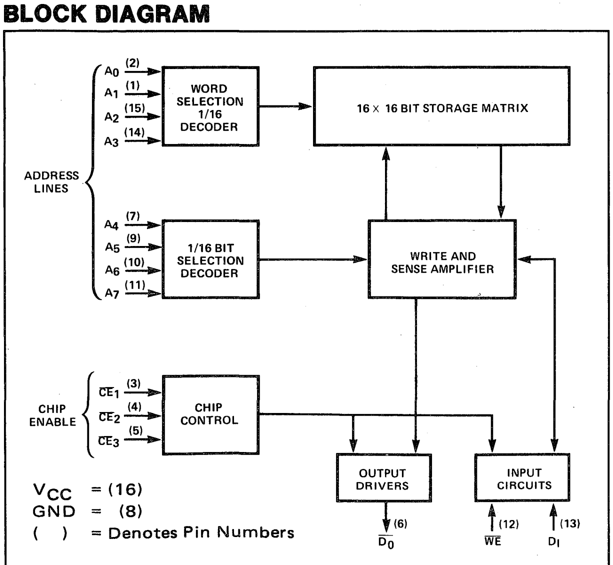
Refer to Bipolar Memory Section

TTL 256x1 RAM — OPEN COLLECTOR 54/74206

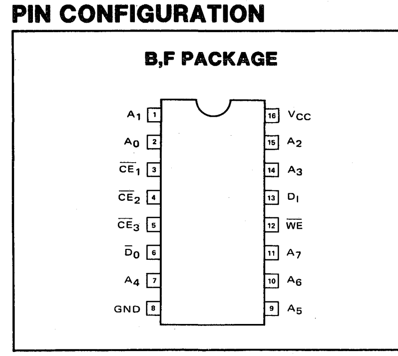
SPEED/PACKAGE AVAILABILITY AND ELECTRICAL CHARACTERISTICS

Refer to Bipolar Memory Section

BLOCK DIAGRAM



PIN CONFIGURATION



TRUTH TABLE

FUNCTION	$\overline{CE}$*	$\overline{WE}$	OUTPUT
Write (Store D_I Complement)	L	L	H
Read	L	H	Stored Data
Inhibit	H	X	H

H = high level, L = low level, X = irrelevant
(*)L = all $\overline{CE}$ inputs low; H = one or more $\overline{CE}$ inputs high.

DESCRIPTION

The 54/74LS221 is a monolithic dual multivibrator which features a negative-transition-triggered input either of which can be used as an inhibit input. Pulse triggering occurs at a particular voltage level and is not directly related to the transition time of the input pulse. Schmitt-trigger input circuitry (TTL hystersis) for B input allows jitter-free triggering from inputs with transition rates as slow as 1 volt/second, providing the circuit with excellent noise immunity of typically 1.2V. A high immunity to Vcc noise of typically 1.5V is also provided by internal latching circuitry.

Once fired, the outputs are independent of further transitions of the A and B inputs and are a function of the timing components, or the output pulse can be terminated by the overriding clear. Input pulses may be of any duration relative to the output pulse. Output pulse length may be varied from 35ns to 49s (54LS221) or 70s (74LS221) by choosing appropriate timing components. With $R_{ext} = 2k\Omega$ and $C_{ext} = 0$, an output pulse of typically 30ns is achieved which may be used as a d-c. triggered reset signal. Output rise and fall times are TTL compatible and independent of pulse length. Typical triggering and clearing sequences are illustrated as a part of the switching characteristics waveforms.

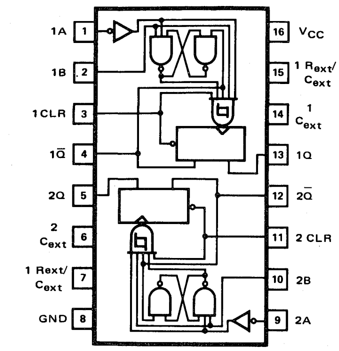
Pulse width stability is achieved through internal compensation and is virtually independent of Vcc and temperature. In most applications, pulse stability will only be limited by the accuracy of external timing components.

Jitter-free operation is maintained over the full temperature and Vcc ranges for more than six decades of timing capacitance (10pF to 10μF) and more than one decade of timing resistance (2kΩ to 70kΩ for the 54LS221, and 2kΩ to 100kΩ for the 74LS221). Throughout these ranges, pulse width is defined by the relationship: $t_{w(out)} = C_{ext}R_{ext}$. In 20.7 C_{ext}-R_{ext}. In circuits where pulse cutoff is not critical, timing capacitance up to 1000μF and timing resistance as low as 1.4k may be used. Also, the range of jitter-free output pulse widths is extended if Vcc is held to 5V and free-air temperature is 25°C. Duty cycles as high as 90% are achieved when using maximum recommended R_T. High duty cycles are available if a certain amount pulse width jitter is allowed. The variance in output pulse width from device to device is typically less than ±0.5% for given external timing components.

Pin assignments for this device are identical to those of the 54LS123/74LS123 so that the 54/74LS221 can be substituted for those products in systems not using the retrigger by merely changing the value of R_{ext} and/or C_{ext}.

PIN CONFIGURATION

B,F,W PACKAGE



positive logic:
Low input to clear reset Q low and Q̄ high regardless of d-c levels at A or B input.

TRUTH TABLE
(EACH MONOSTABLE)

INPUTS			OUTPUTS	
CLEAR	A	B	Q	Q̄
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↑	⎍	⊔
H	↓	H	⎍	⊔

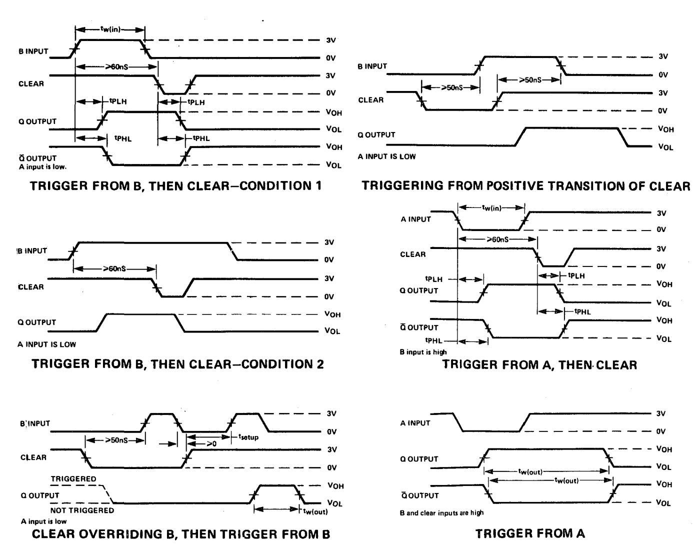
Also see description and switching characteristics

H = high level (steady state)
L = low level (steady state)
↑ = transition from low to high level
↓ = transition from high to low level
⎍ = one high level pulse
⊔ = one low level pulse
X = irrelevant

SPEED/PACKAGE AVAILABILITY

54	F,W	74	B
54LS	F,W	74LS	B

PARAMETER MEASUREMENT INFORMATION



TRIGGER FROM B, THEN CLEAR—CONDITION 1

TRIGGERING FROM POSITIVE TRANSITION OF CLEAR

TRIGGER FROM B, THEN CLEAR—CONDITION 2

TRIGGER FROM A, THEN CLEAR

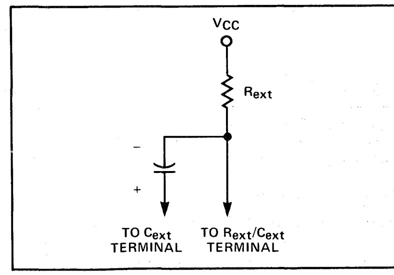
CLEAR OVERRIDING B, THEN TRIGGER FROM B

TRIGGER FROM A

NOTES:
A. Input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_{out} \approx 50\ \Omega$; $t_r \leq 15$ ns, $t_f \leq 6$ ns.
B. All measurements are made between the 1.3V points of the indicated transitions

HYSTERESIS VS. TEMPERATURE — TYPICAL VALUES

PARAMETER	54/74 -55°C	54/74 +25°C	54/74 +125°C	54/74LS -55°C	54/74LS +25°C	54/74LS +125°C	UNIT
V_{T+} Positive going threshold							
A Input		1.4	2				V
B Input		1.55	2				V
V_{T-} Negative going threshold							
A Input	0.8	1.4					V
B Input	0.8	1.35					V
Hysteresis							



TIMING COMPONENT CONNECTIONS

SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

TEST CONDITIONS: 54/74: C_L=15pF, R_L=400Ω, C_{ext} = 80pF, R_{ext} = 2kΩ; 54/74LS: C_L=15pF, R_L=2kΩ, C_{ext} = 80pF, R_{ext}=2kΩ

PARAMETER	FROM INPUT	TO OUTPUT	54/74 MIN	54/74 TYP	54/74 MAX	54/74LS MIN	54/74LS TYP	54/74LS MAX	UNIT
$t_{w(out)}$	A,B	Q,$\overline{Q}$	70	110	150	70	110	150	ns
			C_{ext}=0, R_{ext}=2kΩ			C_{ext}=0, R_{ext}=2kΩ			
			20	30	50	15	25	70	
			C_{ext}=100pF, R_{ext}=10kΩ			C_{ext}=100pF, R_{ext}=10kΩ			
			650	700	750	600	700	750	
			C_{ext}=1µf, R_{ext}=10kΩ			C_{ext}=1µf, R_{ext}=10kΩ			
			6.5	7	7.5	6.0	7	7.5	ms
$t_{w(in)}$			50			50			ns
$t_{w(clear)}$ Width of clear input pulse			20			40			ns
$t_{Setup\ (clear)}$			15			15↑			ns
dv/dt Rate of rise or fall of input pulse									
Schmitt,B			1			1			V/s
Logic Input, A			1			1			V/µs
R_{ext} External timing resistance			(54) 1.4		30	(54) 1.4		70	kΩ
			(74) 1.4		40	(74) 1.4		100	kΩ
C_{ext} External timing capacitance			0		1000	0		1000	µF
Output duty cycle				67			67		%
			R_{ext}=Max			R_T=Max R_{ext}			
				90			90		%
Propagation delay time									
t_{PLH} Low-to-high	A	Q		45	70		45	70	ns
t_{PHL} High-to-low	A	$\overline{Q}$		50	80		50	80	
t_{PLH} Low-to-high	B	Q		35	55		35	55	
t_{PHL} High-to-low	B	$\overline{Q}$		40	65		40	65	
t_{PLH} Low-to-high	Clear	$\overline{Q}$			40			65	
t_{PHL} High-to-low	Clear	Q			27			55	

Load circuit and typical waveforms are shown at the front of section.

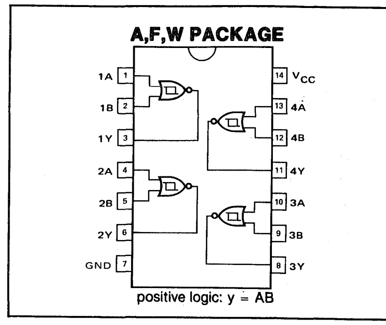
LOGIC

SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

TEST CONDITIONS	54/74 C_L=15pF R_L=400Ω			
PARAMETER	MIN	TYP	MAX	UNIT
Propagation delay time				
t_{PLH} Low-to-high		15	22	ns
t_{PHL} High-to-low		15	22	

Load circuit and typical waveforms are shown at the front of section.

PIN CONFIGURATION



HYSTERESIS VS. TEMPERATURE-TYPICAL VALUES

PARAMETER		54/74 -55°C	+25°C	+125°C	UNIT
V_{T+}	Positive going threshold	1.5	1.7	2	V
V_{T-}	Negative going threshold	0.6	0.9	1.1	V
	Hysteresis	0.4	0.8		V

SPEED/PACKAGE AVAILABILITY

54 F,W 74 A

DATA SELECTOR/MULTIPLEXER W/3-STATE OUTPUTS 54/74251

SPEED/PACKAGE AVAILABILITY

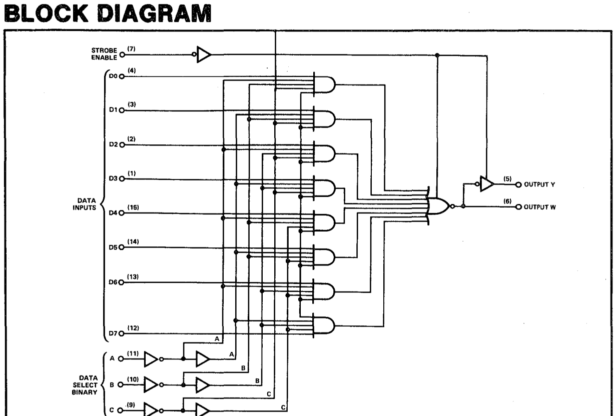
54LS F,W 74LS B
54S F,W 74S B

DESCRIPTION

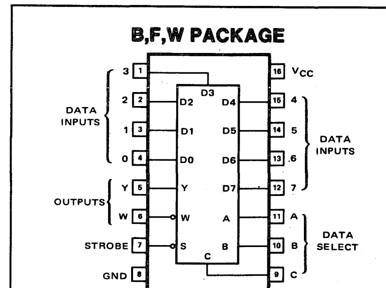
These monolithic data selectors/multiplexers contain full on-chip binary decoding to select one-of-eight data sources and feature a strobe-controlled three-state output. The strobe must be at a low logic level to enable these devices. The three-state outputs permit up to 49 54LS251 and 129 74LS251 outputs to be connected to a common bus. When the strobe input is high, both outputs are in a high-impedance state in which both the upper and lower transistors of each totem-pole output are off, and the output neither drives nor loads the bus significantly. When the strobe is low, the outputs are activated and operate as standard TTL totem-pole outputs.

To minimize the possibility that two outputs will attempt to take a common bus to opposite logic levels, the output control circuitry is designed so that the average output disable time is shorter than the average output enable time.

BLOCK DIAGRAM



PIN CONFIGURATION



TRUTH TABLE

INPUTS				OUTPUTS	
SELECT			STROBE	Y	W
C	B	A	S		
X	X	X	H	Z	Z
L	L	L	L	D0	$\overline{D0}$
L	L	H	L	D1	$\overline{D1}$
L	H	L	L	D2	$\overline{D2}$
L	H	H	L	D3	$\overline{D3}$
H	L	L	L	D4	$\overline{D4}$
H	L	H	L	D5	$\overline{D5}$
H	H	L	L	D6	$\overline{D6}$
H	H	H	L	D7	$\overline{D7}$

H = high logic level, L = low logic level
X = irrelevant, Z = high impedance (off)
D0, D1 . . . D7 = the level of the respective D input

SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C - PAGE 212

TEST CONDITIONS			54/74LS C_L=15pF R_L=2kΩ			54/74S C_L=15pF R_L=280Ω			
PARAMETER	FROM INPUT	TO OUTPUT	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
t_{PLH} Low-to-high	A,B,C (4 levels)	Y		29	45		12	18	ns
t_{PHL} High-to-low				28	45		13	19.5	
t_{PLH} Low-to-high	A,B,C (3 levels)	W		20	33		10	15	
t_{PHL} High-to-low				21	33		9	13.5	
t_{PLH} Low-to-high	Any D	Y		17	28		8	12	
t_{PHL} High-to-low				18	28		8	12	
t_{PLH} Low-to-high	Any D	W		10	15		4.5	7	
t_{PHL} High-to-low				9	15		4.5	7	
Output enable time									
t_{ZH} To high level	Strobe	Y		17	27		13	19.5	
t_{ZL} To low level				26	40		14	21	
t_{ZH} To high level	Strobe	W		17	27		13	19.5	
t_{ZL} To low level				24	40		14	21	
Output disable time			C_L=5pf R_L=2kΩ						
t_{HZ} From high level	Strobe	Y		30	45		5.5	8.5	
t_{ZL} From low level				15	25		9	14	
t_{HZ} From high level	Strobe	W		30	45		5.5	8.5	
t_{LZ} From low level				15	25		9	14	

LOGIC

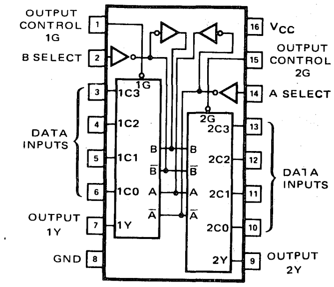
DESCRIPTION

Each of these Schottky-clamped data selectors/multiplexers contains inverters and drivers to supply fully complementary, on-chip, binary decoding data selection to the AND-OR gates. Separate output control inputs are provided for each of the two four-line sections.

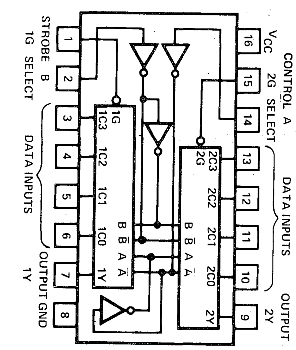
The three-state outputs can interface with and drive data lines of bus-organized systems. With all but one of the common outputs disabled (at a high-impedance state) the low-impedance of the single enabled output will drive the bus line to a high or low logic level.

PIN CONFIGURATION

54/74LS
B,F,W PACKAGE



54/74S
B,F,W PACKAGE



SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

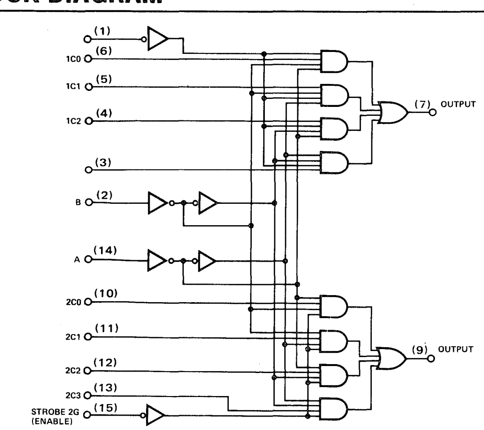
TEST CONDITIONS			54/74LS C_L=15pF R_L=2kΩ			54/74S C_L=15pF R_L=280Ω			
PARAMETER	FROM INPUT	TO OUTPUT	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
Propagation delay time									
t_{PLH} Low-to-high	Data	Y		11	25		6	9	ns
t_{PHL} High-to-low				13	20		6	9	
t_{PLH} Low-to-high	Select	Y		20	45		11.5	18	
t_{PHL} High-to-low				21	32		12	18	
Output enable time									
t_{ZH} To high level	Output control	Y		11	23				
t_{ZL} To low level				15	23				
Output disable time			C_L=5pf		R_L=2k				
t_{HZ} From high level	Output control	Y		27	41				
t_{LZ} From low level				12	27				
t_{PH}	Control	Y					6	13	ns
t_{PL}							7	14	
t_{PLZ}	Control	Y					6	14	
t_{PHZ}							5	8.5	

Load circuit and wave forms shown at front of section (totem pole outputs).

SPEED/PACKAGE AVAILABILITY

54LS	F,W	74LS	B
54S	F,W	74S	B

BLOCK DIAGRAM



TRUTH TABLE

SELECT INPUTS		DATA INPUTS				OUTPUT CONTROL	OUTPUT
B	A	C0	C1	C2	C3	G	Y
X	X	X	X	X	X	H	Z
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

Address inputs A and B are common to both sections.
H = high level. L = low level. X = irrelevant. Z = high impedance (off)

SPEED/PACKAGE AVAILABILITY

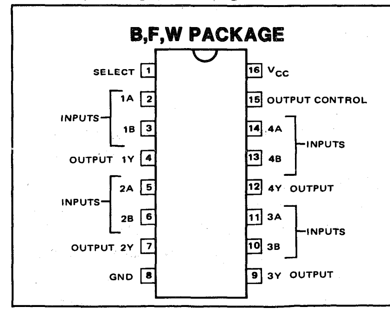
54LS F,W 74LS B
54S F,W 74S B

DESCRIPTION

This Schottky-clamped high-performance multiplexer features three-state outputs that can interface directly with and drive data lines of bus-organized systems. With all but one of the common outputs disabled (at a high-impedance state) the low impedance of the single enabled output will drive the bus line to a high or low logic level. To minimize the possibility that two outputs will attempt to take a common bus to opposite logic levels, the output-enable circuitry is designed such that the output disable times are shorter than the output enable times.

This three-state output feature means that n-bit (paralleled) data selectors with up to 258 sources can be implemented for data buses. It also permits the use of standard TTL registers for data retention throughout the system.

PIN CONFIGURATION

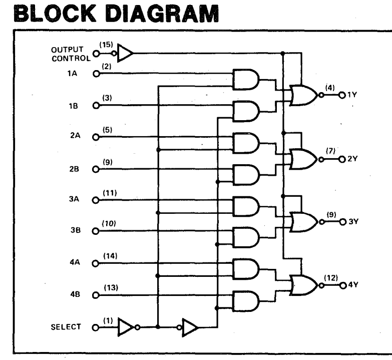


FUNCTION TABLE

INPUTS				OUTPUT Y
OUTPUT CONTROL	SELECT	A	B	
H	X	X	X	Z
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

H = H = high level, L = low level, X = irrelevant, Z = high impedance (off)

BLOCK DIAGRAM



SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

TEST CONDITIONS			54/74LS C_L=15pF			54/74S C_L=15pF R_L=280Ω			
PARAMETER	FROM INPUT	TO OUTPUT	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
Propagation delay time									
t_{PLH} Low-to-high	Data	Any		12	18		5	7.5	ns
t_{PHL} High-to-low				12	18		4.5	6.5	
t_{PLH} Low-to-high	Select	Any		14	21		8.5		
t_{PHL} High-to-low				14	21		8.5		
Output enable time									
t_{ZH} To high level	Output control	Any		20	30		13	19.5	
t_{ZL} To low level				20	30		14	21	
Output disable time			C_L=5pF			C_L=5pF			
t_{HZ} From high level	Output control	Any		14	30		5.5	8.5	
t_{LZ} From low level				14	25		9	14	

Load circuit and wave forms shown at front of section (totem pole outputs).

SPEED/PACKAGE AVAILABILITY

54LS F,W	74LS B
54S F,W	74S B

DESCRIPTION

This Schottky-clamped high-performance multiplexer features three-state outputs that can interface directly with and drive data lines of bus-organized systems. With all but one of the common outputs disabled (at a high-impedance state) the low impedance of the single enabled output will drive the bus line to a high or low logic level. To minimize the possibility that two outputs will attempt to take a common bus to opposite logic levels, the output-enable circuitry is designed such that the output disable times are shorter than the output enable times.

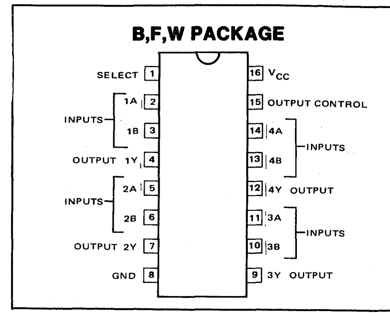
This three-state output feature means that n-bit (paralleled) data selectors with up to 258 sources can be implemented for data buses. It also permits the use of standard TTL registers for data retention throughout the system.

FUNCTION TABLE

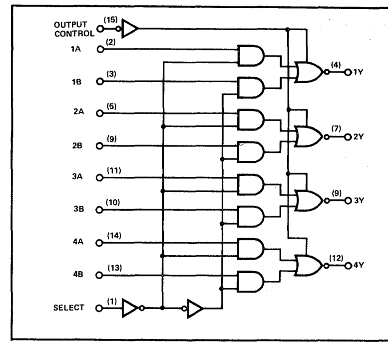
INPUTS				OUTPUT Y
OUTPUT CONTROL	SELECT	A	B	
H	X	X	X	Z
L	L	L	X	H
L	L	H	X	L
L	H	X	L	H
L	H	X	H	L

H = high level, L = low level, X = irrelevant, Z = high impedance (off)

PIN CONFIGURATION



BLOCK DIAGRAM



SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

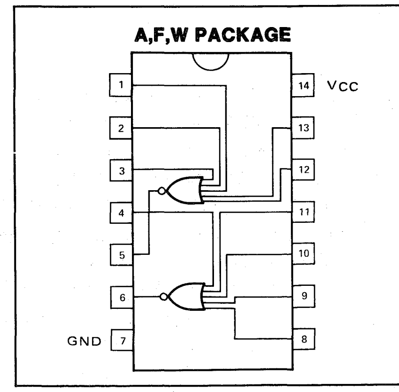
TEST CONDITIONS			54/74LS C_L=15pF			54/74S C_L=15pF R_L=280Ω			
PARAMETER	FROM INPUT	TO OUTPUT	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
Propagation delay time									
t_{PLH} Low-to-high	Data	Any		12	18		4	6	ns
t_{PHL} High-to-low				12	18		4	6	
t_{PLH} Low-to-high	Select	Any		14	21		8	12	
t_{PHL} High-to-low				14	21		7.5	12	
Output enable time									
t_{ZH} To high level	Output control	Any		20	30		13	19.5	
t_{ZL} To low level				20	30		14	21	
Output disable time			C_L=5pF			C_L=5pF			
t_{HZ} From high level	Output	Any		14	30		5.5	8.5	
t_{LZ} From low level	control			14	25		9	14	

Load circuit and waveforms shown at front of section (totem pole outputs).

SPEED/PACKAGE AVAILABILITY

54LS	F,W	74LS	A
54S	F,W	74S	A

PIN CONFIGURATION



SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

TEST CONDITIONS	54/74LS C_L=15pF R_L=2kΩ			54/74S C_L=15pF R_L=280			
PARAMETER	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNIT**
Propagation delay time							
t_{PLH} Low-to-high		10	15		3.5	5.5	ns
t_{PHL} High-to-low		10	15		3.5	5.5	

Load circuit and typical waveforms are shown at the front of section.

SPEED/PACKAGE AVAILABILITY

54LS F,W 74LS B

DESCRIPTION

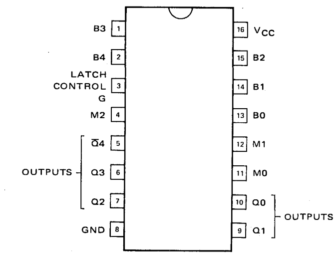
These low-power Schottky circuits are designed to be used in parallel multiplication applications. They perform binary multiplication in two's-complement form, two bits at a time.

The M inputs are for the multiplier bits and the B inputs are for the multiplicand. The Q outputs represent the partial product as a recoded base-4 number. This recoding effectively reduces the Wallace-tree hardware requirements by a factor of two.

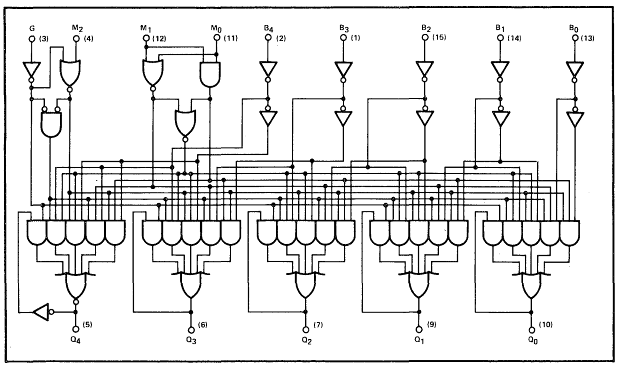
The outputs represent partial products in one's-complement form generated as a result of multiplication. A simple rounding scheme using two additional gates is needed for each partial product to generate two's complement.

The leading (most significant) bit of the product is inverted for ease in extending the sign to square (left justify) the partial-product bits.

PIN CONFIGURATION



BLOCK DIAGRAM



FUNCTION TABLE

INPUTS				OUTPUTS				
LATCH CONTROL G	MULTIPLIER M2	M1	M0	$\overline{Q4}$	Q3	Q2	Q1	Q0
L	X	X	X	$\overline{Q4}_0$	$Q3_0$	$Q2_0$	$Q1_0$	$Q0_0$
H	L	L	L	H	L	L	L	L
H	L	L	H	$\overline{B4}$	B4	B3	B2	B1
H	L	H	L	$\overline{B4}$	B4	B3	B2	B1
H	L	H	H	$\overline{B4}$	B3	B2	B1	B0
H	H	L	L	B4	$\overline{B3}$	$\overline{B2}$	$\overline{B1}$	$\overline{B0}$
H	H	L	H	B4	$\overline{B4}$	$\overline{B3}$	$\overline{B2}$	$\overline{B1}$
H	H	H	L	B4	$\overline{B4}$	$\overline{B3}$	$\overline{B2}$	$\overline{B1}$
H	H	H	H	H	L	L	L	L

H = high level, L = low level, X = irrelevant
$\overline{Q4}_0 \ldots Q0_0$ = The logic level of the same output before the high-to-low- transition of G.
B4 . . .B0 = The logic level of the indicated multiplicand (b) input.

SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	LIMITS MIN	TYP	MAX	UNIT
t_w	Width of enable pulse			C_L = 15pF, R_L = 2kΩ	25			ns
t_{setup}	Input setup time	Any M input	Q		17↓			ns
		Any B input	Q		15↓			ns
t_{Hold}	Input hold time	Any M input	Q		0↓			ns
		Any B input	Q		0↓			ns
t_{PLH}	Propagation delay time Low-to-high-level output	Enable G	Any Q			22	35	ns
t_{PHL}	Propagation delay time High-to-low-level output	Enable G	Any Q			20	30	ns
t_{PLH}	Propagation delay time Low-to-high-level output	Any M input	Any Q			25	40	ns
t_{PHL}	Propagation delay time High-to-low-level output	Any M input	Any Q			22	35	ns
t_{PLH}	Propagation delay time Low-to-high-level output	Any B input	Any Q			27	42	ns
t_{PHL}	Propagation delay time High-to-low-level output	Any B input	Any Q			24	37	ns

Load circuits and typical waveforms are shown at the front of section.

TYPICAL APPLICATION DATA

Multiplication of the numbers 26 (multiplicand) by 29 (multiplier) in decimal, binary, and 2-bit-at-a-time-binary is shown here:

```
DECIMAL        BINARY                    2-BIT-AT-A-TIME BINARY
               Sign                          Sign
               Bit                           Bit
B  26          011010                        011010
M  29          011101                        (+2)(-1)(+1)
  234          011010  ┐               00000011010  ┐ 3
   52          000000  │ 6             111100110    ├ Partial
- 754          011010  ├ Partial       0110100      ┘ Products
              011010   │ Products     01011110010
             011010    │              Sign  Product
            000000     ┘              Bit
            01011110010
            Sign  Product
            Bit
```

Two points should be noted in the 2-bit-at-a-time-binary example above. First, in positioning the partial products beneath each other for final addition, each partial product is shifted two places to the left of the partial products above it instead of one place as is done in regular multiplication. Second, the msb of the partial product (the sign bit) is extended to the sign-bit column of the final answer. A substantial reduction of multiplication time, cost, and power is obtained by implementing a parallel partial-product-generation scheme using a 2-bit-at-a-time algorithm, followed by a Wallace Tree summation.

Partial-product-generation rules of the algorithm are:

1. Examine two bits of multiplier M plus the next lower bit. For the first partial product (PP1) the next lower bit is zero.

```
2^15 2^14 2^13 2^12 2^11 2^10 2^9 2^8 2^7 2^6 2^5 2^4 2^3 2^2 2^1 2^0 0
   PP8      PP7      PP6      PP5     PP4     PP3     PP2     PP1
```

2. Generate partial product (PPi) as shown in the following table:
3. Weight the partial products by indexing each two places left relative to the next-less-significant product.
4. Extend the most-significant bit of the partial product to the sign-bit place value of the final product.

```
                       EXAMPLE OF ALGORITHM

M = 29 = 011101          Operator         B = 26 = 011010
           010           Symbol

         110               +1B            00000011010
011                        -1B            111100110
                           +2B            0110100
```

The summation of these partial products was shown in the 2-bit-at-a-time binary multiplication example above.

The 54/74LS261 generates partial products according to this algorithm with two exceptions:

1. The one's complement is generated for the cases requiring the two's complement. The two's complement can be obtained by adding one to the one's complement; this rounding can be done by using one NAND gate and one AND gate as shown in Figure B.
2. The most-significant bit is complemented to reduce the hardware required to extend the sign bit. This extension can be accomplished by adding a hard-wired logic 1 in bit position 2^{2i+15} of each partial product and also in bit position 2^{16} of the first partial product (PP1).

MULTIPLER BITS FROM STEP 1			OPERATOR SYMBOL	TO OBTAIN PARTIAL PRODUCT
2^{2i-1}	2^{2i-2}	2^{2i-3}		
0	0	0	0	Replace multiplacand by zero
0	0	1	+1B	Copy multiplicand
0	1	0	+1B	Copy multiplicand
0	1	1	+2B	Shift multiplicand left one bit
1	0	0	−2B	Shift two's complement of multiplicand left one bit
1	0	1	−1B	Replace multiplicand by two's complement
1	1	0	−1B	Replace multiplicand by two's complement
1	1	1	0	Replace multiplicand by zero

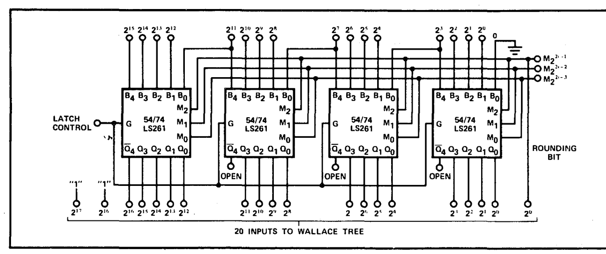


FIGURE A—FIRST PARTIAL PRODUCT, PP1

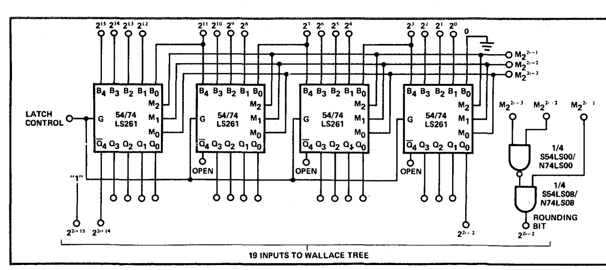


FIGURE B—OTHER PARTIAL PRODUCTS, PPi

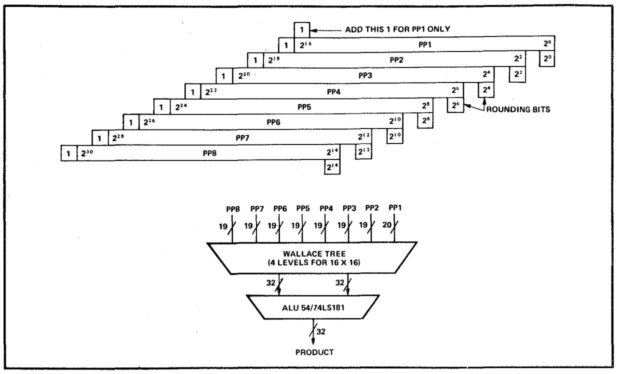


FIGURE C — MANIPULATION OF PARTIAL PRODUCTS FOR ENTRY INTO WALLACE TREE

In general, the 4 x 2 bit 54/74LS261 can be expanded for use in 4m x 2n bit multipliers. Partial-product generation uses m x n 54/74LS261s, m x n ÷ 16 54/74LS00s, and m x n ÷ 16 54/74LS08s. The size of the Wallace Tree and ALU requirements vary depending on the size of the problem. The count for the 16 x 16 bit multiplier is:

32	S54LS261/N74LS261
2	S54LS00/N74LS00
2	S54LS08/N74LS08
56	54H183/74H183*
7	S54LS181/N74LS181
2	S54LS182/N74LS182*

*Not currently available from Signetics.

QUAD 2-INPUT EXCLUSIVE-NOR GATE W/OPEN COLLECTOR OUTPUTS 54/74266

SPEED/PACKAGE AVAILABILITY

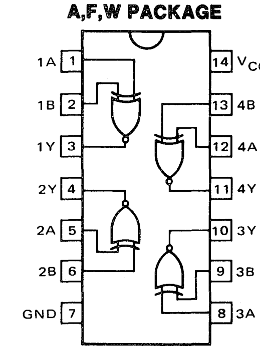
54LS F,W 74LS A

DESCRIPTION

The 54/74LS266 is comprised of four independent 2-input exclusive-NOR gates with open-collector outputs. The open-collector outputs permit tying outputs together for multiple-bit comparisons.

PIN CONFIGURATION

A,F,W PACKAGE



positive logic: $y=\overline{A \oplus B}=\overline{A}\overline{B}+AB$

SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

PARAMETER★	FROM (INPUT)	TEST CONDITIONS		LIMITS MIN	TYP	MAX	UNIT
t_{PLH}	A or B	Other input low	C_L = 15pF, R_L = 2kΩ		18	30	ns
t_{PHL}					18	30	
t_{PLH}	A or B	Other input high			18	30	ns
t_{PHL}					18	30	

★t_{PLH} = propagation delay time, low-to-high-level output
t_{PHL} = propagation delay time, high-to-low-level output
Load circuit and waveforms are shown at the front of the book.

FUNCTION TABLE

INPUTS A	INPUTS B	OUTPUT Y
L	L	H
L	H	L
H	L	L
H	H	H

H = high level, L = low level

QUAD $\overline{S}$-$\overline{R}$ LATCH — 54/74279

SPEED/PACKAGE AVAILABILITY

54 F,W 74 B

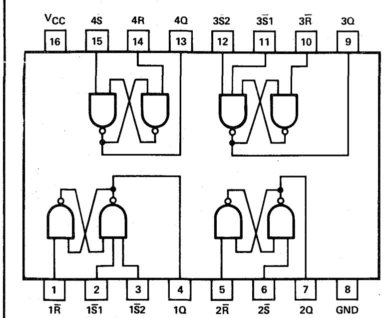
TRUTH TABLE

INPUTS		OUTPUT
$\overline{S}$*	$\overline{R}$	Q
H	H	Q_0
L	H	H
H	L	L
L	L	H[1]

H=high level
L=low level
Q_0=the level of Q before these input conditions were established
*For latches with double $\overline{S}$ inputs:
H=both $\overline{S}$ inputs high
L=one or both $\overline{S}$ inputs low
[1]This output is pseudo-stable; that is, it may not persist when the $\overline{S}$ and $\overline{R}$ inputs return to their inactive (H) level.

PIN CONFIGURATION

B,F,W PACKAGE



SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

TEST CONDITIONS			54/74 C_L=15pF R_L=400			
PARAMETER	FROM INPUT	TO OUTPUT	MIN	TYP	MAX	UNIT
Propagation delay time						
t_{PLH} Low-to-high	$\overline{S}$			12	22	ns
t_{PHL} High-to-low				9	15	
t_{PHL} High-to-low	$\overline{R}$			15	27	

Load circuit and typical waveforms are shown at the front of section.

9-BIT ODD/EVEN PARITY GENERATOR/CHECKER — 54/74280

SPEED/PACKAGE AVAILABILITY

54S F,W 74S A

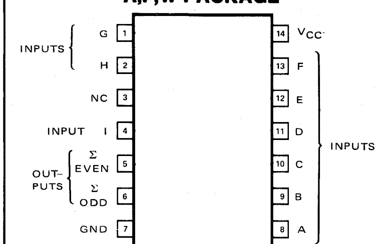
SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

TEST CONDITIONS			54/74S C_L=15pF R_L=180Ω			
PARAMETER	FROM INPUT	TO OUTPUT	MIN	TYP	MAX	UNIT
Propagation delay time						
t_{PLH} Low-to-high	Data	Σ Even		14	21	ns
t_{PHL} High-to-low				11.5	18	
t_{PLH} Low-to-high	Data	Σ Odd		14	21	
t_{PHL} High-to-low				11.5	18	

Load circuit and typical waveforms are shown at the front of section.

PIN CONFIGURATION

A,F,W PACKAGE

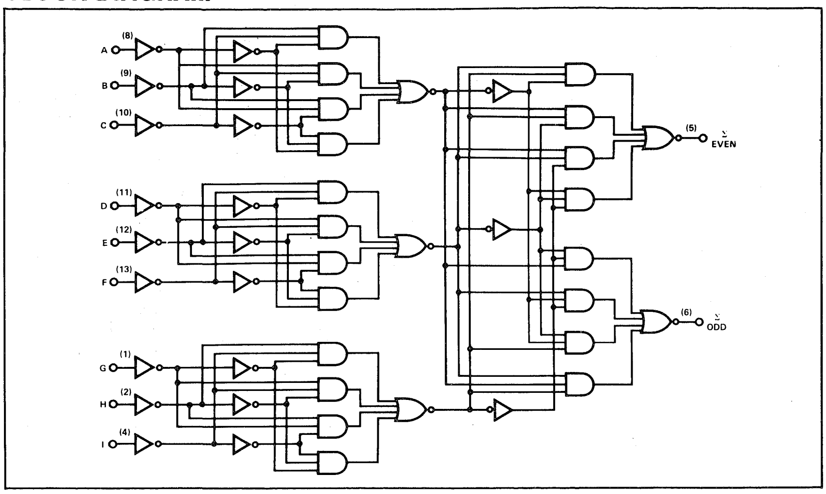


TRUTH TABLE

NUMBER OF INPUTS A THRU I THAT ARE HIGH	OUTPUTS	
	Σ EVEN	Σ ODD
0, 2, 4, 6, 8	H	L
1, 3, 5, 7, 9	L	H

H=high level L=low level

BLOCK DIAGRAM



4-BIT BINARY ADDER 54/74283

SPEED/PACKAGE AVAILABILITY

54LS F,W 74LS B

DESCRIPTION

This improved full adder performs the addition of two 4-bit binary numbers. The sum (Σ) outputs are provided for each bit and the resultant carry (C4) is obtained from the fourth bit. This adder features full internal look ahead across all four bits generating the carry term in ten nanoseconds typically. This provides the system designer with partial look-ahead performance at the economy and reduced package count of a ripple-carry implementation.

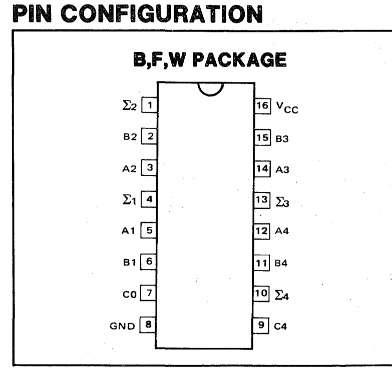
The adder logic, including the carry, is implemented in its true form meaning that the end-around carry can be accomplished without the need for logic or level inversion.

SWITCHING CHARACTERISTICS $V_{CC} = 5V$, $T_A = 25°C$

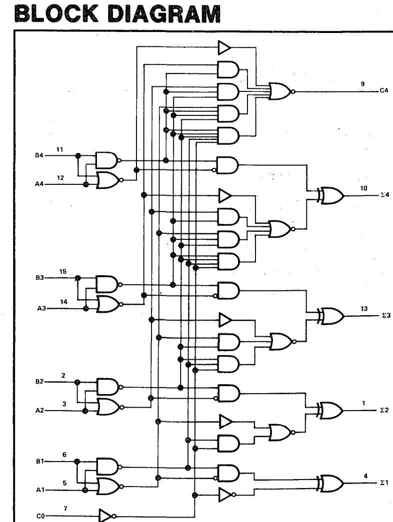
PARAMETER★	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	LIMITS MIN	TYP	MAX	UNIT
t_{PLH} t_{PHL}	C0	Any Σ	$C_L = 15pF$, $R_L = 2k\Omega$		16 15	24 24	ns
t_{PLH} t_{PHL}	A_i or B_i	Σ_i			15 15	24 24	ns
t_{PLH} t_{PHL}	C0	C4			11 11	17 17	ns
t_{PLH} t_{PHL}	A_i or B_i	C4			11 12	17 17	ns

★t_{PLH} = propagation delay time, low-to-high-level output
t_{PHL} = propagation delay time, high-to-low-level output
Load circuit and waveforms are shown at the front of the book.

PIN CONFIGURATION



BLOCK DIAGRAM



TRUTH TABLE

INPUT				OUTPUT WHEN CO=L			OUTPUT WHEN CO=H		
						WHEN C2=L			WHEN C2=H
A1 A3	B1 B3	A2 A4	B2 B4	Σ1 Σ3	Σ2 Σ4	C2 C4	Σ1 Σ3	Σ2 Σ4	C2 C4
L	L	L	L	L	L	L	H	L	L
H	L	L	L	H	L	L	L	H	L
L	H	L	L	H	L	L	L	H	L
H	H	L	L	L	H	L	H	H	L
L	L	H	L	L	H	L	H	H	L
H	L	H	L	H	H	L	L	L	H
L	H	H	L	H	H	L	L	L	H
H	H	H	L	L	L	H	H	L	H
L	L	L	H	L	H	L	H	H	L
H	L	L	H	H	H	L	L	L	H
L	H	L	H	H	H	L	L	L	H
H	H	L	H	L	L	H	H	L	H
L	L	H	H	L	L	H	H	L	H
H	L	H	H	H	L	H	L	H	H
L	H	H	H	H	L	H	L	H	H
H	H	H	H	L	H	H	H	H	H

H = high level, L = low level

NOTE: Input conditions at A1, B1, A, B2, and CO are used to determine outputs Σ1 and Σ2 and the value of the internal carry C2. The values at C2, A3, B3, A4, and B4, are then used to determine outputs Σ3, Σ4, and C4.

DECADE COUNTER 54/74290

SPEED/PACKAGE AVAILABILITY

54LS F,W 74LS A

DESCRIPTION

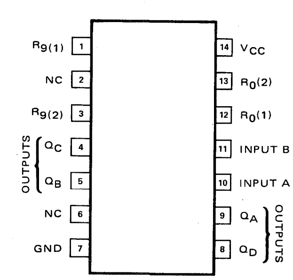
This monolithic counter contains four master-slave flip-flops and additional gating to provide a divide-by-two counter and a three-stage binary counter for which the count cycle length is divide-by-five.

The 54/74LS290 has a gated zero reset and has gated set-to-nine inputs for use in BCD nine's complement applications.

To use the maximum count length (decade or four-bit binary) of these counters, the B input is connected to the Q_A output. The input count pulses are applied to input A and the outputs are as described in the function table. A symmetrical divide-by-ten count can be obtained by connecting the Q_D output to the A input and applying the input count to the B input which gives a divide-by-ten square wave at output Q_A.

PIN CONFIGURATION

A,F,W PACKAGE



BCD COUNT SEQUENCE
(See Note A)

COUNT	OUTPUT Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

BI-QUINARY (5-2)
(See Note B)

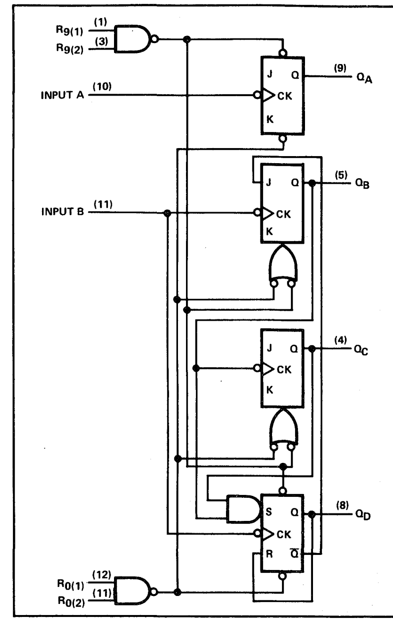
COUNT	OUTPUT Q_A	Q_D	Q_C	Q_B
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	H	L	L	L
6	H	L	L	H
7	H	L	H	L
8	H	L	H	H
9	H	H	L	L

RESET/COUNT FUNCTION TABLE

RESET INPUTS				OUTPUT			
$R_{0(1)}$	$R_{0(2)}$	$R_{9(1)}$	$R_{9(2)}$	Q_D	Q_C	Q_B	Q_A
H	H	L	X	L	L	L	L
H	H	X	L	L	L	L	L
X	X	H	H	H	L	L	H
X	L	X	L	COUNT			
L	X	L	X	COUNT			
L	X	X	L	COUNT			
X	L	L	X	COUNT			

NOTES:
A. Output Q_A is connected to input B for BCD count.
B. Output Q_D is connected to input A for bi-quinary count.
C. Output Q_A is connected to input B.
D. H = high level, L = low level, X = irrelevant

BLOCK DIAGRAM



The J and K inputs shown without connection are for reference only and are functionally at a high level.

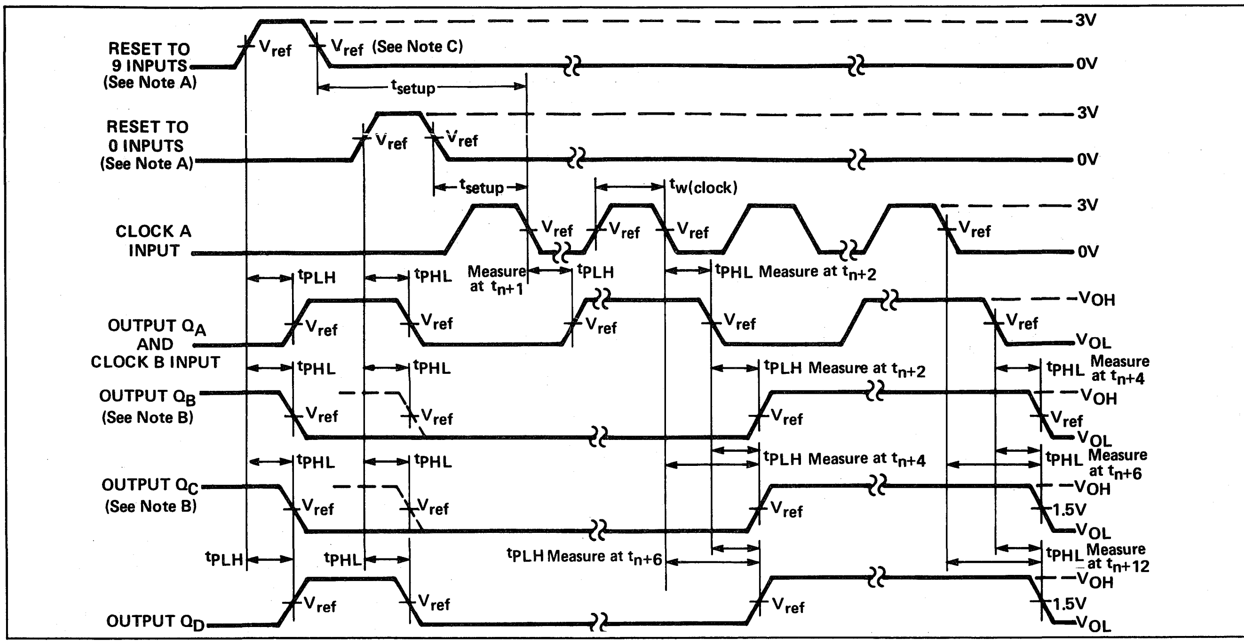
SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

PARAMETER★		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	LIMITS MIN	TYP	MAX	UNIT
f_{Count}		A	Q_A		32	42		MHz
		B	Q_B		16			
t_w	Input pulse width							
		A	Q		15			ns
		B	Q		30			ns
		Reset	Q		15			ns
t_{Setup}	Input setup time				25↓			ns
Propagation delay time								
t_{PLH}	Low-to-high level	A	Q_A	C_L = 15pF, R_L = 2kΩ		10	16	ns
t_{PHL}	High-to-low level					12	18	
t_{PLH}	Low-to-high level	A	Q_D			32	48	ns
t_{PHL}	High-to-low level					34	50	
t_{PLH}	Low-to-high level	B	Q_B			10	16	ns
t_{PHL}	High-to-low level					14	21	
t_{PLH}	Low-to-high level	B	Q_C			21	32	ns
t_{PHL}	Hign-to-low level					23	35	
t_{PLH}	Low-to-high level	B	Q_D			21	32	ns
t_{PHL}	High-to-low level	Set-to-0	Any			23	35	
t_{PHL}	High-to-low level					26	40	ns
t_{PLH}	Low-to-high level	Set-to-9	Q_A, Q_D			20	30	ns
t_{PHL}	High-to-low level		Q_B, Q_C			26	40	

t_{PLH} = low-to-high-level output
t_{PHL} = high-to-low-level output

DECADE COUNTER 54/74290

PARAMETER MEASUREMENT INFORMATION



VOLTAGE WAVEFORMS

NOTES:

A. Input pulses are supplied by a generator having the following characteristics: $t_r \leq$ 15ns, $t_f \leq$ 5ns, PRR = 1 MHz, duty cycle = 50%, $Z_{out} \approx$ 50 ohms.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N916 or 1N3064.
D. Each reset input is tested separately with the other reset at 4.5V.
E. Reference waveforms are shown with dashed lines.
F. V_{ref} = 1.3V.

4-BIT BINARY COUNTER 54/74293

SPEED/PACKAGE AVAILABILITY

54LS F,W   74LS A

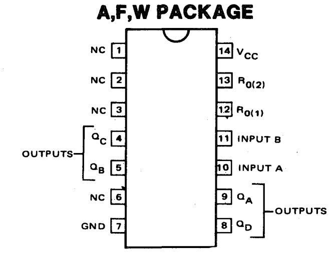
DESCRIPTION

This monolithic counter contains four master-slave flip-flops and a gated zero reset to provide a divide-by-two counter and a three-stage binary counter for which the count cycle length is divide-by-eight.

To use the maximum count length (decade or four-bit binary) of this counter, the B input is connected to the Q_A output. The input count pulses are applied to input A and the outputs are as described in the function table.

PIN CONFIGURATION

A,F,W PACKAGE

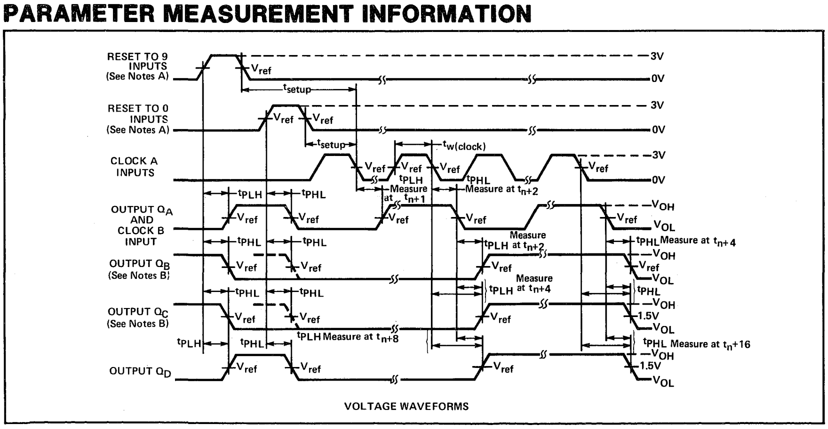


SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

PARAMETER★		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	LIMITS MIN	TYP	MAX	UNIT
f_{Count}		A	Q_A		32	42		MHz
		B	Q_B		16			
t_w	Input pulse width	A	Q		15			ns
		B	Q		30			ns
		Reset	Q		15			ns
t_{Setup}	Input setup time				25↓			ns
t_{PLH}		A	Q_A	C_L = 15pF, R_L = 400Ω		10	16	ns
t_{PHL}						12	18	
t_{PLH}		A	Q_D			46	70	ns
t_{PHL}						46	70	
t_{PLH}		B	Q_B			10	16	ns
t_{PHL}						14	21	
t_{PLH}		B	Q_C			21	32	ns
t_{PHL}						23	35	
t_{PLH}		B	Q_D			34	51	ns
t_{PHL}						34	51	
t_{PHL}		Set-to-0	Any			26	40	ns

★f_{max} = maximum count frequency
t_{PLH} = propagation delay time, low-to-high-level output
t_{PHL} = propagation delay time, high-to-low-level output

PARAMETER MEASUREMENT INFORMATION



VOLTAGE WAVEFORMS

NOTES:
A. Input pulses are supplied by a generator having the following characteristics: $t_r \leq$ 15 ns, $t_f \leq$ 5 ns, PRR = 1 MHz, duty cycle = 50%, $Z_{out} \approx$ 50 ohms.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N916 or 1N3064.
D. Each reset input is tested separately with the other reset at 4.5 V.
E. Reference waveforms are shown with dashed lines.
F. V_{ref} = 1.3 V.

COUNT SEQUENCE

(See Note C)

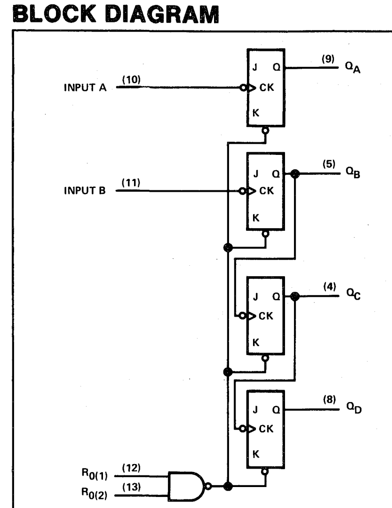
COUNT	OUTPUT Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

RESET/COUNT FUNCTION TABLE

RESET INPUTS $R_{0(1)}$	$R_{0(2)}$	OUTPUT Q_D	Q_C	Q_B	Q_A
H	H	L	L	L	L
L	X	COUNT			
X	L	COUNT			

NOTES:
A. Output Q_A is connected to input B for BCD count.
B. Output Q_D is connected to input A for bi-quinary count.
C. Output Q_A is connected to input B.
D. H = high level, L = low level, X = irrelevant

BLOCK DIAGRAM



The J and K inputs shown without connection are for reference only and are functionally at a high level.

DESCRIPTION

These 4-bit registers feature parallel inputs, parallel outputs, and clock, serial, mode, and output control inputs. The registers have three modes of operation:

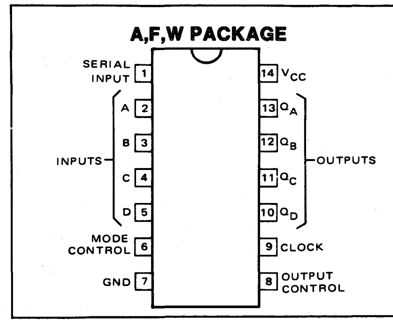
- Parallel (broadside) load
- Shift right (the direction Q_A toward Q_D)
- Shift left (the direction Q_D toward Q_A)

Parallel loading is accomplished by applying the four bits of data and taking the mode control input high. The data is loaded into the associated flip-flops and appears at the outputs after the high-to-low transition of the clock input. During parallel loading, the entry of serial data is inhibited.

Shift right is accomplished when the mode control is low; shift left is accomplished when the mode control is high by connecting the output of each flip-flop to the parallel input of the previous flip-flop (Q_D to input C, etc.) and serial data is entered at input D.

When the output control is high, the normal logic levels of the four outputs are available for driving the loads or bus lines. The outputs are disabled independently from the level of the clock by a low logic level at the output control input. The outputs then present a high impedance and neither load nor drive the bus line; however, sequential operation of the registers is not affected.

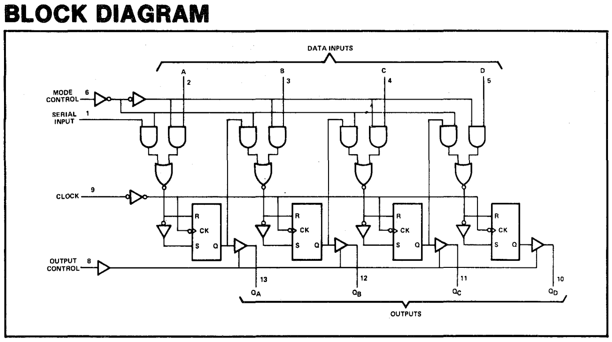
PIN CONFIGURATION



SPEED/PACKAGE AVAILABILITY

54LS F,W 74LS A

BLOCK DIAGRAM



FUNCTION TABLE

INPUTS							OUTPUTS			
MODE CONTROL	CLOCK	SERIAL	PARALLEL A	B	C	D	Q_A	Q_B	Q_C	Q_D
H	H	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
H	↓	X	a	b	c	d	a	b	c	d
H	↓	X	Q_B†	Q_C†	Q_D†	d	Q_{Bn}	Q_{Cn}	Q_{Dn}	d
L	H	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
L	↓	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}
L	↓	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}
When the output control is low, the outputs are disabled to the high impedance state, however, sequential operation of the registers is not affected.										

†Shifting left requires external connection of Q_B to A, Q_C to B, and Q_D to C. Serial data is entered at input D.
H = high level (steady state), L = low level (steady state), X = irrelevant (any input, including transitions)
↓ = transition from high to low level.
a, b, c, d = the level of steady state input at inputs A, B, C, or D, respectively.
Q_{A0}, Q_{B0}, Q_{C0}, Q_{D0} = the level of Q_A, Q_C, or Q_D, respectively, before the indicated steady state input conditions were established.
Q_{An}, Q_{Bn}, Q_{Cn}, Q_{Dn} = the level of Q_A, Q_B, Q_C, or Q_D, respectively, before the most recent ↓ transition of the clock.

SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

PARAMETER		TEST CONDITIONS	LIMITS			
			MIN	TYP	MAX	UNIT
f_{Clock}	Clock frequency		20	28		MHz
$t_{w(Clock)}$	Width of clock pulse		25			ns
t_{Setup}	Input setup time, high or low level		20↓			ns
t_{Hold}	Input hold time, high or low level		20↓			ns
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 15pF,		40	32	ns
t_{PHL}	Propagation delay time, high-to-low-level output	R_L = 2kΩ		47	36	ns
t_{ZH}	Output enable time to high level			15	25	ns
t_{ZL}	Output enable time to low level			21	30	ns
t_{HZ}	Output disable time from high level			39	60	ns
t_{LZ}	Output disable time from low level			32	50	ns

Load circuit and waveforms are shown at the front of the book.

QUAD 2-INPUT MULTIPLEXER WITH STORAGE 54/74298

SPEED/PACKAGE AVAILABILITY

54 F,W 74 B

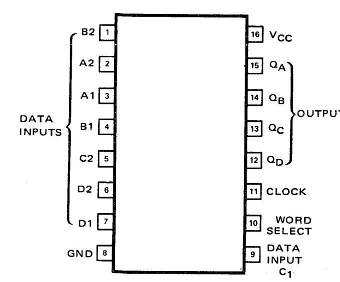
SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

TEST CONDITIONS		54/74 C_L=15pF R_L=400			
PARAMETER		MIN	TYP	MAX	UNIT
t_W	Width of input pulse	20			ns
t_{Setup}	Input setup time Data Word select	 15 25			ns
t_{Hold}	Input hold time Data Word select	 5 0			ns
Propagation delay time					
t_{PLH}	Low-to-high		18	27	ns
t_{PHL}	High-to-low		21	32	

Load circuit and typical waveforms are shown at the front of section.

PIN CONFIGURATION

B,F,W PACKAGE



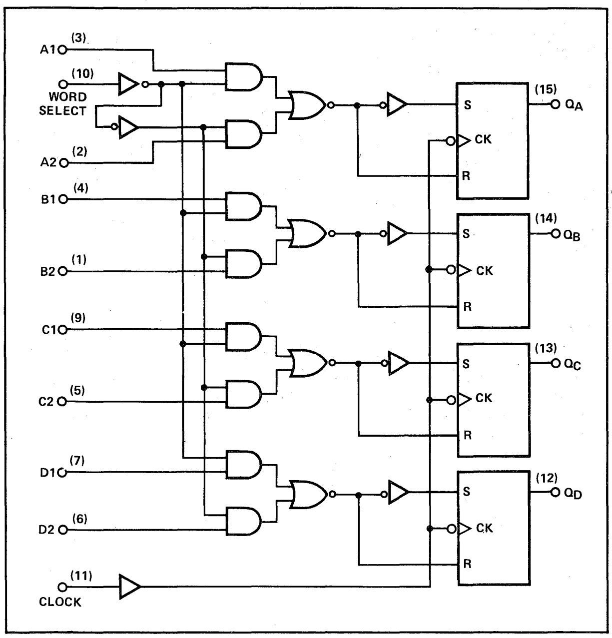
TRUTH TABLE

INPUTS		OUTPUTS			
WORD SELECT	CLOCK	Q_A	Q_B	Q_C	Q_D
L	↓	A1	B1	C1	D1
H	↓	A2	B2	C2	D2
X	H	Q_{AO}	Q_{BO}	Q_{CO}	Q_{DO}

H = high level (steady state)
L = low level (steady state)
X = irrelevant (any input, including transitions)
↓ = transition from high to low level
A1, A2, etc. = the level of steady-state input at A1, A2, etc.
Q_{AO}, Q_{BO}, etc. = the level of Q_A, Q_B, etc. entered on the last ↓ transition of the clock input.

QUAD 2-INPUT MULTIPLEXER WITH STORAGE — 54/74298

BLOCK DIAGRAM



TTL 256x1 RAM-OPEN COLLECTOR — 54/74301

SPEED/PACKAGE AVAILABILITY AND ELECTRICAL CHARACTERISTICS

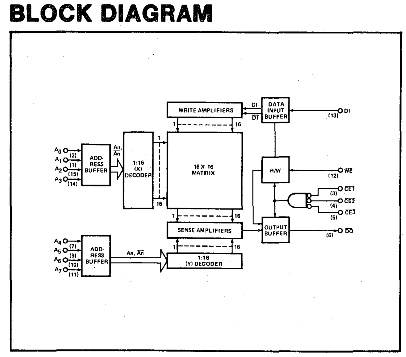
Refer to Bipolar Memory Section

TRUTH TABLE

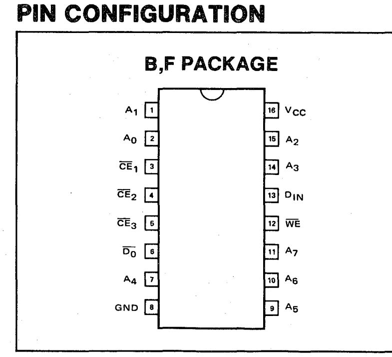
MODE	$\overline{CE}$*	$\overline{WE}$	D_{IN}	$\overline{D}_{OUT}$ 54/74S301
READ	0	1	X	STORED $\overline{DATA}$
WRITE "0"	0	0	0	1
WRITE "1"	0	0	1	1
DISABLED	1	X	X	1

*"0" = all $\overline{CE}$ inputs low; "1" = one or more $\overline{CE}$ inputs high.
X = don't care.

BLOCK DIAGRAM



PIN CONFIGURATION



SPEED/PACKAGE AVAILABILITY

54LS F,W 74LS A

FUNCTION TABLE

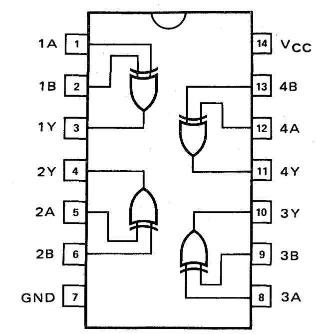
(EACH GATE)

INPUTS		OUTPUT
A	B	
L	L	L
L	H	H
H	L	H
H	H	L

H = high level
L = low level

PIN CONFIGURATION

A,F,W PACKAGE



POSITIVE LOGIC: $Y = A \oplus B = \bar{A}B + A\bar{B}$

SWITCHING CHARACTERISTICS $V_{CC} = 5V, T_A = 25°C$

PARAMETER★	FROM (INPUT)	TEST CONDITIONS		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT
t_{PLH}	A or B	Other input low	$C_L = 15pF$, $R_L = 2k\Omega$		10	23	ns
t_{PHL}					10	17	
t_{PLH}	A or B	Other input high			10	30	ns
t_{PHL}					10	22	

★t_{PLH} = propagation delay ti

SPEED/PACKAGE AVAILABILITY

54LS F,W 74LS B

DESCRIPTION

The S54LS670 and N74LS670 MSI 16-bit TTL register files incorporate the equivalent of 98 gates. The register file is organized as 4 words of 4 bits each and separate on-chip decoding is provided for addressing the four word locations to either write-in or retrieve data. This permits simultaneous writing into one location and reading from another word location.

Four data inputs are available which are used to supply the 4-bit word to be stored. Location of the word is determined by the write-address inputs A and B in conjunction with a write-enable signal. Data applied at the inputs should be in its true form. That is, if a high-level signal is desired from the output, a high-level is applied at the data input for that particular bit location. The latch inputs are arranged so that new data will be accepted only if both internal address gate inputs are high. When this condition exists, data at the D input is transferred to the latch output. When the write-enable input, G_W, is high, the data inputs are inhibited and their levels can cause no change in the information stored in the internal latches. When the read-enable input, G_R, is high, the data outputs are inhibited and go into the high-impedance state.

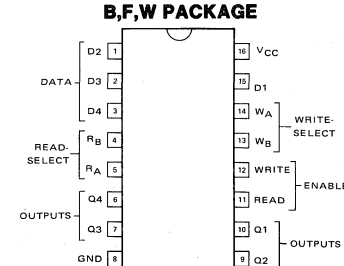
The individual address lines permit direct acquisition of data stored in any four of the latches. Four individual decoding gates are used to complete the address for reading a word. When the read address is made in conjunction with the read-enable signal, the word appeaars at the four outputs.

This arrangement—data-entry addressing separate from data-read addressing and individual sense line—eliminates recovery times, permits simultaneous reading and writing, and is limited in speed only by the write time (27 nanoseconds typical). The register file has a nondestructive readout in that data is not lost when addressed.

All inputs except read enable and write enable are buffered to lower the drive requirements to one Series 54LS/74LS standard load, and input-clamping diodes minimize switching transients to simplify system design. High-speed, double-ended AND-OR-INVERT gates are employed for the read-address function and have high-sink-current, three-state outputs. Up to 128 of these outputs may be wire-AND connected for increasing the capacity up to 512 words. Any number of these registers may be paralleled to provide n-bit word length.

PIN CONFIGURATION

B,F,W PACKAGE



WRITE FUNCTION TABLE

(See Notes A, B and C)

WRITE INPUTS			WORD			
W_B	W_A	G_W	0	1	2	3
L	L	L	Q=D	Q_0	Q_0	Q_0
L	H	L	Q_0	Q=D	Q_0	Q_0
H	L	L	Q_0	Q_0	Q=D	Q_0
H	H	L	Q_0	Q_0	Q_0	Q=D
X	X	H	Q_0	Q_0	Q_0	Q_0

READ FUNCTION TABLE

(See Notes A and D)

READ INPUTS			OUTPUTS			
R_B	R_A	G_R	Q1	Q2	Q3	Q4
L	L	L	W0B1	W0B2	W0B3	W0B4
L	H	L	W1B1	W1B2	W1B3	W1B4
H	L	L	W2B1	W2B2	W2B3	W2B4
H	H	L	W3B1	W3B2	W3B3	W3B4
X	X	H	Z	Z	Z	Z

NOTES:

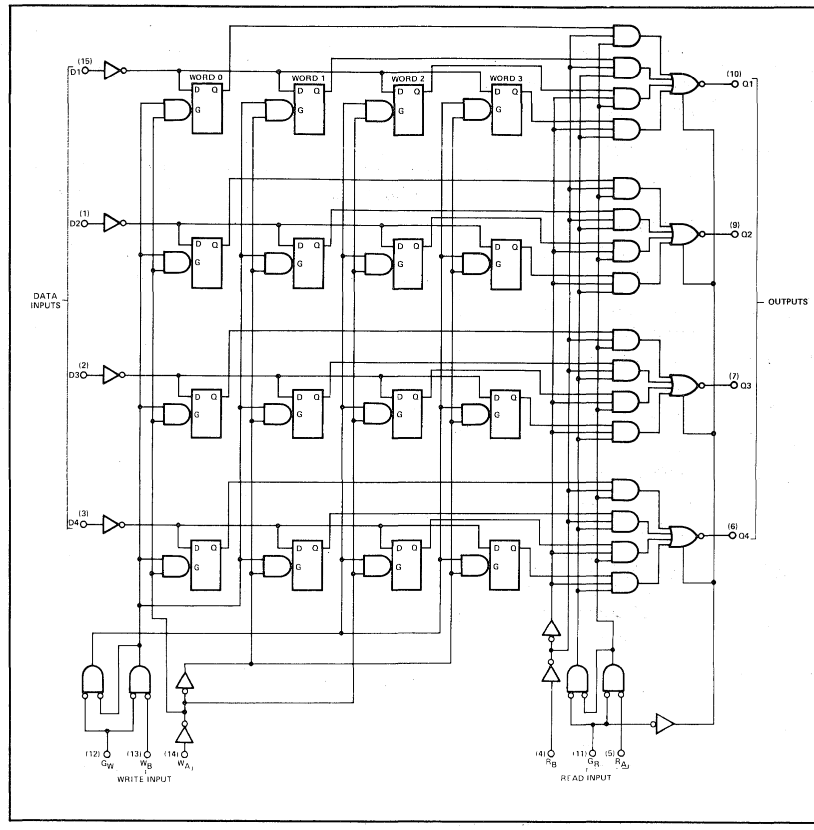
A. H = high level, L = low level, X = irrelevant, Z = high impedance (off).

B. (Q = D) = The four selected internal flip-flop outputs will assume the inverse of the states applied to the four external data inputs.

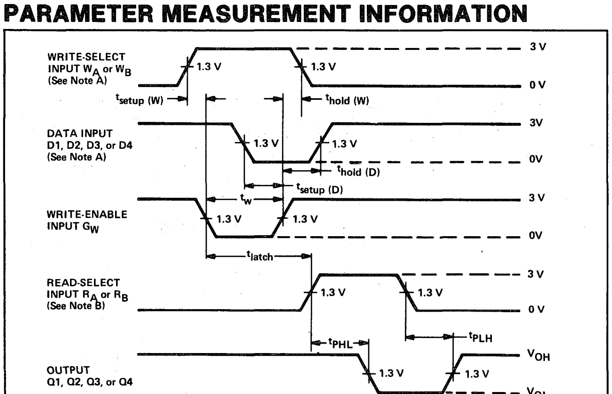
C. Q_0 = the level of Q before the indicated input conditions were established.

D. W0B1 = The first bit of word 0, etc.

FUNCTIONAL BLOCK DIAGRAM



PARAMETER MEASUREMENT INFORMATION



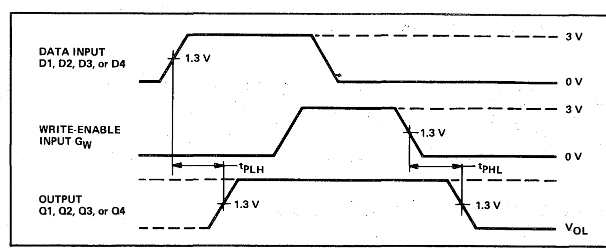
VOLTAGE WAVEFORMS (S1 AND S2 ARE CLOSED)

NOTES:

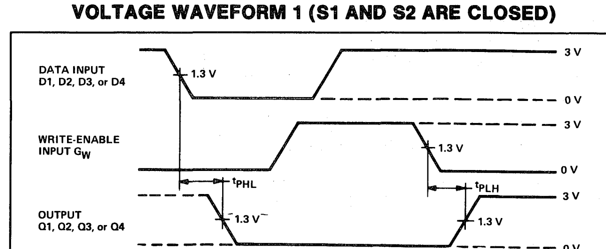
A. High-level input pulses at the select and data inputs are illustrated; however, times associated with low-level pulses are measured from the same reference points.

B. When measuring delay times from a read-select input, the read-enable input is low.

C. Input waveforms are supplied by generators having the following characteristics: PRR ≤ 2 MHz, $Z_{out} \approx 50\ \Omega$, duty cycle ≤ 50%, $t_r \leq 15$ ns, $t_f \leq 6$ ns.



VOLTAGE WAVEFORM 1 (S1 AND S2 ARE CLOSED)



VOLTAGE WAVEFORM 2 (S1 AND S2 ARE CLOSED)

NOTES:

A. Each select address is tested. Prior to the start of each of the above tests both write and read address inputs are stabilized with $W_A = R_A$ and $W_B = R_B$. During the test G_R is low.

B. Input waveforms are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_{out} \approx 50\ \Omega$, duty cycle ≤ 50%, $t_r \leq 15$ ns, $t_f \leq 6$ ns.

Load circuit is shown at front of book (for three state outputs).

SWITCHING CHARACTERISTICS $V_{CC} = 5V$, $T_A = 25°C$

	PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	LIMITS MIN	TYP	MAX	UNIT
t_W	Width of write-enable or read-enable pulse				25			ns
t_{Setup}	Input setup time (See fig. 2)	Data input Write-select	Write-enable Write-enable		10 15			ns
t_{Hold}	Input hold time (See note 2 & fig. 2)	Data input Write-select	Write-enable Write-enable		15 5			ns
t_{Latch}	Latch time for new data (Note 3)				25			ns
Propagation delay time								
t_{PLH} t_{PHL}	Low-to-high High-to-low	Read select	Any Q			23 25	40 45	ns
t_{PLH} t_{PHL}	Low-to-high High-to-low	Write enable	Any Q	$C_L = 15pF$, $R_L = 2k\Omega$		26 28	45 50	ns
t_{PLH} t_{PHL}	Low-to-high High-to-low	Data	Any Q			25 23	45 40	ns
t_{ZH}	Output enable time to high level					15	35	ns
t_{ZL}	Output enable time to low level		Any Q			22	40	
t_{HZ}	Output disable time from high level	Read enable				30	50	ns
t_{LZ}	Output disable time from low level					16	35	

NOTES:
1. Voltage values are with respect to network ground terminal.
2. Write-select setup time will protect the data written into the previous address. If protection of data in the previous address is not required, $t_{Setup(w)}$ can be ignored as any address selection sustained for the final 30 ns of the write-enable pulse and during $t_{Hold(w)}$ will result in data being written into that location. Depending on the duration of the input conditions, one or a number of previous addresses may have been written into.
3. Latch time is the time allowed for the internal output of the latch to assume the state of new data. See Figure 2. This is important only when attempting to read from a location immediately after that location has received new data.

4-BIT SHIFT REGISTER 9300

SPEED/PACKAGE AVAILABILITY

S9300 F,W N9300 B

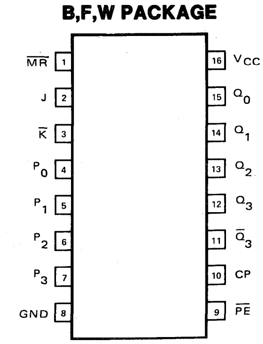
TRUTH TABLE

J	$\overline{K}$	Q at t
L	L	L
L	H	Q at t (no change)
H	L	$\overline{Q}$ at t (toggles)
H	H	H

$\overline{PE}$ = High, $\overline{MR}$ = High. (n + 1) indicates state after next clock.

PIN CONFIGURATION

B,F,W PACKAGE



SWITCHING CHARACTERISTICS $V_{CC} = 5V$, $T_A = 25°C$

TEST CONDITIONS		9300 $C_L = 15pf$			
PARAMETER		**MIN**	**TYP**	**MAX**	**UNIT**
t_{PD+}	Turn off delay		20	35	ns
t_{PD-}	Turn on delay		25	45	ns
f_{SR}	Shift right register	15	25		MHz
CP_{pw}	Clock pulse width	35	15		ns
t_s	Setup time	35	17		ns
t_r	Release time		16	0	ns
$t_{s(\overline{PE})}$	Setup time for $\overline{PE}$	45	26		ns
$t_{r(\overline{PE})}$	Release time for $\overline{PE}$		25	10	ns
$t_{PD-(\overline{MR})}$	Reset time for $\overline{MR}$		35		ns
$t_{rec}(\overline{MR})$	Recovery time for $\overline{MR}$		20		ns
$\overline{MR}_{pw}$	Min reset pulse width		15		ns

NOTE:
For electrical specifications, refer to 54/74195 data sheet.
Load circuit and typical waveforms shown in 54/74195 section.

ONE-OF-TEN DECODER 9301

SPEED/PACKAGE AVAILABILITY

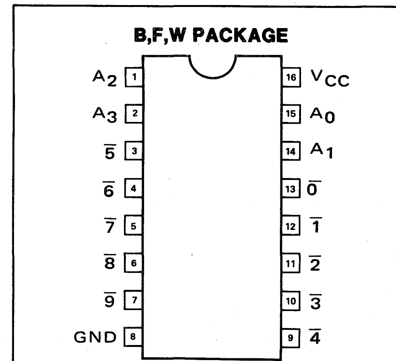
S9301 F,W N9301 B

TRUTH TABLE

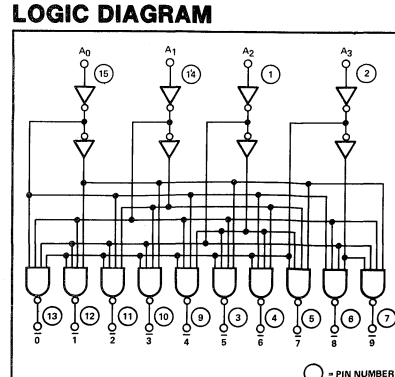
A_0	A_1	A_2	A_3	$\overline{0}$	$\overline{1}$	$\overline{2}$	$\overline{3}$	$\overline{4}$	$\overline{5}$	$\overline{6}$	$\overline{7}$	$\overline{8}$	$\overline{9}$
L	L	L	L	L	H	H	H	H	H	H	H	H	H
H	L	L	L	H	L	H	H	H	H	H	H	H	H
L	H	L	L	H	H	L	H	H	H	H	H	H	H
H	H	L	L	H	H	H	L	H	H	H	H	H	H
L	L	H	L	H	H	H	H	L	H	H	H	H	H
H	L	H	L	H	H	H	H	H	L	H	H	H	H
L	H	H	L	H	H	H	H	H	H	L	H	H	H
H	H	H	L	H	H	H	H	H	H	H	L	H	H
L	L	L	H	H	H	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L
L	H	L	H	H	H	H	H	H	H	H	H	H	H
H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H
H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	H	H	H	H	H	H	H	H	H	H	H	H	H
H	H	H	H	H	H	H	H	H	H	H	H	H	H

NOTES:
For electrical characteristics, refer to 8252 data sheet.
H = High voltage level
L = Low voltage level

PIN CONFIGURATION



LOGIC DIAGRAM



DUAL 4-INPUT MULTIPLEXER 9309

SPEED/PACKAGE AVAILABILITY

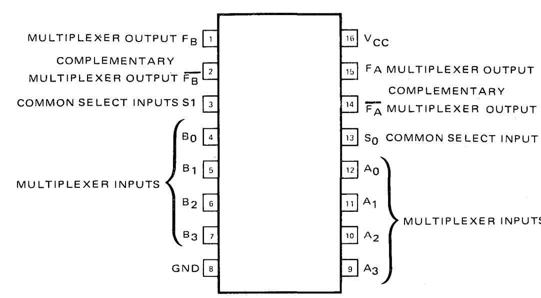
S9309 F,W N9309 B,F

TRUTH TABLE

SELECT INPUTS		INPUTS				OUTPUTS	
S_0	S_1	A_0	A_1	A_2	A_3	F_A	$\bar{F}_A$
L	L	L	X	X	X	L	H
L	L	H	X	X	X	H	L
H	L	X	L	X	X	L	H
H	L	X	H	X	X	H	L
L	H	X	X	L	X	L	H
L	H	X	X	H	X	H	L
H	H	X	X	X	L	L	H
H	H	X	X	X	H	H	L
S_0	S_1	B_0	B_1	B_2	B_3	F_B	$\bar{F}_B$
L	L	L	X	X	X	L	H
L	L	H	X	X	X	H	L
H	L	X	L	X	X	L	H
H	L	X	H	X	X	H	L
L	H	X	X	L	X	L	H
L	H	X	X	H	X	H	L
H	H	X	X	X	L	L	H
H	H	X	X	X	H	H	L

L = low voltage level
H = high voltage level
X = either high or low logic level

PIN CONFIGURATION



SWITCHING CHARACTERISTICS $V_{CC} = 5V$, $T_A = 25°C$

TEST CONDITIONS				9309 $C_L = 15pF$		
PARAMETER	FROM INPUT	TO OUTPUT	MIN	TYP	MAX	UNIT
t_{PD+} Turn off delay	S_0	Z_a		24 or 24	32 36	ns
t_{PD-} Turn on delay				24 or 24	32 36	ns

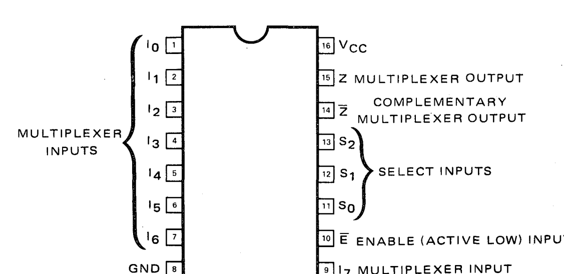
Load circuit and typical waveforms are shown at the front of section.

8-INPUT MULTIPLEXER 9312

SPEED/PACKAGE AVAILABILITY

S9312 F,W N9312 B,F

PIN CONFIGURATION



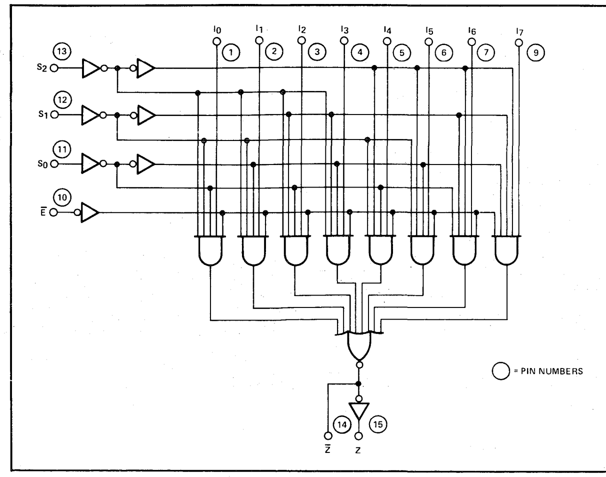
8-INPUT MULTIPLEXER 9312

TRUTH TABLE

$\overline{E}$	S_2	S_1	S_0	I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7	$\overline{Z}$	Z
H	X	X	X	X	X	X	X	X	X	X	X	H	L
L	L	L	L	L	X	X	X	X	X	X	X	H	L
L	L	L	L	H	X	X	X	X	X	X	X	L	H
L	L	L	H	X	L	X	X	X	X	X	X	H	L
L	L	L	H	X	H	X	X	X	X	X	X	L	H
L	L	H	L	X	X	L	X	X	X	X	X	H	L
L	L	H	L	X	X	H	X	X	X	X	X	L	H
L	L	H	H	X	X	X	L	X	X	X	X	H	L
L	L	H	H	X	X	X	H	X	X	X	X	L	H
L	H	L	L	X	X	X	X	L	X	X	X	H	L
L	H	L	L	X	X	X	X	H	X	X	X	L	H
L	H	L	H	X	X	X	X	X	L	X	X	H	L
L	H	L	H	X	X	X	X	X	H	X	X	L	H
L	H	H	L	X	X	X	X	X	X	L	X	H	L
L	H	H	L	X	X	X	X	X	X	H	X	L	H
L	H	H	H	X	X	X	X	X	X	X	L	H	L
L	H	H	H	X	X	X	X	X	X	X	H	L	H

H = high voltage level
L = low voltage level
X = level does not affect output.

LOGIC DIAGRAM

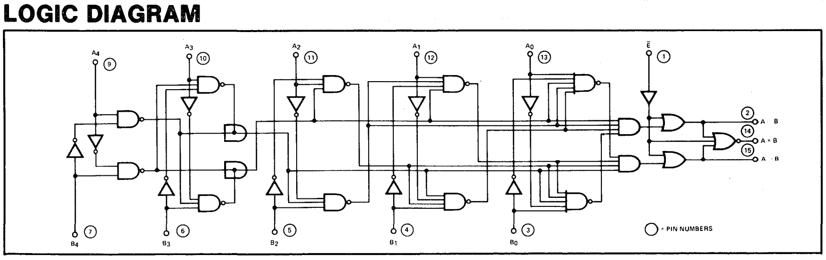


5-BIT COMPARATOR 9324

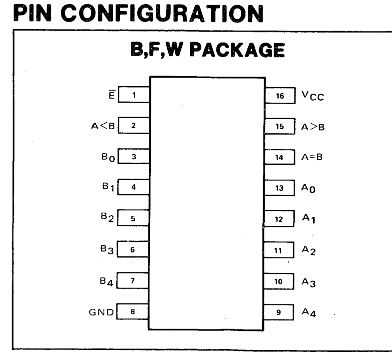
SPEED/PACKAGE AVAILABILITY

S9324 F,W N9324 B,F

LOGIC DIAGRAM



PIN CONFIGURATION



SWITCHING CHARACTERISTICS $V_{CC} = 5V$, $T_A = 25°C$

TEST CONDITIONS			9324 $C_L = 15pF$ $R_L = 400\Omega$			
PARAMETER	FROM INPUT	TO OUTPUT	MIN	TYP	MAX	UNIT
Propagation delay time						
t_{PLH} Low-to-high	A_2	A>B		23	28	ns
t_{PHL} High-to-low				19	23	
t_{PLH} Low-to-high	A_2	A=B		40	45	
t_{PHL} High-to-low				35	42	
t_{PLH} Low-to-high	A_2	A<B		29	37	
t_{PHL} High-to-low				24	29	
t_{PLH} Low-to-high	$\overline{E}$	A=B		12	17	
t_{PHL} High-to-low				10	16	

Load circuit and typical waveforms are shown at the front of section.

TRUTH TABLE

$\overline{E}$	Ay	By	A<B	A>B	A=B
H	X	X	L	L	L
L	Word A=Word B		L	L	H
L	Word A>Word B		L	H	L
L	Word B>Word A		H	L	L

H = high voltage level
L = low voltage level
X = either high or low voltage level

8-BIT ADDRESSABLE LATCH 9334

SPEED/PACKAGE AVAILABILITY

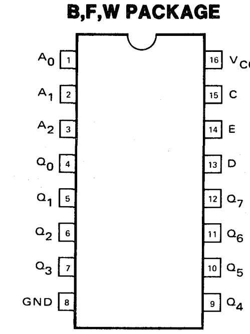
S9334 F,W N9334 B

TRUTH TABLE

$\overline{C}$	$\overline{E}$	D	A_0	A_1	A_2	Q_0	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7	MODE
						PRESENT OUTPUT STATES								
L	H	X	X	X	X	L	L	L	L	L	L	L	L	CLEAR
L	L	L	L	L	L	L	L	L	L	L	L	L	L	DEMULTIPLEX
L	L	H	L	L	L	H	L	L	L	L	L	L	L	
L	L	L	H	L	L	L	L	L	L	L	L	L	L	
L	L	H	H	L	L	L	H	L	L	L	L	L	L	
L	L	H	H	H	H	L	L	L	L	L	L	L	H	
H	H	X	X	X	X	Q_{N-1} →								MEMORY
H	L	L	L	L	L	L	Q_{N-1}	Q_{N-1}	Q_{N-1} →					ADDRESSABLE LATCH
H	L	H	L	L	L	H	Q_{N-1}	Q_{N-1} →						
H	L	L	H	L	L	Q_{N-1}	L	Q_{N-1} →						
H	L	H	H	L	L	Q_{N-1}	H	Q_{N-1} →						
H	L	L	H	H	H	Q_{N-1} →						Q_{N-1}	L	
H	L	H	H	H	H	Q_{N-1} →						Q_{N-1}	H	

X = don't care condition
L = low voltage level
H = high voltage level
Q_{N-1} = previous output state

PIN CONFIGURATION

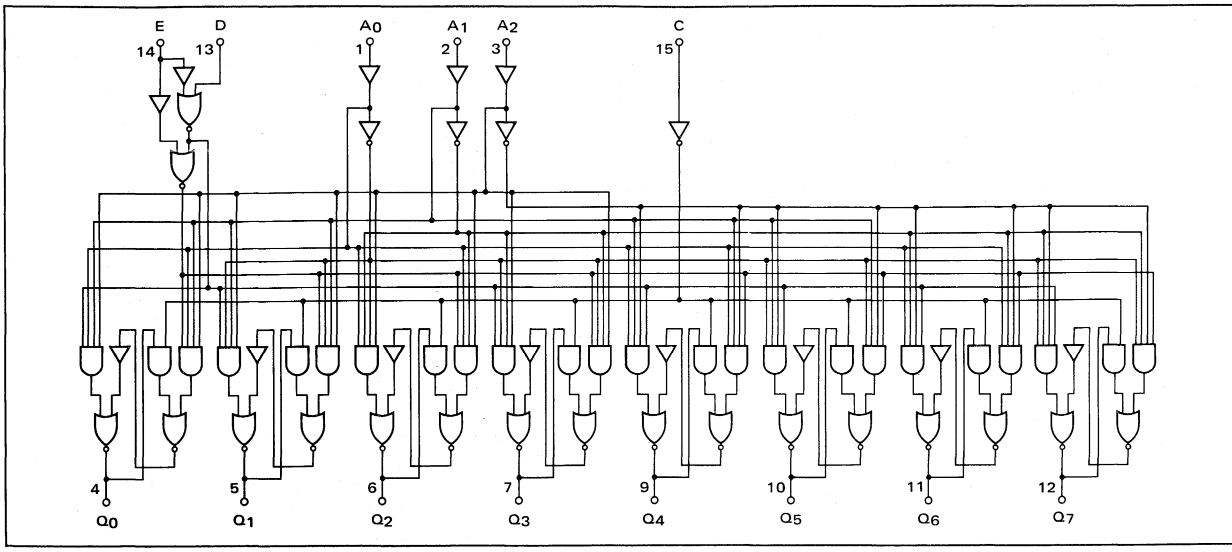


SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

TEST CONDITIONS				9334 C_L=15pF R_L=680Ω			
PARAMETER		FROM INPUT	TO OUTPUT	MIN	TYP	MAX	UNIT
Propagation delay time							
t_{PLH}	Low-to-high	Delay enable	Output		19	23	ns
t_{PHL}	High-to-low				16	24	
t_{PLH}	Low-to-high	Delay Data	Output		28	35	
t_{PHL}	High-to-low				16	24	
t_{PLH}	Low-to-high	Delay Address	Output			35	
t_{PHL}	High-to-low					35	
t_{PHL}	High-to-low	Delay Clear	Output		21	25	

Load circuit and typical waveforms are shown at the front of section.

LOGIC DIAGRAM

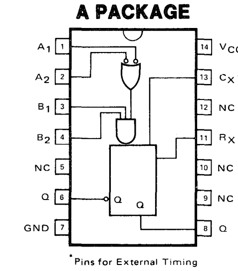


RETRIGGERABLE MONOSTABLE MULTIVIBRATOR 9601

SPEED/PACKAGE AVAILABILITY

N9601 A,F

PIN CONFIGURATION



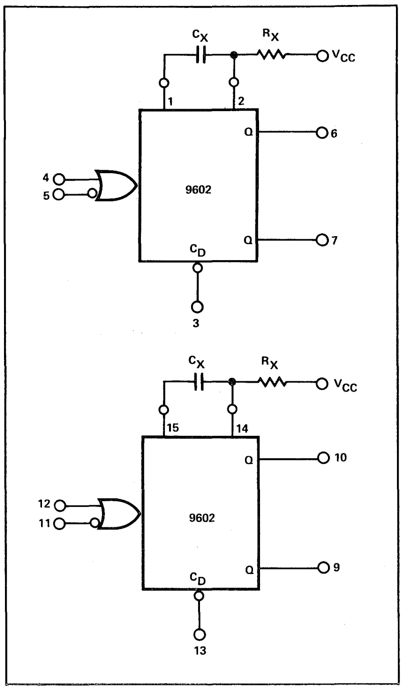
Load circuit and waveform shown at front of section.

LOGIC

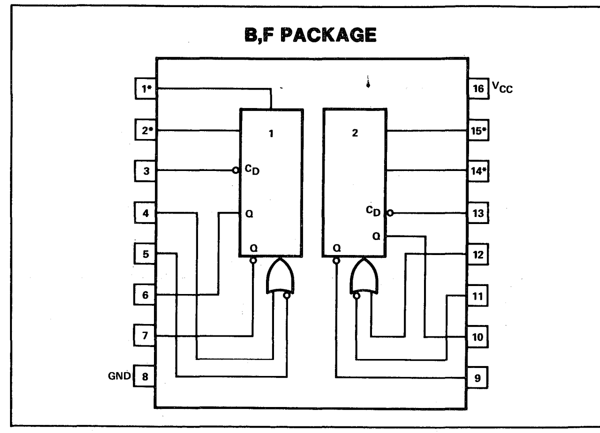
SPEED/PACKAGE AVAILABILITY

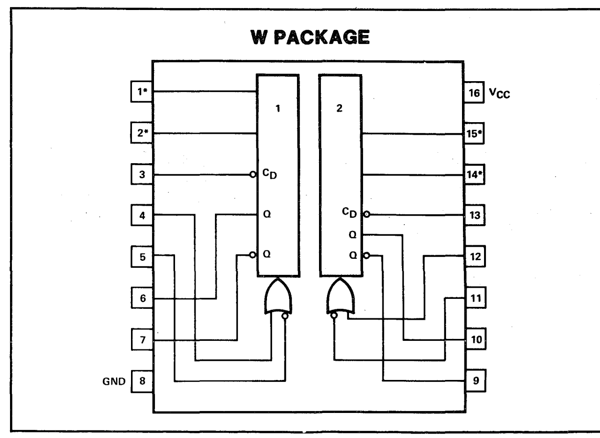
S9602 F,W N9602 B,F

BLOCK DIAGRAM



PIN CONFIGURATION





SWITCHING CHARACTERISTICS V_{CC} = 5V ± 10%, T_A = -55°C to 125°C

TEST CONDITIONS			9602 R_X=5.0Ω C_X=0Ω C_L=15pF			
PARAMETER	**FROM INPUT**	**TO OUTPUT**	**MIN**	**TYP**	**MAX**	**UNIT**
Propagation delay time						
t_{PLH} Low-to-high		True		25	35	ns
t_{PHL} High-to-low		Complement		29	43	ns
$t_{(min)}$		True		72	90	ns
		Complement		78	100	ns
			R_X=10k C_X=1000pF			
t			3.08	3.42	3.76	μs
V_{CC} = 5V ± 5%, T_A = 0°C to 75°C						
Propagation delay time						
t_{PLH} Low-to-high		True		25	40	ns
t_{PHL} High-to-low		Complement		29	48	ns
$t_{(min)}$		True		72	100	ns
		Complement		78	110	
			R_X=10k C_X=1000pF			
t			3.08	3.42	3.76	μs

Load circuit and typical waveforms are shown at the front of section.

LOGIC

ABSOLUTE MAXIMUM RATINGS

Over Operating Free-Air Temperature Range (unless otherwise noted)

The absolute maximum ratings constitute limiting values above which serviceability of the device may be impaired. Provisions should be made in system design and testing to limit voltages in accordance with Table 1.

Table 1

Input Voltage	+5.5V
Output Voltage	+7.0V
V_{CC} (Note 2)	+7.0V
Storage Temperature Range	
A,B,N packages	−65°C to +175°C
F,I,Q,W packages	−65°C to +200°C

NOTES:

1. All devices must be derated at elevated temperatures based on maximum allowable junction temperature.
   (See maximum storage temperature above and the thermal resistance of the package, given in section 8).
2. Operating V_{CC} for the 8200 Series is specified at +5V ± 5%. None of the Signetics MSI elements will be damaged by supply voltages of 7 volts or less; however, in some of the more complex functions, power dissipation at such voltages could become excessive. It is recommended therefore, that such over-voltages be limited to a maximum of 1 second duration.

ORDERING INFORMATION

Unless otherwise specified all devices are available in the "S" and "N" temperature ranges:

"S" = −55°C to +125°C
"N" = 0°C to + 75°C

PART IDENTIFICATION
Y8XXXZ

Y	=	Operating Temperature Range
"S"	=	−55°C to +125°C (Military)
"N"	=	0°C to + 75°C (Commercial)

NOTE:
82XX =standard MSI
82SXX=Schottky MSI
8TXX =interface circuit

Z	=	Package Type Designator
V	=	8-pin Dual-in-line Plastic Package
A	=	14-pin Dual-in-line Plastic Package
B	=	16-pin Dual-in-line Plastic Package
N	=	24-pin Dual-in-line Plastic Package
F	=	14, 16, 24-pin Dual-in-line Ceramic Package (Cerdip)
W	=	14, 16-pin Ceramic Flat Package (Cerpac)
I	=	14, 16, 24-pin Ceramic Dual-in-line Package
Q	=	14, 16, 24-pin Ceramic Flat Package

SYSTEMS DESIGN CONSIDERATIONS

DC Fan-Out and Noise Margin

Because of the growing complexity of new MSI and memory products, loading and noise margin tables are not included in this section. The numbers are easily generated for individual cases as shown below. The lower of the two numbers is the DC fan-out.

DC FAN OUT ("0" Output Condition)

$$= \frac{\text{"0" maximum output current of driving element}}{\text{"0" maximum input current requirement of driven element}}$$

DC FAN OUT ("1" Output Condition)

$$= \frac{\text{"1" maximum output current of driving element}}{\text{"1" maximum input current requirement of driven element}}$$

DC Noise Margin ("0" state) is obtained by subrtracting the maximum "0" level output voltage for the driving gate from the minimum "0" threshold for the driven gate.

DC Noise Margin ("1" state) is obtained by subtracting the maximum "1" level input threshold of the driven gate from the minimum "1" output voltage level of the driving gate.

OUTPUT STRUCTURES

Certain guidelines should be observed to ensure optimum system performance. Systems incorporating TTL elements such as gates, binaries and MSI circuits have inherent V_{CC} and GROUND transients attributable to the current spike produced by "totem pole" output structures.

Figure 1 shows totem pole structures commonly used in MSI designs as output buffers to increase fan-out and provide adequate switching speeds.

DECOUPLING MSI

The current spike produced by the totem pole output structure during switching transitions can cause MSI subsystems to malfunction if V_{CC} is not adequately decoupled to GROUND. With the large number of SSI and MSI devices available it is almost impossible to establish a general rule for decoupling. When in doubt, a capacitor of 2000pF or more, for each totem pole structure should be connected from V_{CC} to GROUND. The non-inductive capacitor (ceramic disc, tantalum slug, etc.) should be mounted with leads as short as possible and should be placed in close proximity to the MSI package to minimize lead length inductance. A properly designed printed circuit board should have the total required capacitance evenly distributed throughout the board. Example: A printed circuit board contains 25 packages averaging four totem pole structures per package. The total capacitance required is 25 packages x 4 totem pole structures x 2000pF or 0.2μF ceramic disc capacitors evenly distributed, satisfy the V_{CC} to GROUND decoupling requirements.

POWER SUPPLY AND GROUND DISTRIBUTION SYSTEMS

High-frequency distribution techniques should be used for V_{CC} and GROUND. These techniques should include a large ground plane to minimize DC offsets and to provide an extremely low impedance path to reduce transient voltage signals on the printed circuit board. The power supply should be +5V ±5% with R-F (1GHz) bypassing. Catastrophic damage can occur if V_{CC} is not properly regulated.

Power distributed from the main supply must, by necessity, come through a path which displays finite resistance (R_{ps}), inductance (L_{ps}) and capacitance (C_{ps}), as illustrated in Figure 2. The resistive component of the power lines is small, producing very little DC voltage drop at the V_{CC} and GROUND inputs to the printed circuit board. However, the inductance in the power lines can cause the noise generated by current spiking to be transmitted throughout the system on the V_{CC} and GROUND lines. If the printed circuit boards are adequately decoupled, the power line noise will be reduced significantly. In order to repel power line noise transmitted to a printed circuit board, ferrite beads may be placed on the incoming V_{CC} and GROUND lines as shown in Figure 3. A 10μf tantalum capacitor, per 25 packages, connected from V_{CC} to GROUND should be placed on the printed circuit board in the position shown. In conjunction with the distributed ceramic disc capacitors, this approach will prevent most system malfunctions attributable to internally generated noise.

COMMON TOTEM POLE OUTPUT STRUCTURES

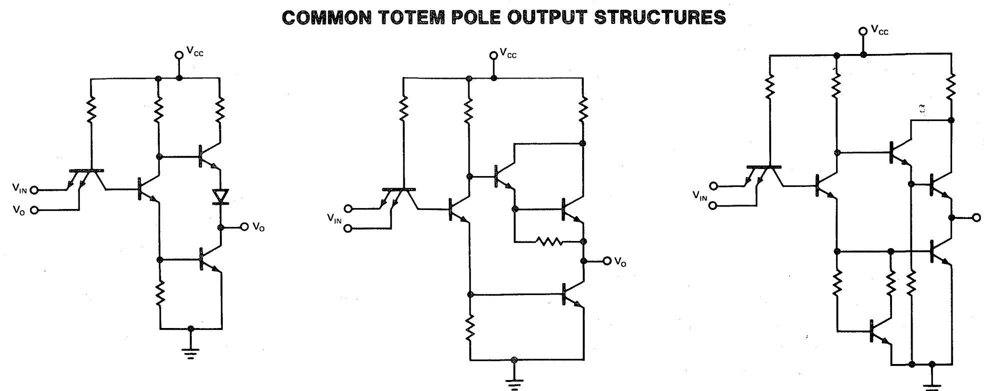


Figure 1

LOGIC

POWER CHARACTERISTIC IMPEDANCE

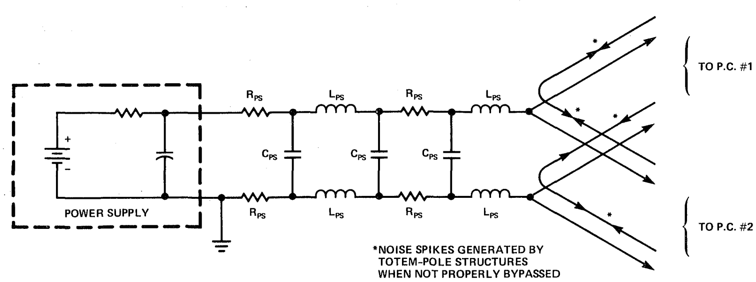


Figure 2

FERRITE BEAD ISOLATION OF GENERATED NOISE

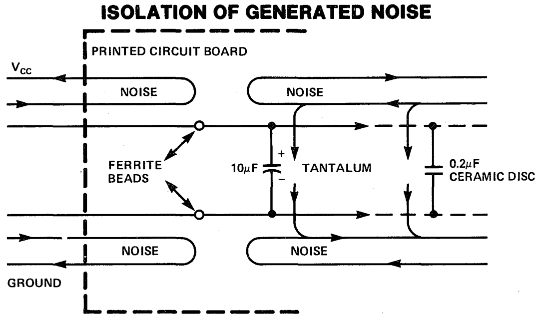


Figure 3

ISOLATION DIODES

NEVER REVERSE THE V_{CC} AND GROUND POTENTIALS. Catastrophic failure can occur if more than 100mA is conducted through a forward biased substrate (isolation) diode.

DISPOSITION OF UNUSED INPUTS

Electrically open inputs degrade AC noise immunity as well as the switching speed of an MSI circuit. To optimize performance, each input must be connected to a low impedance source. Depending on their logical activating level, unused inputs should be tied to V_{CC}, GROUND or a driving source. When paralleling an unused input with a driven input of the same multiple emitter transistor (MET), care should be taken to remain within the "1" level fan-out specifications for the driving source. The AND or NAND structures do not affect the "0" level fan-out of the driving source. When an unused input of an OR or NOR structure is commoned with a driven input, both the "1" and "0" level fan-out of the driving source are affected.

If fan-out of the driving source will be exceeded or if there is no convenient connection to an appropriate driven input, a second method of avoiding open inputs is useful. Inputs which activate on "0" (AND and NAND) may be tied directly to V_{CC} or tied to V_{CC} through a current limiting resistor of 1 KΩ or more.

The current limiting resistor is required if power supply transients can exceed 5.5V for longer than 1μsec; since the power dissipated in the emitter junction under these conditions can destroy the junction.

More than one unused input can be tied to V_{CC} through a single resistor.

INPUT CLAMP DIODES

MSI circuits contain input clamp diodes as shown in Figure 4. At the input, these diodes limit negative excursions which exceed −1V by providing a low impedance current source from GROUND through the forward biased diode clamp. The clamps are designed to minimize ringing which may result from interconnect wires in excess of six inches in length.

INPUT CLAMP DIODES

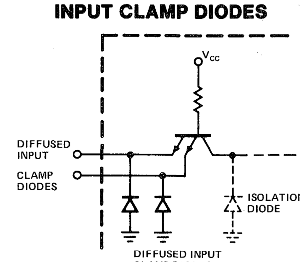


Figure 4

SIGNAL PROCESSING

The rise and fall times of all incoming data signals should be less than 200ns. The amplitude of incoming data signals should be 2.4V or greater. Figure 5 shows the transfer characteristic of the classic TTL gate. In the input threshold region, from point one to point two, the gate has approximately 25dB of gain. In this region, any discontinuity of the input waveform will be amplified more than 10 times at the output of the gate.

TTL TRANSFER CHARACTERISTIC

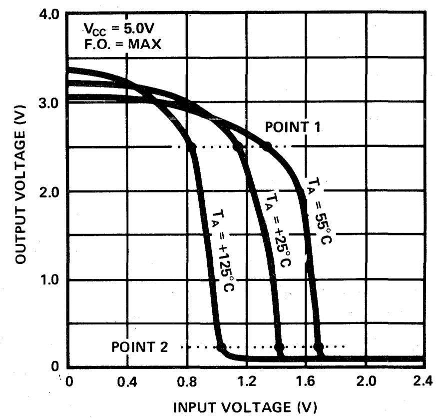


Figure 5

Should the input voltage remain in the threshold region (approximately 200mV wide) for more than 15ns, a typical TTL gate tends to oscillate as shown in Figure 6. The equivalent circuit in Figure 7 illustrates the potential oscillatory feed-back paths. The primary contributor to oscillation is the changing power supply voltage with the chip, caused by the current spiking which occurs during switching transitions. Since output voltage is directly proportional to V_{CC} and threshold voltage tends also to drop with lower supply voltage, the net effect is a positive feedback loop from output to input.

TYPICAL TTL GATE OSCILLATION WITH SLOW INPUT TRANSITIONS

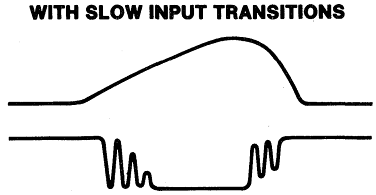


Figure 6

POTENTIAL OSCILLATORY FEEDBACK PATHS

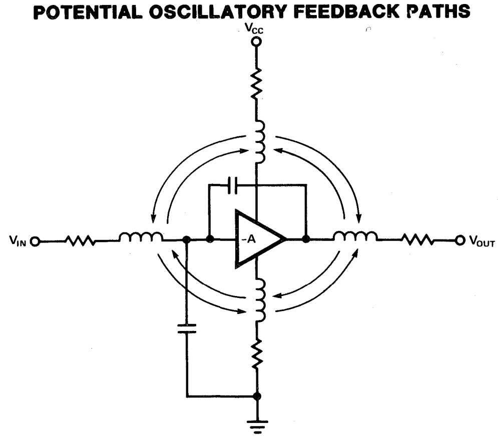


Figure 7

WIRED-AND APPLICATIONS OF OPEN-COLLECTOR MSI

Open-collector MSI, when supplied with a proper load resistor (R_L) can be paralleled with other similar MSI or open collector TTL gates to perform the WIRED-AND function, and simultaneously, will drive several TTL loads. For any of these conditions an appropriate load resistor value must be determined for the desired circuit configuration. The user may choose a load resistor that must be between the following limits: A maximum resistor value must be determined which will ensure that sufficient load current to the TTL loads to be driven, as well as leakage current to the paralleled outputs, is available during the logical "1" state at the output. A minimum resistor value must be determined which will ensure that current through this resistor and sink current from the TTL loads will not cause the output voltage to rise above the logical "0" level even if one of the paralleled outputs is sinking all the current.

LOGICAL "1" (off level) CALCULATIONS FOR R_L MAX

The maximum value of load resistance $R_{L\ MAX}$) is determined by the maximum voltage drop across R_L caused by the total leakage current which will still ensure a minimum logical "1" at the common collector node. As shown in Figure 8:

Total leakage current $I(1)_{total} = n\,I(1)_{off} + m\,I(1)_{in}$
n = number of commoned collectors (driving gates)
m = number of fan-outs (driven gates)

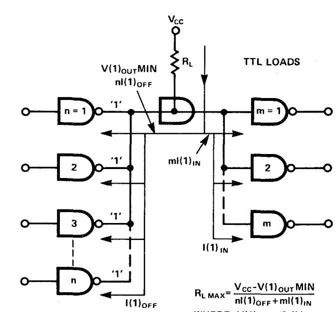


Figure 8

LOGIC

LOGICAL "0" (on level) CALCULATIONS FOR R_L MIN

The minimum value of load resistance ($R_{L\ MIN}$) is determined from the worst case maximum logical "0" state in which only one element is sinking current. This condition is illustrated in Figure 9:

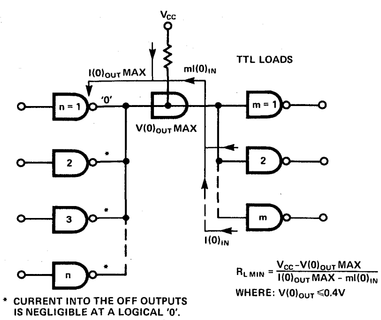


Figure 9

PROPAGATION DELAY

Propagation delay for the 8000 Series elements is specified in terms of t_{on} and t_{off} switching times which provides a figure of merit by which comparison can be made with similar products. The guaranteed delay times given in the electrical characteristics section take into consideration the logical "1" and logical "0" input current and load capacitance as shown in the AC test figures. Inverting and non-inverting paths are measured as shown in Figure 10.

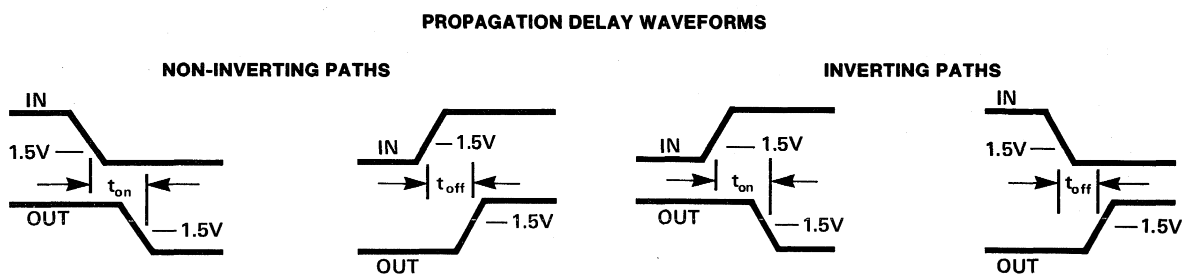


Figure 10

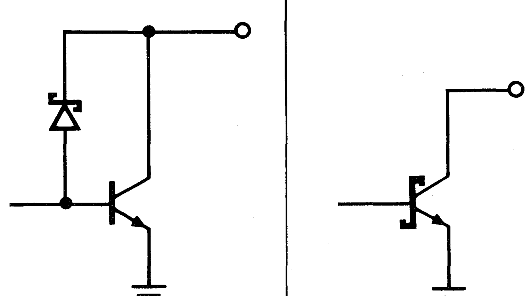
82S OPTIMIZED SCHOTTKY MSI

Series 82S optimized Schottky MSI circuits are implemented with Schottky-barrier-Diode (SBD) clamping to achieve ultra-high speed previously only attainable with emitter-coupled logic and in addition low current PNP inputs provide numerous systems advantages. These integrated circuits are directly compatible with other TTL circuits such as the 8000 MSI circuits, 82/82S bipolar memories, 54/74 and 54S/74S as well as MOS/CMOS.

The Schottky barrier diode is a metal-semiconductor diode that is characterized by the absence of minority carriers near the forward biased junction, thus making it possible to switch the diode rapidly since there is no stored charge. Another major difference between the Schottky diode and a p-n junction diode is that the SBD has a lower forward voltage for a given current. SBD clamping from the base to the collector of a switching transistor is shown in Figure 1. The Schottky diode prevents the transistor from saturating and there is no stored charge either in the diode or the transistor. Thus recovery times that contribute significantly to the overall propagation delays experienced in saturated digital-logic design are eliminated.

The Schottky-clamped transistors are formed by using Schottky-barrier-diodes in parallel with the base-collector junction. The SBD is realized physically by depositing metal over the base and N region of the collector forming a metal-silicon diode. The effect of this diode, which has a lower forward voltage than the collector-base function is to hold the transistor out of saturation by diverting the excess base current. The reduction in stored-charge plus the use of smaller geometries results in a major improvement of switching characteristics.

SCHOTTKY TRANSISTOR



EQUIVALENT REPRESENTATION WITH TRANSISTOR (SCHOTTKY DIODE)

SYMBOL FOR SCHOTTKY TRANSISTOR

FIGURE 1

The standard processing approach to charge storage reduction in conventional IC's has been gold doping. Since this is no longer necessary in Schottky circuits, elimination of gold doping has made it possible to use smaller geometries and shallower diffusions for higher speed transistors.

By eliminating gold doping normally employed in conventional TTL processing to reduce storage time, PNP transistors can also be used to advantage by the circuit designers.

In 82S MSI circuits PNP transistors are used to reduce input loading as illustrated in Figure 2. Maximum low level input current is specified at 400μA which allows the systems' designer to upgrade existing designs without encountering fanout limitations as well as interface with MOS and CMOS.

INPUT TRANSISTORS COMPARISON

ADVANCED SIGNETICS 82S INPUT

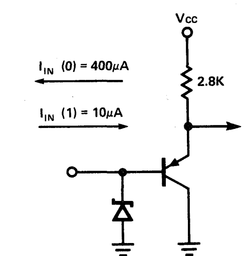


FIGURE 2a

CONVENTIONAL 74S INPUT

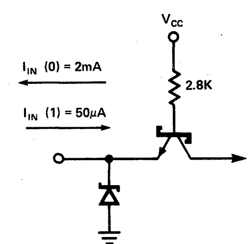


FIGURE 2b

Since the 82S/74S output structure is the same, far more devices can be driven from one output since the 82S input loading is only one-fifth that of standard 74S Schottky inputs. Should a termination resistor be needed when driving long lines in addition to 10 PNP loads, it can be accommodated easily without fan-out reduction.

82S/74S OUTPUT STRUCTURE

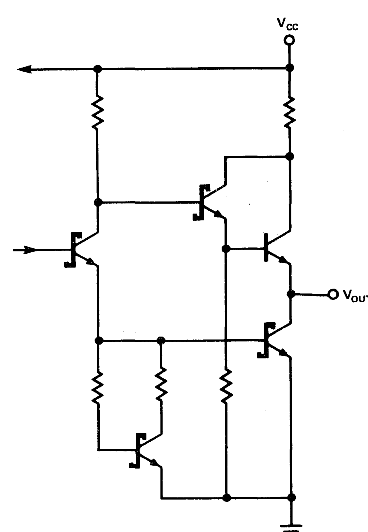


FIGURE 3

FEATURES

- 3 ns typical gate propagation delay
- 20 mW per gate typical power dissipation
- Low current pnp inputs (400A max.)
- Schottky diode clamped inputs
- High output drive capability

BENEFITS

- Compatible with 8000 series, 54/74, 54S/74S TTL as well as DTL and C-MOS
- Terminated, controlled impedance lines not normally required
- Drives high capacitive loads
- Low A.C. noise susceptibility

Absolute maximum ratings (Over operating free-air temperature range unless otherwise noted)

The absolute maximum ratings constitute limiting values above which serviceability of the device may be impaired. Provisions should be made in system design and testing to limit voltages in accordance with Table 1.

Imput Voltage	+5.5V
Output Voltage (Off-State)	VCC
VCC (Note 2)	+7.0 V
Storage or Junction Temperature Range	
A, B, N, F Packages	-65°C to +175°C
Operating Free-Air Temperature	0°C to 75°C

NOTES
1.All devices must be derated at elevated temperatures based on maximum allowable junction temperature.
(See maximum storage temperature above and the thermal resistance of the package, given in Section 8).
2.Operating VCC for the 82S Series is specified at +5V±5%. None of the Signetics MSI elements will be damaged by supply voltages of 7 volts or less; however, in some of the more complex functions, power dissipation at such voltages could become excessive. It is recommended therefore, that such over-voltages be limited to a maximum of 1 second duration.

FUNCTION TABLE

Function	Typical Speed	Comments
82S30 8-Input Digital Multiplexer 82S31 8-Input Digital Multiplexer 82S32 8-Input Digital Multiplexer	7 ns	Replaces FSC 9312 or T.I. SN 29312 and Signetics 8230 for higher speed. Replaces Signetics 8231 and Signetics 8232 for higher speed.
82S33 2-Input 4-Bit 82S34 Digital Multiplexer	7 ns	Replace equivalent non-Schottky parts for higher speed.
82S41 Quad Exclusive OR 82S42 Quad Exclusive NOR	7 ns	Replaces 8241 for higher speed. Replaces FSC 9386 and 8242 for speed.
82S50 BIN to Octal Decoder 82S51 BCD to Decimal Decoder 82S52 BCD to Decimal Decoder	12 ns	Replaces 8250 for higher speed. Replaces 8251 for higher speed. Replaces FSC 9301, T.I. SN29301, and 8252 for higher speed.
82S62 9-Bit Parity Checker/ Generator	17 ns	Replaces 8262 for higher speed and is pin-for-pin replacement for 93S62.
82S66 2-Input 4-Bit Digital 82S67 Multiplexers and Conditional Complementers	8 ns	Replaces equivalent non-Schottky parts for higher speed.
82S70 4-Bit Shift Register 82S71 4-Bit Shift Register w/Clear	60 MHz	Replaces 8270, T.I. 74178 and FSC 93178 for higher speed. Replaces 8271, T.I. 72179 and FSC 93179 for higher speed.
82S82 BCD Arithmetic Unit 82S83 BCD Adder	20 ns	Replaces many MSI and Gate elements Primarily these are implementations that use multiples of 7483's and Gates.
82S90 Presettable Decade Counter 82S91 Presettable Binary Counter	100 MHz	Replaces 8280, 8290, T.I. 74176, T.I. 74196, FSC 93176, FSC 93196. Replaces 8281, 8291, T.I. 74177, T.I. 72197, FSC 93177, FSC 93197 for higher speed.

8200 MSI CHARACTERISTICS

	INPUT VOLTAGE						OUTPUT CURRENT			INPUT VOLTAGE		
PARAMETER	V_{OL} (V) 7 LOW LEVEL			V_{OH}(V)6 HIGH LEVEL			I_{CBO}(μA) 8 LEAKAGE CURRENT			INPUT VOLTAGE RATING		
TEST CONDITIONS	V_{CC}=MIN V_{IN}=★ I_{OL}=16mA			V_{CC}=MIN V_{IN}=★ I_{OH}=-800μA			V_{IN}=2.0V			V_{IN}=10MA		
DEVICE	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
8200		I_{OL}=9.6mA	0.4	2.6	3.5			N/A		5.5		
8201		I_{OL}=9.6mA	0.4	2.6	3.5			N/A		5.5		
8202		I_{OL}=9.6mA	0.4	2.6	3.5			N/A		5.5		
8203		I_{OL}=9.6mA	0.4	2.6	3.5			N/A		5.5		
8230			0.4	2.6	3.5			N/A		5.5		
8231			0.4	2.6	3.5				150	5.5		
8232			0.4	2.6	3.5			N/A		5.5		
8233			0.4	2.6	3.5			N/A		5.5		
8234			0.4		N/A				100	5.5		
8235			0.4		N/A				100	5.5		
8241			0.4	2.6	3.5			N/A		5.5		
8242		I_{OL}=25mA	0.4		N/A				25	5.5		
8243		I_{OL}=12.8mA	0.4		N/A				150	5.5		
8250			0.4	2.6	3.5			N/A		5.5		
8251			0.4	2.6	3.5			N/A		5.5		
8252			0.4	2.6	3.5			N/A		5.5		
8260		I_{OL} (F_N, C_G, C_R)= 9.6 mA	0.4	2.6	3.5			N/A		5.5		
8261		I_{OL}-9.6mA	0.4	2.6	3.5			N/A		5.5		
8262			0.4	2.6	3.5			N/A		5.5		

LOGIC

8200 MSI SERIES PRODUCT FAMILY INFORMATION

8200 MSI CHARACTERISTICS

	INPUT CURRENT						OUTPUT CURRENT					
PARAMETER	I_{IL}(MA) LOW LEVEL			I_{IH}(μA) HIGH LEVEL			I_{OS}(MA) 9 SHORT CIRCUIT			POWER/CURRENT CONSUMPTION (MW/MA)		
TEST CONDITIONS	V_{CC}=MAX V_{IN}=0.4V			V_{CC}=MAX V_{IN}=4.5V			V_{CC}=MAX V_{OUT}=OV			V_{CC}=MAX V_{IN}=OV		
DEVICE	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
8200	-0.1		-1.6			40	-20		-70		409/77.7	580/110
8201	-0.1		-1.6			40	-20		-70		409/77.7	580/110
8202	-0.1		-1.6			40	-20		-70		409/77.7	580/110
8203	-0.1		-1.6			40	-20		-70		409/77.7	580/110
8230	-0.1		-1.6		Input INH	40 80	-20		-70		184/35	250/47.7
8231	-0.1		-1.6		Input INH	40 80	-20		-70		184/35	250/47.7
8232	-0.1		-3.2		Input INH	40 80	-20		-70		173/33	262/50.0
8233	-0.1		-1.6			40	-20		-70		200/38	252/48
8234	-0.1		-1.6			40		N/A			160/31	210/40
8235	-0.1		-1.6			40		N/A			V_{IN}=4.5V 230/44	310/59
8241	-01.		-3.2			80	-20		-70		225/42.4	300.57.1
8242	-0.1		-3.2			80	-20		-70		170/32	250/47.5
8243	-0.1		-1.6		Data In	40 80		N/A			315/60	500/75.2
8250	A,B,C -0.1 D -0.1		-1.2 -1.0			40	-10		-55			124/23.8
8251	-0.1		-1.2			40	-10		-55			135/25.7
8252	-0.1		-1.6			40	-10		-55			135/25.7
8260	-0.1 -0.1	X_N,C_{INH},Y_N E_{INH}, C_{INI}, Through C_{IN5}	-3.2 -1.6		X_N,C_{INH},Y_N E_{INH}, C_{INI}, Through C_{IN5}	80 40	-20 -30	F_N,C_G,C_R C_P	-70 -90		400/76.2	600/114.1
8261	G,A,B,P_I P_2 P_3 P_4,P_5		-1.6 -3.2 -4.8 -6.4	G,A,B,P_I P_2 P_3 P_4,P_5		40 80 120 160	-20		-70		115/22	158/30
8262	-0.1 -0.1	Data Inputs Inhibit	-1.6 -3.2		Data Inputs Inhibit	80 160	-20		-70		300/57	370/70

8200 MSI CHARACTERISTICS

	INPUT VOLTAGE						OUTPUT CURRENT			INPUT VOLTAGE		
PARAMETER	V_{OL} (V) 7 LOW LEVEL			V_{OH}(V)6 HIGH LEVEL			I_{CBO}(μA) 8 LEAKAGE CURRENT			INPUT VOLTAGE RATING		
TEST CONDITIONS	V_{CC}=MIN V_{IN}=★ I_{OL}=16mA			V_{CC}=MIN V_{IN}=★ I_{OH}=-800μA			V_{IN}=2.0V			V_{IN}=10MA		
DEVICE	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
8263		I_{OL}-9.6mA	0.4	2.6	3.5			N/A		5.5		
8264			0.4		N/A				200	5.5		
8266			0.4	2.6	3.5			N/A		5.5		
8267			0.4		N/A				25	5.5		
8268			0.4	2.6	I_{OH}=−500μA 3.5			N/A		5.5		
8269		0.2	0.4	2.6	3.5			N/A		5.5		
8270		I_{OL}=11.2mA	0.4	2.6	3.5			N/A		5.5		
8271		I_{OL}=11.2mA	0.4	2.6	3.5			N/A		5.5		
8273		I_{OL}=9.6mA 0.2	0.4	2.6	I_{OH}=−500μA 3.5			N/A		5.5		
8274		0.2	0.4	2.6	3.5			N/A		5.5		
8275			0.4	2.6	3.5			N/A		5.5		
8276			0.4	2.6	3.5			N/A		5.5		
8277			0.4	2.6	3.5			N/A		5.5		
8280			0.4	2.6	3.5			N/A		5.5		
8281			0.4	2.6	3.5			N/A		5.5		

LOGIC

8200 MSI CHARACTERISTICS

	INPUT CURRENT						OUTPUT CURRENT					
PARAMETER	I_{IL}(MA) LOW LEVEL			I_{IH}(μA) HIGH LEVEL			I_{OS}(MA) 9 SHORT CIRCUIT			POWER/CURRENT CONSUMPTION (MW/MA)		
TEST CONDITIONS	V_{CC}=MAX V_{IN}=0.4V			V_{CC}=MAX V_{IN}=4.5V			V_{CC}=MAX V_{OUT}=OV			V_{CC}=MAX V_{IN}=OV		
DEVICE	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
8263	-0.1 S_0,S_I -0.1		-1.6 -3.2	 S_0,S_I		40 80	-20		-70		378/72	420/80
8264	-0.1 S_0,S_I -0.1		-1.6 -3.2	 S_0,S_I		40 80		N/A			400/76	475/90.4
8266	-0.1		-1.6			40	-20		-70		200/38.1	275/52.4
8267	-0.1		-1.6			40		N/A			200/38.1	275/52.4
8268	 -0.1 $\overline{X},\overline{Y}$ -0.1 -0.1	X_1,X_2,X_C,Y_1,Y_2,Y_C C_{IN}	 -1.6 -2.6 -8.0	C_{IN}		40 160	$\Sigma,\overline{\Sigma}$ -18 -18	 $\overline{C}_{OUT}$	 -57 -70		152/29	185/35
8269	-0.1		-3.2			80	-18		-55		278/53	
8270	-0.1		-1.2			40		N/A			168/32	247/47
8271	-0.1		-1.2			40		N/A			271/52	344/65
8273	-0.1		-1.6			40	-20		-70		341/65	540/103
8274	 -0.2 Clock -0.2	D_N,S_0,S_I	 -1.2 -1.6			40	-20		-70		380/72	567/108
8275	Data -0.1 Enable -0.1		 -3.2 -6.4	Data Enable		 80 160	-20		-70		205/39	265/50
8276	-0.1		-1.6			40	-18		-55		205/39	340/65
8277	 -0.1 -0.1	Data,Reset,Clock Separate Data,Select,Clock Common	 -1.6 -3.2		Data,Reset,Clock Separate Data,Select,Clock Common	 40 80		N/A				540/103
8280	 -0.1 -0.1 -0.1	Data Inputs $\overline{Strobe}$ $\overline{Reset}$ Clk 1,2	 -1.2 -1.6 -3.2		$\overline{Strobe}$,Data,Inputs $\overline{Reset}$,Clk 1, Clk 2	 40 80	-10		-60		184/35	236/45
8281	 -0.1 -0.1 -0.1	Data Inputs $\overline{Strobe}$,Clk 2 $\overline{Reset}$,Clk 1	 -1.2 -1.6 -3.2		$\overline{Strobe}$,Data Inputs,Clk 2 $\overline{Reset}$ Clk 1	 40 80	-10		-60		184/35	236/45

8200 MSI CHARACTERISTICS

	INPUT VOLTAGE						OUTPUT CURRENT			INPUT VOLTAGE		
PARAMETER	V_{OL} (V) 7 LOW LEVEL			V_{OH}(V)6 HIGH LEVEL			I_{CBO}(μA) 8 LEAKAGE CURRENT			INPUT VOLTAGE RATING		
TEST CONDITIONS	V_{CC}=MIN V_{IN}=★ I_{OL}=16mA			V_{CC}=MIN V_{IN}=★ I_{OH}=-800μA			V_{IN}=2.0V			V_{IN}=10MA		
DEVICE	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
8284		I_{OL}=9.6mA	0.4	2.6	3.5			N/A		5.5		
8285		I_{OL}=9.6mA	0.4	2.6	3.5			N/A		5.5		
8288			0.4	2.6	3.5			N/A		5.5		
8290		I_{OL}=9.6mA	0.4	2.6	I_{OH}=200μA 3.5			N/A		5.5		
8291		I_{OL}=9.6mA	0.4	2.6	I_{OH}=200μA 3.5			N/A		5.5		

	INPUT CURRENT						OUTPUT CURRENT					
PARAMETER	I_{IL}(MA) LOW LEVEL			I_{IH}(μA) HIGH LEVEL			I_{OS}(MA) 9 SHORT CIRCUIT			POWER/CURRENT CONSUMPTION (MW/MA)		
TEST CONDITIONS	V_{CC}=MAX V_{IN}=0.4V			V_{CC}=MAX V_{IN}=4.5V			V_{CC}=MAX VOUT=OV			V_{CC}=MAX V_{IN}=OV		
DEVICE	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
8284		Reset,Count,			Reset,Count,		-20		-70		315/60	420/80
		Enable,Clk,			Enable,Clk							
		Up/Down			Up/Down							
	-0.1		-1.6			40						
		Carry In			Carry In							
	-0.1		-3.2			120						
		Set			Set							
	-0.1		-6.4			200						
8285		Reset,Count			Reset,Count		-20		-70		315/60	420/80
		Enable, Clk			Enable Clk,							
		Up/Down			Up/Down							
	-0.1		-1.6			40						
		Carry In			Carry In							
	-0.1		-3.2			120						
		Set			Set							
	-0.1		-6.4			200						
8288		Data Inputs			Data Strobe		-10		-60		184/35	236/45
					Data Input							
	-0.1		-1.2			40						
		Data Strobe,										
		Clk 2										
	-0.1		-1.6									
		Reset Clk 1			Reset, Clk 1							
					Clk 2							
	-0.1		-3.2			80						
		Data Inputs			Data Inputs,			A				
8290	-0.1		-1.2				-20		-70		190/36.5	255/48.5
					Data Strobe							
		Data Strobe				40						
	-0.1		-1.6									
					Reset Clk 1			B,C,D				
		Reset				80	-10		-60			
	-0.1		-2.8									
		Clk1,Clk2			Clk 2	120						
	-0.1		-4.8									
		Data Inputs			Data Strobe,			A				
8291	-0.1		-1.2		Data Inputs		-20		-70		190/36.5	255/48.5
		Data Strobe				40		B,C,D				
	-0.1		-1.6		Reset,Clk1		-10		-60			
		Clock 2			Clk 2	80						
	-0.1		-2.4									
		Reset										
	-0.1		-2.8									
		Clock 1										
	-0.1		-4.8									

8200 MSI CHARACTERISTICS

	INPUT VOLTAGE						OUTPUT CURRENT			INPUT VOLTAGE		
PARAMETER	V_{OL} (V) 7 LOW LEVEL			V_{OH}(V)6 HIGH LEVEL			I_{CBO}(μA) 8 LEAKAGE CURRENT			INPUT VOLTAGE RATING		
TEST CONDITIONS	V_{CC}=MIN V_{IN}=★ I_{OL}=16mA			V_{CC}=MIN V_{IN}=★ I_{OH}=-800μA			V_{IN}=2.0V			V_{IN}=10MA		
DEVICE	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**
8292		I_{OL}=3.2mA	0.4	2.6	I_{OH}=100μA 3.5			N/A		5.5		
8293		I_{OL}=3.2mA	0.4	2.6	I_{OH}=100μA 3.5			N/A		5.5		

By DC tests per the truth table, all inputs have guaranteed thresholds of 0.8V for low level, and 2.0V for high level.

NOTES:

1. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are tied to Vcc.
2. All measurements are taken with ground pin tied to zero volts.
3. Positive current is defined as into the terminal referenced.
4. Positive logic definition: "UP" level = "1". "DOWN" level is "0".
5. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings.
6. Output source current is supplied through a resistor to ground.
7. Output sink current is supplied through a resistor to Vcc.
8. Connect an external 1K ± 1% resistor from Vcc to the output for this test.
9. Not more than one output should be shorted at one time.

8200 MSI CHARACTERISTICS

	INPUT CURRENT						OUTPUT CURRENT					
PARAMETER	I_{IL}(MA) LOW LEVEL			I_{IH}(μA) HIGH LEVEL			I_{OS}(MA) 9 SHORT CIRCUIT			POWER/CURRENT CONSUMPTION (MW/MA)		
TEST CONDITIONS	V_{CC}=MAX V_{IN}=0.4V			V_{CC}=MAX V_{IN}=4.5V			V_{CC}=MAX V_{OUT}=OV			V_{CC}=MAX V_{IN}=OV		
DEVICE	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
8292		Data Inputs, Data Strobe			Data Inputs, Data Strobe		-5		-45		52.5/10	69/13.1
	-0.1		-0.4			20						
		Reset,Clk1			Reset,Clk 1							
	-0.1		-0.6			40						
		Clock 2			Clock 2							
	-0.1		-1.2			80						
8293		Data Inputs, Data Strobe			Data Inputs, Data Strobe		-5		-45		52.5/10	69/13.1
	-0.1		-0.4			20						
		Reset,Clk 1 Clk 2			Reset,Clk 1 Clk 2							
	-0.1		-0.6			40						

8200,01,02,03—N,F,Q

DESCRIPTION

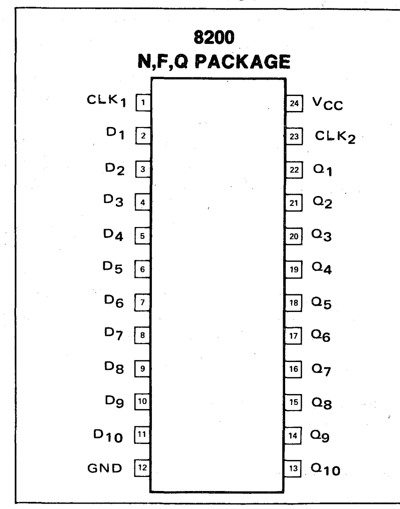
The 8200/8201/8202/8203 MSI Buffer Registers are arrays of ten clocked "D" flip-flops especially suited for parallel-in parallel-out register applications. They are also suitable for general purpose applications as parallel-in serial-out, serial-in parallel-out registers.

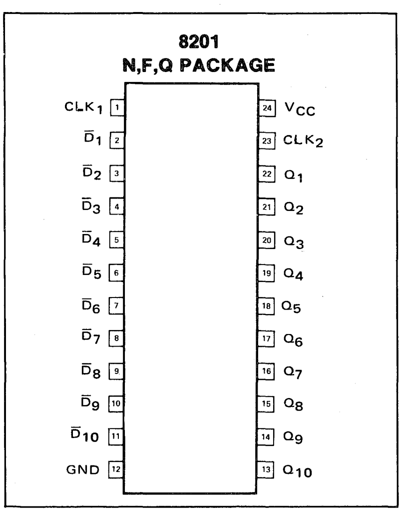
The flip-flops are arranged as dual 5 arrays, (8200 & 8201) and single 10 arrays with reset, (8202 & 8203). The true output of each bit is made available to the user.

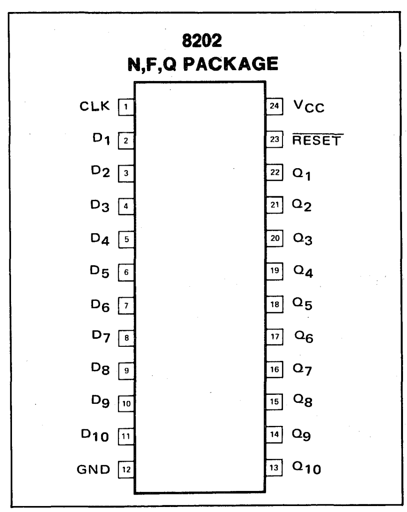
The 8200 and 8202 feature true "D" inputs. The logic state presented at these "D" inputs will appear at the Q outputs after a negative transition of the clock.

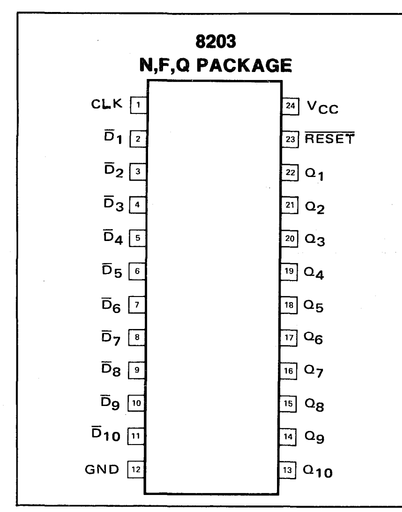
The 8201 and 8203 feature complementing "D" inputs ("$\overline{D}$"). The logic state presented at these "$\overline{D}$" inputs will invert and appear at the Q outputs after a negative going transition of the clock. This complementing input feature ("$\overline{D}$") permits the use of standard AND-OR-INVERT gates to achieve the AND-OR function without additional gate delays.

PIN CONFIGURATION









TRUTH TABLE

	D_n	$\overline{D}_n$	$\overline{\text{RESET}}$	Q_{n+1}
8200	1	—	—	1
	0	—	—	0
8201	—	1	—	0
	—	0	—	1
8202	1	—	1	1
	0	—	1	0
8203	0	—	1	1
	1	—	1	0

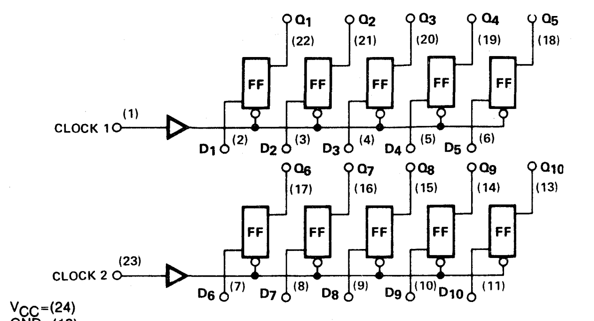
SWITCHING CHARACTERISTICS $T_A = 25°C$, $V_{CC} = 5V$

PARAMETER	FROM INPUT	TO OUTPUT	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT
Propagation delay time						
t_{on} turn-on time	Clock	Q		30	45	ns
	Reset	Q		30	45	
t_{off} turn-off time	Clock	Q		25	40	
t_{setup} setup time				6	15	ns
t_{hold} hold time[2]				0	5	ns
t_W input pulse width min, clock				12	17	ns
Transfer rate			15	35		MHz

8200,01,02,03-N,F,Q

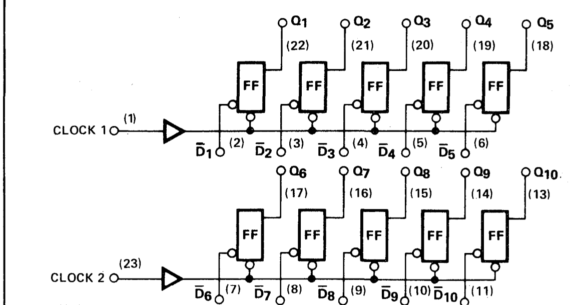
LOGIC DIAGRAMS

8200 DUAL 5-BIT BUFFER REGISTER



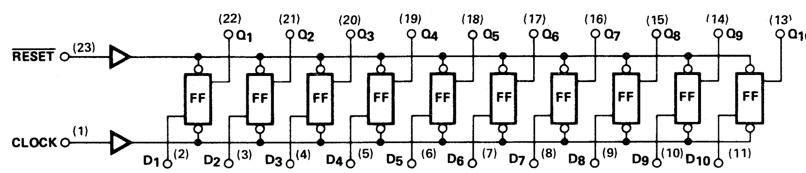
V_{CC}=(24)
GND=(12)
( )=denotes pin numbers

8201 DUAL 5-BIT BUFFER REGISTER-INVERTED INPUTS



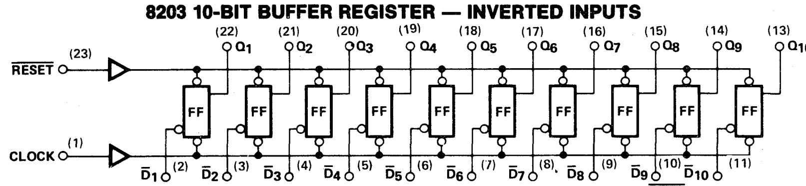
V_{CC}=(24)
GND=(12)
( )=denotes pin numbers

8202 10-BIT BUFFER REGISTER



V_{CC}=(24)
GND=(12)
( )=denotes pin numbers

8203 10-BIT BUFFER REGISTER — INVERTED INPUTS

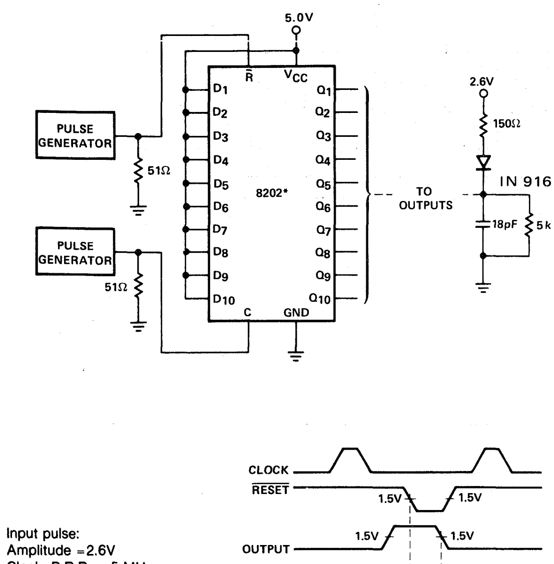


V_{CC} = (24)
GNSD=(12)
( )= denotes pin numbers

Reset=0 → Q = 0
(overrides clock)
n is time prior to clock
n+1 is time following clock

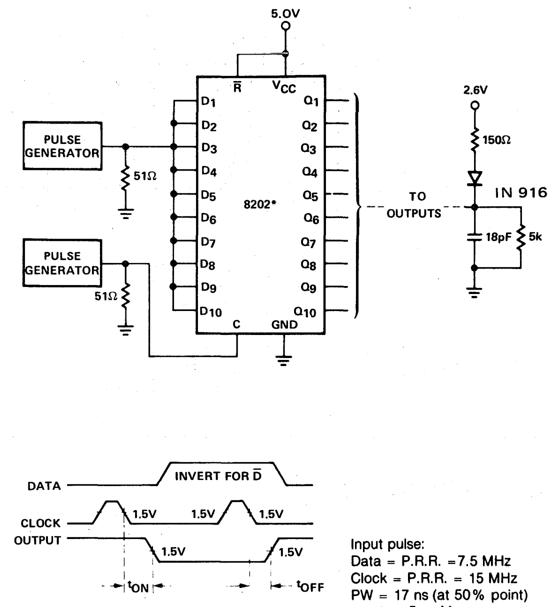
AC TEST FIGURES AND WAVEFORMS

t_{on} FROM RESET TO Q



Input pulse:
Amplitude = 2.6V
Clock: P.R.R. = 5 MHz
Reset: P.R.R. = 5 MHz
PW = 30 ns (at 50% point)
$t_r = t_f = 5$ ns

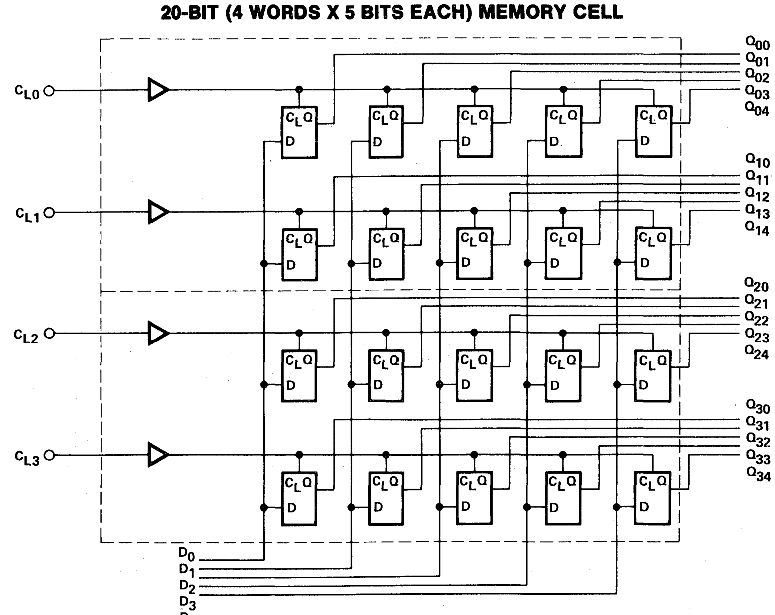
t_{pd} FROM CLOCK TO Q



Input pulse:
Data = P.R.R. = 7.5 MHz
Clock = P.R.R. = 15 MHz
PW = 17 ns (at 50% point)
$t_r = t_f = 5$ ns Max
Amplitude = 2.6V

TYPICAL APPLICATIONS

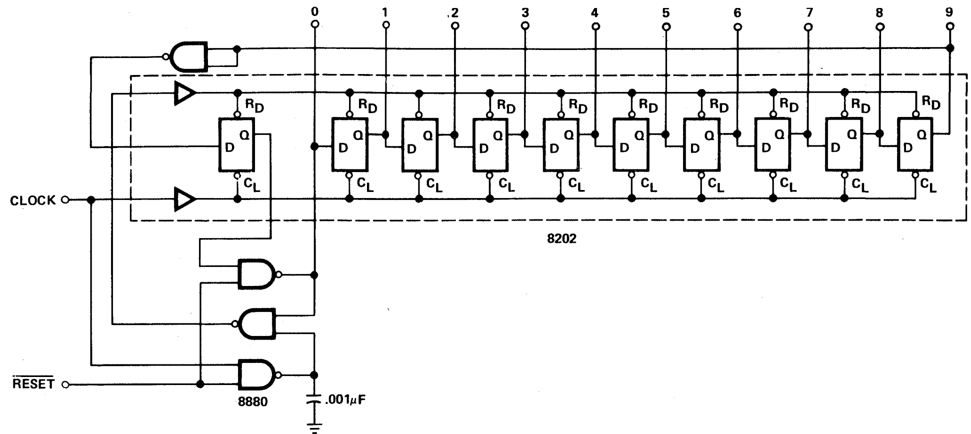
20-BIT (4 WORDS X 5 BITS EACH) MEMORY CELL



LOGIC

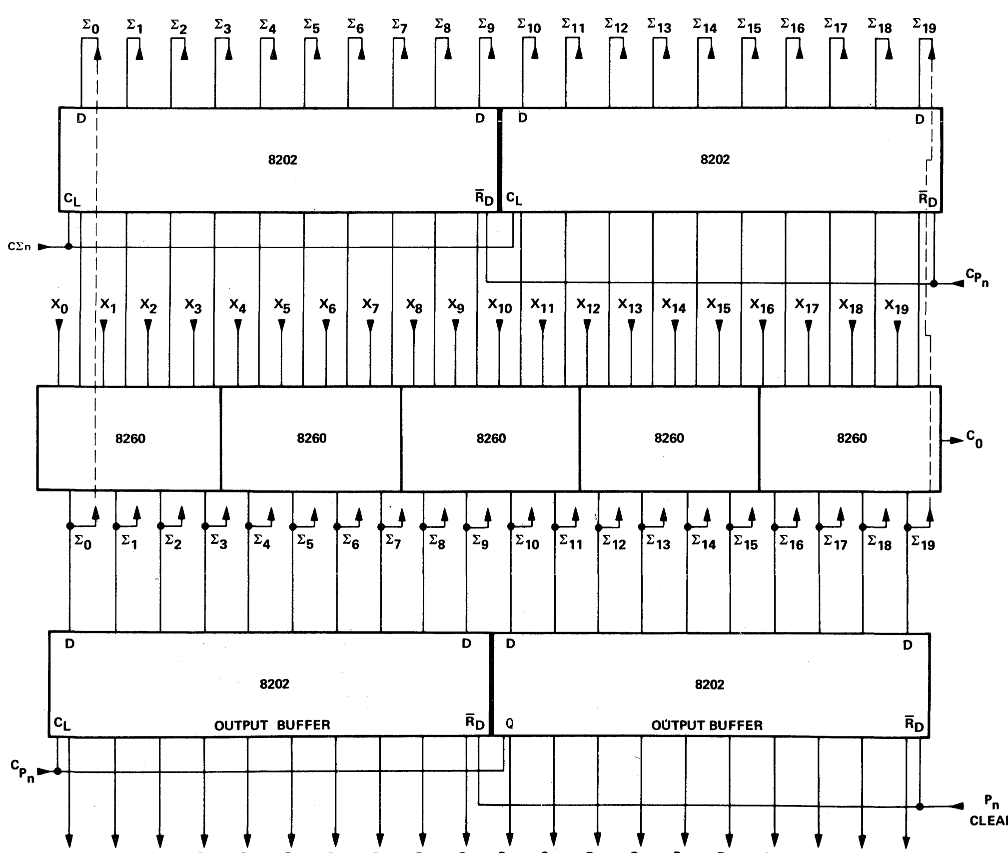
TYPICAL APPLICATIONS (Cont'd)

ONE OUT OF TEN - COUNTER/DISPLAY (SELF-CORRECTING)



TYPICAL APPLICATIONS

MULTIPLICATION AT 10 MHz OF A 20-BIT BINARY WORD



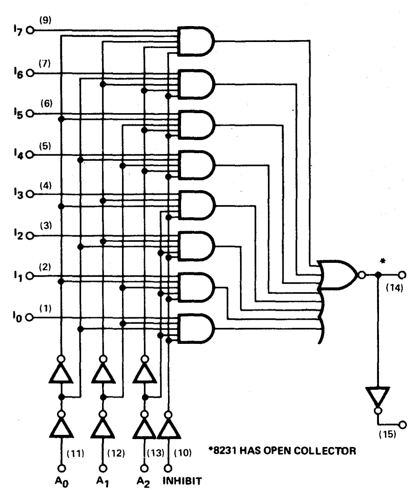
$P_n = (X_n)M$ where $X_n \equiv$ multiplicand
$M \equiv$ multiplier

SPEED/PACKAGE AVAILABILITY

8230, 31, 32—B, F, W
82S30, 31, 32—B, F

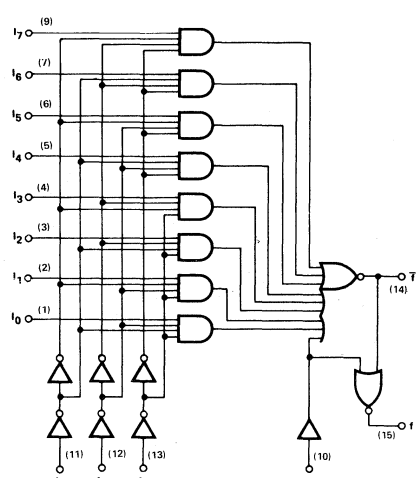
LOGIC DIAGRAMS

8230/31



V_{CC} = (16)
GND = (8)
( ) = denotes pin numbers

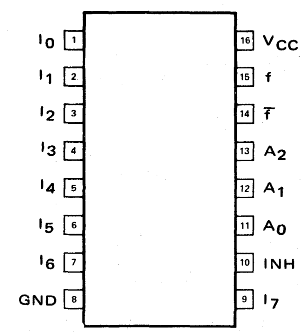
8232



V_{CC} = (16)
GND = (8)
( ) = denotes pin numbers

PIN CONFIGURATION

B,F,W PACKAGE



DESCRIPTION

The 8-Input Digital Multiplexer is the logical equivalent of a single-pole, 8 position switch whose position is specified by a 3-bit input address.

The 8230 incorporates an INHIBIT input which, when low, allows the one-of-eight inputs selected by the address to appear on the f output and, in complement, on the f̄ output. With the INHIBIT input high, the f output is unconditionally low and the f̄ output is unconditionally high. The 8230 is a functional and pin-for-pin replacement for the 9312.

The 8231 is a variation of the 8230 that provides open collector output f̄ for expansion of input terms. The 8232 is similar to the 8230 except in the effect of the INHIBIT input on the f̄ output. With the INHIBIT input low, the selected input appears at the f output and, in complement, on the f̄ output. With the INHIBIT input high, both the f and the f̄ output are unconditionally low.

TRUTH TABLE

ADDRESS			DATA INPUTS									OUTPUT		
A_2	A_1	A_0	I_7	I_6	I_5	I_4	I_3	I_2	I_1	I_0	INH	f	8230/ 82S30 8231/ 82S31 $\bar{f}$	8232/ 82S32 $\bar{f}$
0	0	0	x	x	x	x	x	x	x	1	0	1	0	0
0	0	1	x	x	x	x	x	x	1	x	0	1	0	0
0	1	0	x	x	x	x	x	1	x	x	0	1	0	0
0	1	1	x	x	x	x	1	x	x	x	0	1	0	0
1	0	0	x	x	x	1	x	x	x	x	0	1	0	0
1	0	1	x	x	1	x	x	x	x	x	0	1	0	0
1	1	0	x	1	x	x	x	x	x	x	0	1	0	0
1	1	1	1	x	x	x	x	x	x	x	0	1	0	0
0	0	0	x	x	x	x	x	x	x	0	0	0	1	1
0	0	1	x	x	x	x	x	x	0	x	0	0	1	1
0	1	0	x	x	x	x	x	0	x	x	0	0	1	1
0	1	1	x	x	x	x	0	x	x	x	0	0	1	1
1	0	0	x	x	x	0	x	x	x	x	0	0	1	1
1	0	1	x	x	0	x	x	x	x	x	0	0	1	1
1	1	0	x	0	x	x	x	x	x	x	0	0	1	1
1	1	1	0	x	x	x	x	x	x	x	0	0	1	1
x	x	x	x	x	x	x	x	x	x	x	1	0	1	0

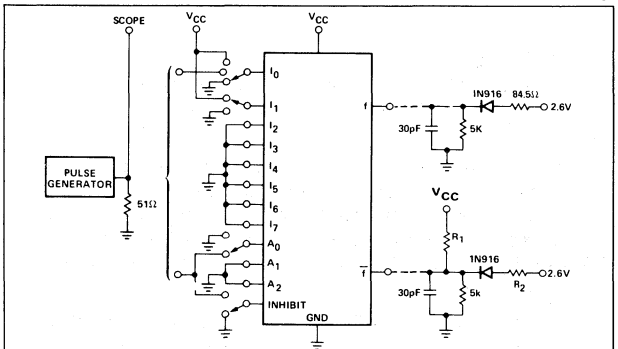
x = don't care

LOGIC

SWITCHING CHARACTERISTICS $T_A = 25°C$, $V_{CC} = 5V$

	LIMITS												
	8230		8231		8232		82S30		82S31		82S32		
PARAMETER	TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	UNIT
Propagation Delay													
A_n to $\bar{f}$	19	30	19	30	19	30	14	17	16	19	14	17	ns
I_n to $\bar{f}$	11	20	13	24	11	20	7	10	9	12	7	10	ns
$\bar{f}$ to f	10	15	10	15	10	15	6	9	6	9	6	9	ns
INH to $\bar{f}$	18	30	18	30	-	-	12	16	14	18	12	16	ns
INN to f or $\bar{f}$	-	-	-	-	11	20	-	-	-	-	-	-	ns

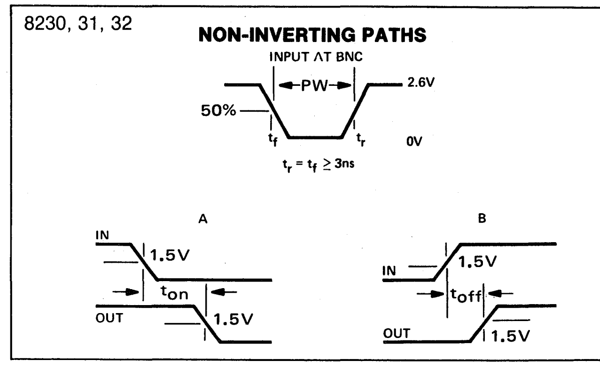
AC TEST FIGURE AND WAVEFORMS (8230/31/32)

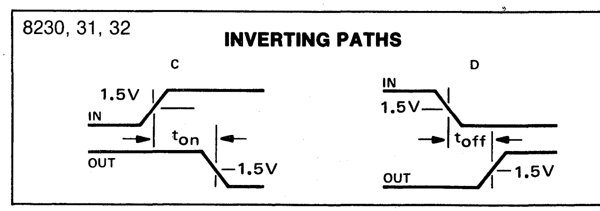


	8302/32	8231
R_1	∞	360Ω
R_2	84.5Ω	440Ω

NOTES:
1. 5K, 30pF load includes test jigs and scope impedance.
2. Scope terminals to be < 1½" from package pins.
3. See truth table for logical conditions.

AC TEST FIGURES AND WAVEFORMS





AC TEST CONDITIONS— 8230, 31, 32

STEP NO.	TYPE/S	DELAY FROM-TO	INPUTS				WAVE-FORM TYPE
			I_0	I_1	A_0	INH	
1	ALL	A_0 to $\bar{f}$	0V	V_{CC}	P.G.	0V	C, D
2	ALL	I_0 to $\bar{f}$	P.G.	0V	0V	0V	C, D
3	ALL	f to f*	P.G.	0V	0V	0V	C, D
4	8230 8231	INH to $\bar{f}$	V_{CC}	0V	0V	P.G.	A, B
5	8232	INH to $\bar{f}$	0V	0V	0V	P.G.	C, D
6	8232	INH to f	V_{CC}	0V	0V	P.G.	C, D

NOTE: 1. P.G. = pulse generator
*Both f and $\bar{f}$ are simultaneously loaded.

AC TEST CONDITIONS—82S30, 31, 32

TEST NO.	INPUTS												OUTPUTS	
	A_0	A_1	A_2	INH	I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7	$\bar{F}$	F
1	PG	0	0	0	0	1	0	0	0	0	0	0	T	T
2	0	PG	0	0	0	0	1	0	0	0	0	0	T	
3	0	0	PG	0	0	0	0	0	1	0	0	0	T	
4	0	1	1	PG	0	0	0	0	0	1	0	0	T	
5	1	1	1	0	0	0	0	0	0	0	0	PG	T	

F. "I" = 2.7V "0" = GROUND

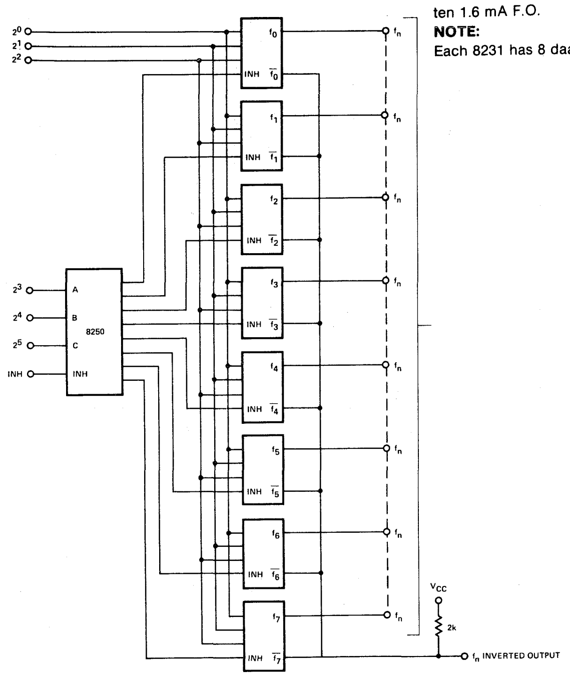
NOTE
1. AC test jigs must not have any switches.
2. AC test jigs must have less than ⅛ inch lead lengths from package pins.

TYPICAL APPLICATIONS

EXPANSION OF 8231 TO MULTIPLEXER 64 LINES

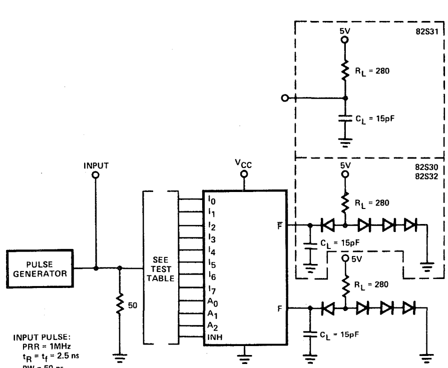
fn=f0+f1+f2. . . . . . f7
True Output
All Outputs may be tied together
to drive 8 x 16mA (eight 1.6mA F.O.)
or each Output may drive separately
ten 1.6 mA F.O.

NOTE:
Each 8231 has 8 daa inputs which are not shown.

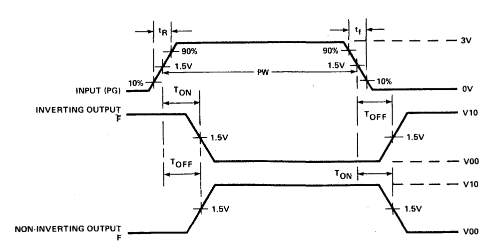


NOTE: ALL RESISTORS VALUES ARE TYPICAL AND IN OHMS.

A.C. TEST FIGURE AND WAVEFORMS



INPUT PULSE:
PRR = 1MHz
$t_R = t_f = 2.5$ ns
PW = 50 ns
ALL DIODES ARE 1N3064
C_L INCLUDES PROBE AND JIG CAPACITANCE
ALL RESISTORS VALUES ARE TYPICAL AND IN OHMS



DESCRIPTION

These devices are 2-input, 4-bit Digital Multiplexers designed for general purpose data-selection applications.

The 8233 features *non-inverting* data paths; and, the 8234 features *inverting* data paths.

The 8235 is designed for input to adders, registers and general paralleled data handling due to its capability to perform CONDITIONAL COMPLEMENTING (TRUE/COMPLEMENT). When the two inputs for each bit position (Ai, Bi) are connected together, the f output will provide either the *True* or *Complement* of the input data. This capability is especially useful for transferring data into parallel adders where both true data for adding or multiplying and also complemented data for subtracting or dividing are needed.

The 8234 and 8235 designs have open collector outputs which permit direct wiring to other open collector outputs (collector logic) to yield "free" four-bit words. As many as one hundred four-bit words can be multiplexed by using fifty 8234/8235s in the WIRED-AND mode.

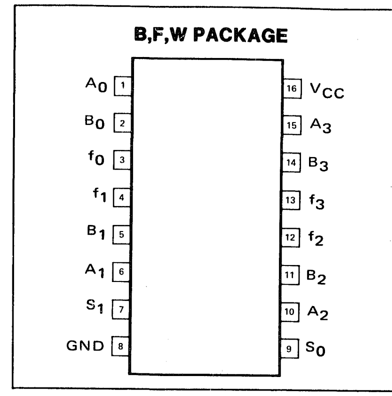
The inhibit state $S_0 = S_1 = 1$ can be used to facilitate transfer operations in an arithmetic section.

TRUTH TABLE

	S_0	S_I	f_n
8233/82S33	0	0	B
	1	0	A
	0	1	B
	1	1	0
8234/82S34	0	0	$\overline{B}$
	1	0	$\overline{A}$
	0	1	$\overline{B}$
	1	1	1
8235	0	0	$\overline{A}_n B_n$
	0	1	B_n
	1	0	$\overline{A}n$
	1	1	1

V_{CC} = (16)
GND = (8)
( ) = denotes pin numbers

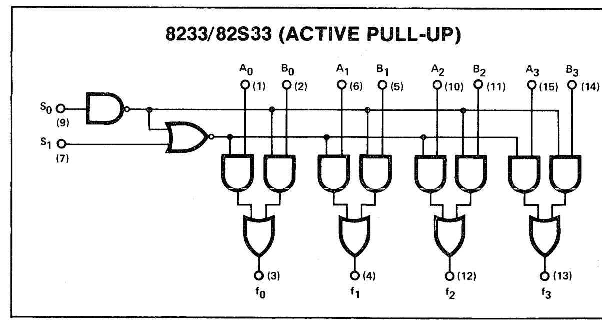
PIN CONFIGURATION

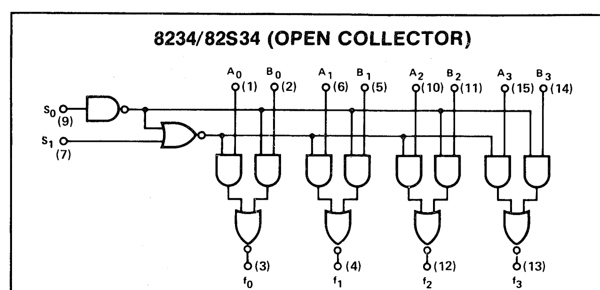


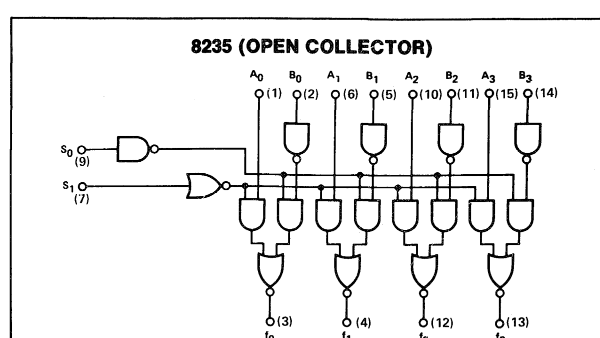
SPEED/PACKAGE AVAILABILITY

8233, 34, 35—B, F, W
82S33, S34—B, F

LOGIC DIAGRAMS

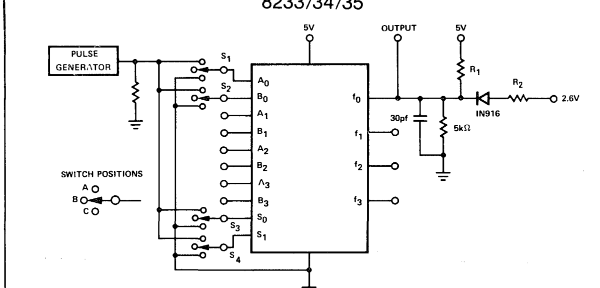






AC TEST FIGURE

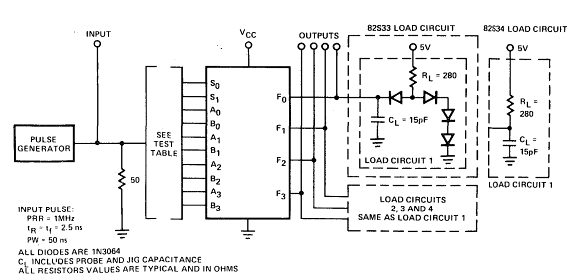
8233/34/35



	R_1	R_2
8233	∞	84.5Ω
8234 8235	360Ω	440Ω

Input pulse:
Amplitude = 2.6v
PW = 200ns
PRR = 1 MHz
$t_r = t_f$ = 5ns

82S33, 82S34

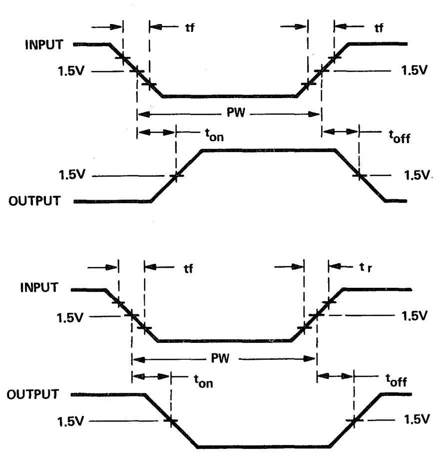


SWITCHING CHARACTERISTICS $T_A=25°C$, $V_{CC}=5V$

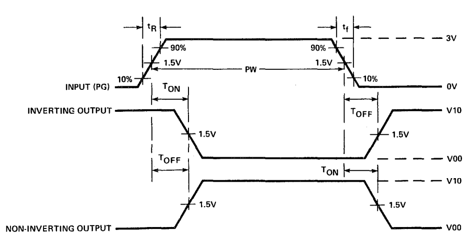
PARAMETER	LIMITS										UNIT
	8233		8234		8235		82S33		82S34		
	TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
t_{on} Turn-on Time											
A_n,B_n to f_n	16	25	16	25	-	-	7	12	7	12	ns
S_0 to f_n	27	38	27	38	27	38	13	18	13	18	ns
S_1 to f_n	27	38	27	38	27	38	11	16	11	16	ns
A_n to f_n	-	-	-	-	16	25	-	-	-	-	ns
B_n to f_n	-	-	-	-	24	35	-	-	-	-	ns
t_{off} Turn-off Time											
A_n, B_n to f_n	16	25	16	25	-	-	7	12	7	12	ns
S_0 to f_n	27	38	27	38	27	38	13	18	13	18	ns
S_1 to f_n	27	38	27	38	27	38	11	16	11	16	ns
A_n to f_n	-	-	-	-	16	25	-	-	-	-	ns
B_n to f_n	-	-	-	-	24	35	-	-	-	-	ns

PULSE REQUIREMENTS

82S33/82S34



82S33/82S34



AC TEST CONDITIONS— 8233, 8234, 8235

PRODUCT	PATH	PARAMETER	S_1	S_2	S_3	S_4
ALL	A_0 to f_0	t_{on} t_{off}	a	b	b	c
8233 8234	B_0 to f_0	t_{on} t_{off}	c	a	c	b
8233 8234	S_0 to f_0	t_{on} t_{off}	b	b	a	b
8233 8234	S_0 to f_0	t_{on} t_{off}	b	c	a	c
8235	B_0 to f_0	t_{on} t_{off}	c	a	c	b
8235	B_0 to f_0	t_{on} t_{off}	b	c	a	b
8235	S_1 to f_0	t_{on} t_{off}	b	b	c	a
8233 8234	S_1 to f_0	t_{on} t_{off}	b	c	b	a

AC TEST CONDITIONS—82S33, 82S34

TEST NO.	INPUTS										OUTPUTS			
	S_0	S_1	A_0	B_0	A_1	B_1	A_2	B_2	A_3	B_3	F_0	F_1	F_2	F_3
1	PG	0	1	0	1	0	1	0	1	0	T			
2	PG	0	1	0	1	0	1	0	1	0	T	T	T	T
3	PG	0	0	1	0	1	0	1	0	1		T		
4	1	PG	1	0	1	0	1	0	1	0			T	
5	0	0	0	PG	0	0	0	0	0	0	T			
6	0	1	0	0	0	PG	0	0	0	0		T		
7	1	0	0	0	0	0	PG	0	0	0			T	
8	1	0	0	0	0	0	0	0	PG	0				T

"1"=2.7V "0"=GROUND

NOTE
1. AC test jigs must not have any switches.
2. AC test jigs must have less than ⅛ inch lead length from package pins.

SPEED/PACKAGE AVAILABILITY

8241, 42—A, F, W
82S41, S42—A, F

DESCRIPTION

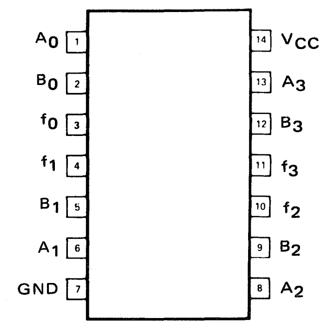
The 8241 contains four independent gating structures to perform the Exclusive-OR function on two input variables.

The output of the 8241 employs the totem-pole structure characteristic of TTL devices.

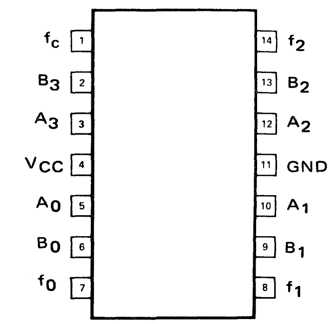
The 8242 contains four independent Exclusive-NOR gates which may be used to implement digital comparison functions. The 8242 outputs are bare collector to facilitate implementation of multiple-bit comparisons; a 4-bit comparison is made by connecting the outputs of the four independent gates together.

PIN CONFIGURATION

A,F PACKAGE



W PACKAGE



TRUTH TABLE

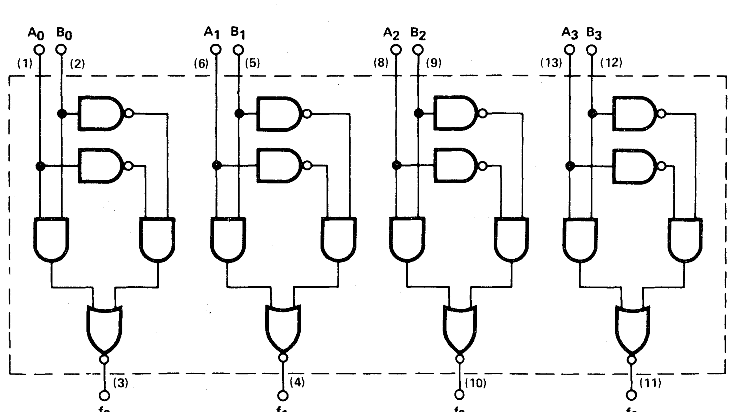
	A	B	f
8241/82S41	0	0	0
	1	0	1
	0	1	1
	1	1	0
8242/82S42	0	0	1
	1	0	0
	0	1	0
	1	1	1

SWITCHING CHARACTERISTICS $T_A=25°C$, $V_{CC}=5V$

PARAMETER	LIMITS								
	8241		8242		82S41		82S42		
	TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	UNIT
Propagation Delay									
t_{on} Turn-on time	17	23			7	10	9	14	ns
t_{off} Turn-off time	11	17			7	10	9	14	
Inverting path									
t_{on} Turn-on time			12	20					
t_{off} Turn-off time			14	23					
Non-inverting path									
T_{on} Turn-on time			14	2					
t_{off} Turn-off time			20	28					

LOGIC DIAGRAM

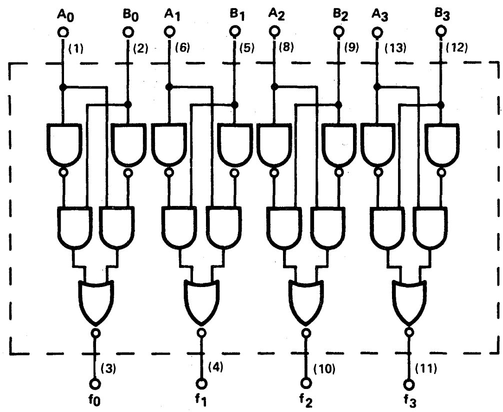
8241, 82S41 QUAD EXCLUSIVE-OR



V_{CC} = (14)
GND = (7)
( ) = denotes pin numbers for 14-pin dual-in-line package

LOGIC DIAGRAM

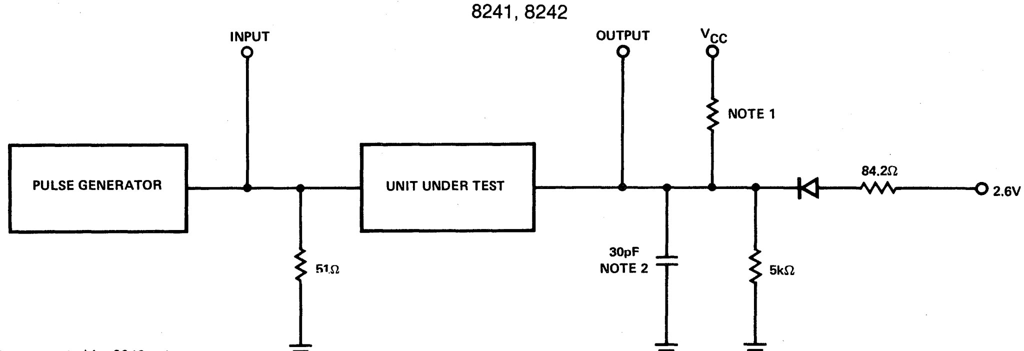
8242 4-BIT DIGITAL COMPARATOR (OPEN COLLECTOR)



V_{CC} = (14)
GND = (7)
( ) = denotes pin numbers for 14 pin dual-in-line package

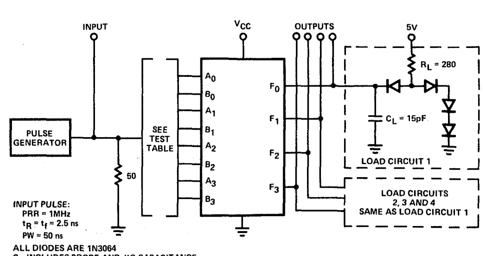
AC TEST FIGURE

8241, 8242

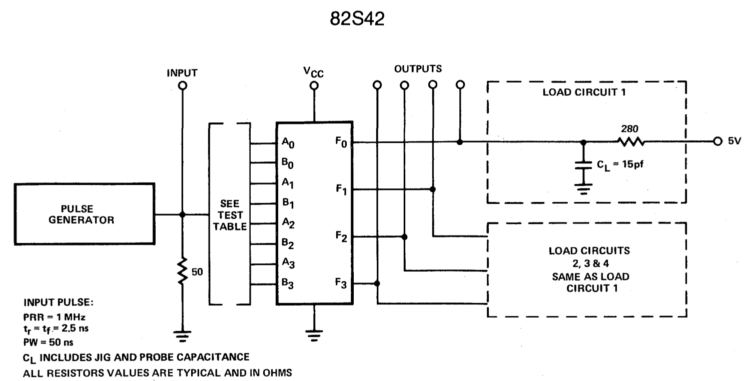


NOTE:
1. 530Ω resistor connected for 8242 only.
2. 5kΩ and 30pF includes jig and scope.

82S41



AC TEST FIGURE



TEST TABLE—82S41

—	A0	B0	A1	B1	A2	B2	A3	B3	F0	F1	F2	F3
	INPUTS								OUTPUTS			
	0	0	PG	1	0	0	0	0		T		
	0	0	1	PG	0	0	0	0		T		
3	PG	1	0	0	0	0	0	0	T			
	1	PG	0	0	0	0	0	0	T			
5	0	0	0	0	1	PG	0	0		T		
6	0	0	0	0	PG	1	0	0			T	
7	0	0	0	0	0	0	1	PG				T
8	0	0	0	0	0	0	0	PG	1			T

"1"=2.7V, "0"=GROUND

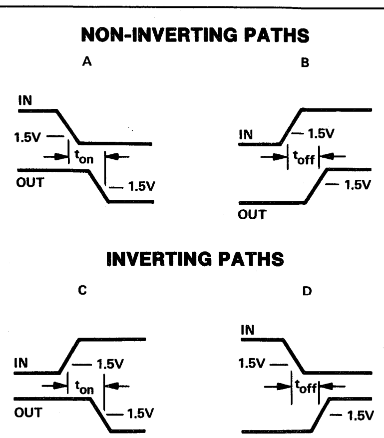
TEST TABLE—82S42

TEST #	A0	B0	A1	B1	A2	B2	A3	B3	F0	F1	F2	F3
	INPUTS								OUTPUTS			
1	0	0	PG	1	0	0	0	0		T		
2	0	0	1	PG	0	0	0	0		T		
3	PG	1	0	0	0	0	0	0	T			
4	1	PG	0	0	0	0	0	0	T			
5	0	0	0	0	1	PG	0	0			T	
6	0	0	0	0	PG	1	0	0			T	
7	0	0	0	0	0	0	1	PG				T
8	0	0	0	0	0	0	PG	1				T

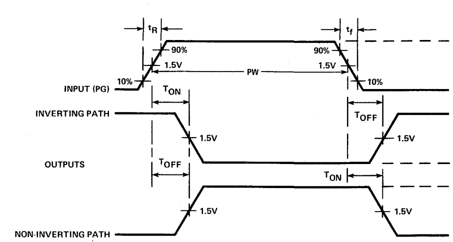
"1" = 2.7V, "0" = GROUND

NOTE
1. AC test jigs must not have any switches.
2. AC test jigs must have less than ⅛ inch lead length from package pins.

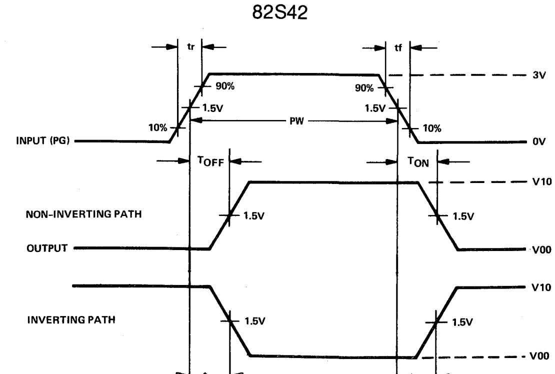
PROPAGATION DELAY WAVEFORMS



82S41

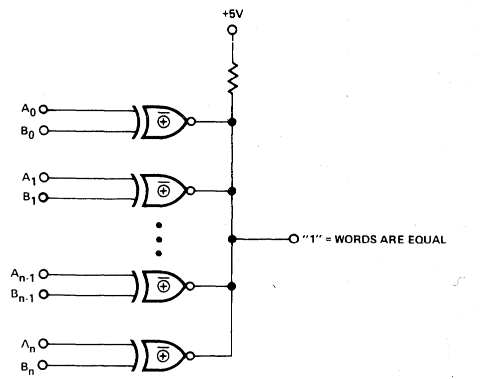


82S42

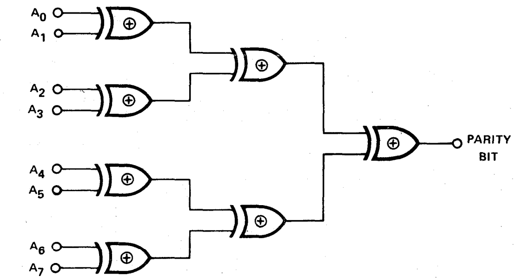


TYPICAL APPLICATIONS

EQUALITY GATE USED FOR COMPARISON



PARITY GENERATOR/TESTER



8-BIT POSITION SCALER 8243

8243-N,F,Q

DESCRIPTION

The 8243 8-Bit Position Scaler is an MSI array of approximately 70 gate complexity. The primary function of the 8243 is to scale (or shift) data bit positions by a selection of a 3-bit binary selector code.

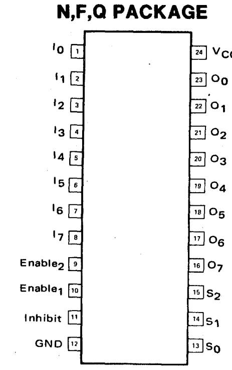
The most significant bit input (I_7) may be shifted 8 positions to the least significant bit output (O_0). At zero shift, or scale select, all eight input data bits are transferred and inverted to their respective outputs, (I_0 to O_0, I_1 to O_1, I_2 to O_2, etc.) At a shift, or scale select, of one, each input bit (I_n) will shift to the next lower output bit (O_{n-1}). See truth table for other shift codes.

The 8243's advantages over shift registers are the speed of operation and lower complexity of external logic required to effect a scale function. The speed of the 8243 Scaler is a function of gate propagation delays—the speed of equivalent shift registers is the time for clock periods plus the propagation delay to effect a scale function.

The 8243 is provided with open collector outputs to provide expansion to larger scaling functions. Data input logic zero loading is reduced to less than —100μA when the unit is disabled.

PIN CONFIGURATION

N,F,Q PACKAGE

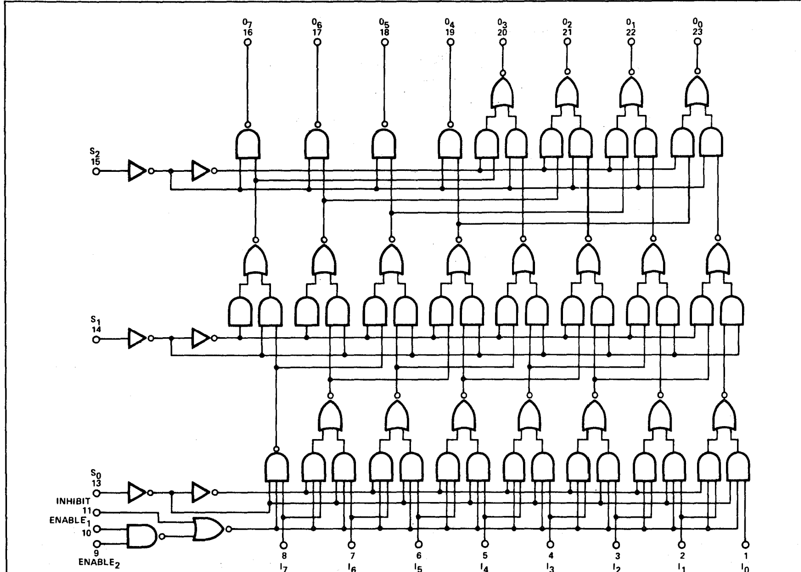


TRUTH TABLE

INHIBIT	ENABLE 1 & 2	S_0	S_1	S_2	O_0	O_1	O_2	O_3	O_4	O_5	O_6	O_7
0	1	0	0	0	$\bar{I}_0$	$\bar{I}_1$	$\bar{I}_2$	$\bar{I}_3$	$\bar{I}_4$	$\bar{I}_5$	$\bar{I}_6$	$\bar{I}_7$
0	1	1	0	0	$\bar{I}_1$	$\bar{I}_2$	$\bar{I}_3$	$\bar{I}_4$	$\bar{I}_5$	$\bar{I}_6$	$\bar{I}_7$	1
0	1	0	1	0	$\bar{I}_2$	$\bar{I}_3$	$\bar{I}_4$	$\bar{I}_5$	$\bar{I}_6$	$\bar{I}_7$	1	1
0	1	1	1	0	$\bar{I}_3$	$\bar{I}_4$	$\bar{I}_5$	$\bar{I}_6$	$\bar{I}_7$	1	1	1
0	1	0	0	1	$\bar{I}_4$	$\bar{I}_5$	$\bar{I}_6$	$\bar{I}_7$	1	1	1	1
0	1	1	0	1	$\bar{I}_5$	$\bar{I}_6$	$\bar{I}_7$	1	1	1	1	1
0	1	0	1	1	$\bar{I}_6$	$\bar{I}_7$	1	1	1	1	1	1
0	1	1	1	1	$\bar{I}_7$	1	1	1	1	1	1	1
1	X	X	X	X	1	1	1	1	1	1	1	1
X	0	X	X	X	1	1	1	1	1	1	1	1

X indicates either logic "1" or logic "0" may be present.

LOGIC DIAGRAM



V_{CC} = (24)
GND = (12)
( ) = denotes pin numbers

NOTE: All inputs have diode clamps.

SWITCHING CHARACTERISTICS T_A = 25°C and V_{CC} = 5.0V

PARAMETER	TEST CONDITIONS	LIMITS TYP	LIMITS MAX	UNIT
Propagation delay				
Data in	I_n,S_0,S_1,S_2,	20	32	ns
Select S_n	Enable 1 & 2	30	40	
Inhibit	Inhibit = 10mA	25	35	
Enable 1 & 2		30	45	

NOTES
I_n "O" threshold 0.7 volts for S8243.

AC TEST TABLES

SCALE FACTOR	OUTPUTS 1	2	3	4	5	6	7	
0	A	B	C	D	E	F	G	SCALE
1	1	A	B	C	D	E	F	RIGHT
2	1	1	A	B	C	D	E	
3	1	1	1	A	B	C	D	
4	1	1	1	1	A	B	C	
5	1	1	1	1	1	A	B	SCALE = 0
6	1	1	1	1	1	1	A	AROUND = 0
7	1	1	1	1	1	1	1	

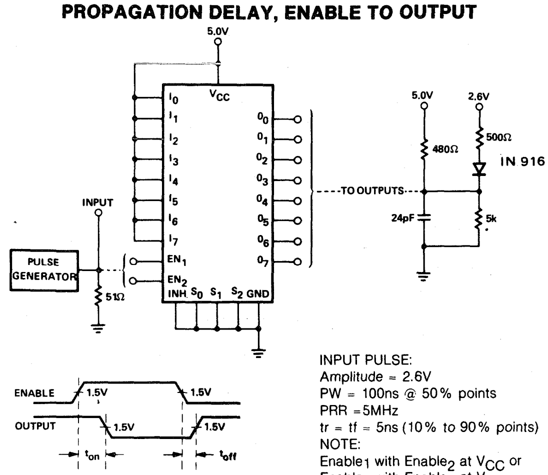
SCALE FACTOR	OUTPUTS 1	2	3	4	5	6	7	
0	A	B	C	D	E	F	G	SCALE
1	B	C	D	E	F	G	1	LEFT
2	C	D	E	F	G	1	1	
3	D	E	F	G	1	1	1	
4	E	F	G	1	1	1	1	
5	F	G	1	1	1	1	1	SCALE = 1
6	G	1	1	1	1	1	1	AROUND = 0
7	1	1	1	1	1	1	1	

SCALE FACTOR	OUTPUTS 1	2	3	4	5	6	7	
0	A	B	C	D	E	F	G	SCALE
1	G	A	B	C	D	E	F	RIGHT
2	F	G	A	B	C	D	E	& AROUND
3	E	F	G	A	B	C	D	
4	D	E	F	G	A	B	C	
5	C	D	E	F	G	A	B	SCALE = 0
6	B	C	D	E	F	G	A	AROUND = 1
7	A	B	C	D	E	F	G	

SCALE FACTOR	OUTPUTS 1	2	3	4	5	6	7	
0	A	B	C	D	E	F	G	SCALE
1	B	C	D	E	F	G	A	LEFT
2	C	D	E	F	G	A	B	& AROUND
3	D	E	F	G	A	B	C	
4	E	F	G	A	B	C	D	
5	F	G	A	B	C	D	E	SCALE = 1
6	G	A	B	C	D	E	F	AROUND = 1
7	A	B	C	D	E	F	G	

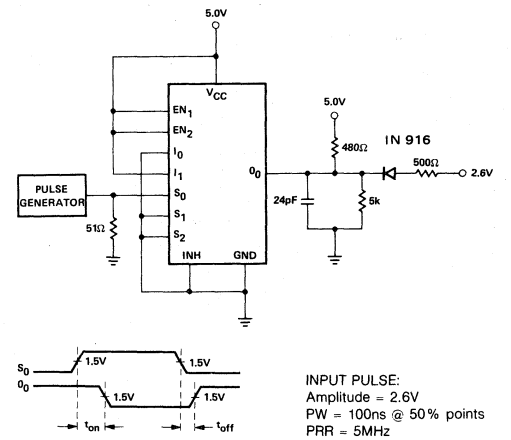
AC TEST FIGURE AND WAVEFORMS

PROPAGATION DELAY, ENABLE TO OUTPUT



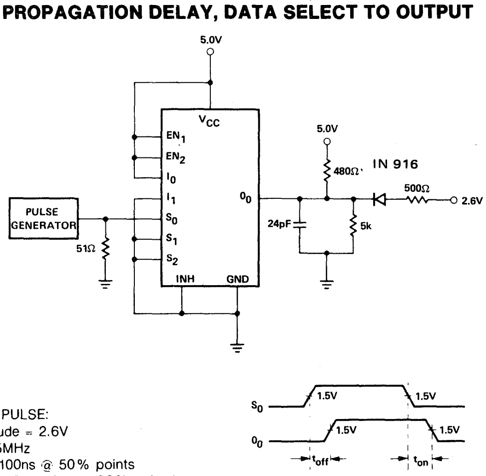
INPUT PULSE:
Amplitude = 2.6V
PW = 100ns @ 50% points
PRR = 5MHz
tr = tf = 5ns (10% to 90% points)
NOTE:
$Enable_1$ with $Enable_2$ at V_{CC} or $Enable_2$ with $Enable_1$ at V_{CC}.

PROPAGATION DELAY, DATA INPUT TO DATA OUTPUT



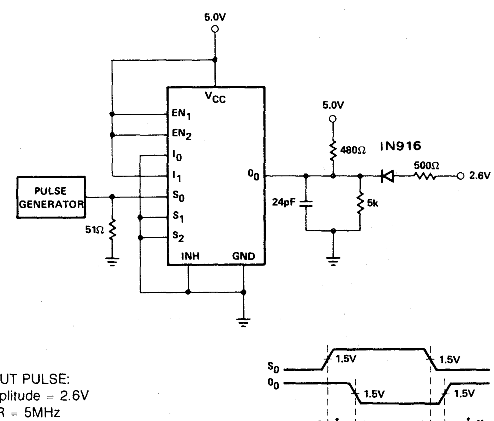
INPUT PULSE:
Amplitude = 2.6V
PW = 100ns @ 50% points
PRR = 5MHz
tr = tf = 5ns (10% to 90% points)

PROPAGATION DELAY, DATA SELECT TO OUTPUT



INPUT PULSE:
Amplitude = 2.6V
PRR = 5MHz
PW = 100ns @ 50% points
tr = tf = 5ns (10% to 90% points)

PROPAGATION DELAY, DATA SELECT TO OUTPUT



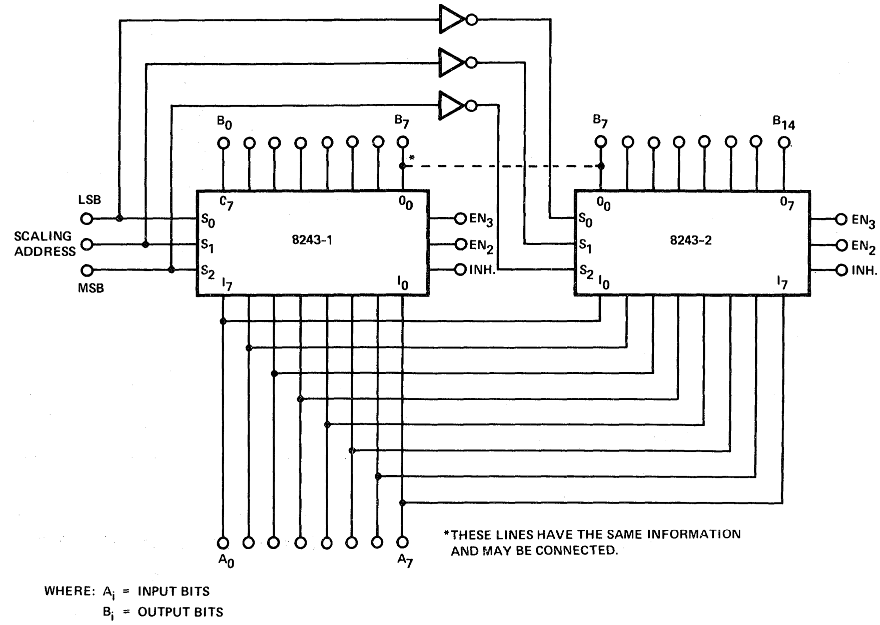
INPUT PULSE:
Amplitude = 2.6V
PRR = 5MHz
PW = 100ns @ 50% points
tr = tf = 5ns (10% to 90% points)

TRUTH TABLE FOR ARRAY EXPANSION

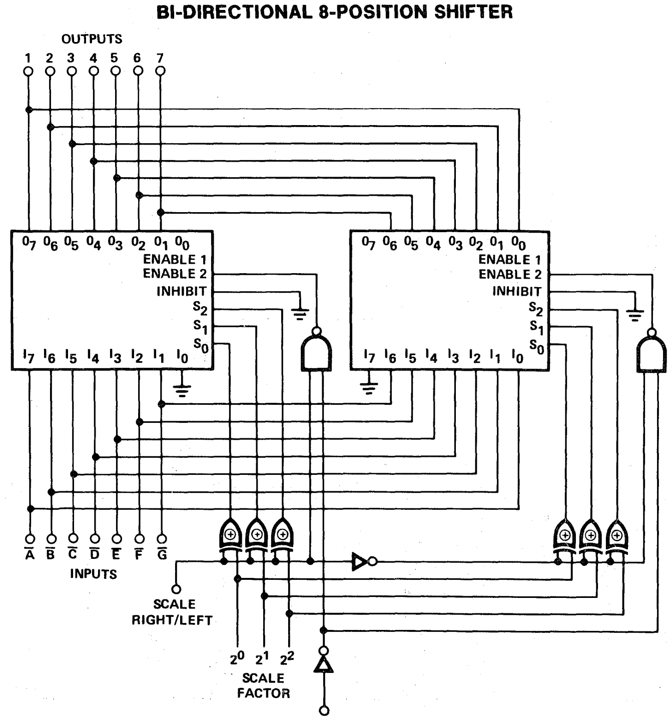
SCALE ADDRESS			8243-1								8243-2							
MSB		LSB	B_0	B_1	B_2	B_3	B_4	B_5	B_6	B_7	B_7	B_8	B_9	B_{10}	B_{11}	B_{12}	B_{13}	B_{14}
0	0	0	$\overline{A_0}$	$\overline{A_1}$	$\overline{A_2}$	$\overline{A_3}$	$\overline{A_4}$	$\overline{A_5}$	$\overline{A_6}$	$\overline{A_7}$	$\overline{A_7}$	1	1	1	1	1	1	1
0	0	1	1	$\overline{A_0}$	$\overline{A_1}$	$\overline{A_2}$	$\overline{A_3}$	$\overline{A_4}$	$\overline{A_5}$	$\overline{A_6}$	$\overline{A_6}$	$\overline{A_7}$	1	1	1	1	1	1
0	1	0	1	1	$\overline{A_0}$	$\overline{A_1}$	$\overline{A_2}$	$\overline{A_3}$	$\overline{A_4}$	$\overline{A_5}$	$\overline{A_5}$	$\overline{A_6}$	$\overline{A_7}$	1	1	1	1	1
0	1	1	1	1	1	$\overline{A_0}$	$\overline{A_1}$	$\overline{A_2}$	$\overline{A_3}$	$\overline{A_4}$	$\overline{A_4}$	$\overline{A_5}$	$\overline{A_6}$	$\overline{A_7}$	1	1	1	1
1	0	0	1	1	1	1	$\overline{A_0}$	$\overline{A_1}$	$\overline{A_2}$	$\overline{A_3}$	$\overline{A_3}$	$\overline{A_4}$	$\overline{A_5}$	$\overline{A_6}$	$\overline{A_7}$	1	1	1
1	0	1	1	1	1	1	1	$\overline{A_0}$	$\overline{A_1}$	$\overline{A_2}$	$\overline{A_2}$	$\overline{A_3}$	$\overline{A_4}$	$\overline{A_5}$	$\overline{A_6}$	$\overline{A_7}$	1	1
1	1	0	1	1	1	1	1	1	$\overline{A_0}$	$\overline{A_1}$	$\overline{A_1}$	$\overline{A_2}$	$\overline{A_3}$	$\overline{A_4}$	$\overline{A_5}$	$\overline{A_6}$	$\overline{A_7}$	1
1	1	1	1	1	1	1	1	1	1	$\overline{A_0}$	$\overline{A_0}$	$\overline{A_1}$	$\overline{A_2}$	$\overline{A_3}$	$\overline{A_4}$	$\overline{A_5}$	$\overline{A_6}$	$\overline{A_7}$

TYPICAL APPLICATIONS

ARRAY EXPANSION



BI-DIRECTIONAL 8-POSITION SHIFTER



SPEED/PACKAGE AVAILABILITY

8250—A,F,W
8251,52—B,F,W
82S50—A,F
82S52—B,F

DESCRIPTION

The 8250, 8251 and 8252 are gate arrays for decoding and logic conversion applications.

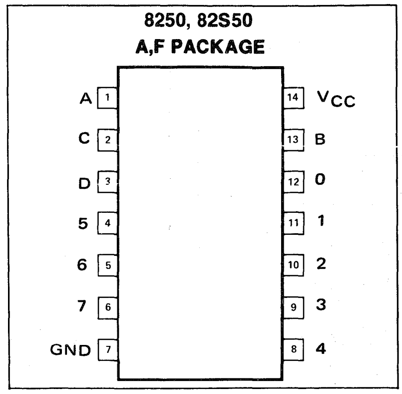
The 8250 converts 3 lines of input to a one-of-eight output. The fourth input line (D) is utilized as an inhibit to allow use in larger decoding networks.

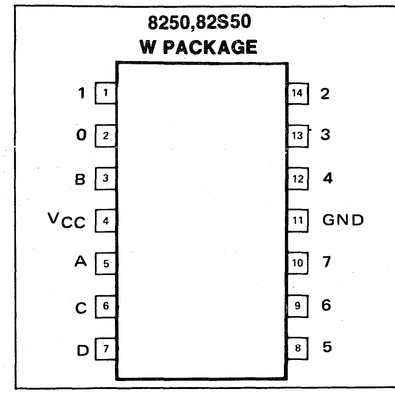
The 8251 and 8252 convert a 4 line input code (with 1-2-4-8 weighting) to a one-of-ten output as shown in the Truth Table.

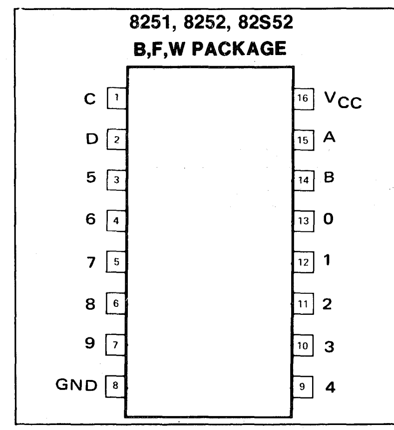
The 8252 is a direct replacement for the 9301 with all outputs being forced high when a binary code greater than nine is applied to the inputs.

The selected output is a logic "0".

PIN CONFIGURATION







TRUTH TABLE

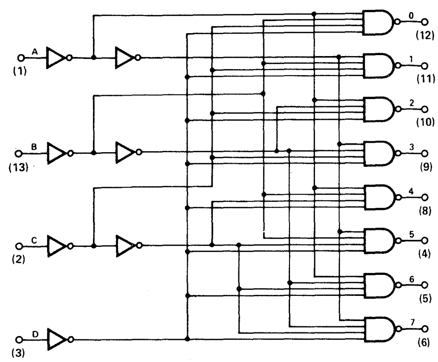
INPUT STATE				OUTPUT STATES											
				8250/82S50								8251		8252/ 82S52	
A	B	C	D	0	1	2	3	4	5	6	7	8	9	8	9
0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1
1	0	0	0	1	0	1	1	1	1	1	1	1	1	1	1
0	1	0	0	1	1	0	1	1	1	1	1	1	1	1	1
1	1	0	0	1	1	1	0	1	1	1	1	1	1	1	1
0	0	1	0	1	1	1	1	0	1	1	1	1	1	1	1
1	0	1	0	1	1	1	1	1	0	1	1	1	1	1	1
0	1	1	0	1	1	1	1	1	1	0	1	1	1	1	1
1	1	1	0	1	1	1	1	1	1	1	0	1	1	1	1
0	0	0	1	1	1	1	1	1	1	1	1	0	1	0	1
1	0	0	1	1	1	1	1	1	1	1	1	1	0	1	0
0	1	0	1	1	1	1	1	1	1	1	1	0	1	1	1
1	1	0	1	1	1	1	1	1	1	1	1	1	0	1	1
0	0	1	1	1	1	1	1	1	1	1	1	0	1	1	1
1	0	1	1	1	1	1	1	1	1	1	1	1	0	1	1
0	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1
1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1

SWITCHING CHARACTERISTICS $T_A = 25°C$, $V_{CC} = 5V$

PARAMETER		LIMITS										
		8250		8251		8252		82S50		82S52		
		TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	UNIT
t_{on}	TURN-ON DELAY	20	35	20	35	20	35	12	16	12	16	ns
t_{off}	TURN-OFF DELAY	20	35	20	35	20	35	12	16	12	16	ns

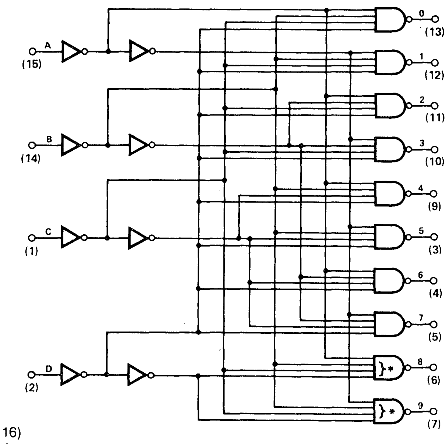
LOGIC DIAGRAMS

8250,82S50



VCC=(14)
GND = (7)
( ) = Denotes pin numbers

8251, 8252, 82S52



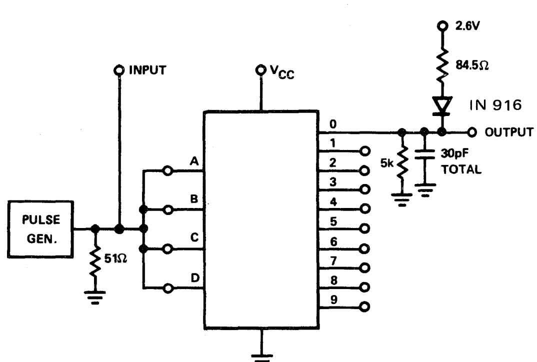
VCC = (16)
GND = (8)
( ) = Denotes pin numbers

*Connections made on 8252 only

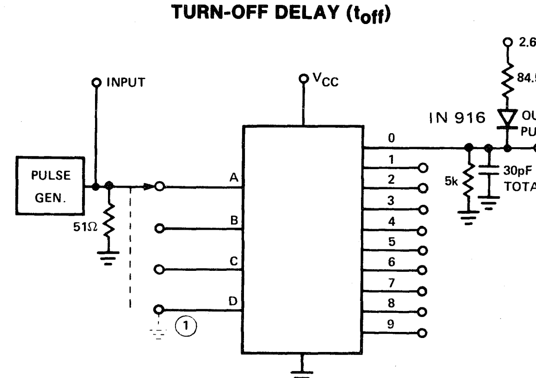
AC TEST FIGURE

8250, 8251, 8252

TURN-ON DELAY (t_{on})

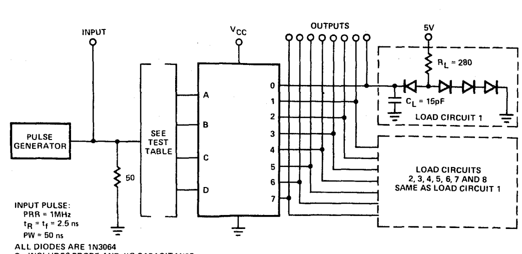


TURN-OFF DELAY (t_{off})



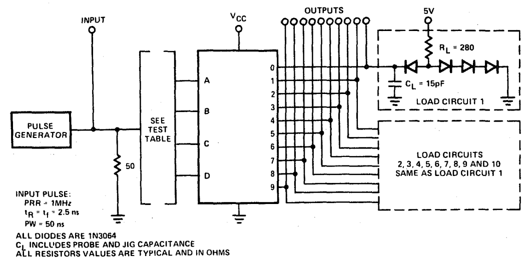
① Non-selected inputs are connected to ground.

82S50



AC TEST FIGURE (CONT'D.)

82S52



AC TEST TABLE

82S50

TEST	INPUTS				OUTPUTS							
NO.	A	B	C	D	0	1	2	3	4	5	6	7
1	1	1	PG	0								T
2	1	1	PG	0				T				T
3	PG	1	0	0			T	T				
4	0	PG	1	0					T		T	
5	0	0	0	PG	T							
6	1	0	PG	0		T				T		

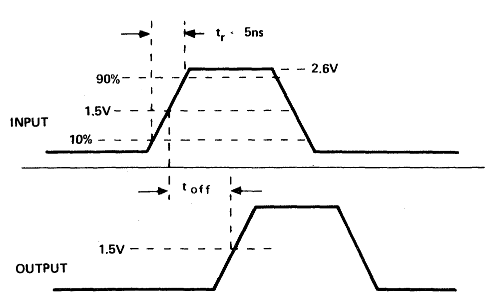
82S52

TEST	INPUTS				OUTPUTS									
NO.	A	B	C	D	0	1	2	3	4	5	6	7	8	9
1	0	0	PG	0					T					
2	PG	1	0	0			T	T						
3	0	0	0	PG	T								T	
4	1	0	PG	0		T				T				
5	1	PG	0	1										T
6	PG	1	1	0										

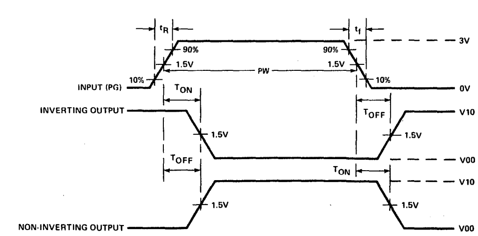
"1" = 2.7V "0" = Ground

VOLTAGE WAVEFORMS

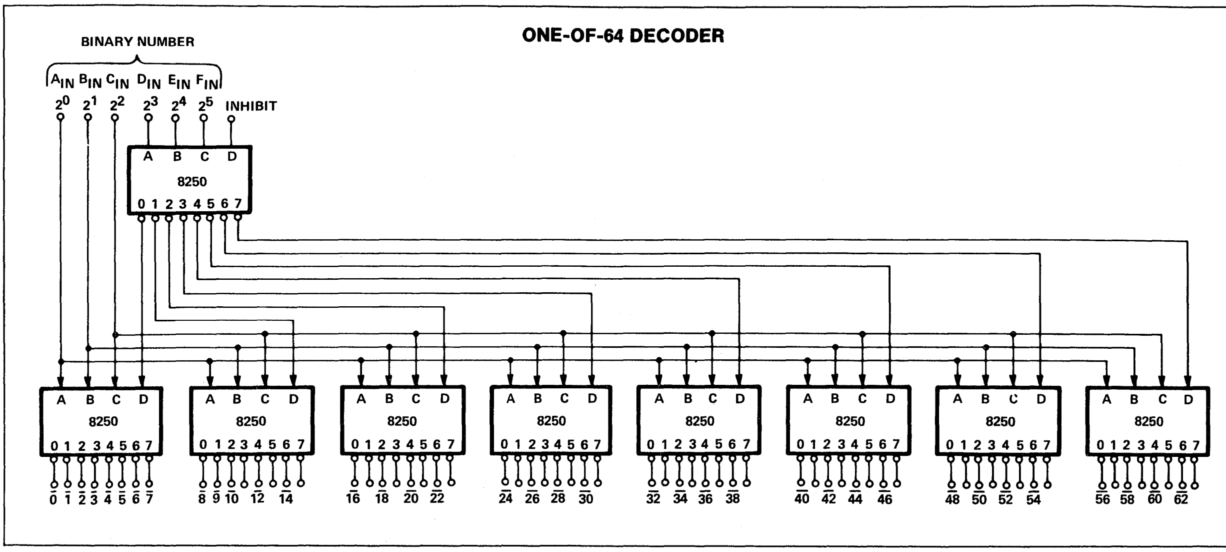
8250, 8251, 8252



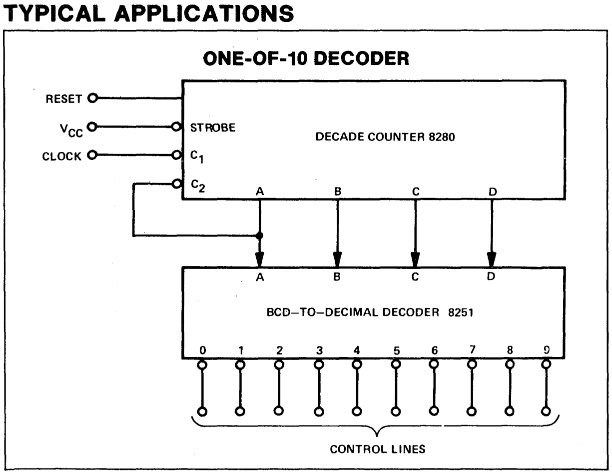
82S50, 82S52



TYPICAL APPLICATIONS



TYPICAL APPLICATIONS



8260-N,F,Q

DESCRIPTION

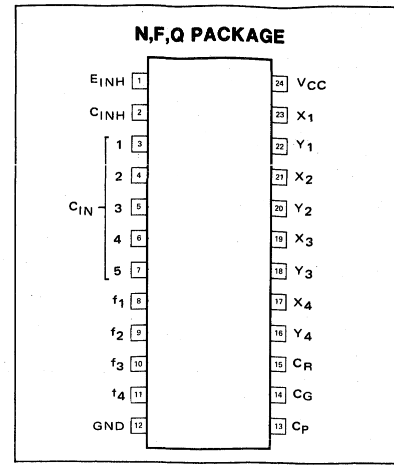
The 8260 Arithmetic Logic Element is a monolithic gate array incorporating four full-adders structured in a look-ahead mode. The device may be used as four mutually independent exclusive NOR or AND gates by proper addressing of the inhibit lines.

As a four-bit adder the 8260 permits high speed parallel addition of four sets of data and features both simultaneous addition on a character to character and on a bit to bit basis within the package.

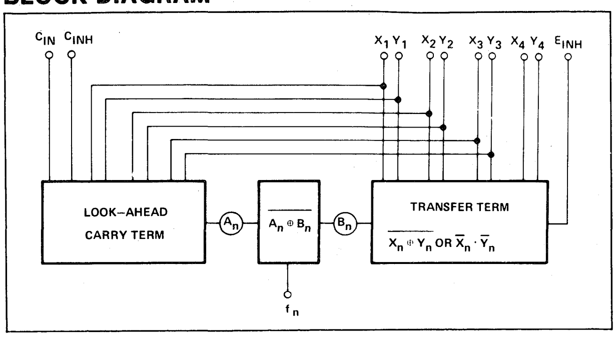
When true input variables are used, the true sum is formed at the f output. Inverted input variables produce the complement of the sum of the true variables.

The carry-outs available are: Internally Generated (C_G); Propagated (C_P); and Ripple (C_R). This gives the 8260 complete flexibility when used in Ripple Carry or Anticipated Carry Adder Systems.

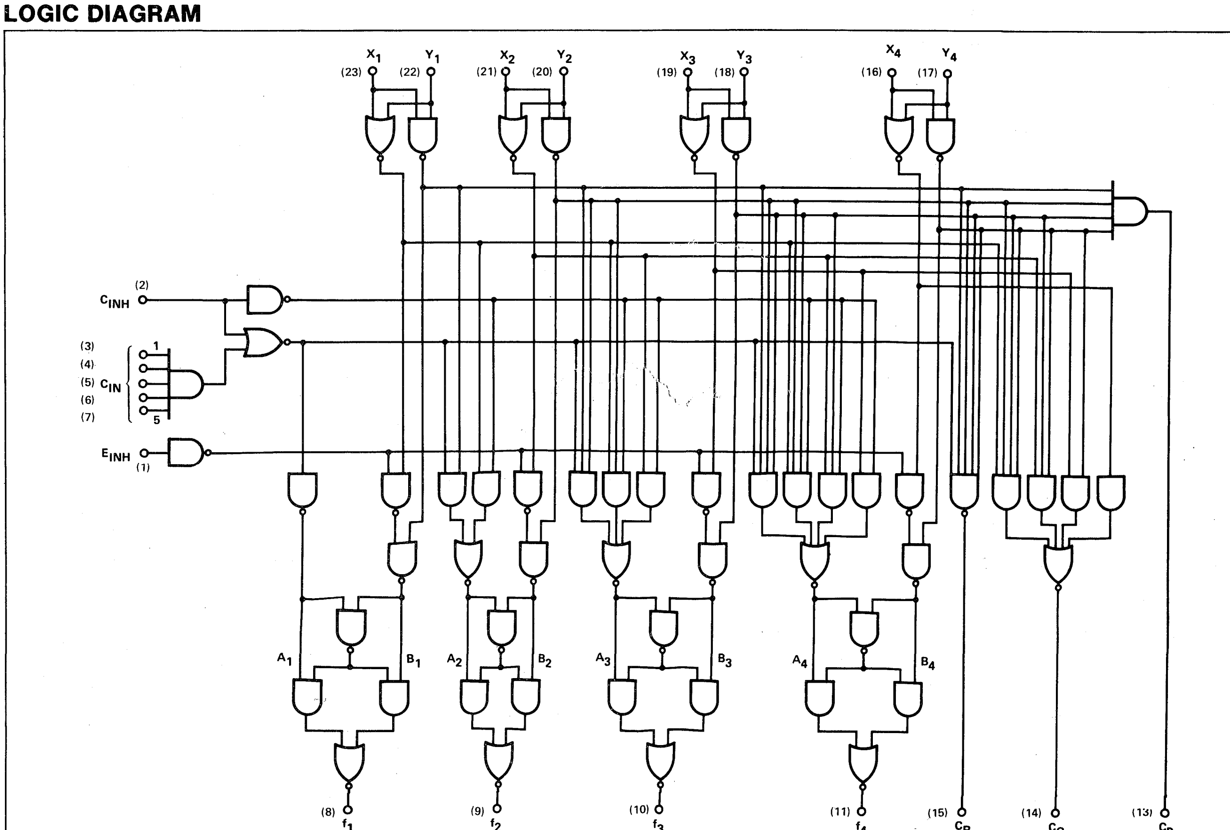
PIN CONFIGURATION



BLOCK DIAGRAM



LOGIC DIAGRAM



LOGIC

8260-N,F,Q

TRUTH TABLE

$C_{INH} = 1 \longrightarrow A_n = 1$
$C_{INH} = 0 \longrightarrow A_n = \downarrow$

C_{IN}	A_1	A_1	X_1	Y_1	A_2	A_2	X_2	Y_2	A_3	A_3	X_3	Y_3	A_4
0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	1	0	0	1	0	0	0	1	0	0	0	1	0
		0	1	0	0	0	1	0	0	0	1	0	0
		0	1	1	1	0	1	1	1	0	1	1	1
		1	0	0	0	1	0	0	0	1	0	0	0
		1	0	1	1	1	0	1	1	1	0	1	1
		1	1	0	1	1	1	0	1	1	1	0	1
		1	1	1	1	1	1	1	1	1	1	1	1

A_n	B_n	f_n
0	0	1
0	1	0
1	0	0
1	1	1

E_{INH}	X_n	Y_n	B_n
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

SWITCHING CHARACTERISTICS $T_A = 25°C$, $V_{CC} = 54$

PARAMETER	LIMITS TYP	LIMITS MAX	UNIT
Propagation Delay			
X_n, Y_n, C_{in} to C_R	14	20	ns
X_n, Y_n to C_p, C_G	14	20	
X_n, Y_n to f_n	24	33	
C_{in} to f_n	14	22	

MODE OF OPERATION

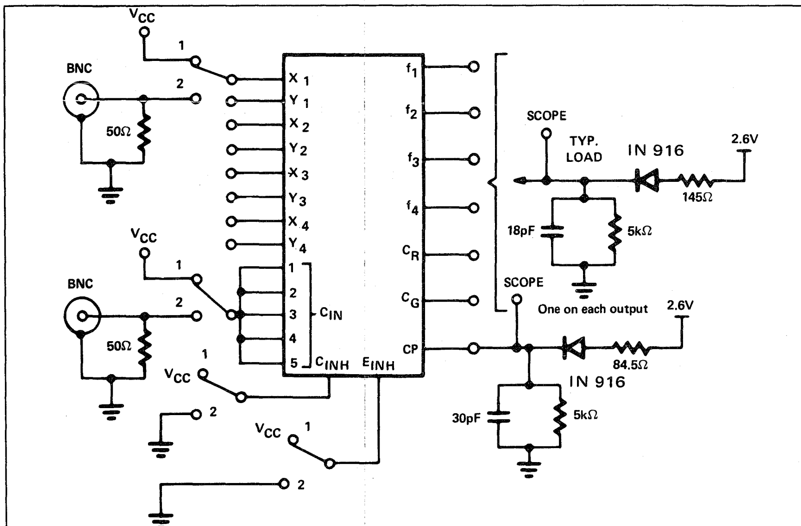
INPUTS	Least Significant C_{IN} Inputs to be*	CONTROLS C_{INH}	CONTROLS E_{INH}	f	
X_n, Y_n	0	0	0	Σ_n	Add
↓	0	0	1	--	Not used
↓	0	1	0	$X_nY_n + \overline{X}_n\overline{Y}_n$	Coincidence
↓	0	1	1	X_nY_n	AND
$\overline{X}_n$, $\overline{Y}_n$	1	0	0	$\overline{\Sigma}_n$	Add
↓	1	0	1	---	Not Used
↓	1	1	0	$\overline{X}_n\overline{Y}_n + X_nY_n$	Coincidence
↓	1	1	1	$\overline{X}_n\overline{Y}_n$	AND

*Least significant of a "Multiple Package"- adder system.

AC TEST TABLE

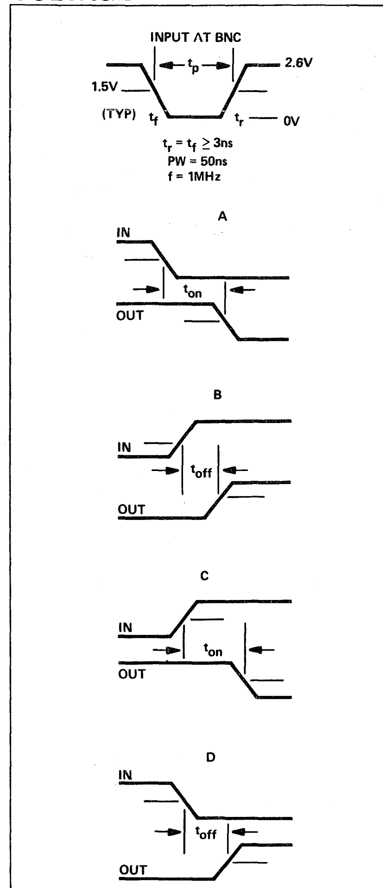
STEP NO.	DELAY FROM-TO	SWITCH POSITION: DRIVEN INPUTS	OTHER INPUTS X_1	Y_1	X_2	Y_2	X_3	Y_3	X_4	Y_4	C_{IN}	E_{INH}	C_{INH}	WAVEFORM TYPE
1	X_n to C_R or X_n to C_P	2	2	1	2	1	2	1	2	1	2	2	2	A,B / C,D
2	Y_n to C_R or Y_n to C_P	2	1	2	1	2	1	2	1	2	2	2	2	A,B / C,D
3	X_n, Y_n to f_n	2	1	1	1	1	1	1	1	1	1	1	1	A,B
4	C_{IN} to C_R	2	2	2	2	2	2	2	2	2	2	2	2	A,B
5	C_{IN} to f_n	2	1	2	1	2	1	2	1	2	2	2	2	C,D

AC TEST FIGURE



NOTE: Scope terminals to be ≤ ½" from Package Pins.

VOLTAGE WAVEFORM



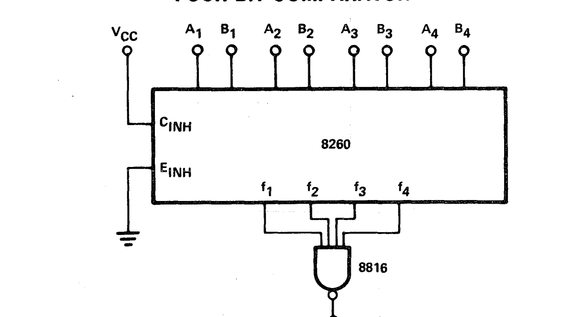
TYPICAL APPLICATIONS

The 8260 contains the control logic necessary to allow operation as a general purpose arithmetic logic device. Below, the internal carries are inhibited to effect Exclusive-NOR or coincidence operation. The 87260 may also be operated as four independent AND gates to implement masking and similar requirements of micro-programming.

The Ripple Adder System is the simplest but also the slowest application of the 8260. The typical total addition time (input to sum output for 12-bit ripple adder is 42ns).

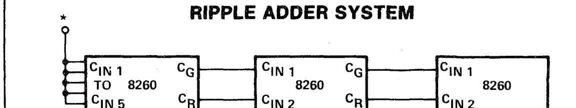
The Fast Adder System provides complete carry look-ahead addition for words to 24 bits in length and is the fastest application of the 8260 units. The typical total addition time for a 24 bit fast adder is 42ns.

FOUR-BIT COMPARATOR



"0" • A B

RIPPLE ADDER SYSTEM

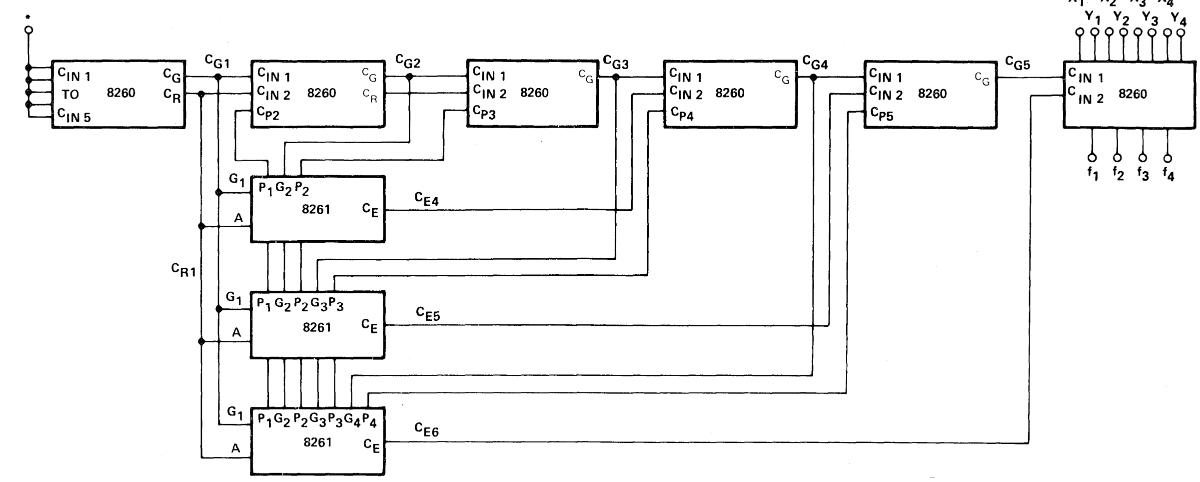


*Tied to V_{CC} if not-true inputs are used, otherwise to ground.

8260-N,F,Q

TYPICAL APPLICATIONS

24-BIT FAST ADDER SYSTEM



*Tied to V_{CC} if not-true inputs are used, otherwise to ground.

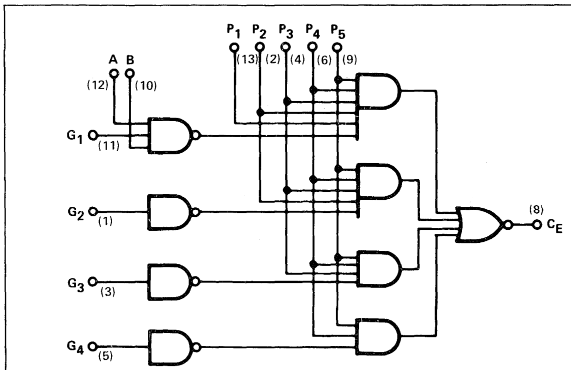
FAST CARRY EXPANDER 8261

8261-A,F,W

DESCRIPTION

The 8261 Fast Carry Extender is a monolithic gate array designed specifically to be used in conjunction with the 8260 Arithmetic Logic element. A 8260/8261 combination facilitates the implementation of the look-ahead technique in adder systems, thus considerably improving propagation times. The circuit structure of this array is of the familar TTL type.

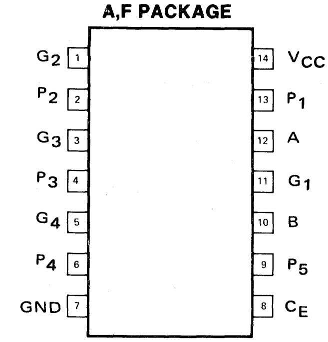
LOGIC DIAGRAM



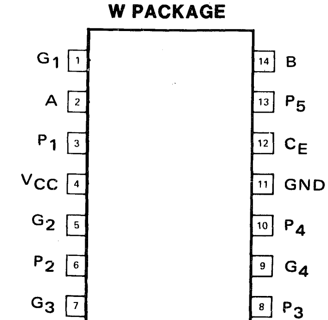
V_{CC} = (14)
GND = (7)
( ) = Denotes Pin Numbers

PIN CONFIGURATION

A,F PACKAGE



W PACKAGE



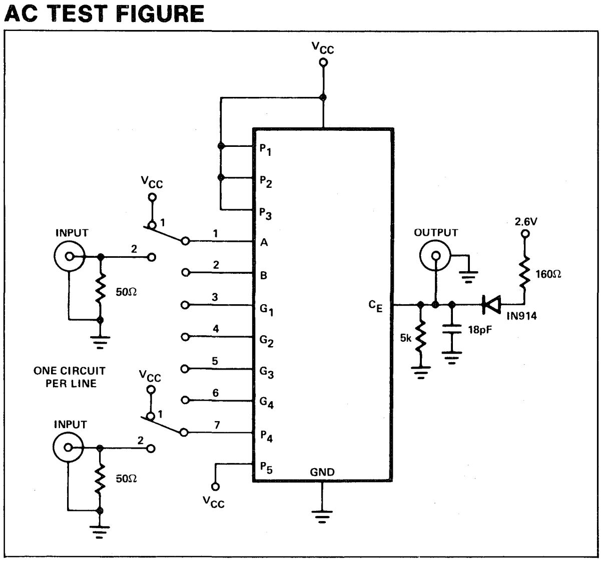
SWITCHING CHARACTERISTICS $T_A = 25°C$, $V_{CC} = 5V$

PARAMETER		LIMITS		UNIT
		TYP	MAX	
t_{on}	Turn-on delay			
	G to C_E	16	25	ns
	P to C_E	13	25	
t_{off}	Turn-off delay			
	G to C_E	16	23	ns
	P to C_E	9	15	

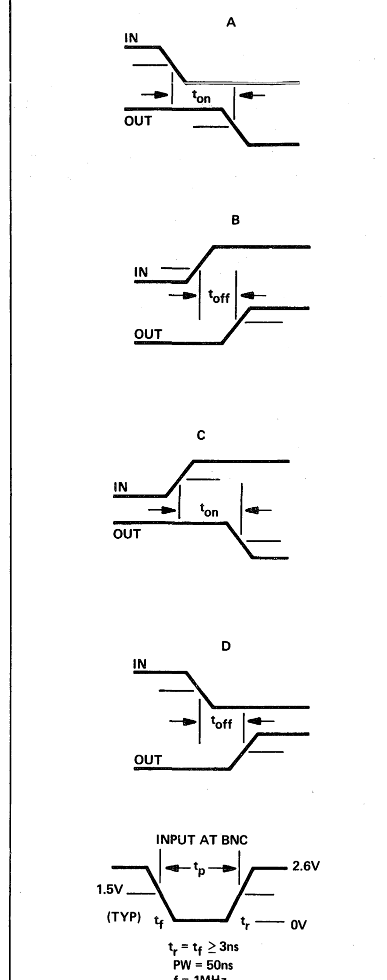
AC TEST TABLE

PIN DESIGNATION	INPUT							WAVEFORM
	A	B	G_1	G_2	G_3	G_4	P_4	
1	PULSE	1	1	1	1	1	1	A,B
2	1	PULSE	1	1	1	1	1	
3	1	1	PULSE	1	1	1	1	
4	1	1	1	PULSE	1	1	1	
5	1	1	1	1	PULSE	1	1	
6	1	1	1	1	1	PULSE	1	
7	2	2	2	2	2	2	PULSE	C,D

AC TEST FIGURE



VOLTAGE WAVEFORMS

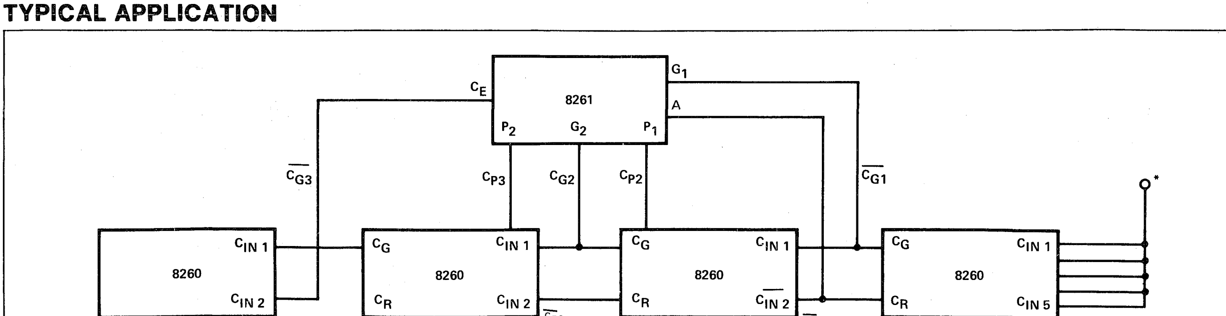


NOTES:

A. Position 1 on all switches provides a logical "1". Position 2 on all switches provides a logical "0" when input signal is not present.

B. All measurements are made at 1.5 volts level.

TYPICAL APPLICATION



16 BIT, T_A = 42ns, typical Fast Adder System (5 packages)

*Tied to V_{CC} if not-true inputs are used, otherwise to ground. Unused 8261 pins should be tied to V_{CC}.

SPEED/PACKAGE AVAILABILITY

8262—A,F,W
82S62—A,F

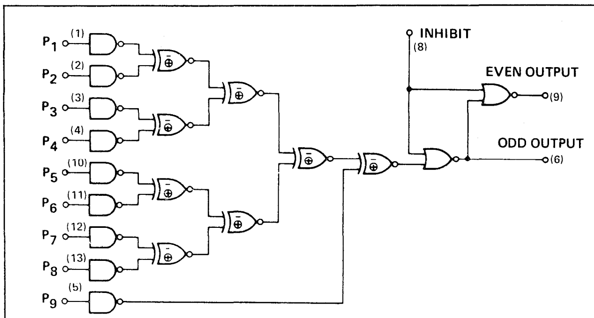
DESCRIPTION

The 8262 9-Input Parity Generator/Parity Checker is a versatile MSI device commonly used to detect errors in data transmission or in data retrieval. Two outputs (EVEN and ODD) are provided for versatility. An INHIBIT input is provided to disable both outputs of the 8262. (A logic 1 on the INHIBIT input forces both outputs to a logic 0).

When used as a Parity Generator, the 8262 supplies a parity bit which is transmitted together with the data word.

At the receiving end, the 8262 acts as a Parity Checker and indicates that data has been received correctly or that an error has been detected.

LOGIC DIAGRAM



V_{CC} = (14)
GND = (7)
( ) = Denotes Pin Numbers

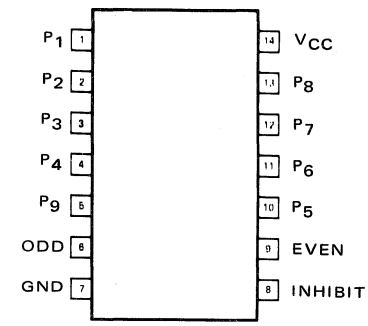
LOGIC EQUATIONS:

Odd =
$P_1 \oplus P_2 \oplus P_3 \oplus P_4 \oplus P_5 \oplus P_6 \oplus P_7 \oplus P_8 \oplus P_9$

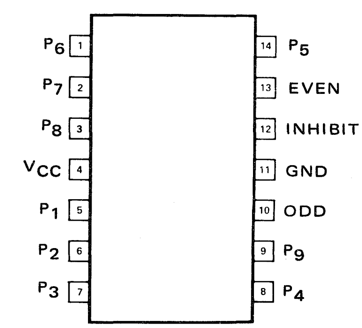
Even =
$\overline{P_1 \oplus P_2 \oplus P_3 \oplus P_4 \oplus P_5 \oplus P_6 \oplus P_7 \oplus P_8 \oplus P_9}$

PIN CONFIGURATION

A,F PACKAGE



W PACKAGE



TRUTH TABLE 8262

MEASURE DELAY FROM	SWITCH POSITION			WAVEFORM	
	INH	P_8	P_9	EVEN	ODD
P_8 to ODD	1	2	1		1
P_9 to ODD	1	1	2		2
P_8 to EVEN	1	2	1	2	
P_9 to EVEN	1	1	2	1	
INH to EVEN	2	1	1	2	

SWITCHING CHARACTERISTICS $T_A = 25°C$, $V_{CC} = 5V$

	PARAMETER	TEST CONDITIONS	8262 TYP	8262 MAX	82S62 TYP	82S62 MAX	UNIT
t_{on}	Turn-on Times						
	P_1-P_8 to even	Under test: pulse	35	50	17	23	ns
	P_1-P_8 to odd	Under test: pulse	30	45	18	28	ns
	P_9 to even	Under test: pulse	20	35	7	12	ns
	P_9 to odd	Under test: pulse	15	30	12	18	ns
	Inhibit to even	Inhibit: pulse	8	15	7	9	ns
	Inhibit to odd	Inhibit: pulse	8	15	6	9	ns
t_{off}	Turn-off times						
	P_1-P_8 to even	Under test: pulse	38	55	17	23	ns
	P_1-P_8 to odd	Under test: pulse	32	45	18	28	ns
	P_9 to even	Under test: pulse	23	40	7	12	ns
	P_9 to odd	Under test: pulse	20	35	12	18	ns
	Ihhibit to even	Inhibit: pulse	10	18	7	9	ns
	Inhibit to odd	Inhibit: pulse	10	18	6	9	ns

AC TEST TABLE—82S62

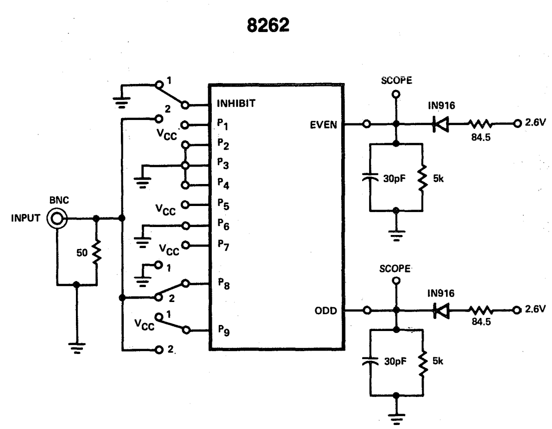
Test No.	Inputs P1	P2	P3	P4	P5	P6	P7	P8	P9	INH	Outputs Even	Odd
1	PG	0	0	0	0	0	0	0	0	0	T	T
2	0	0	PG	0	0	0	0	0	0	0	T	T
3	0	0	0	0	PG	0	0	0	0	0	T	T
4	0	0	0	0	0	0	PG	0	0	0	T	T
5	0	0	0	0	0	0	0	0	PG	0	T	T
6	0	0	0	0	0	0	0	0	0	PG	T	
7	0	0	0	0	0	0	0	0	1	PG		T

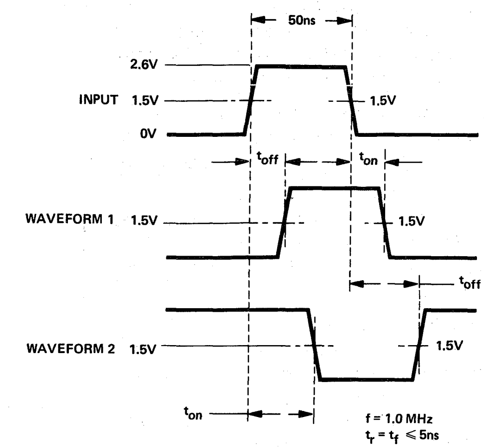
"1" = 2.7V "0" = Ground "T" = Test

NOTE:
1. AC Test Jig Must Not Have Any Switches.
2. AC Test Jigs Must Have Less Than ⅛ Inch Lead Length From Package Pins.

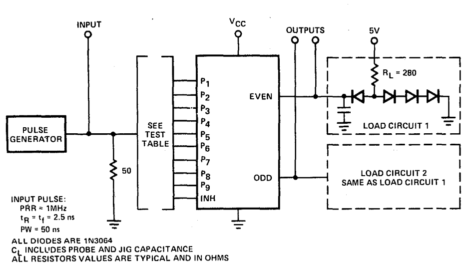
AC TEST FIGURE AND WAVEFORMS

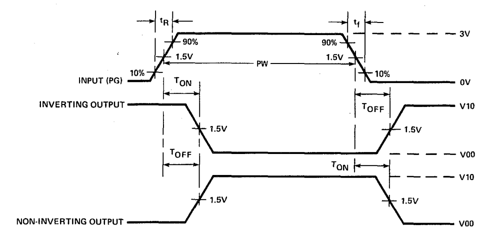
8262



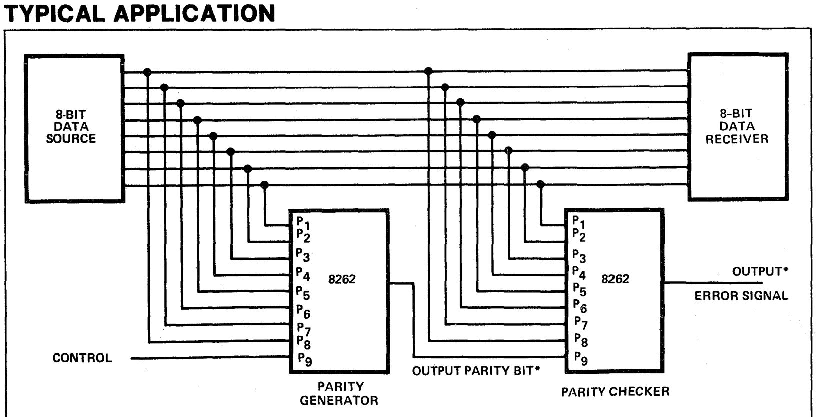


82S62





TYPICAL APPLICATION



*Output can be conditioned for odd or even parity.

An "even parity bit" checking code has a parity bit such that the sum of the 1's in the data word plus the parity bit is always an even number.

An "odd parity bit" checking code has a parity bit such that the sum of the 1's in the data word plus the parity bit is always an odd number.

8263-N,F,Q • 8264-N,F,Q

DESCRIPTION

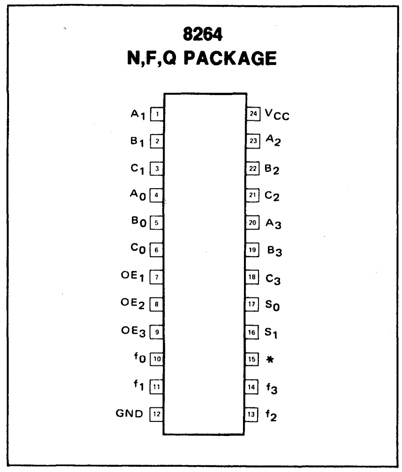
The 8263/8264 3-Input, 4-Bit Multiplexer is a gating array whose function is analogous to that of a 4-pole, 3-position switch. Four bits of digital data are selected from one of three inputs. A 2-bit channel-selection code determines which input is to be active.

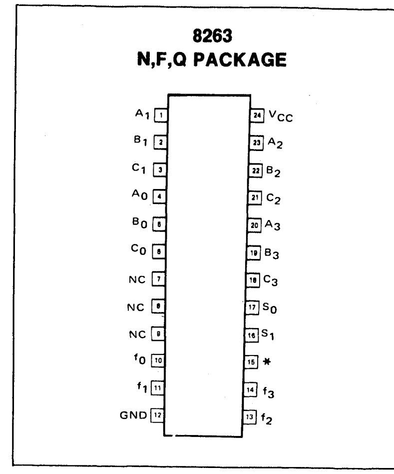
The Data Complement input controls the conditional complement circuit at the Multiplexer output to effect either inverting or non-inverting data flow.

The 8263 employs active output structures to effect minimum delays: the 8264 utilizes bare collector outputs for expansion of input terms.

The 8264 may be expanded by connecting its outputs to the outputs of another 8264. Provision is made for use of a 3-bit code to determine which Multiplexer is selected; thus, eight Multiplexers may be commoned to effect a 4-pole, 24-position switch.

PIN CONFIGURATION





*DATA COMPLEMENT

TRUTH TABLE

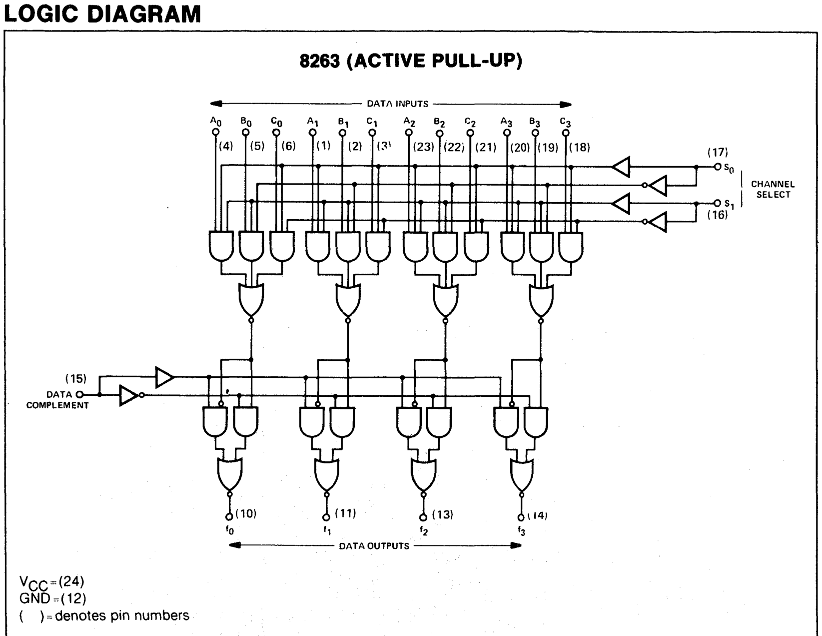
DATA INPUT A_n	B_n	C_n	CHANNEL SELECT S_0	S_1	DATA COMPLEMENT	OUTPUT ENABLE (8264)	DATA OUTPUTS
A_n	x	x	1	1	0	1	A_n
x	B_n	x	0	1	0	1	B_n
x	x	C_n	1	0	0	1	C_n
x	x	x	0	0	0	1	0
A_n	x	x	1	1	1	1	$\overline{A_n}$
x	B_n	x	0	1	1	1	$\overline{B_n}$
x	x	C_n	1	0	1	1	$\overline{C_n}$
x	x	x	0	0	1	1	1
x	x	x	x	x	x	0	1

X either state

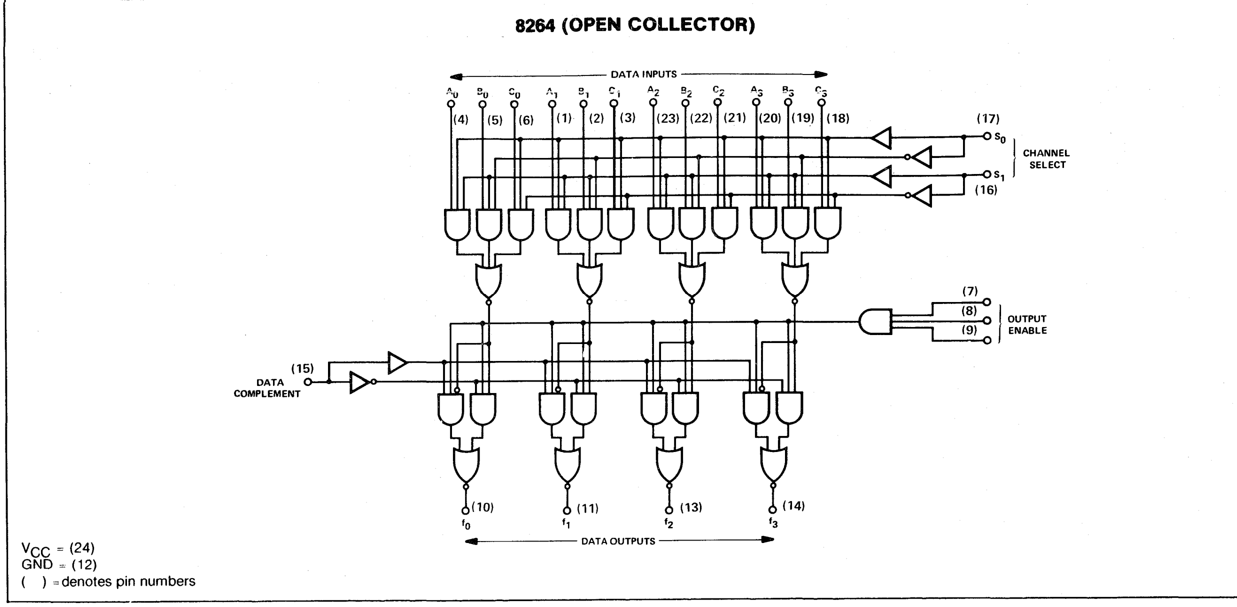
SWITCHING CHARACTERISTICS $T_A = 25°C$, $V_{CC} = 5V$

PARAMETER	LIMITS 8263 TYP	8263 MAX	8264 TYP	8264 MAX	UNIT
Propagation Delay					
A_n to f_n	17	26	25	36	ns
S_0, S_1 to f_n	25	36	25	36	
DC to f_n	17	26	20	30	
OE to f_n			20	30	

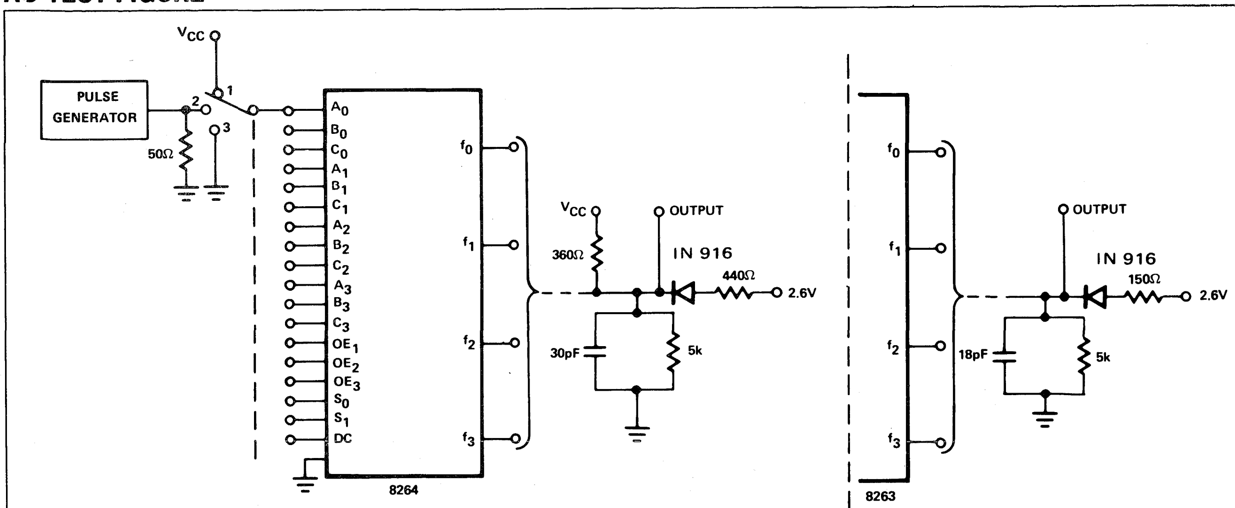
LOGIC DIAGRAM



LOGIC DIAGRAM



AC TEST FIGURE



NOTES
1. Scope terminals to be < 1½" from package pins.
2. Position 1 on switch provides a logical "1".
   Position 2 on switch provides pulse.
   Position 3 on switch provides a logical "0".
3. All measurements are made at 1.5V level.
4. See truth table for logical conditions.

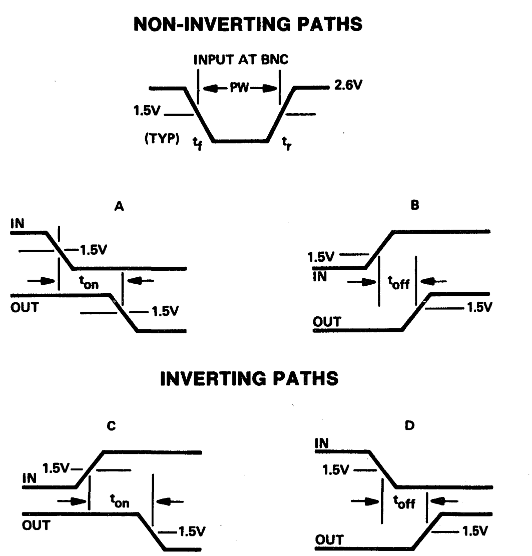
LOGIC

AC TESTING

STEP NO.	DELAY FROM-TO	DRIVEN INPUTS	A_0	B_0	C_0	A_1	B_1	C_1	A_2	B_2	C_2	A_3	B_3	C_3	OE	OE	OE	S_0	S_1	DC	WAVEFORM TYPES
		SWITCHING POSITIONS — OTHER INPUTS																			
1	A_n to f_n	2	2	1	1	2	1	1	2	1	1	2	1	1	1	1	1	1	1	1	C, D
2	S_0 to f_n	2	3	1	1	3	1	1	3	1	1	3	1	1	1	1	1	2	1	1	A, B
3	S_0 to f_n	2	1	3	1	1	3	1	1	3	1	1	3	1	1	1	1	2	1	1	C, D
4	S_1 to f_n	2	1	1	3	1	1	3	1	1	3	1	1	3	1	1	1	1	2	1	C, D
5	DC to f_n	2	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	2	C, D
6	OE_n to f_n	2	1	1	1	1	1	1	1	1	1	1	1	1	*	*	*	1	1	1	C, D

NOTE:
Step number 6 is for 8264 only.
*Test one input at a time — others remain at "1".

WAVEFORMS



$t_r = t_f \leq 3ns$
Amplitude = 2.6V
PW = 200ns
PRR = 1MHz

EXPANDING THE 8264

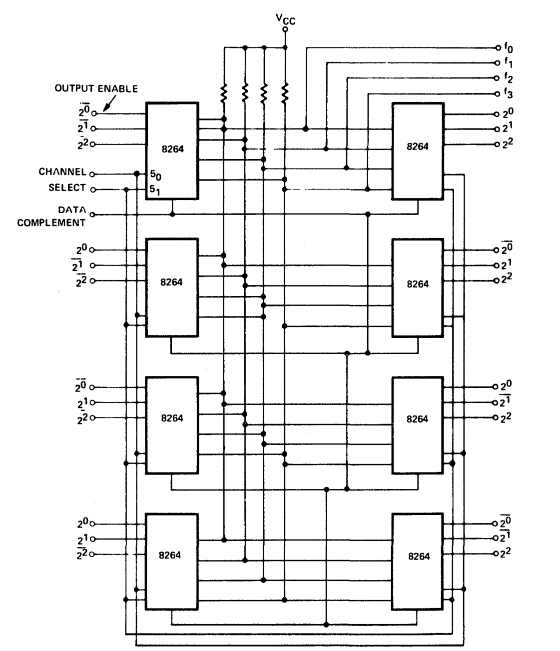


Figure 1

TYPICAL APPLICATIONS

An approach to expanding the 8264 (bare collector output) is shown in Figure 1. The idea is to use common collectors with external pull-up resistors (one resistor for each of the four outputs) and make use of the output enable code.

As can be seen, the channel select lines are tied common, while a different enable code would be used to selecty a particular 8264. All non-selected 8264's have their outputs in the logic "1" condition, thus allowing the selected multiplexer to predominate.

Figure 2 illustrates a typical example using the 8263 (totem pole output) along with the 8281 (4-bit binary counter) and the 8270/71 (4-bit shift register), to implement a variable modulus counter. The 8270's act as a 3-register memory. The outputs of the 8270's are fed to the corresponding inputs of the 8263. Now there are three different presettable 4-bit words that can be chosen by the 8264. By alternating the channel select codes, the 8281 counter is preset with one of three words and produces an output whose repetition rate is dependent on the inputs from the multiplexer.

VARIABLE MODULUS COUNTER

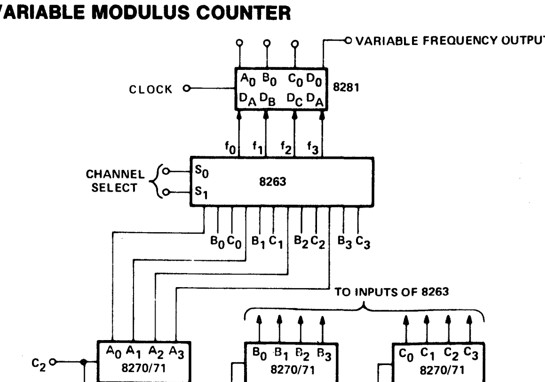


FIGURE 2

8266-B,F,W • 8267-B,F,W

DESCRIPTION

The 8266/8267 2-Input, 4-Bit Digital Multiplexer is a monolithic array utilizing familiar TTL circuit structures. The 8267 features a bare-collector output to allow expansion with other devices.

The multiplexer is intended for use at the inputs to adders, registers and in other parallel data handling applications.

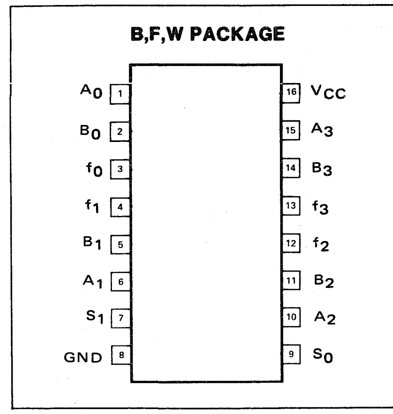
SPEED/PACKING AVAILABILITY

8266,67—B,F,W
82S66,S67—B,F

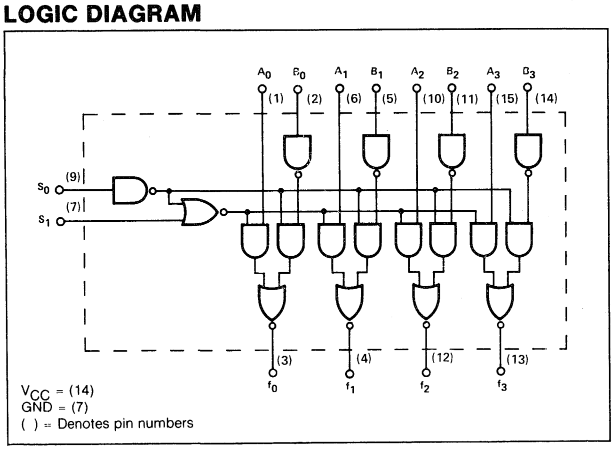
The multiplexer is able to choose from two different input sources, each containing 4 bits: A = (A_0, A_1, A_2, A_3), B = (B_0, B_1, B_2, B_3). The selection is controlled by the input S_0, while the second control input, S_1, is held at zero.

For conditional complementing, the two inputs (A_n, B_n) are tied together to form the function TRUE/COMPLEMENT, which is needed in conjunction with added elements to perform ADDITION/SUBTRACTION. Further, the inhibit state $S_0 = S_1 = 1$ can be used to facilitate transfer operations in an arithmetic section.

PIN CONFIGURATION



LOGIC DIAGRAM



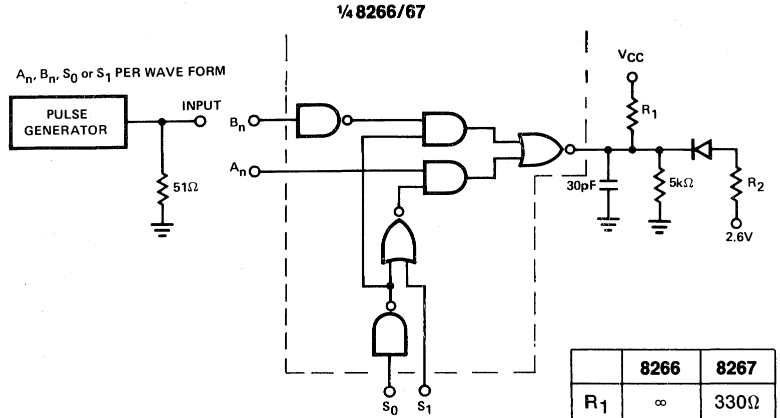
TRUTH TABLE

SELECT LINES		OUTPUTS
S_0	S_1	f_n (0, 1, 2, 3)
0	0	B_n
0	1	B_n
1	0	$\overline{A}_n$
1	1	1

SWITCHING CHARACTERISTICS $T_A = 25°C$, $V_{CC} = 5V$

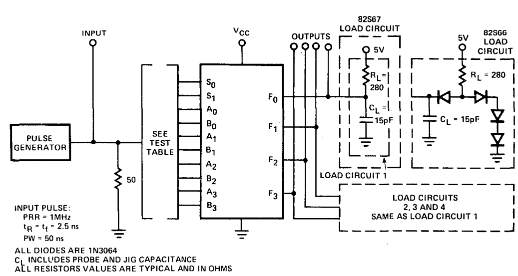
PARAMETER	LIMITS								UNIT
	8266		8267		82S66		82S67		
	TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
Propagation delay									
S_0 to f_n (short path)	18	28	18	28	12	18	15	20	ns
S_0 to f_n (long path)	20	30	27	36	—	—	—	—	
A_n to f_n	13	20	15	20	5	10	8	12	
B_n, S_1 to f_n	14	25	21	28	—	—	—	—	
S1 to fn					10	15	13	18	
Bn to fn					8	12	10	15	

AC TEST FIGURE



	8266	8267
R_1	∞	330Ω
R_2	84.5Ω	470Ω

82S66, 82S67



AC TEST TABLE—82S66,82S67

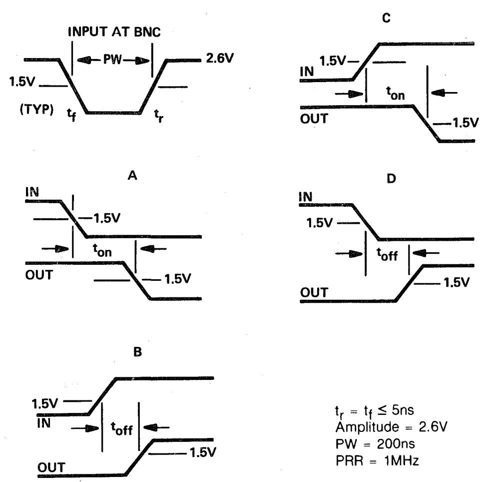
TEST	INPUTS										OUTPUTS			
NO.	S_0	S_1	A_0	B_0	A_1	B_1	A_2	B_2	A_3	B_3	F_0	F_1	F_2	F_3
1	1	PG	1	1	1	1	1	1	1	1	T			
2	1	PG	1	1	1	1	1	1	1	1	T	T	T	T
3	PG	0	1	1	1	1	1	1	1	1	T	T		T
4	0	0	0	0	0	PG	0	0	0	0		T		
5	0	0	0	0	0	0	0	PG	0	0			T	
6	1	0	PG	1	0	1	0	1	0	1	T			
7	1	0	0	1	0	1	0	1	PG	1				T

"1" = 2.7V "0" = Output

NOTES:
1. AC Test Jigs Must Not Have Any Switches.
2. AC Test Jigs Must Have Less Than ⅛ Inch Lead Length From Package Pins.

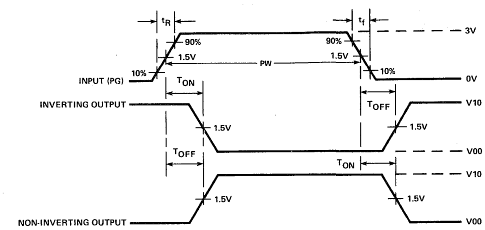
VOLTAGE WAVEFORMS

8266, 8267

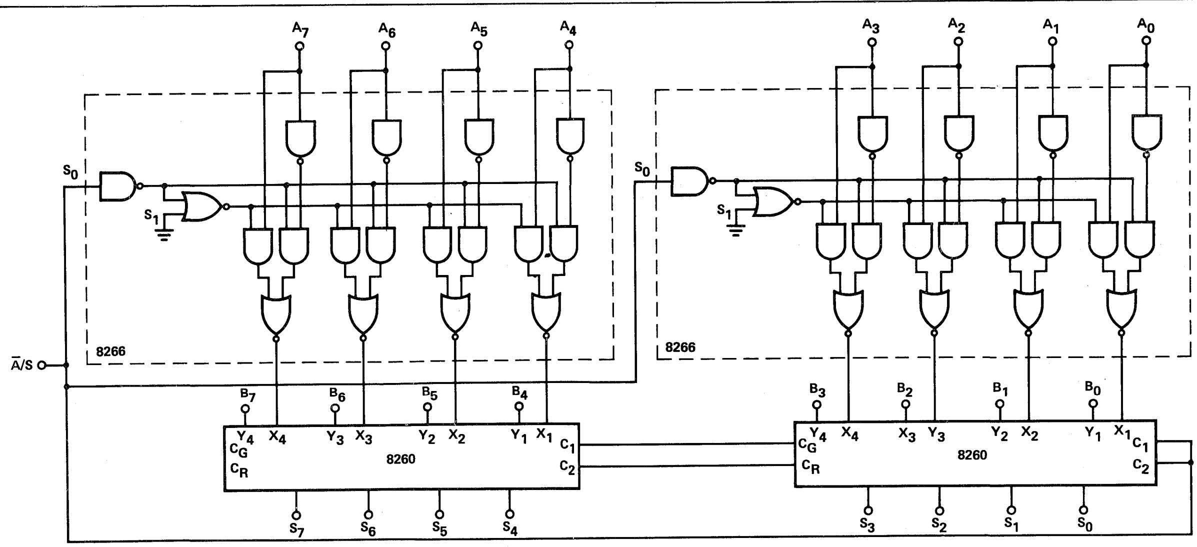


$t_r = t_f \leq 5ns$
Amplitude = 2.6V
PW = 200ns
PRR = 1MHz

82S66, 82S67



TYPICAL APPLICATIONS



The 8266 can be used in conuunction with the 8260 (Look-Ahead Carry Adder) to form an adder-subtractor.

LOGIC

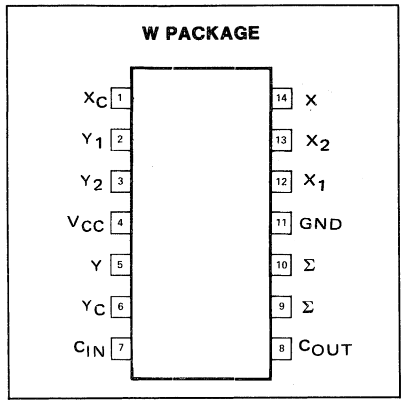
8268-A,F,W

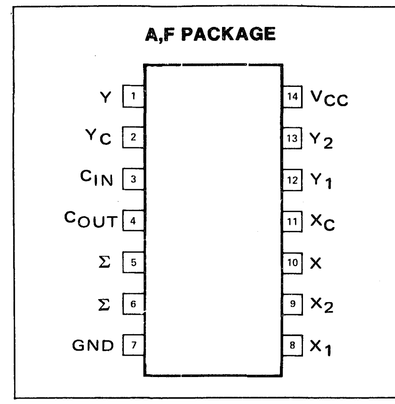
DESCRIPTION

The 8268 is a single-bit full adder with gated true and complementary inputs, complementary sum (Σ and $\overline{\Sigma}$) outputs and an inverted carry output. By taking advantage of the unique true or inverted inputs and true or inverted outputs, parallel addition speed is greatly enhanced (by eliminating unnecessary inversions).

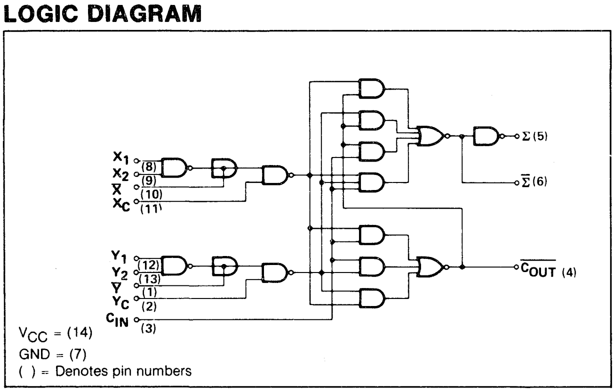
The device is designed for medium speed parallel and serial adder systems.

PIN CONFIGURATION





LOGIC DIAGRAM



TRUTH TABLE

C_{IN}	Y	X	$\overline{C_{OUT}}$	Σ	$\overline{\Sigma}$
0	0	0	1	0	1
0	0	1	1	1	0
0	1	0	1	1	0
0	1	1	0	0	1
1	0	0	1	1	0
1	0	1	0	0	1
1	1	0	0	0	1
1	1	1	0	1	0

NOTES:

1. $X = \overline{X} \cdot X_C$; $Y = \overline{Y} \cdot Y_C$ where $\overline{X} = \overline{X_1 \cdot X_2}$; $\overline{Y} = \overline{Y_1 \cdot Y_2}$
2. When $\overline{X}$ or $\overline{Y}$ are used as inputs, X_1 and X_2 or Y_1 or Y_2 respectively must be tied to GND.
3. When X_1 and X_2 or Y_1 and Y_2 are used as inputs, $\overline{X}$ or $\overline{Y}$ respectively must be left open or used to perform the WIRED-AND function.

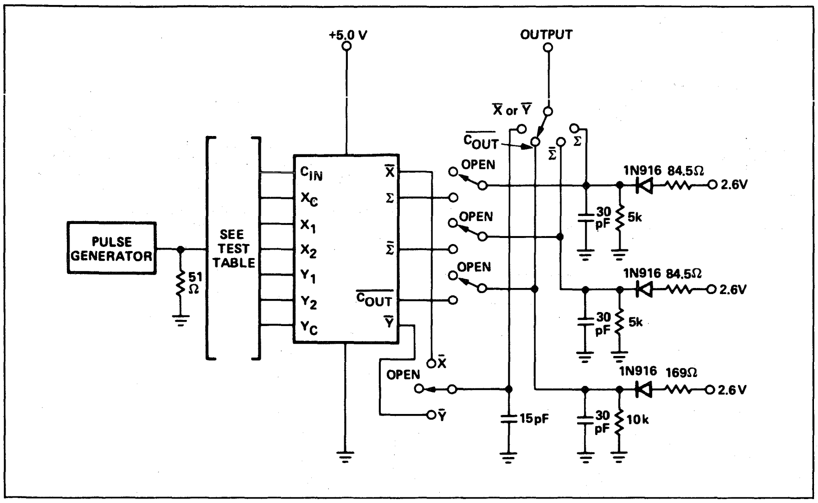
SWITCHING CHARACTERISTICS $T_A = 25°C$, $V_{CC} = 5V$

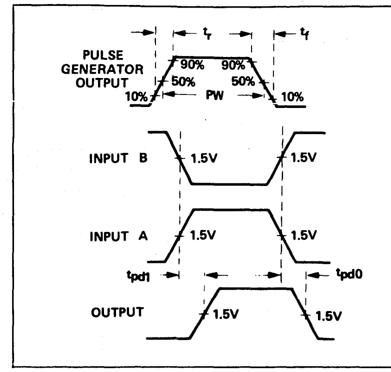
PARAMETER	FROM INPUT	TO OUTPUT	TEST CONDITIONS	LIMITS TYP	LIMITS MAX	UNIT
Propagation delay time						
t_{PLH} Low-to-high	C_{IN}	$\overline{C}_{OUT}$		8	13	ns
t_{PHL} High-to-low				8	13	
t_{PLH} Low-to-high	Y_c	$\overline{C}_{OUT}$		20	25	
t_{PHL} High-to-low				20	25	
t_{PLH} Low-to-high	X_c	Σ		35	45	
t_{PHL} High-to-low				35	45	
t_{PLH} Low-to-high	Y_c	$\overline{\Sigma}$		25	35	
t_{PHL} High-to-low				25	35	
t_{PLH} Low-to-high[1]	X_1, X_2	$\overline{X}$		30	40	
t_{PHL} High-to-low[1]				15	20	
t_{PLH} Low-to-high[1]	Y_1, y_2	$\overline{Y}$		30	40	
t_{PHL} High-to-low[1]				15	20	

NOTES:

1. This test is a measure of the required worst-case data set-up time.

AC TEST FIGURE AND WAVEFORMS





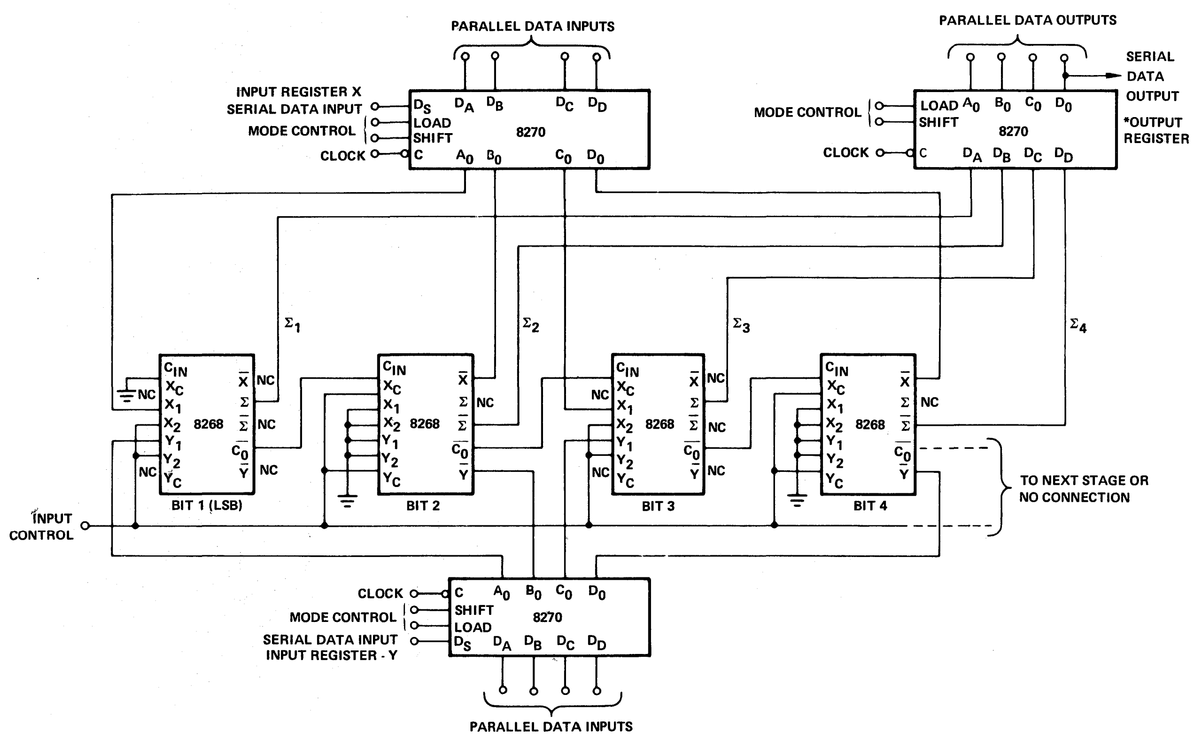
NOTES:
1. Perform test in accordance with test table.
2. Each output is tested separately.
3. Voltage values are with respect to network GND terminal.
4. The generator has the following characteristics: V_{gen} = 2.6V, tr = t^f ≤ 15ns, PW = 0.5ns, PRR = 1MHz.
5. Inputs and outputs not otherwise specified are open.
6. Capacitance shown include probe and jig capacitance.
7. All resistances are in ohms.

TEST TABLE (See Note 5)

TEST NO.	OUTPUTS UNDER TEST	APPLY INPUT A TO	APPLY INPUT B TO	APPLY +2.6V TO	APPLY GND TO	APPLY OUTPUT LOADING TO
1	$\overline{C}_{out}$	None	C_{in}	None	Y_1	$\overline{C}_{out}$
2	$\overline{C}_{out}$	None	C_{in}	None	Y_1	$\overline{C}_{out}$
3	$\overline{C}_{out}$	Y_C	None	C_{in}	X_1, Y_1	$\overline{C}_{out}$
4	$\overline{C}_{out}$	Y_C	None	C_{in}	X_1, Y_1	$\overline{C}_{out}$
5	Σ	X_C	None	C_{in}	X_1, Y_1	Σ $\overline{\Sigma}$ $\overline{C}_{out}$
6	Σ	X_C	None	C_{in}	X_1, Y_1	Σ $\overline{\Sigma}$ $\overline{C}_{out}$
7	$\overline{\Sigma}$	Y_C	None	C_{in}	Y_1	$\overline{\Sigma}$
8	$\overline{\Sigma}$	Y_C	None	C_{in}	Y_1	$\overline{\Sigma}$
9	$\overline{X}$	None	X_1	X_2	None	$\overline{X}$ (CL = 15 pF)
10	$\overline{X}$	None	X_1	X_2	None	$\overline{X}$ (CL = 15 pF)
11	$\overline{Y}$	None	Y_1	Y_2	None	$\overline{Y}$ (CL = 15pF)
12	$\overline{Y}$	None	Y_1	Y_2	None	$\overline{Y}$ (CL = 15 pF)

TYPICAL APPLICATIONS

N-BIT PARALLEL ADDER

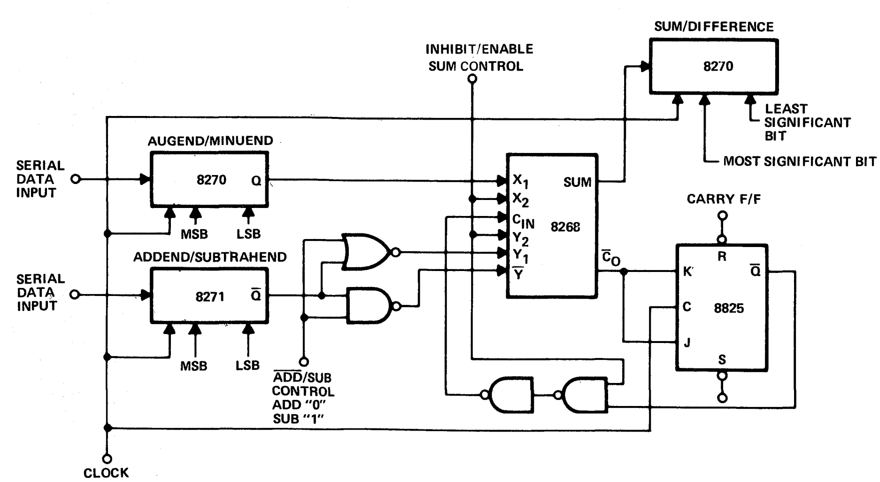


NOTES:

To expand storage register for serial/parallel operation, connect D_0 to D_S of next stage and common the mode control lines and the clock line of the first stage to their respective second stage equivalents.

* To expand output register for parallel outputs common clock, shift and load lines with their respective counterparts. For serial data output, also connect D_0 of first register to D_S of next register.

4-BIT SERIAL ADD/SUBTRACTOR



8269-A,F,W

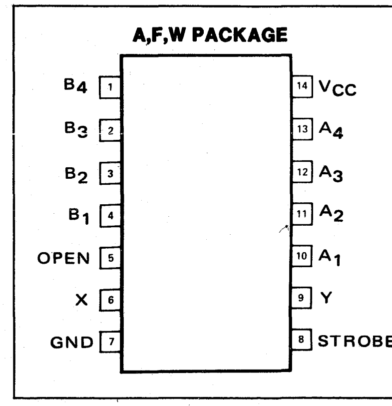
DESCRIPTION

The 8269 4-Bit Comparator is an array of gates designed to perform the numerical comparison of two four-bit binary numbers. The outputs indicate whether the two numbers are equal in value, or which number is the greater. The 8269 is a functional and pin-for-pin replacement for the DM8200.

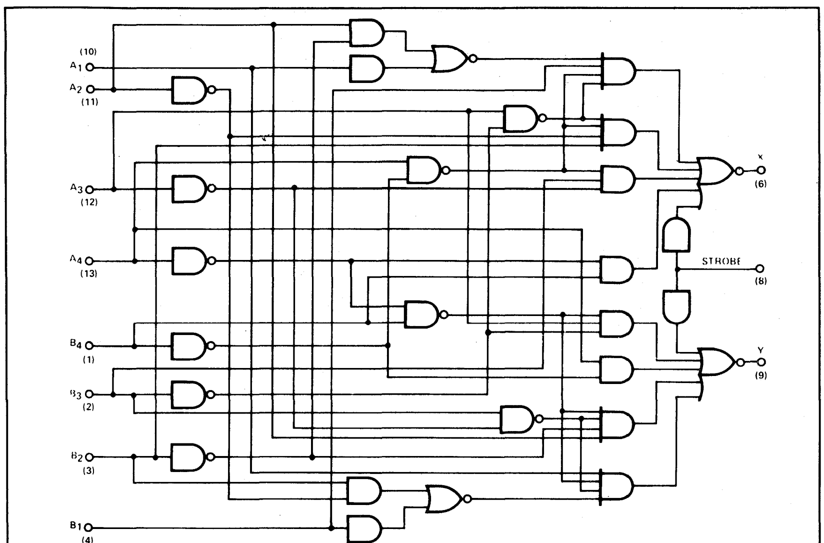
TRUTH TABLE

INPUT				OUTPUT	
A_n		B_n	STROBE	X	Y
A	>	B	0	1	0
A	<	B	0	0	1
A	=	B	0	1	1
A	≷	B	1	0	0

PIN CONFIGURATION



LOGIC DIAGRAM



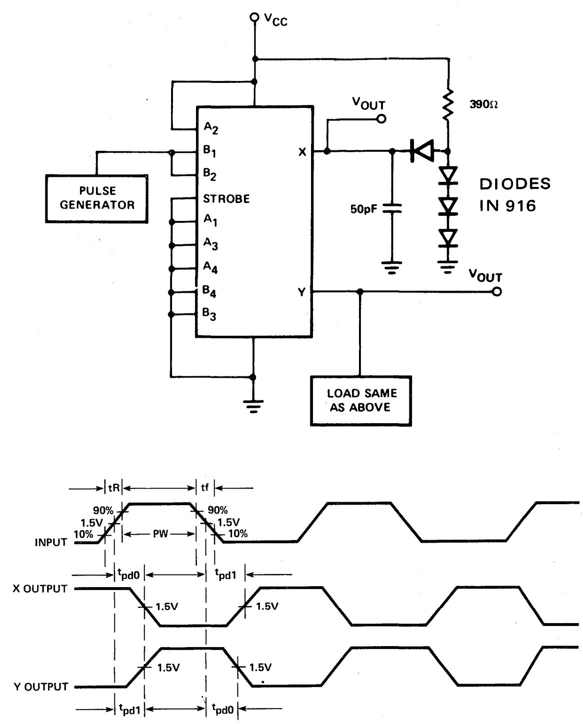
V_{CC} = (14)
GND = (7)
( ) = denotes pin numbers

SWITCHING CHARACTERISTICS $T_A=25°C$, $V_{CC}=5V$

PARAMETER	FROM INPUT	TO OUTPUT	TEST CONDITIONS	LIMITS MAX	UNIT
Propagation Delay Time					
t_{PLH} Low-to-high	Data		Test Figure 1	40	ns
t_{PHL} High-to-low				30	
t_{PLH} Low-to-high	Strobe		Test Figure 2	27	
t_{PHL} High-to-low				18	

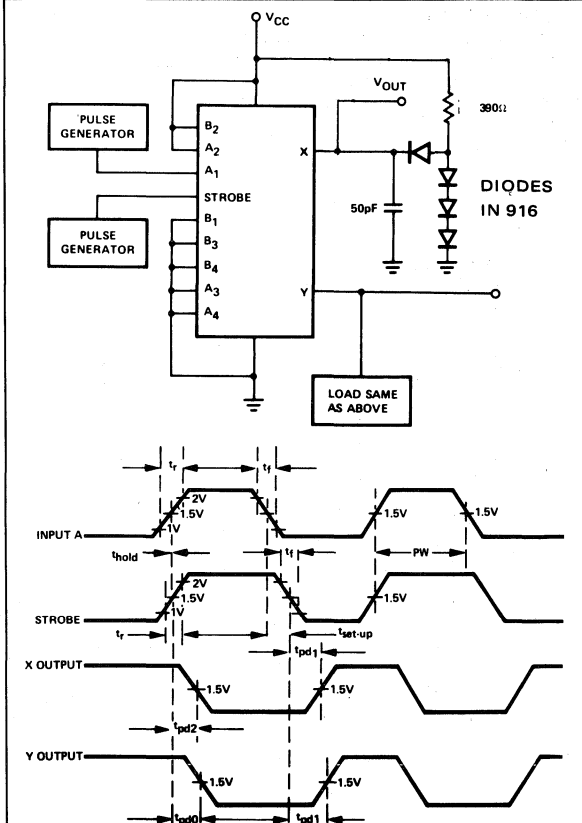
8269-A,F,W

AC TEST FIGURE AND WAVEFORMS



Input Pulse:
f = 1MHz
PW = 100ns
$t_r = t_f = 10ns \pm 1ns$
AMP. = 3.0V

FIGURE 1



Input Pulse:
Input A
f = 1MHz
PW = 100ns
$t_r = t_f = 10ns \pm 1ns$
AMP. = 3.0V

Strobe Input
f = 1MHz
t_{hold} = 0ns
$t_{set\text{-}up}$ = 10ns
$t_r = t_f = 10ns \pm 1ns$

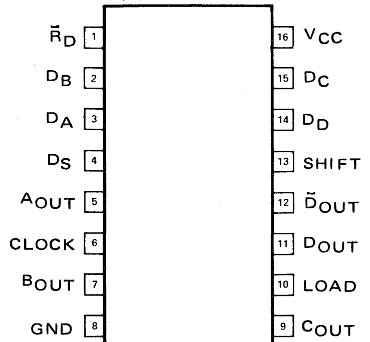
FIGURE 2

4-BIT SHIFT REGISTER 8270/71

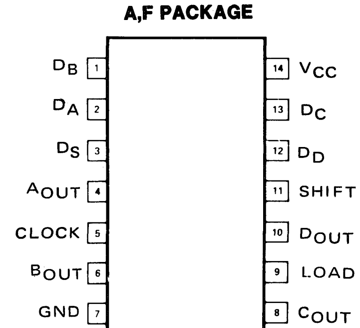
8270-A,F,W • 8271-B,F,W

PIN CONFIGURATION

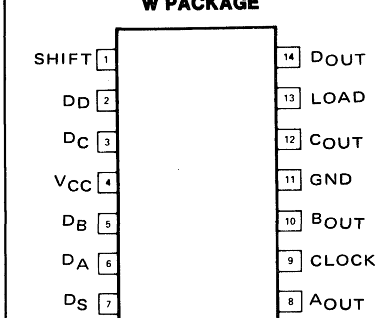
8271
B,F,W PACKAGE



8270
A,F PACKAGE



8270
W PACKAGE



SPEED/PACKAGE AVAILABILITY

8270—B,F,W/8271—A,F,W
82S70—B,F/82S71—A,F

DESCRIPTION

The 8270 is a 4-bit Shift Register with both serial and parallel data entry capability.

The data input lines are single-ended true input data lines which condition their specific register bit location after an enabled clocking transition. Since data transfer is synchronous with clock, data may be transferred in any serial/parallel input/output relationship.

The internal design uses level sensitive binaries which respond to the negative-going clock transition. A buffer clock driver has been included to minimize input clock loading.

Mode control logic is available to determine three possible control states. These register states are serial shift right mode, parallel enter mode, and no change or hold mode. These states accomplish logical decoding for system control.. The truth table for the control mades is shown below.

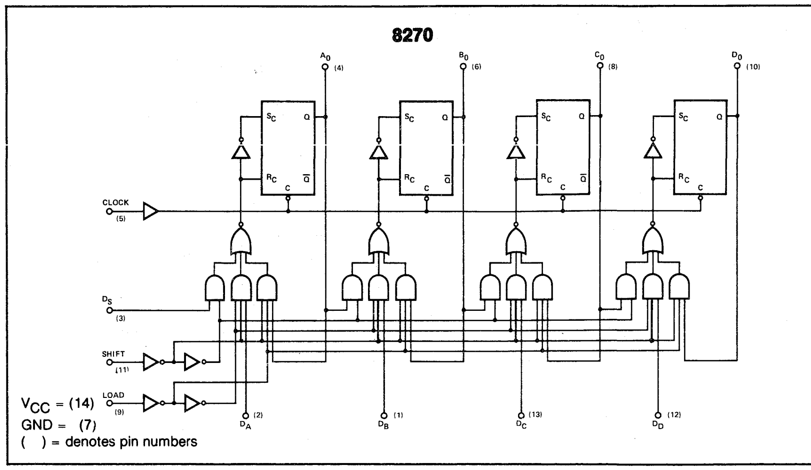
For applications not requiring the hold mode, the load input may be tied high and the shift input used as the mode control.

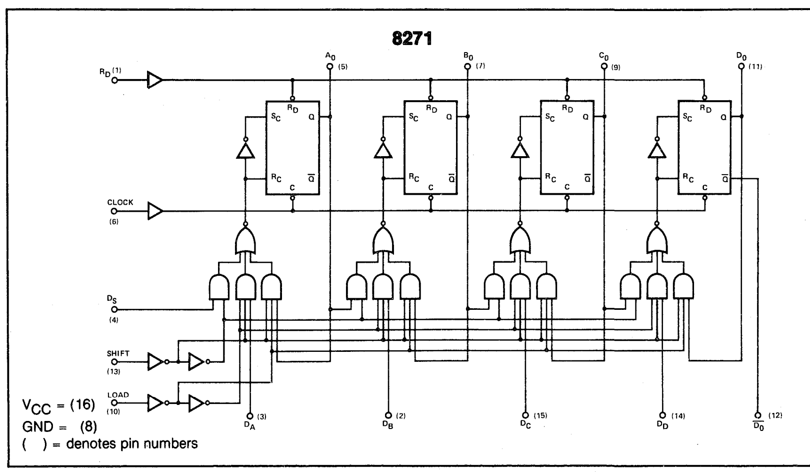
The 8271 provides a direct reset (R_D), and a $\overline{D_{out}}$ line in addition to the available outputs of the 8270 element. The fan-out specification for this output is the same as the true outputs of the 8270 element.

TRUTH TABLE

CONTROL STATE	LOAD	SHIFT
Hold	0	0
Parallel Entry	1	0
Shift Right	0	1
Shift Right	1	1

LOGIC DIAGRAM





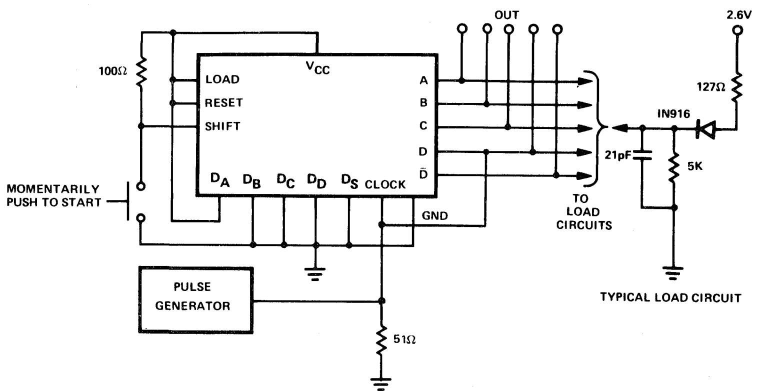
SWITCHING CHARACTERISTICS $T_A=25°C$, $V_{CC}=5V$

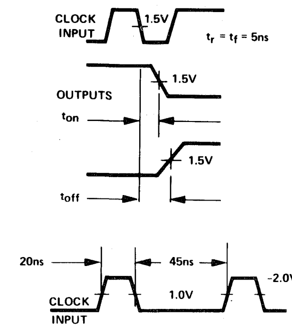
PARAMETER	TEST CONDITIONS	8270/71			82S70/S71			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
t_{on} Turn-on delay time						11	20	
All binaries			25	40		11	16	ns
t_{off} Turn-off delay time All binaries			25	40	11	11	20	ns
Clock Interval (High)	Clock=2V	20			8	11	16	ns
Transfer Rate		15	22		40	60		MHz
t_{setup} Set-up time Load			20	30		3	6	ns
Data			7	15		1	3	

AC TEST FIGURES AND WAVEFORMS

8270, 8271

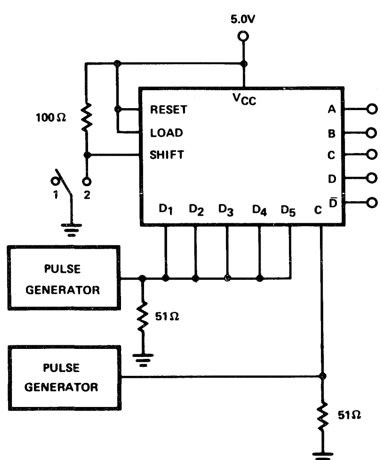
TURN ON/OFF AND TRANSFER RATE

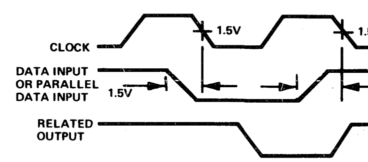




Notes:
1. t_{on}/t_{off}
2. Transfer rate & min clock "1" level: check that binary outputs are changing.

DATA SET-UP TIME





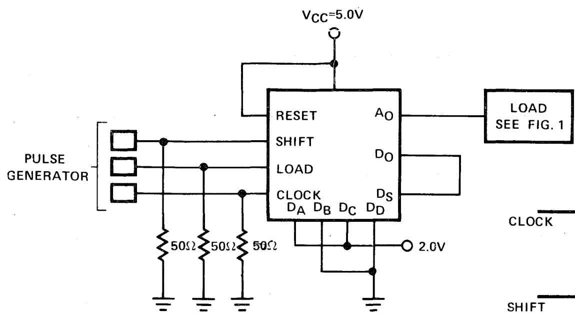
Notes
1. Switch in position 1 to test serial data input.
2. Switch in position 2 to test parallel data input.

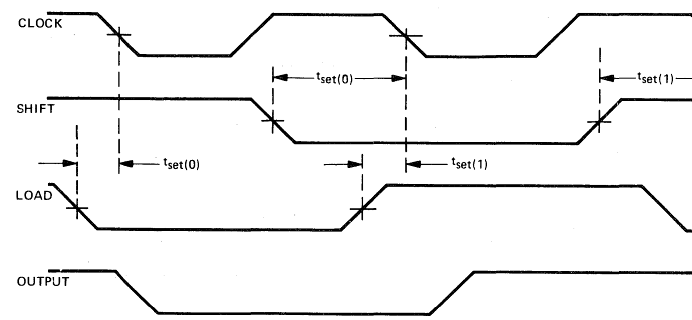
Adjust data input or parallel input delays to test condition and verify output operation.

AC TEST FIGURE AND WAVEFORMS (CONT'D.)

8270, 8271

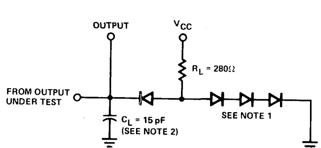
SHIFT/LOAD SET-UP TIME





NOTES:
1. All resistor values are in ohms.
2. All capacitance values are in picofarads and include jig and probe capacitance. Capacitance as measured on Boonton Electronic Corporation Model 75A-S8 Capacitance Bridge or equivalent. f = 1 MHz, V_{AC} = mV rms.
3. All diodes are 1N916.

82S70, 82S71

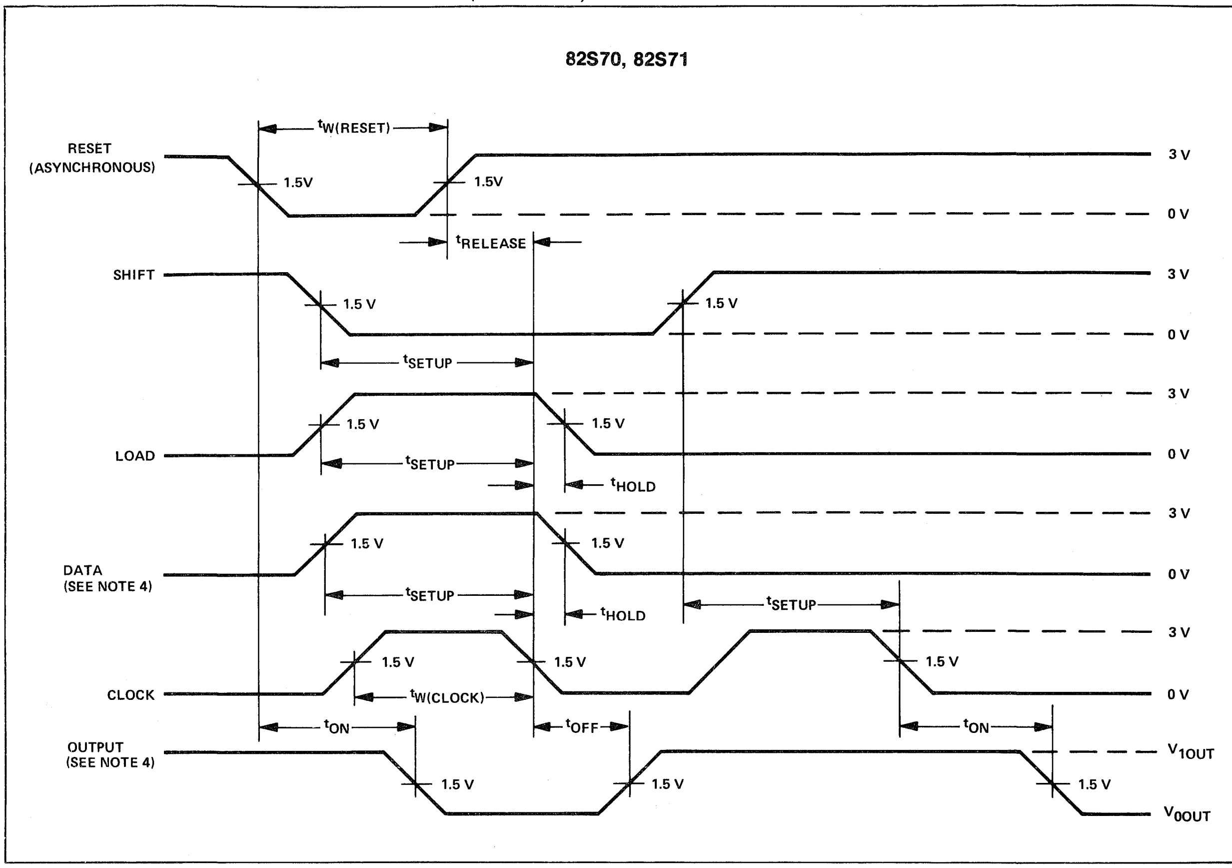


NOTES
1. All diodes are 1N3064.
2. C_L includes Jig and Probe Capacitance
3. Input pulses are supplied by pulse generators having Z_{OUT} = 50Ω and the following characteristics:
   CLOCK INPUT PULSE
   $t_r = t_f$ = 2.5ns (10% to 90%)
   Pulse amplitude = 3V
   PRR (t_{on}, t_{off}) = 1 MHz
   t_W (t_{on}, t_{off}) = 50 ns
   PRRR (Max. Freq.) = 40MHz
4. Data input and output are any related pair. Serial and other data inputs are at ground. The serial input is tested with the A output when in the shift mode.

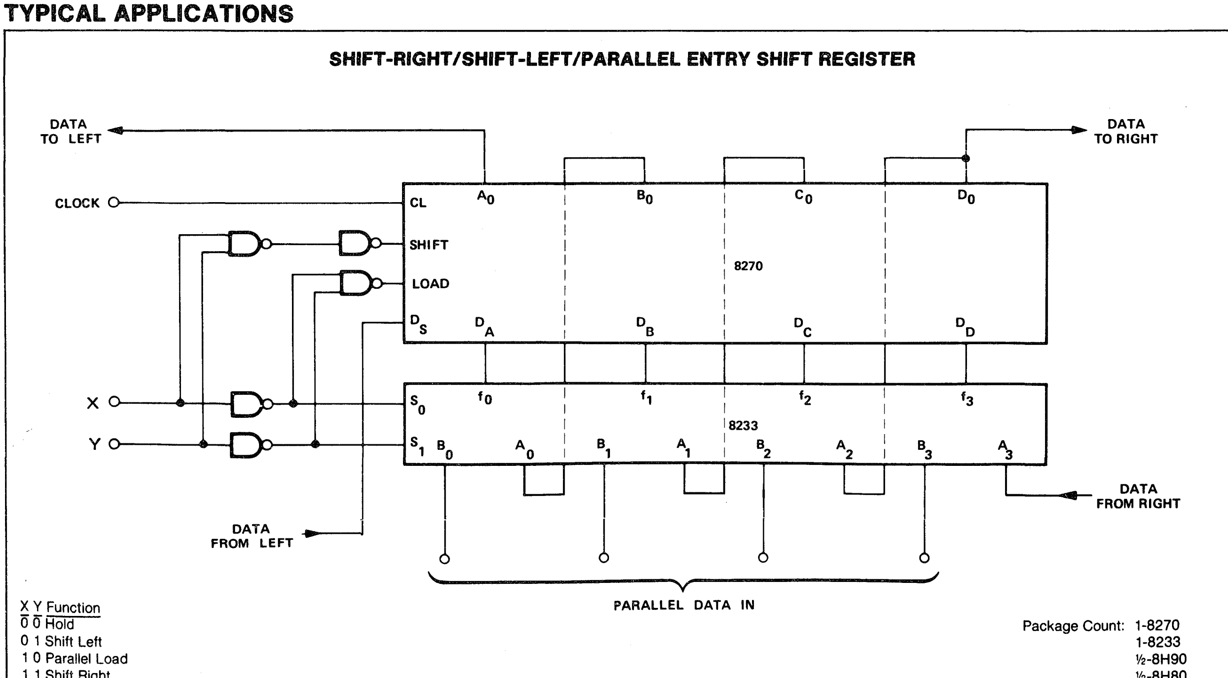
SHIFT/LOAD AND DATA INPUT PULSE
$t_r = t_f$ = 2.5 ns (10% to 90%)
Pulse amplitude = 3V
PRR = ½ of Clock Freq.
t_W = 50% Duty Cycle

LOGIC

AC TEST FIGURE AND WAVEFORMS (CONT'D.)



TYPICAL APPLICATIONS



8273-B,F,W

DESCRIPTION

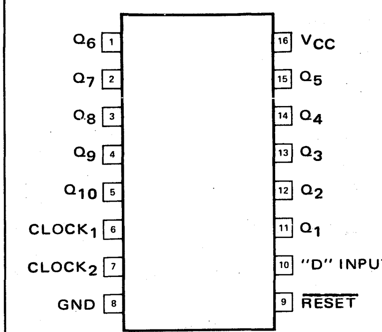
The 8273, 10-Bit Shift Register is an array of binary elements interconnected to perform the serial-in, parallel-out shift function. This device utilizes a common buffered reset and operates from either a positive or negative edge clock pulse. Clock 1 is triggered by a negative going clock pulse and Clock 2 is triggered by a positive going clock pulse. The unused clock input performs the inhibit function. The circuit configuration is arranged as a single serial input register with ten true parallel outputs.

TRUTH TABLE

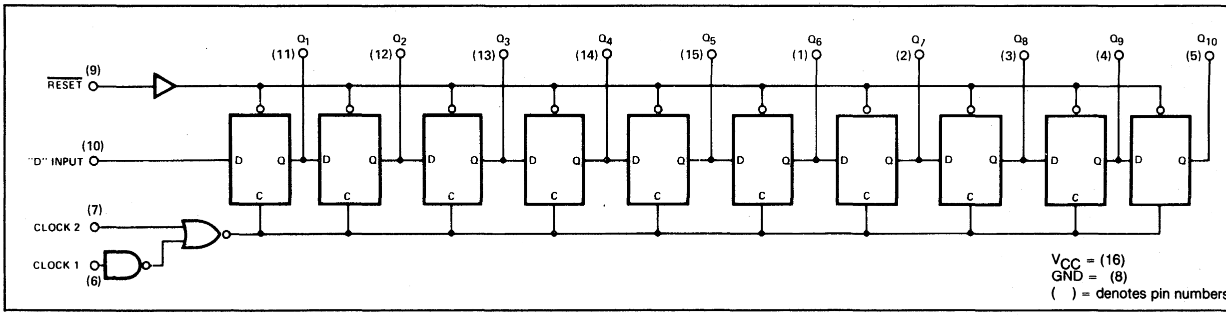
INPUT	$\overline{RESET}$	CLOCK 1	CLOCK 2	$Q_n + 1$
1	1	Pulse	0	1
0	1	Pulse	0	0
1	1	1	Pulse	1
0	1	1	Pulse	0
1	1	Pulse	1	Q
0	1	Pulse	1	Q
1	1	0	Pulse	Q
0	1	0	Pulse	Q

NOTE:
The unused clock input performs the INHIBIT function.
$\overline{RESET} = 0 \rightarrow Q = 0$

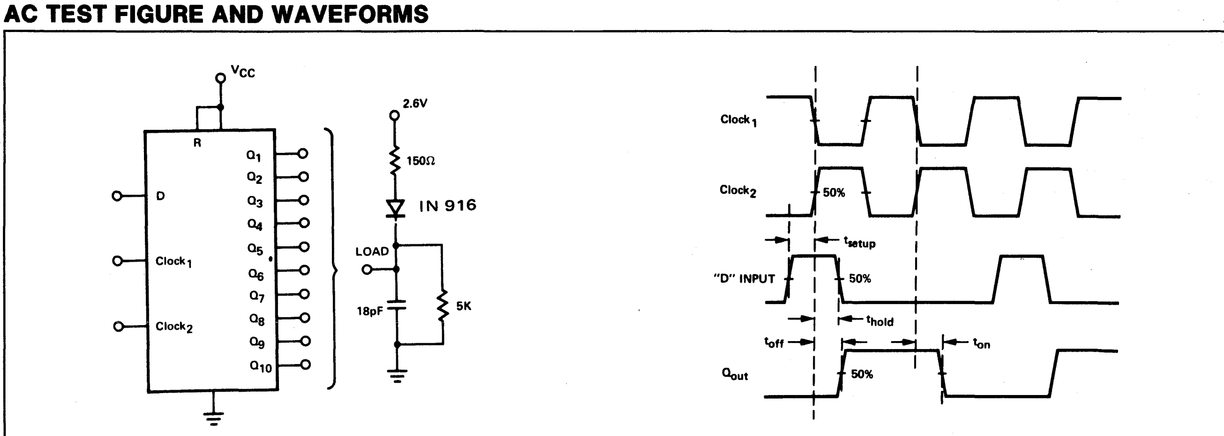
PIN CONFIGURATION



LOGIC DIAGRAM



AC TEST FIGURE AND WAVEFORMS



NOTES:
1. Unused clock 2 input must be grounded.
2. Input pulse characteristics
   CLOCK
   Amplitude = 3.0V
   $t_r = t_f \leq 5ns$.

LOGIC

8273-B,F,W

SWITCHING CHARACTERISTICS $T_A=25°C$, $V_{CC}=5V$

PARAMETER		FROM INPUT	TO OUTPUT	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT
Data Transfer Rate					25	35		MHz
t_{on}	Turn-on delay	Clock 1		Clock 2 = OV:				
				Reset=4.5V		32	40	
		Clock 2		Reset=4.5V		28	40	ns
		Reset		Clock 1=4.5V		35	50	
t_{off}	Turn-off delay	Clock 1		Clock 2=OV		25	40	ns
		Clock 2		Clock 1=4.5V		19	40	
$t_{w(clock)}$	Width of clock	Clock 1		Clock 2=OV		16	25	ns
	Input pulse	Clock 2		Clock 1=4.5V		12	20	
t_{set-up}	Setup time	Clock 1		Clock 2=OV			15	ns
		Clock 2		Clock 1=4.5V			10	
t_{hold}	Hold time	Clock 1		Clock 2=OV			15	ns
		Clock 2		Clock 1=4.5V			10	

10-BIT PARALLEL-IN SERIAL-OUT SHIFT REGISTER 8274

8274-B,F,W

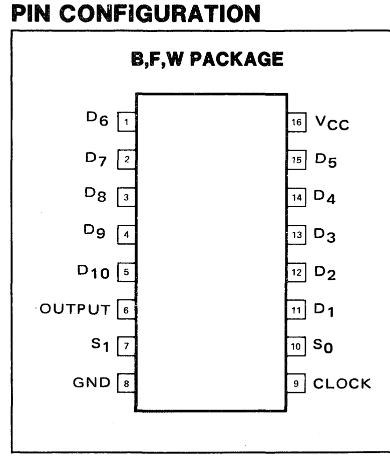
DESCRIPTION

The 8274 10-Bit Shift Register is an array of binary elements interconnected to perform the parallel-in serial-out shift function. The circuit has ten parallel inputs and a single true serial output. The D_1 input can also be used for serial entry. Two control inputs, S_0 and S_1, determine the operating mode of the shift register as shown in the Truth Table. A single buffered clock line connects all ten flip-flops which are activated on the high-to-low transition of the clock pulse. Guaranteed input clock frequency is 25MHz. With the exception of the Hold Mode, the control inputs may be changed when the clock is in either the high or low state without causing false triggering. The Hold Mode can be entered only when the clock is low. Applications for the 8274 Shift Register include Parallel-to-Serial conversion, Modem Data Transmision, Pseudo-Random Code generation and Modulo-N Frequency Division.

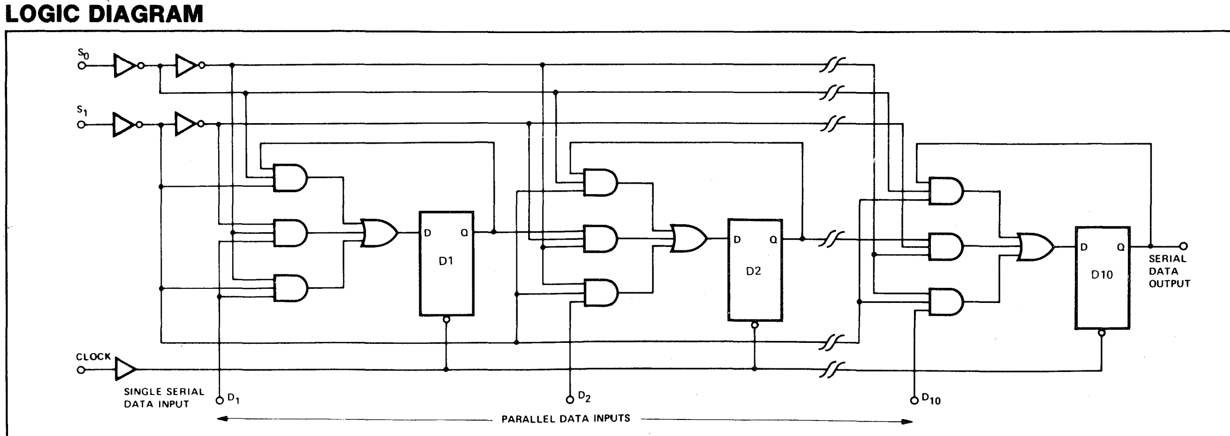
TRUTH TABLE

S_0	S_1	OPERATING MODE
0	0	Hold
0	1	Clear
1	0	Load
1	1	Shift

PIN CONFIGURATION



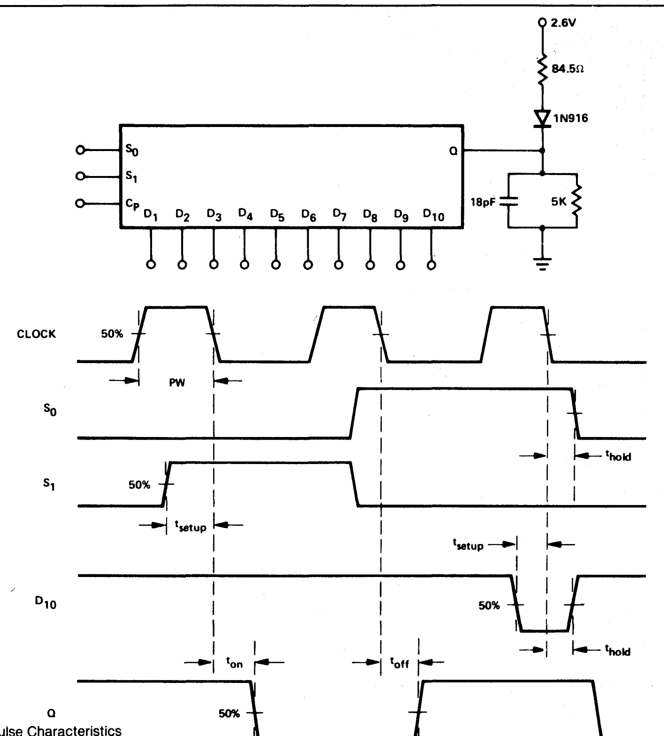
LOGIC DIAGRAM



SWITCHING CHARACTERISTICS $T_A=25°C$, $V_{CC}=5V$

PARAMETER		LIMITS			UNIT
		MIN	TYP	MAX	
Data Transfer Rate		25	30		MHz
t_{on}	Turn-on delay Clock to output		27	40	ns
t_{off}	Turn-off delay Clock to output		21	40	ns
t_W	Width of clock pulse		15	20	ns
t_{setup}	Setup time D_n		16	10	ns
	S_0, S_1		16	25	

AC TEST FIGURE AND WAVEFORMS



Clock Pulse Characteristics
Pulse Amplitude = 3.0V
t_r, $t_f \leq$ 10ns
PW $\leq$ 50ns

LOGIC

8275-B,F,W

DESCRIPTION

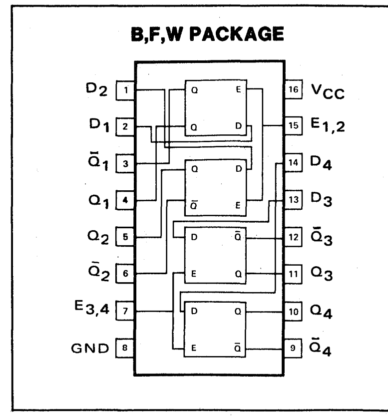
The 8275 is a QUAD LATCH circuit designed to provide temporary storage of four bits of information. A common application is as a holding register between a counter and a display driver (such as the 8280 and 8T01.) Separate enable lines to latches 1-2 and 3-4 allow individual control of each pair of latches. Initially, data is transferred on the rising edge of the enable pulse. While the enable is high, output Q follows the data input. When the enable falls, the input data present at fall time is retained at the Q output. Both Q and $\overline{Q}$ are accessible.

TRUTH TABLE (EACH LATCH)

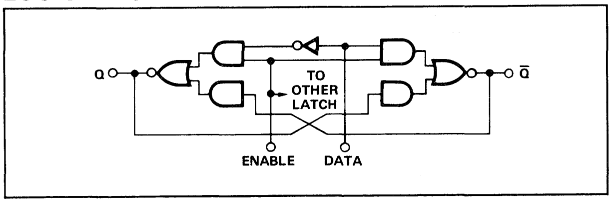
ENABLE	DATA	Q	$\overline{Q}$
1	1	1	0
1	0	0	1
0	1	*	*
0	0	*	*

*No change.

PIN CONFIGURATION



LOGIC DIAGRAM



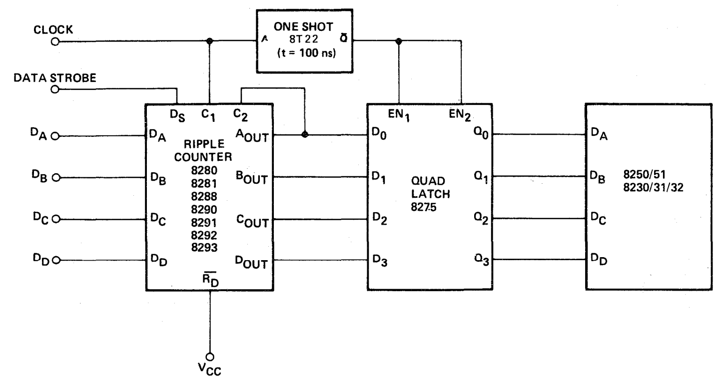
SWITCHING CHARACTERISTICS $T_A = 25°C$, $V_{CC} = 5V$

PARAMETER		FROM INPUT	TO OUTPUT	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT
t_{setup}	Setup time[1]							
	Low	D				14	20	ns
	High					12	20	
t_{hold}	Hold time[2]							
	Low	D			0	6		ns
	High				0	15		
Propagation Delay Time								
t_{PLH}	Low-to-high	D	Q			16	30	ns
t_{PHL}	High-to-low					14	25	
t_{PLH}	Low-to-high	D	$\overline{Q}$			24	40	
t_{PHL}	High-to-low					7	15	
t_{PLH}	Low-to-high	E	Q			16	30	
t_{PHL}	High-to-low					12	20	
t_{PLH}	Low-to-high	E	$\overline{Q}$			16	30	
t_{PHL}	High-to-low					12	20	

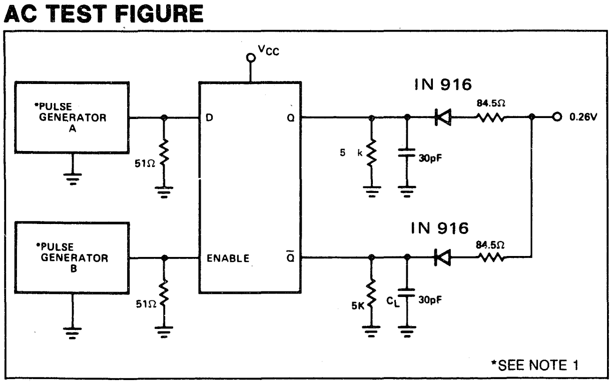
NOTES:
1. t_{setup} is defined as the time prior to the fall of the clock.
2. t_{hold} is defined as the time after the fall of the clock.

TYPICAL APPLICATION

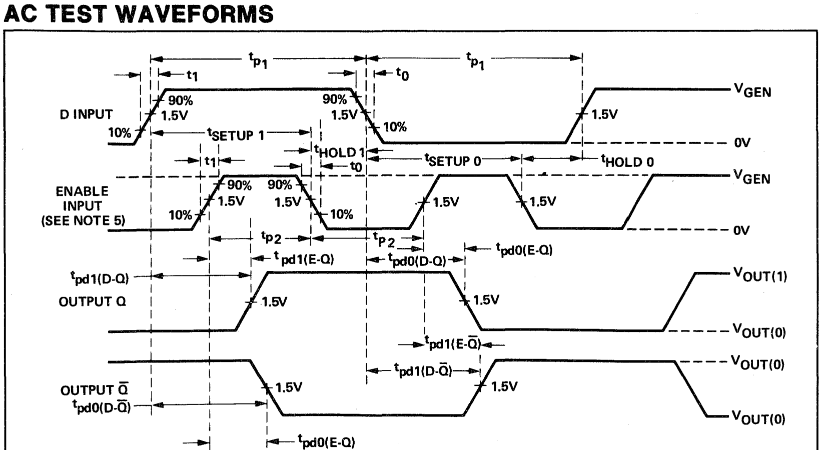
OUTPUT STROBING OF RIPPLE COUNTER TO ACHIEVE SYNCHRONOUS OUTPUT CHANGES



AC TEST FIGURE



AC TEST WAVEFORMS



NOTES:

1. The pulse generators have the following characteristics: $V_{gen} = 3V$, $t_1 = t_0 \leq 10ns$, and $Z_{out} \approx 50\Omega$. For pulse generator A, $t_{p1} = 1\mu s$ and PRR = 500Hz. For pulse generator B, tp2 = 500ns and Prr = 1MHz. Positions of D-input and enable input pulses are varied with respect to each other to verify setup and hold times.
2. Each latch is tested separately.
3. C_L includes probe and jig capacitance.
4. When measuring $t_{pd}1$ (D-Q), $t_{pd}0$ (D-Q), $t_{pd}0$ (D-$\overline{Q}$), and $t_{pd}1$(D-$\overline{Q}$), enable input must be held at logical 1.

8276-A,F

Product available in 0° to 75°C temp. range only.

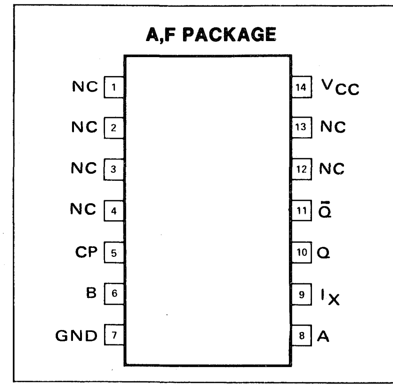
DESCRIPTION

The 8276 is a serial-in, serial-out 8-Bit Shift Register composed of eight R-S master slave flip-flops. This shift register has input gating and an internal clock driver. In addition, a data transfer inhibit input is provided.

Data Input and Data Enable are gated through inputs A and B. An internal inverter provides the complementary inputs to the first bit of the shift register. All inputs are fully buffered. Complementary Q and $\overline{Q}$ outputs are provided.

The internal clock driver/inverter causes the 8276 to shift data to the output on the positive edge of the input clock pulse, making the shift register compatible with the 8825 J-K Binary and the 8828 Dual D type Binary. The register is inhibited from shifting data when the Transfer Inhibit line is high. The inhibit function is achieved by preventing data transfer from master to slave sections of the register elements when the inhibit line is used.

PIN CONFIGURATION



SWITCHING CHARACTERISTICS $T_A = 25°C$, $V_{CC} = 5V$

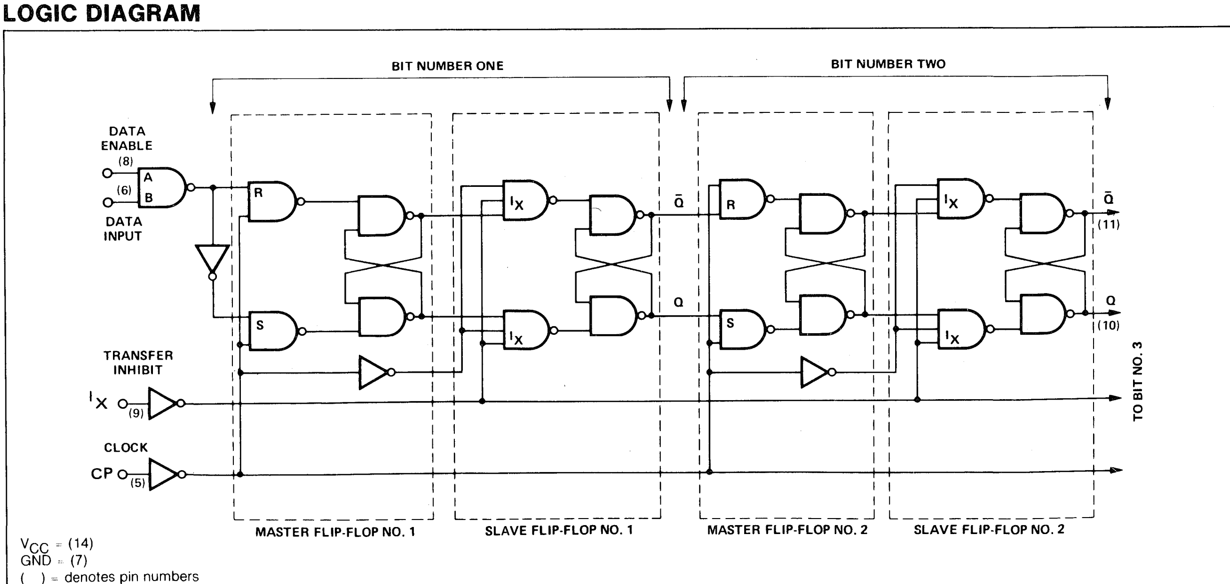
PARAMETER		LIMITS MIN	TYP	MAX	UNIT
Transfer rate		15	20		MHz
t_{on}	Turn-on delay Clock to output		22	33	ns
t_{off}	Turn-off delay Clock to output		22	33	ns
t_w	Clock pulse width	25			ns
t_{Setup}	Setup time (logical) Low at A or B input	25			ns
	High at A or B input	25			

TRUTH TABLE

t_n		t_{n+8}
A (Data Enable)	B (Data Input)	Q
0	0	0
0	1	0
1	0	0
1	1	1

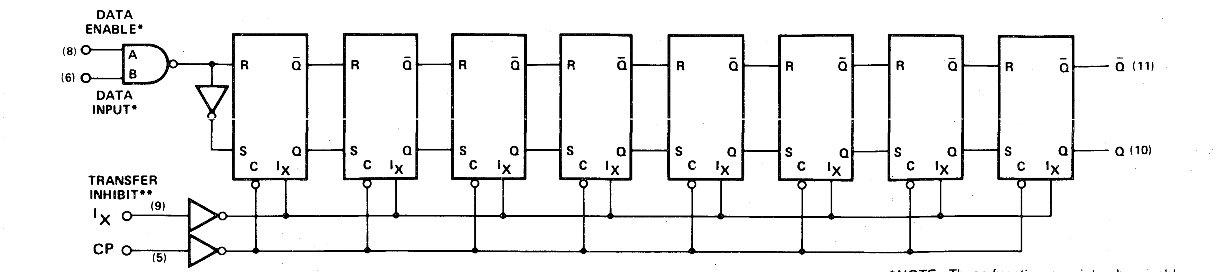
NOTES:
t_n Bit time before clock pulse.
t_{n+8} Bit time after 8 clock pulses.

LOGIC DIAGRAM



8276-A,F

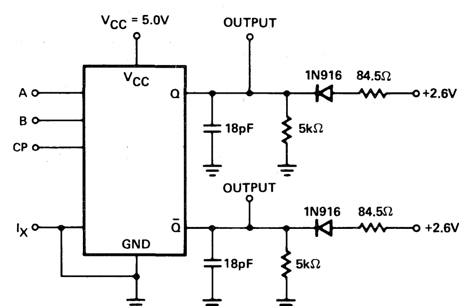
LOGIC DIAGRAM



V_{CC}=(14)
GND=(7)
( ) denotes pin numbers

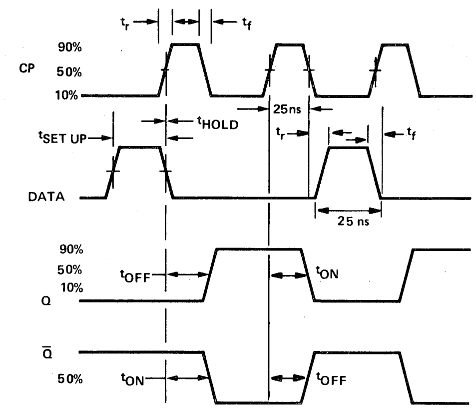
*NOTE: These functions are interchangeable.
**NOTE: Transfer inhibits prevents transfer of data from master to slave.

AC TEST FIGURE AND WAVEFORMS



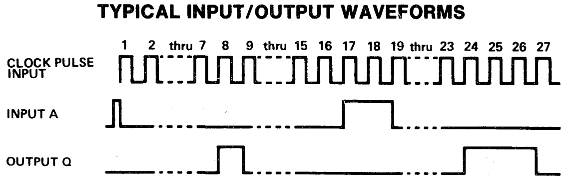
NOTES:
1. Unused input connected to 2.6V
2. Input pulse characteristics:
3. Setup time = 25ns
   Hold time = Ons

CLOCK:
Amplitude = 3.0 max
$t_r = t_f$ = 5ns max
PRR = 15 MHz
Pulse width = 25ns at 50% points



INPUT:
Amplitude = 3.0V
$t_r = t_f$ = 5ns max
PRR = 7.5 MHz
Pulse width = 25ns at 50% points

TYPICAL INPUT/OUTPUT WAVEFORMS



NOTE: Input B is connected to 2.6V. Transfer inhibit connected to OV

LOGIC

8277-B,F

Product available in 0° to 75°C temp. range only.

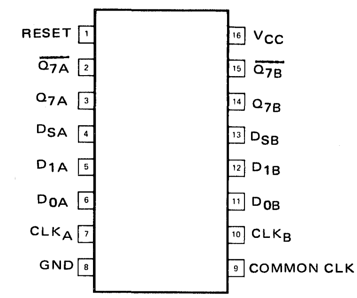
DESCRIPTION

The 8277 is a dual 8-Bit Shift Register which provides the designer with sixteen (16) bits of serial storage operating at a typical shift rate of 20MHz. Features of the 8277 are:

1. TRUE and COMPLEMENT outputs are provided on each register's eighth bit.
2. Positive edge triggering on clock input.
3. SEPARATE CLOCK lines (pins 7 and 10) for each 8-bit register are provided as well as a COMMON CLOCK line (pin 9) for all sixteen storage bits.
4. Common RESET (pin 1).
5. AND-OR gating to the input of each 8-bit register is provided to accomplish the multiplex function.
6. Direct replacement for 9328.

PIN CONFIGURATION

B, F PACKAGE



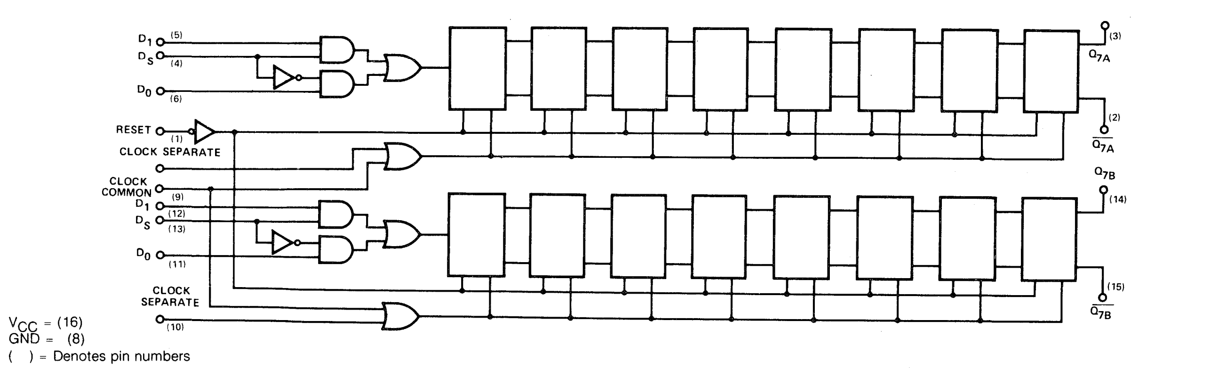
SWITCHING CHARACTERISTICS T_A=25°C, V_{CC}=5V

PARAMETER		LIMITS MIN	TYP	MAX	UNIT
t_{on}	Turn-on delay				
	Clock to output		25	40	ns
	Reset to output		25	40	
t_{off}	Turn-off delay				
	Clock to output		25	40	ns
	Reset to output		25	40	
t_W	Width of clock pulse	15			ns
	Shift rate	15	20		MHz
t_{setup}	Data setup time		20	30	ns
t_{Hold}	Data hold time			5	ns

TRUTH TABLE

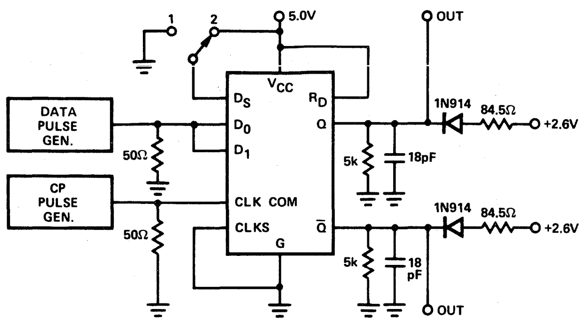
D_S	D_0	D_1	Reset	Function
0	0	x	1	Shift in "0"
0	1	x	1	Shift in "1"
1	x	0	1	Shift in "0"
1	x	1	1	Shift in "1"
x	x	x	0	Reset "Q" to "0'

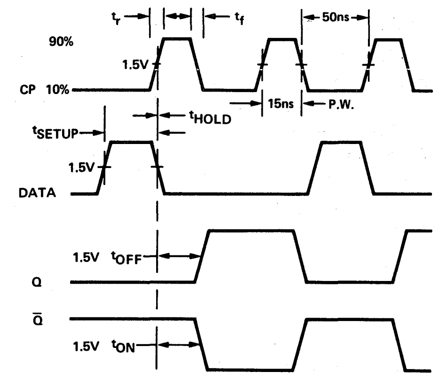
LOGIC DIAGRAM



8277-B,F

AC TEST FIGURE AND WAVEFORMS





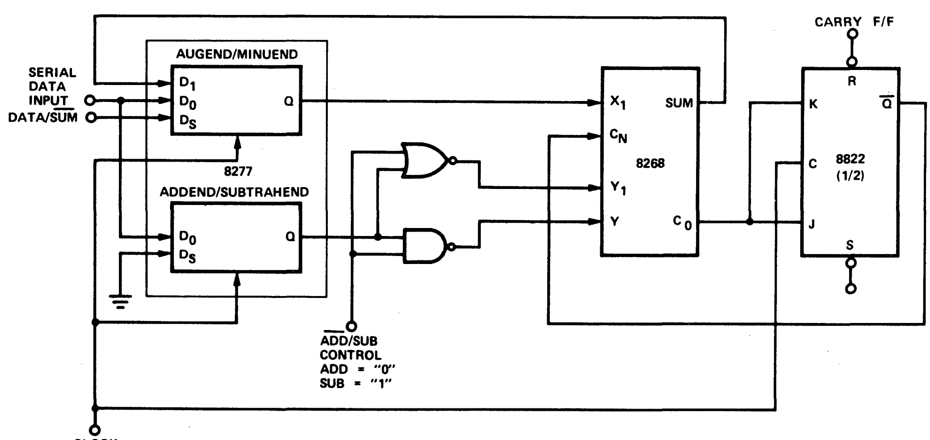
CLOCK PULSE:
P.A. = 3.0V
P.R.R. = 15 MHz
P.W. = 15 ns
$T_r = T_f = 5ns$

DATA PULSE:
P.A. = 3.0V
P.R.R. = 7.5 MHz
P.W. = 25ns
$T_r = T_f = 5ns$
$T_{SETUP} = 25ns$
$T_{HOLD} = 0$ ns

NOTES:
1. Each register is tested separately.
2. All T delay measurements taken at 1.5V level.
3. Tie all unused inputs to 2.6V.
4. 18pF on outputs includes probe and jug capacitance.

TYPICAL APPLICATION

8-BIT SERIAL ADD/SUBTRACTOR



LOGIC

BCD DECADE COUNTER/STORAGE ELEMENT
4-BIT BINARY COUNTER/STORAGE ELEMENT

8280/81

8280-A,F,W • 8281-A,F,W

DESCRIPTION

The 8280 Decade Counter and 8281 16-State Binary Counter are four-bit subsystems providing a wide variety of counter/storage register applications with a minimum number of packages.

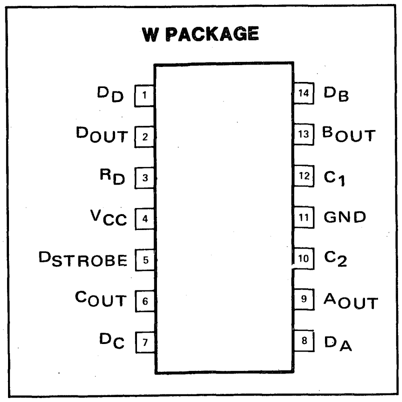
The 8280 Decade Counter can be connected in the familiar BCD counting mode, in a divide-by-two and divide-by-five configuration or in the Bi-Quinary mode. The Bi-Quinary mode produces a square wave output which is particularly useful in frequency synthesizer applications.

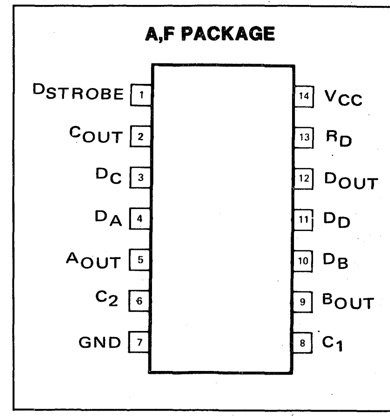
The 8281 Binary Counter may be connected as a divide-by-two, eight, or sixteen counter.

Both devices have strobed parallel-entry capability so that the counter may be set to any desired output state. A "1" or "0" at a data input will be transferred to the associated output when the strobe input is put at the "0" level. For additional flexibility, both units are provided with a reset input which is common to all four bits. A "0" on the reset line produces "0" at all four outputs.

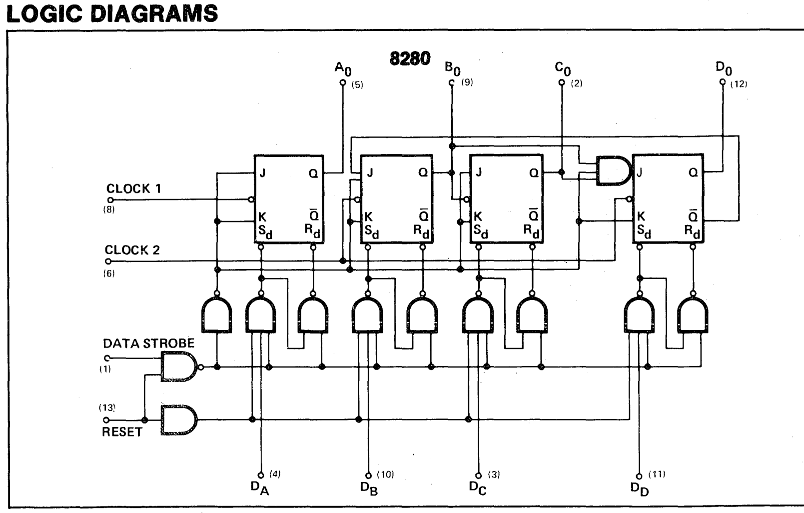
The counting operation is performed on the falling (negative-going) edge of the input clock pulse, however there is no restriction on the transition time since the individual binaries are level-sensitive.

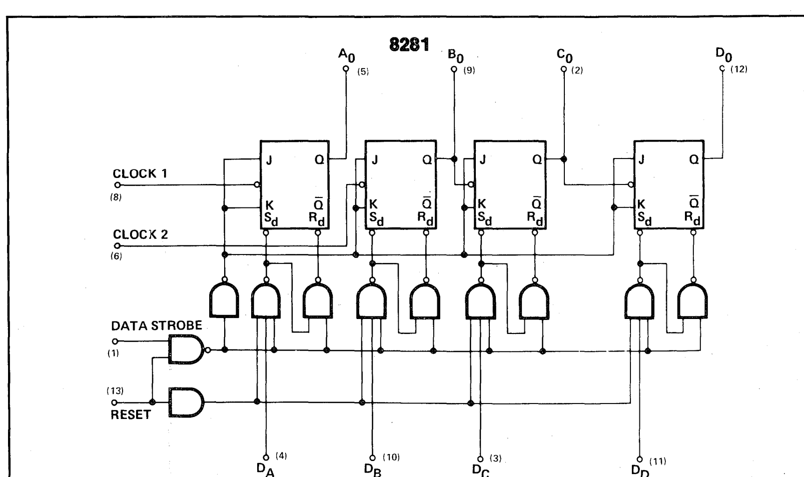
PIN CONFIGURATION





LOGIC DIAGRAMS

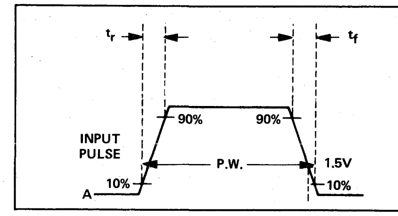




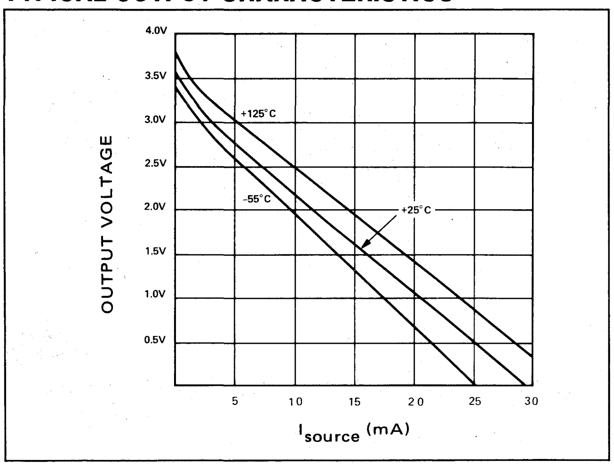
SWITCHING CHARACTERISTICS $T_A = 25°C$, $V_{CC} = 5V$

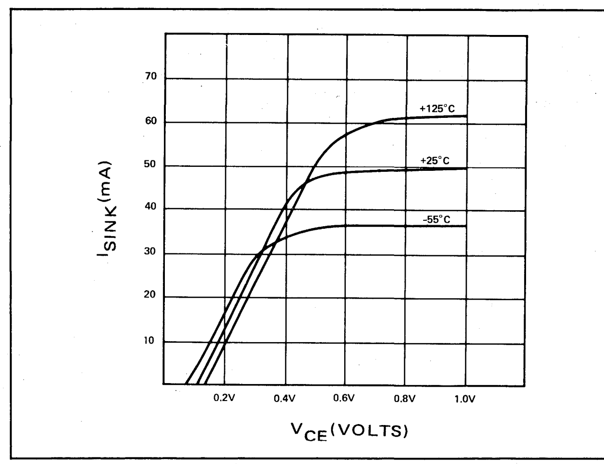
PARAMETER		TEST CONDITIONS	LIMITS 8280/8281 MIN	TYP	MAX	UNIT
t_{on}	Turn-on delay time					
	Clock mode	Bit A,B,C,D		15	25	ns
	Data/strobe			25	35	
t_{off}	Turn-off delay time					
	Clock mode	Bit A,B,C,D,		15	25	ns
	Data strobe			30	40	
Toggle rate			20	25		MHz
t_w	Width of input pulse					
	$\overline{\text{Strobe}}$			20	35	ns
	$\overline{\text{Reset}}$			20	35	
$t_{release}$	Release time					
	$\overline{\text{Strobe}}$			30	40	ns
	$\overline{\text{Reset}}$			50	75	

AC WAVEFORM

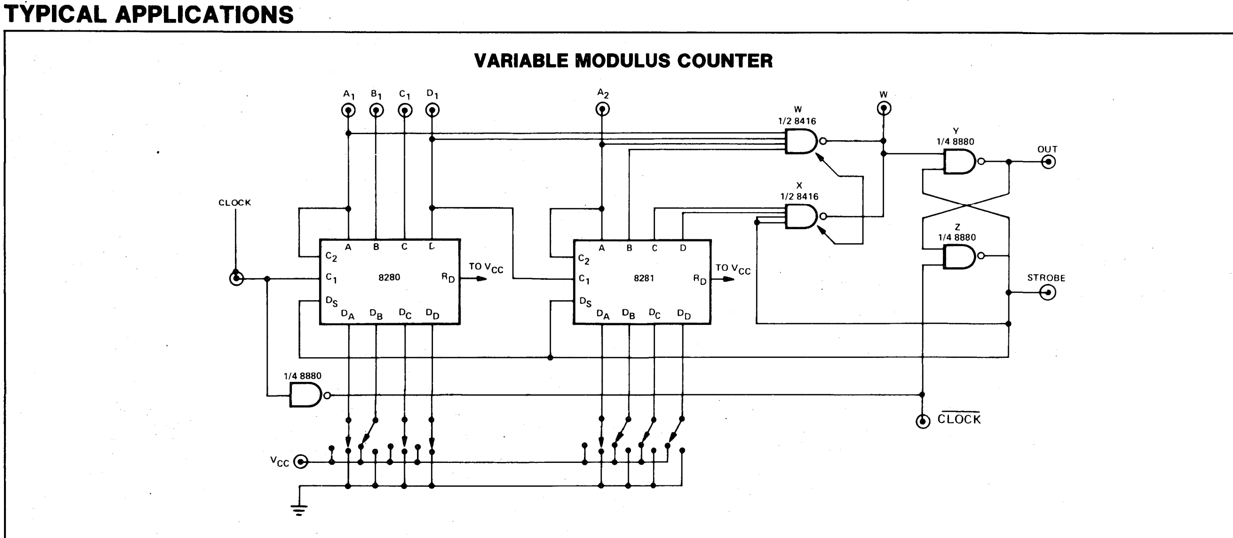


TYPICAL OUTPUT CHARACTERISTICS





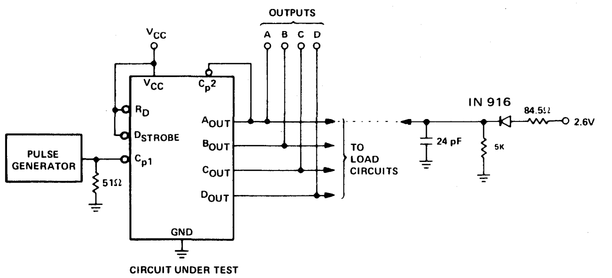
TYPICAL APPLICATIONS

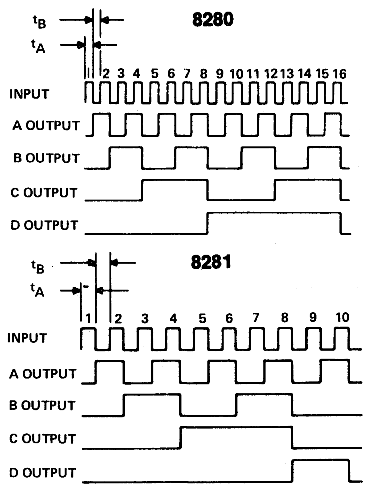


LOGIC

AC TEST FIGURES AND WAVEFORMS

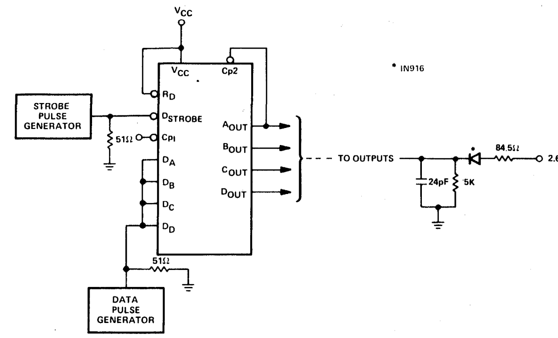
TOGGLE RATE

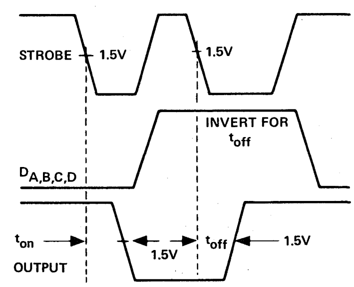




Input pulse:
Amplitude = 2.6V
t_A = 25ns, t_B = 25ns,
t_r = t_f = 5ns max.

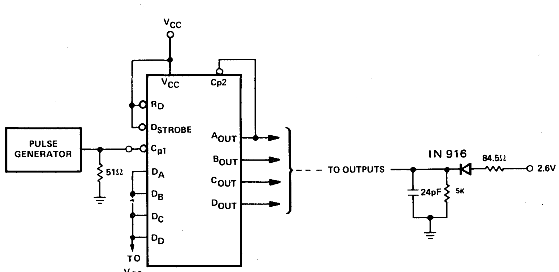
DATA/STROBE t_{on}/t_{off}

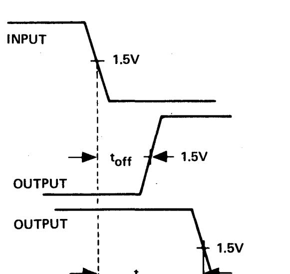




Strobe, P.A. = 2.6V
P.W. = 300ns
PRR = 1 MHz
t_r = t_f = 5ns
Data, P.A. = 2.6V
P.W. = 500ns
PRR = 500 KHz
t_r = t_f = 5ns.

CLOCK MODE t_{on}/t_{off} DELAY

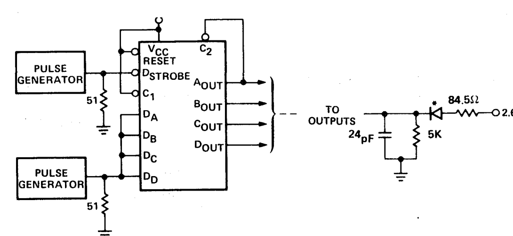


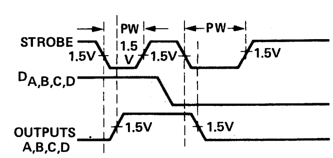


Input pulse:
Amplitude = 2.6V
P.W. = 30ns
t_r = t_f = 5ns.

1. t_{on} and t_{off} are measured from the clock input of each binary to the Q output of that binary.
2. Each Q output will be loaded with a load circuit as shown.

MINIMUM STROBE PULSE WIDTH

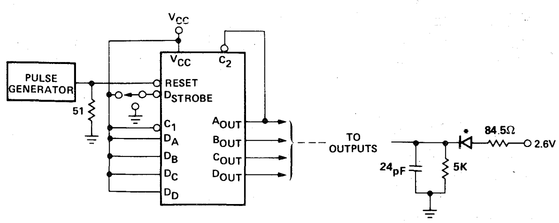


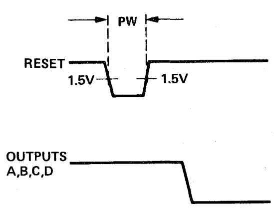


INPUT PULSE:
Amplitude = 2.6V
t_r = t_f = 5ns.

AC TEST FIGURES AND WAVEFORMS

MINIMUM RESET PULSE WIDTH

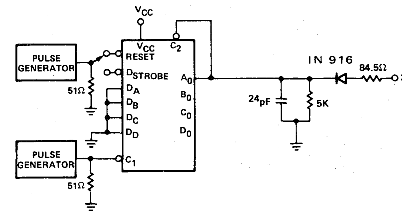


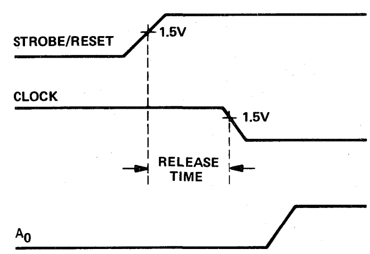


INPUT PULSE:
Amplitude = 2.6V
$t_r = t_f$ = 5ns max.

Note: Outputs must be previously brought high by placing a "0" on the D strobe input. A pulse generator may be substituted for the switch.

STROBE/RESET RELEASE TIME

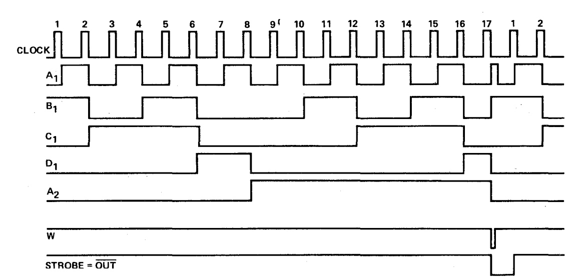




Clock, Strobe/Reset:
Ampl = 2.6V
tr = tf = 5ns max.
PRR = 1 MHz 50% Duty Cycle.

NOTES:
1. All resistor values are in ohms.
2. All capacitance values are in picofarads and include jig and probe capacitance.
3. Input pulse notations apply unless otherwise specified.

TIMING DIAGRAM



LOGIC

SPEED / PACKAGE AVAILABILITY
82S N,F

DESCRIPTION

The 82S82 binary coded (BCD) arithmetic unit is a high speed Schottky MSI circuit with lookahead carry/$\overline{\text{borrow}}$ that has been designed for easy systems usage. Depending on the state of the $\overline{\text{add}}$/subtract control line, the unit produces the BCD sum or difference of two decimal numbers presented to the BCD inputs in the 8-4-2-1 weighted BCD format. A comparison output (A=B) is provided as well. When in the subtract mode, this output indicates if two BCD numbers are equal and its open collector feature allows easy comparison of several decades.

The 82S82 BCD arithmetic unit has been designed such that input and output logic levels including the carry/$\overline{\text{borrow}}$ are in their true logic form. Compared to multichip hardware solutions previously at the designer's disposal, the 82S82 arithmetic unit generates the BCD carry/$\overline{\text{borrow}}$ terms internally in the look-ahead mode and does BCD arithmetic directly. For more than one BCD decade the carry/$\overline{\text{borrow}}$ term may ripple between 82S82's. For ultra fast BCD arithmetic operations the Signetics 74182 fast-carry extender may be used together with the 82S82's. The 74182 suitably combines the 82S82's active low carry generate ($\overline{\text{CgOUT}}$) and carry propagate ($\overline{\text{CpOUT}}$) terms for complete look-ahead carry between decades.

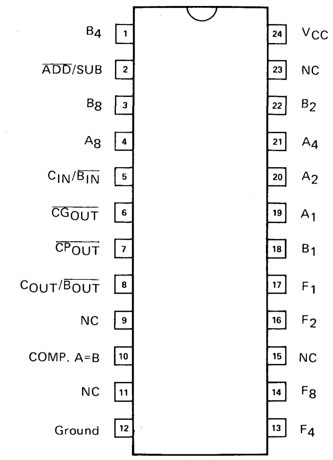
When the $\overline{\text{ADD}}$/SUBTRACT control input is low, BCD addition is performed (A + B + CIN = F). Input codes above 9 to either the A_N or B_N inputs are not defined to give valid output sums except for the special case of binary to BCD conversion. In the normal BCD addition mode the F outputs show true BCD results and an active high carryout signal results for sums greater than 9.

For subtraction the $\overline{\text{ADD}}$/SUBTRACT control input must be high. Internally subtraction is performed by 9's complement addition yielding the difference (A - B - 1 = F) of two BCD numbers when the CIN/$\overline{\text{BIN}}$ input is low. If the CIN/$\overline{\text{BIN}}$ is high during subtraction, the absence of a borrow in signal gives A-F=F. For A $\geq$ B the BCD difference is available at the F outputs in its true form. If A $<$ B, the 10's complement of the correct answer appears at the F outputs with CIN/$\overline{\text{BIN}}$ high or if CIN/$\overline{\text{BIN}}$ is low the 9's complement results. As long as A $<$ B an active low borrow is also generated.

The 82S82 BCD arithmetic unit is also useful for binary to BCD conversion. By summing B=0 with binary inputs $0 \leq A \leq 15$, where A is the number being converted, a true BCD output results. A carry is generated to the next decade for A$>$9.

The function table for the 82S82 summarizes the device operation. In those applications where only BCD addition is required, the Signetics 82S82 BCD adder should be considered.

N,F PACKAGE



TRUTH TABLE

BCD CODE				
DECIMAL EQUIVALENT	BCD NUMBER 8	4	2	1
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1

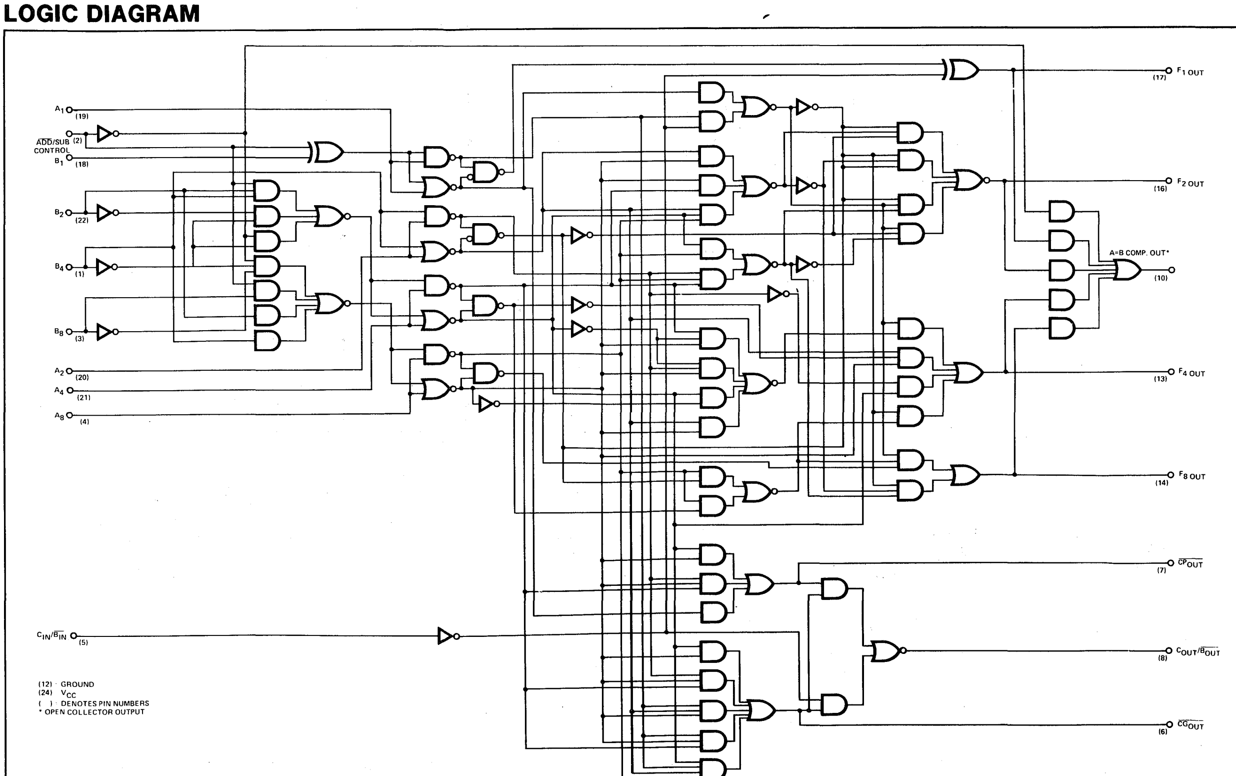
FUNCTION TABLE

FUNCTION	$\overline{\text{ADD}}$/SUB	A(A_8,A_4,A_2,A_1)	B(B_8,B_4,B_2,B_1)	$C_{in}/\overline{B_{in}}$	F(F_8,F_4,F_2,F_1)	$C_{out}/\overline{B_{out}}$	COMPARE (A = B)
Add	0	BCD Augend	BCD Addend	1=Carry 0=No Carry	IF C_{in} = 1 F = A + B + 1 IF C_{in} = 0 F = A + B	F≤9 $C_{out}/\overline{B_{out}}$=0 F>9 $C_{out}/\overline{B_{out}}$=1	X
Subtract	1	BCD Minuend	BCD Subtrahend	0=Borrow 1=No Borrow	IF B_{in} = 0 F = A - B - 1 IF B_{in} = 1 F = A - B	A>B $C_{out}/\overline{B_{out}}$=1 A≤B $C_{out}/\overline{B_{out}}$=0 A<B $C_{out}/\overline{B_{out}}$=0 A≥B $C_{out}/\overline{B_{out}}$=1	X
Compare	1	BCD Word A	BCD Word B	1	A - B	A<B $C_{out}/\overline{B_{out}}$=0 A>B $C_{out}/\overline{B_{out}}$=1	If A=B Compare =1 If A≠B Compare =0
Binary to BCD Conversion	0	0≤A≤ 15	B = 0	X	BCD	A≤9 C_{out} = 0 A>9 C_{out} = 1	X

SWITCHING CHARACTERISTICS TA = 25°C and VCC = 5.0V

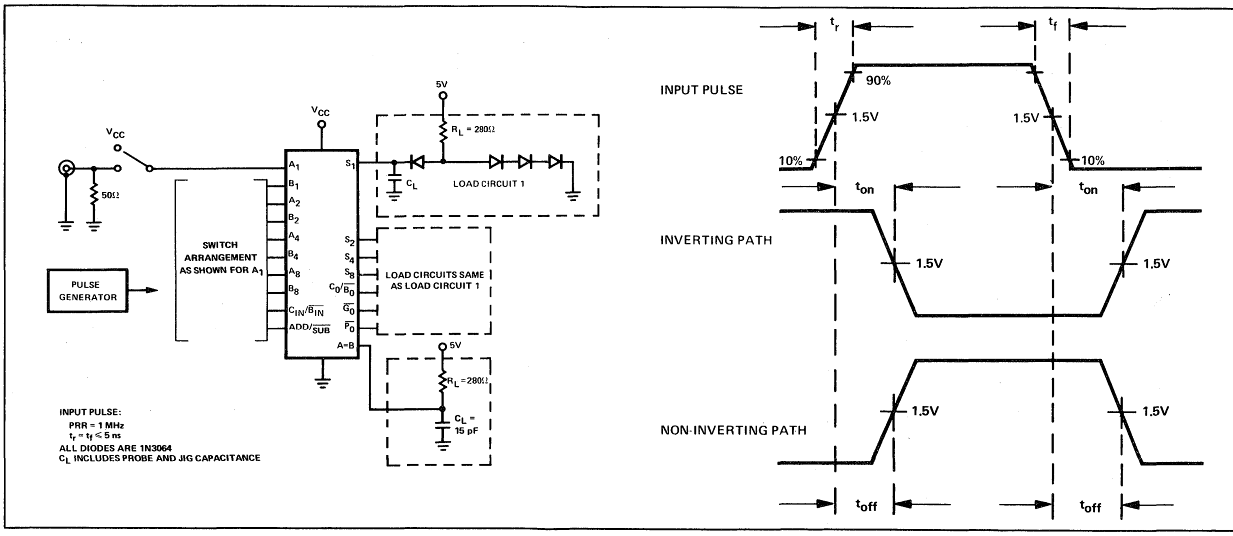
CHARACTERISTIC		TEST CONDITIONS	LIMITS			
			MIN.	TYP.	MAX.	UNITS
Turn On/Turn Off Delays						
Any A_N, B_N, $C_{in}/\overline{B_{in}}$ to F_N				22	35	ns
				22	35	ns
Any A_N to $C_{out}/\overline{B_{out}}$	t_{on}			32	40	ns
	t_{off}			22	35	ns
Any B_N to $C_{out}/\overline{B_{out}}$	t_{on}			35	45	ns
	t_{off}			26	35	ns
$C_{in}/\overline{B_{in}}$ to $C_{out}/\overline{B_{out}}$	t_{on}	$R_L = 280\Omega$		17	25	ns
	t_{off}	$C_L = 15pF$		10	15	ns
Add/$\overline{Sub}$ to F_N	t_{on}			25	35	ns
	t_{off}			25	35	ns
A_N, B_N, to $\overline{Cp_{out}}$	t_{on}			19	25	ns
	t_{off}			19	25	ns
A_N, B_N to $\overline{Cg_{out}}$	t_{on}			19	25	ns
	t_{off}			25	32	ns
A_N, B_N to (A = B)	t_{on}			32	50	ns
	t_{off}			40	50	ns

LOGIC DIAGRAM



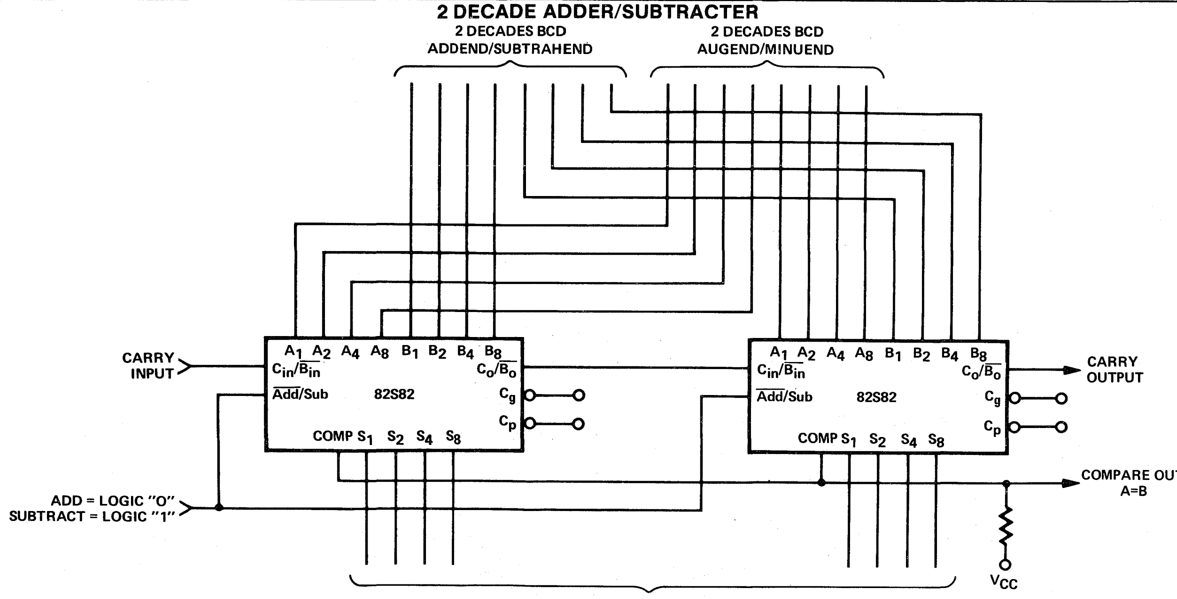
LOGIC

AC TEST FIGURES AND WAVEFORMS

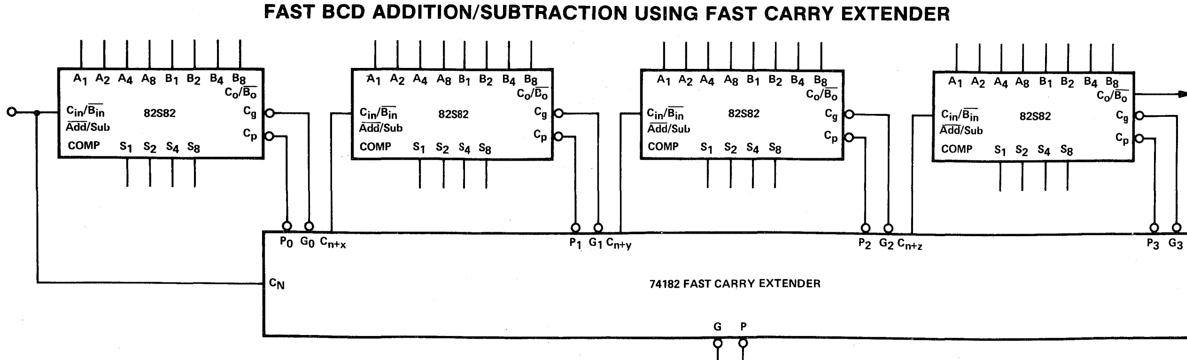


TYPICAL APPLICATIONS

2 DECADE ADDER/SUBTRACTER

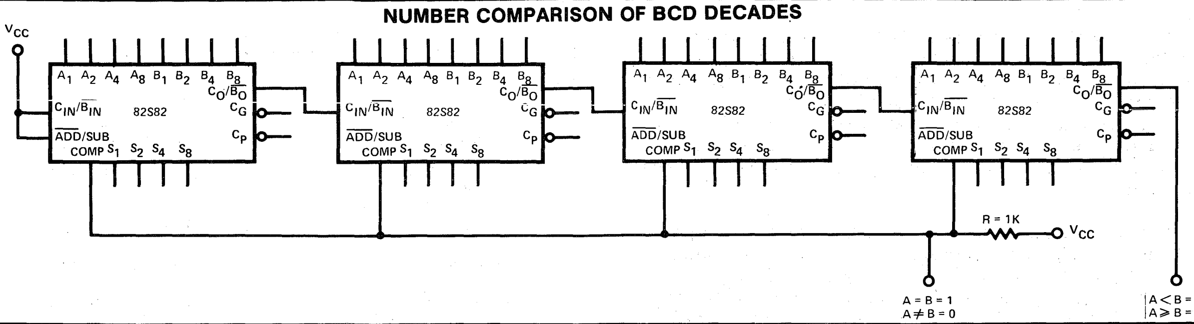


FAST BCD ADDITION/SUBTRACTION USING FAST CARRY EXTENDER

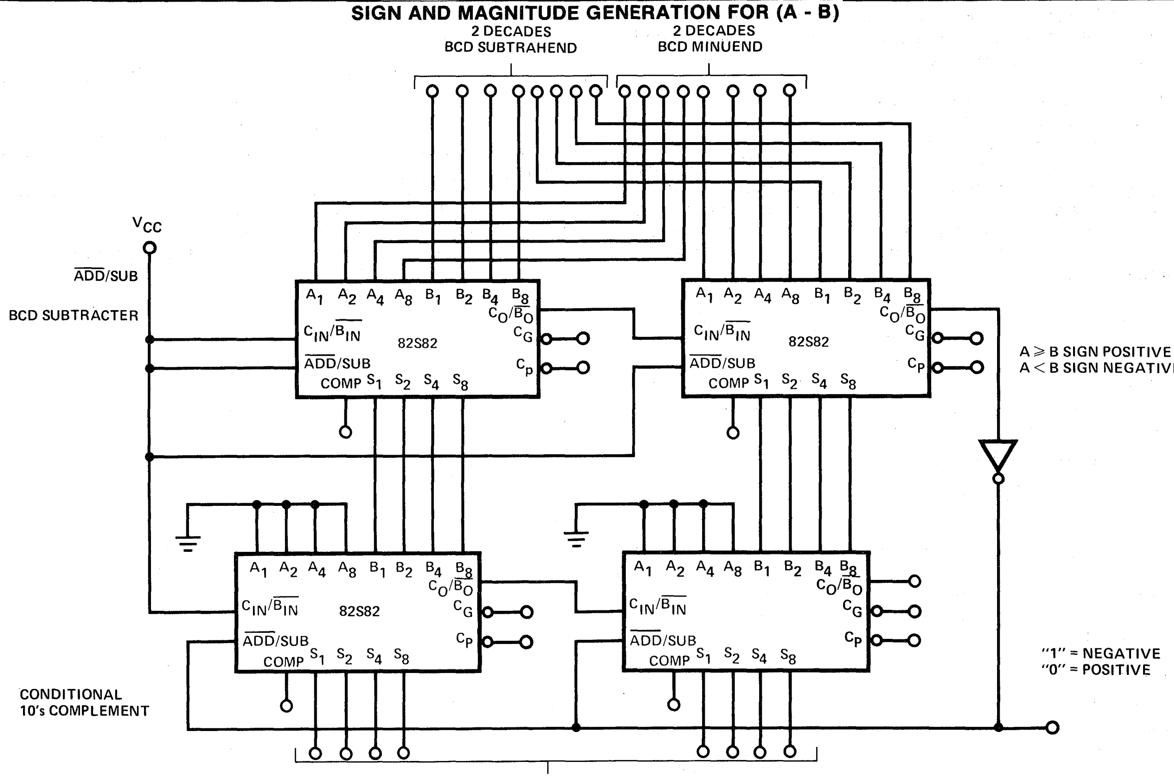


TYPICAL APPLICATIONS (CONT'D.)

NUMBER COMPARISON OF BCD DECADES

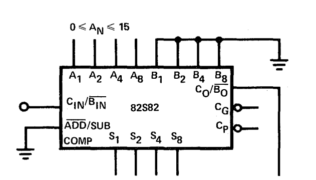


SIGN AND MAGNITUDE GENERATION FOR (A - B)



BINARY TO BCD CONVERSION

TRUTH TABLE FOR BINARY TO BCD CONVERSION ($10 \leq A_N \leq 15$, $B_N = 0$)										
Add/Sub	C_{in}/B_{in}	A_8	A_4	A_2	A_1	S_8	S_4	S_2	S_1	$C_{out}/\overline{B_{out}}$
0	0	1	0	1	0	0	0	0	0	1
0	0	1	0	1	1	0	0	0	1	1
0	0	1	1	0	0	0	0	1	0	1
0	0	1	1	0	1	0	0	1	1	1
0	0	1	1	1	0	0	1	0	0	1
0	0	1	1	1	1	0	1	0	1	1
0	1	1	0	1	0	0	0	0	1	1
0	1	1	0	1	1	0	0	1	0	1
0	1	1	1	0	0	0	0	1	1	1
0	1	1	1	0	1	0	1	0	0	1
0	1	1	1	1	0	0	1	0	1	1
0	1	1	1	1	1	0	1	1	0	1



LOGIC

SPEED/PACKAGE AVAILABILITY

DESCRIPTION

The 82S83 4-bit binary coded (BCD) adder is a high speed Schottky MSI circuit that has been designed for easy systems usage. This unit produces the BCD sum of two decimal numbers presented in the 8-4-2-1 weighted BCD format. Carry-in and carry-out terms are provided for easy expansion to any number of decades. The 82S83 BCD adder has been designed such that input and output logic levels including the carry are in their true logic form.

Compared to cumbersome hardware implementations previously at the designer's disposal that consist of binary addition followed by decimal correction, the 82S83 BCD adder generates the BCD carry terms internally in the look-ahead mode and does BCD addition directly. For valid BCD numbers (0 through 9) at the A and B inputs the BCD sum is formed at the output. If addition (A+B+CIN) would yield a number greater than 9, a valid BCD number and a carry result.

Input codes above 9 are not defined except for binary to BCD conversion. Binary to BCD conversion is obtained by applying any 4-bit binary number to the AN or BN inputs while the remaining inputs are grounded. For input codes 0 through 9 a BCD number result at the output is usual. If binary inputs 10 through 15 are applied a carry term is generated and the carry output together with the sum out are the BCD equivalent of the binary input. Conversion of binary numbers greater than 16 can be achieved by cascading 82S83's.

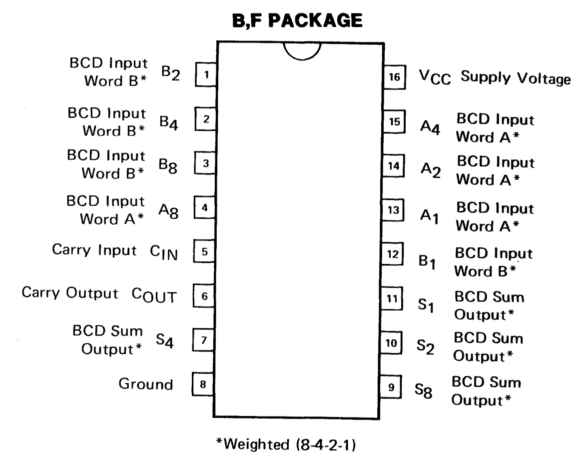
Subtraction can be done with the 82S83 by using 9's complement addition. Rather than implementing a 9's complement circuit with gates or ROM's, the 82S83 BCD arithmetic unit should be used. The 82S83 incorporates the 9's complement feature and performs BCD addition, BCD subtraction, and number comparison.

SWITCHING CHARACTERISTICS

TA = 25°C and VCC = 5.0V

PARAMETER		LIMITS			
		MIN.	TYP.	MAX.	UNITS
Turn-On/Turn-Off Delays					
Any AN, BN, Cin	ton		20	35	ns
to SN	toff		20	35	ns
Any AN, BN, to	ton		33	40	ns
Cout	toff		17	25	ns
Cin to Cout	ton		17	25	ns
	toff		10	15	ns

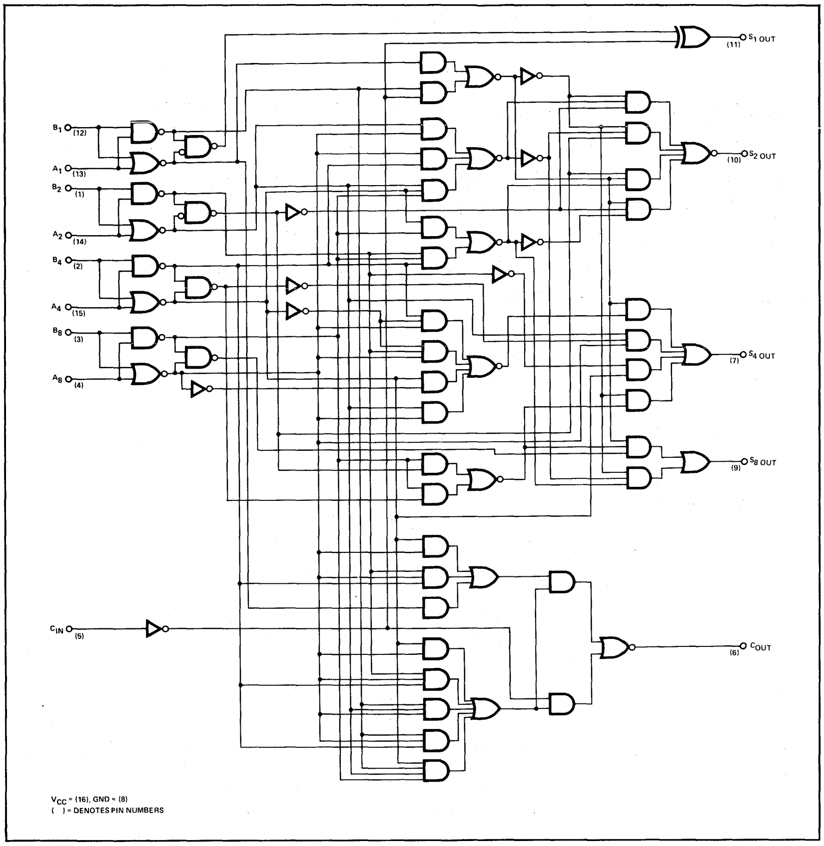
PIN CONFIGURATION



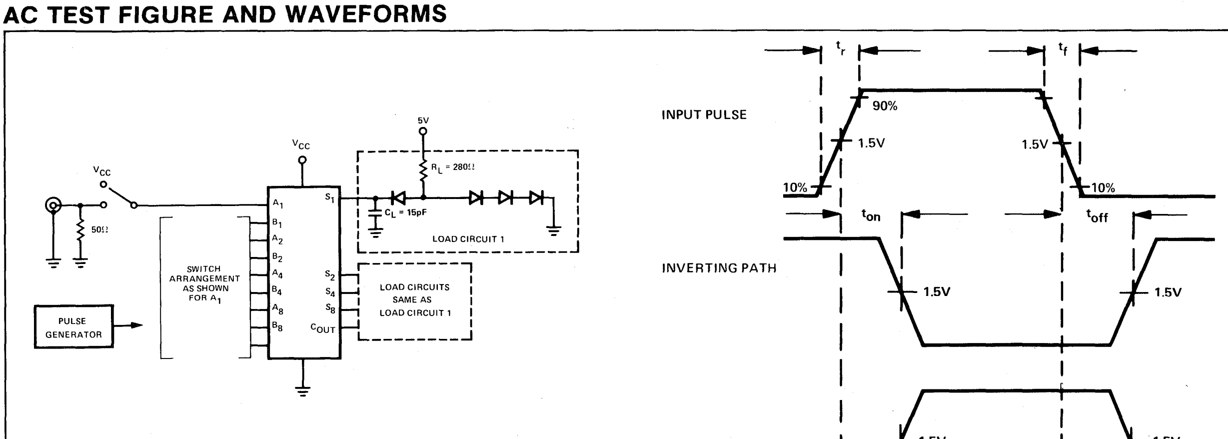
TRUTH TABLE

BCD CODE				
Decimal Equivalent	BCD Number			
	8	4	2	1
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1

LOGIC DIAGRAM



AC TEST FIGURE AND WAVEFORMS

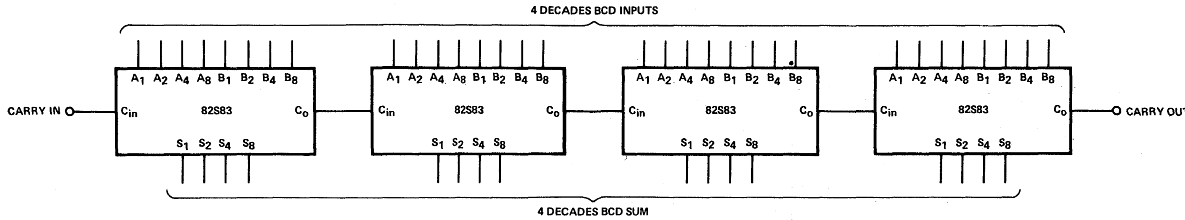


INPUT PULSE:
PRR = 1 MHz
tr = tf = 5 ns
ALL DIODES ARE 1N3064
CL INCLUDES PROBE AND JIG CAPACITANCE

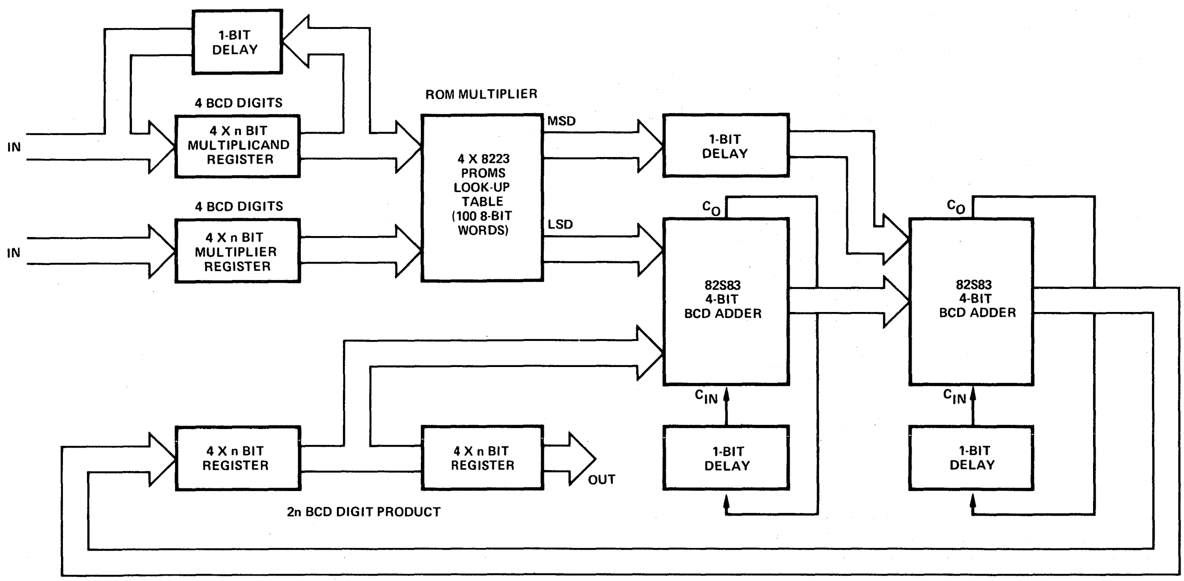
LOGIC

TYPICAL APPLICATIONS

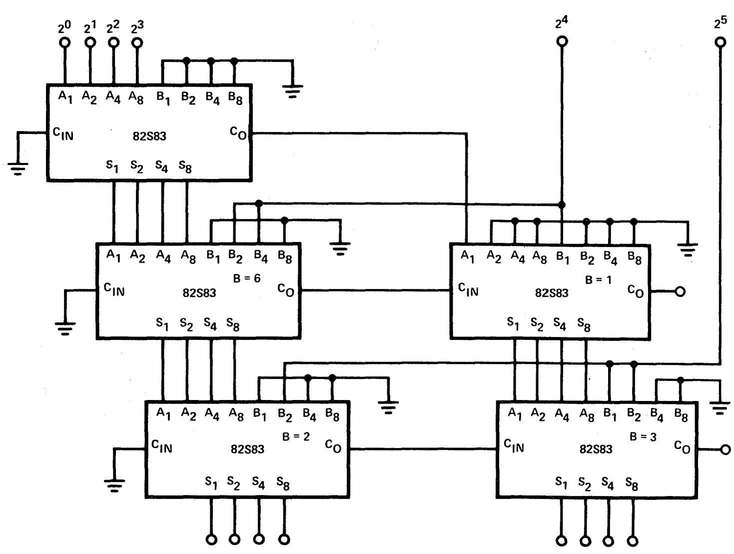
PARALLEL ADDITION OF FOUR DECADES



BIT PARALLEL-WORD SERIAL BCD MULTIPLIER



BINARY TO BCD CONVERSION FOR TWO DECADES

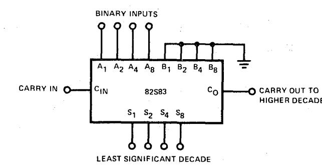


TYPICAL APPLICATIONS (CONT'D.)

BINARY TO BCD CONVERSION USING A_i INPUTS

PARTIAL TRUTH TABLE FOR Ai > 9, Bi = 0

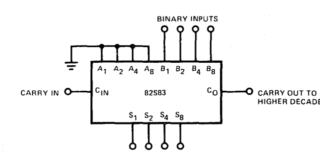
CIN	A1	A2	A4	A8	B1	B2	B4	B3	S1	S2	S4	S8	CO
0	0	1	0	1	0	0	0	0	0	0	0	0	1
0	1	1	0	1	0	0	0	0	1	0	0	0	1
0	0	0	1	1	0	0	0	0	0	1	0	0	1
0	1	0	1	1	0	0	0	0	1	1	0	0	1
0	0	1	1	1	0	0	0	0	0	0	1	0	1
0	1	1	1	1	0	0	0	0	1	0	1	0	1
1	0	1	0	1	0	0	0	0	1	0	0	0	1
1	1	1	0	1	0	0	0	0	0	1	0	0	1
1	0	0	1	1	0	0	0	0	1	1	0	0	1
1	1	0	1	1	0	0	0	0	0	0	1	0	1
1	0	1	1	1	0	0	0	0	1	0	1	0	1
1	1	1	1	1	0	0	0	0	0	1	1	0	1



BINARY TO BCD CONVERSION USING B_i INPUTS

PARTIAL TRUTH TABLE FOR Bi > 9, Ai = 0

CIN	A1	A2	A4	A8	B1	B2	B4	B8	S1	S2	S4	S8	CO
0	0	0	0	0	0	1	0	1	0	0	0	0	1
0	0	0	0	0	1	1	0	1	1	0	0	0	1
0	0	0	0	0	0	0	1	1	0	1	0	0	1
0	0	0	0	0	1	0	1	1	1	1	0	0	1
0	0	0	0	0	0	1	1	1	1	0	0	1	0
0	0	0	0	0	1	1	1	1	1	0	1	0	1
1	0	0	0	0	0	1	0	1	1	0	0	0	1
1	0	0	0	0	1	1	0	1	0	1	0	0	1
1	0	0	0	0	0	0	1	1	1	1	0	0	1
1	0	0	0	0	1	0	1	1	0	0	1	0	1
1	0	0	0	0	0	1	1	1	1	0	1	0	1
1	0	0	0	0	1	0	0	0	0	1	1	0	1



LOGIC

8284-A,F,W • 8285-A,F,W

DESCRIPTION

The Up/Down Counter is a monolithic SI circuit containing gates and binaries interconnected to provide a bidirectional divide-by-ten (decade) or divide-by-sixteen (hexadecimal) result as a function of the clock input.

The output code of the decade up/down counter is the commonly used BCD (8421) code, and the output sequence generated is the binary equivalent of the decimal numbers 0 through 9.

The hexadecimal up/down counter provides the output sequence 0 through 15 which is presented in a weighted binary code (8421).

Set and Reset on the binary elements provide asynchronous entry with respect to the clock line, causing a count of "0" or "15" (8284) or of "0" or "9" (8285), and also inhibit propagation of count enable data.

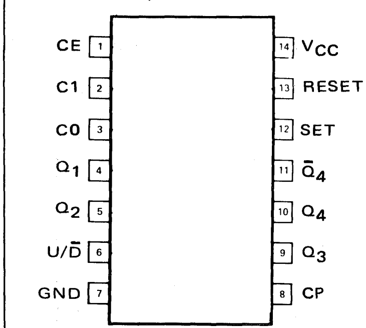
Entry and propagation of data is performed in a synchronous manner with the clock line, which is active on its negative going excursion. The input from a previous stage or other source is channeled through "Carry In" and its propagation can be inhibited by the "Count Enable" line. "Carry In" and "Count Enable" input duality gives added flexibility in multiple package cascading applications.

Direction of the counter is steered from a single line (Up/$\overline{\text{Down}}$), where a "0" level will cause a "down" count and a "1" level will accomplish an "up" count.

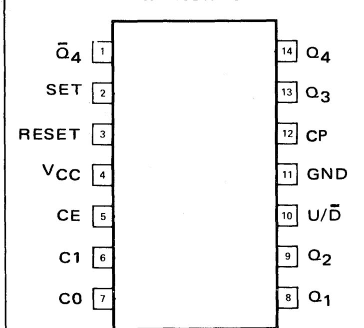
In addition to all Q outputs of the four binaries the $\overline{Q}$ output of the most significant binary (Q4) and the Carry Out term are available.

PIN CONFIGURATION

A,F PACKAGE



W PACKAGE

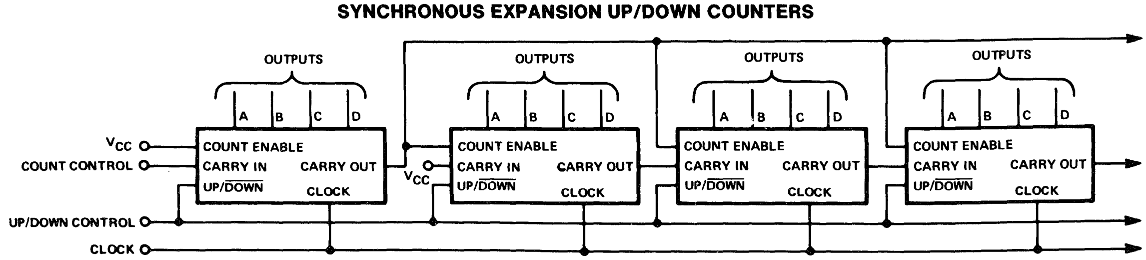


SWITCHING CHARACTERISTICS $T_A=25°C$, $V_{CC}=5V$

PARAMETER	FROM INPUT	TO OUTPUT	LIMITS MIN	TYP	MAX	UNIT
t_{on} turn-on time	Clock	Q4, $\overline{Q}_4$		32	45	ns
	Clock	Q_1, Q_2, Q_3		28	40	
	Reset	Qn		24	35	
	Reset	$\overline{Q}_n$		32	45	
				15	25	
t_{off} Turn-off time	Carry In	Carry Out		20	30	
	Clock	Q_n, $\overline{Q}_n$		25	35	
	Set	Qn		15	25	
Clock Min High Interval			20	15		ns
Count Rate			20	30		MHz
t_{Setup} Setup time	Carry In, Count Enable			15	25	ns
t_{Hold} Hold time	Up/Down			0	2	ns
t_w Input pulse width	Set/Reset			20	25	ns

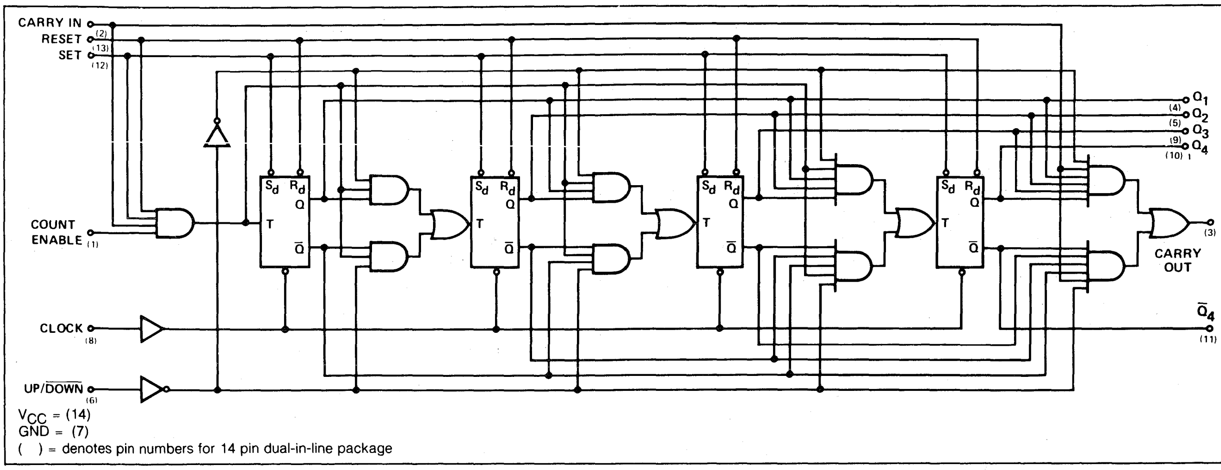
TYPICAL APPLICATIONS

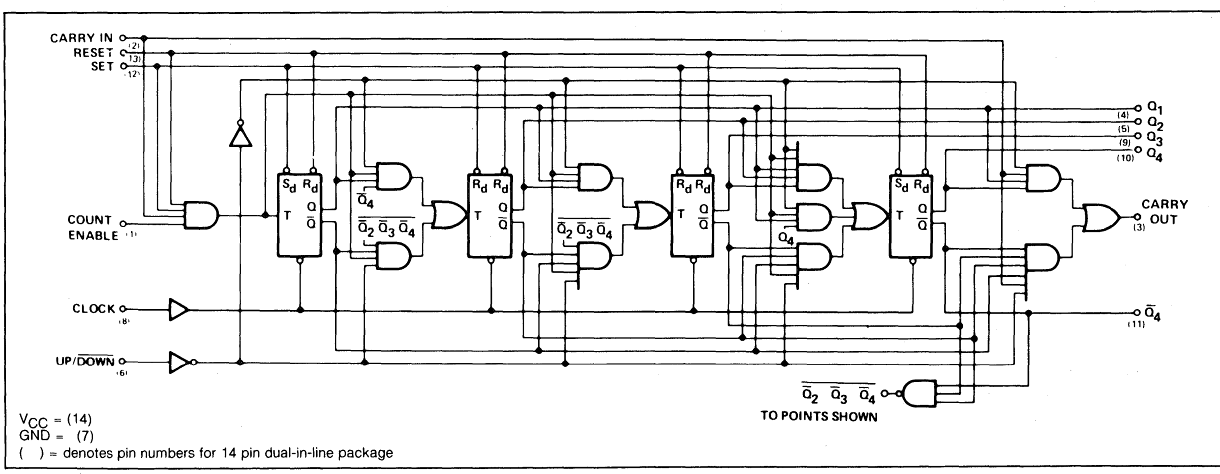
SYNCHRONOUS EXPANSION UP/DOWN COUNTERS



8284-A,F,W • 8285-A,F,W

LOGIC DIAGRAMS





AC TEST TABLE

MODE OF OPERATION	SET	RESET	CARRY IN	COUNT ENABLE	UP/$\overline{DOWN}$	FUNCTION
A. Asynchronous	1	0	x	x	x	"0" (0 0 0 0)
8284 Only	0	1	x	x	x	"15" (1 1 1 1)
8285 Only	0	1	x	x	x	"9" (1 0 0 1)
B. Synchronous						
	1	1	0	x	x	Hold*
	1	1	x	0	x	Hold*
	1	1	1	1	0	"Down" Count*
	1	1	1	1	1	"Up" Count*

*Function is synchronous with NEGATIVE going transition of the Clock pin.
X = don't care.

CARRY OUT

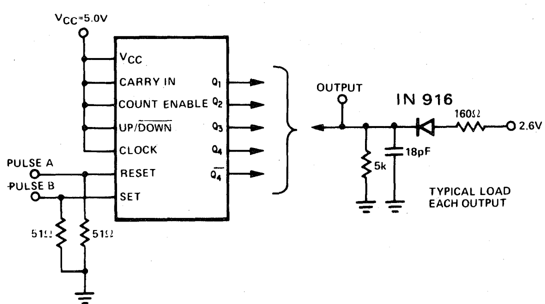
$\text{Carry Out}_{8284} = \text{Carry In} (Q_1Q_2Q_3Q_4\ \text{UP} + \overline{Q}_1\overline{Q}_2\overline{Q}_3\overline{Q}_4\ \overline{\text{DOWN}}$

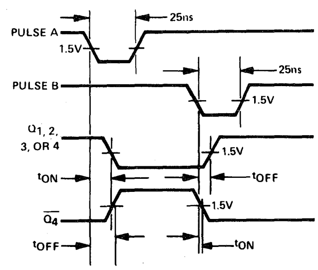
$\text{Carry Out}_{8285} = \text{Carry In} (Q_1Q_4\ \text{UP} + \overline{Q}_1\overline{Q}_2\overline{Q}_4\ \overline{\text{DOWN}}$

LOGIC

AC TEST FIGURES AND WAVEFORMS

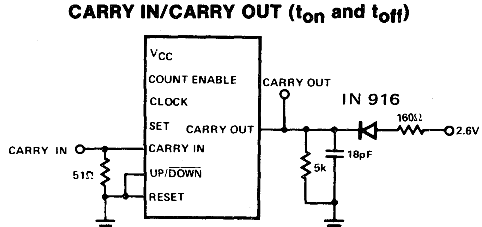
SET/RESET MODE (t_{on} and t_{off})

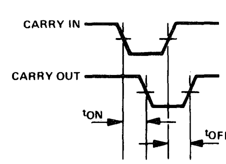




Pulse A and B
Pulse amplitude = 2.6V
Pulse Width (0) = 25ns
Frequency = 5MHz
tr = Tf = 5ns at 10% to 90% points

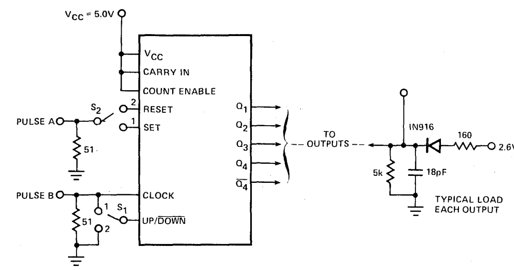
CARRY IN/CARRY OUT (t_{on} and t_{off})



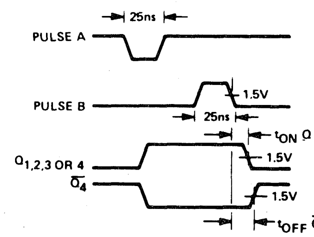


Carry in pulse
Pulse amplitude = 2.6V
Pulse width (0) = 50ns
Frequency = 10MHz
tr = tf = 5ns at 10% to 90% points

CLOCK MODE (t_{on} AND t_{off})

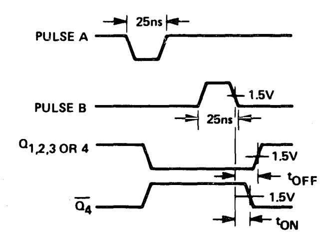


NOTE: ALL RESISTORS VALUES ARE TYPICAL AND IN OHMS.



Reset Tied To V_{CC}
S_1' Position 1
S_2' Position 1

PULSE A
Pulse amplitude = 2.0V
Pulse width $_{(0)}$ = 25ns at 1.5V
Frequency = 5MHz
$t_r = t_f$ = 5ns at 10%
to 90% points



Set Tied to V_{CC}
S_1' Position 2
S_2' Position 2

PULSE B
Pulse amplitude = 2.0V
Pulse Width = 25ns at 1.5V
Frequency = 5 MHz
$t_r = t_f$ = 5ns at 10%
to 90% points

8288-A,F,W

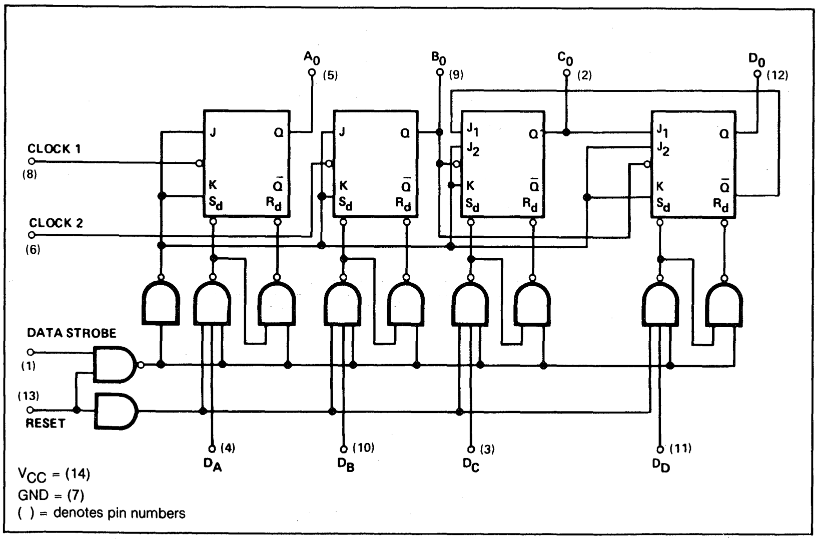
DESCRIPTION

The 8288 Divide by Twelve Counter is a four-bit subsystem consisting of divide by two and divide by six counters in a 14 pin package. For Divide-by-Twelve operation, output A is connected externally to the clock 2 input.

The 8288 has strobed paralleled data entry capability so that the counter may be preset to any desired output state. A "1" or "0" at a data input will be transferred to the associated output when the strobe input is put at a "0" level. For additional flexibility, the 8288 is provided with a common reset. A "0" on the reset line produces "0" at all four outputs.

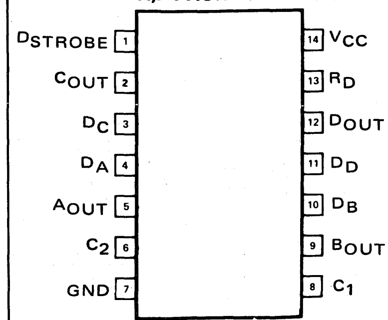
The counting operation is performed on the falling (negative going) edge of the input clock pulse, however, there is no restriction on transition time since the individual binaries are level sensitive. The data strobe and reset functions are asynchronous with respect to the clock.

LOGIC DIAGRAM

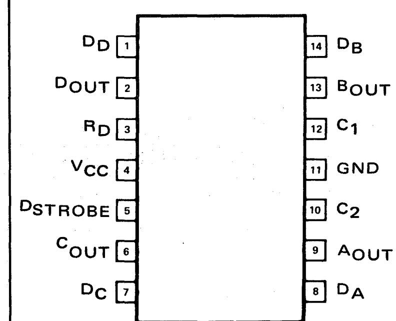


PIN CONFIGURATION

A,F PACKAGE



W PACKAGE



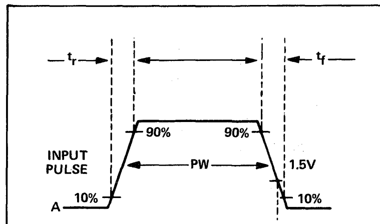
TRUTH TABLE

	OUTPUT			
Count	D	C	B	A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1

SWITCHING CHARACTERISTICS $T_A=25°C$, $V_{CC}=5V$

PARAMETER		TEST CONDITIONS	LIMITS MIN	TYP	MAX	UNIT
t_{on}	Turn-on delay time					
	Clock mode	Bit A,B,C,D		15	25	ns
	Data/strobe			20	35	
t_{off}	Turn-off time					
	Clock mode	Bit A,B,C,D		15	25	ns
	Data/strobe			25	40	
Toggle rate			20	25		MHz
t_{hold}	Hold time	V_{IN} = 0.8V:Reset=2V:				
	Strobe	Clock 1 = 2V: Clock 2 = Output A		25	35	ns
	Reset	Data strobe = 2V: V_{IN} = 0.8V:		20	35	
		Clock 1 = 2V: Clock 2 = Output A				
$t_{release}$	Release time			30	40	ns
	Strobe					
	Reset			50	75	

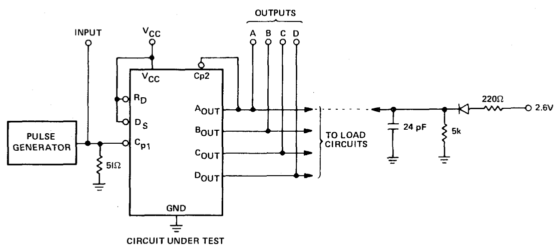
AC WAVEFORMS

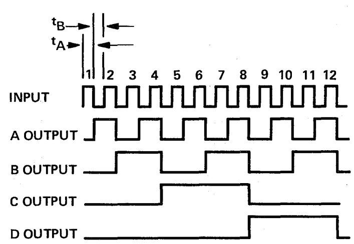


NOTE:
Input pulse notations apply unless otherwise specified.

AC TEST FIGURES AND WAVEFORMS

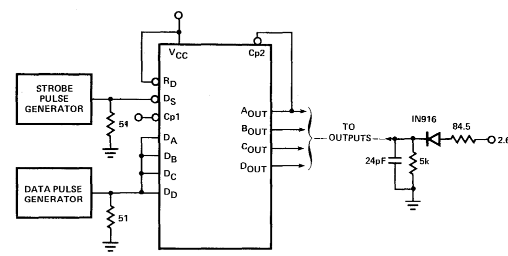
TOGGLE RATE

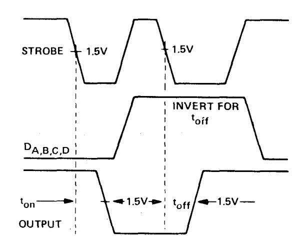




Input pulse
Amplitude = 3.4V
t_A = 100ns
t_r = 20ns
t_B = 300ns

DATA/STROBE t_{on} t_{off}

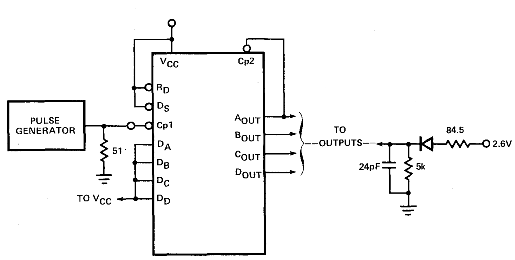


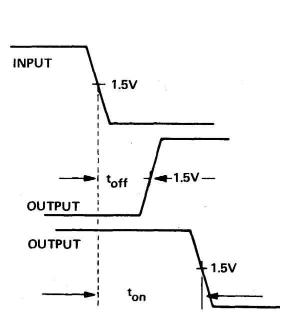


Input Pulse
Amplitude = 2.6V
t_r = t_f = 5ns

CLOCK MODE t_{on}/t_{off} DELAY

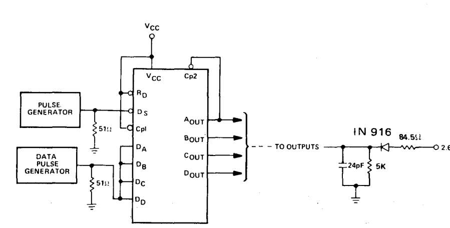
1. t_{on} and t_{off} are measured from the clock input of each binary to the Q output of that binary.
2. Each Q output will be loaded with the following load circuit:

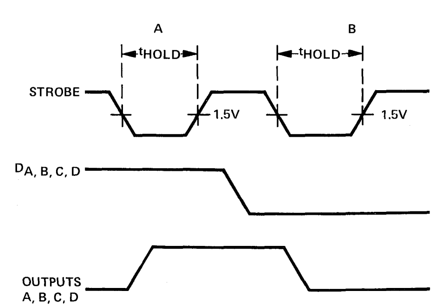




Input pulse:
Amplitude = 2.6V
P.W. = 30ns
t_r = t_f = 5ns

STROBE HOLD TIME



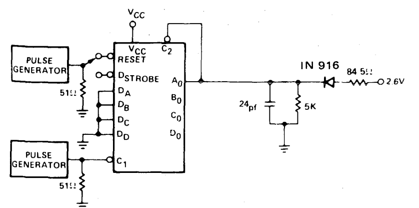


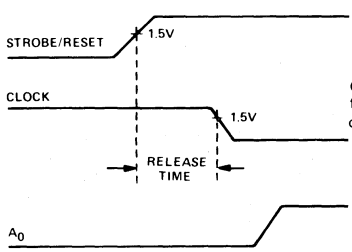
Input pulse
Amplitude=2.6V
t_r=t_f=5ns

NOTES:
1. All resistor values are in ohms.
2. All capacitance values are in picofarads and include jig and probe capacitance.

AC TEST FIGURES AND WAVEFORMS (CONT'D)

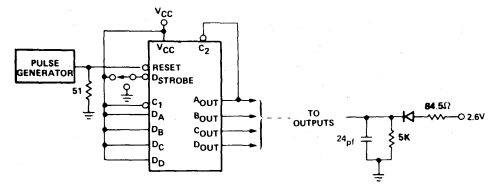
STROBE/RESET RELEASE TIME

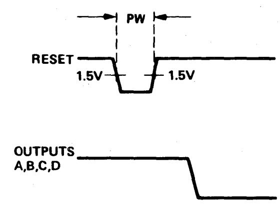




Clock, strobe/reset amplitude = 2.6V $t_r = t_f$ = 5ns max. PRR = 1MHz 50% duty cycle.

MINIMUM RESET PULSE WIDTH





Input pulse:
Amplitude = 2.6V
$t_r = t_f$ = 5ns max.
Note: outputs must be previously brought high by placing a "0" on the D strobe input. A pulse generator may be substituted for the switch.

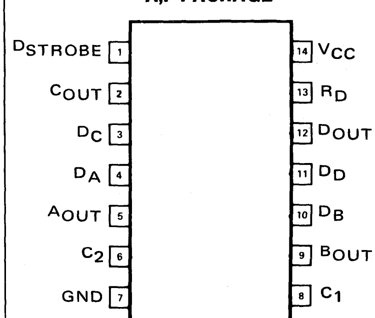
PRESETTABLE HIGH SPEED DECADE/BINARY COUNTER 8290/91

SPEED/PACKAGE AVAILABILITY

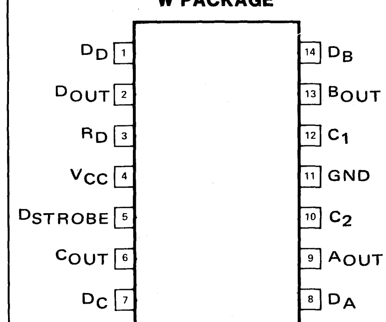
8290, 8291 A,F,W
82S90, 82S91 A,F

PIN CONFIGURATION

8290/91 82S90/82S91
A,F PACKAGE



8290/91
W PACKAGE



PIN DESIGNATIONS

CP1	Clock input to counter first stage (active low going edge)
CP2	Clock input to counter last three stages (active low going edge)
DS	Data Strobe Input for enabling data entry (active low)
RS	Reset Input for resetting all stages and outputs to zero (active low)
DA, DB, DC, DD	Data Inputs
AO, BO, CO, DO	Data Outputs

LOGIC

8290-A,F,W • 8291-A,F,W

DESCRIPTION

The 8290 Decade Counter and 8291 Binary Counter are high speed devices providing a wide variety of counter/storage register applications with a minimum number of packages.

The 8290 Decade Counter can be connected in the familiar BCD counting mode, in a divide-by-two and divide-by-five configuration or in the Bi-Quinary mode. The Bi-Quinary mode produces a square wave output which is particularly useful in frequency synthesizer applications.

The 8291 Binary Counter may be connected as a divide-by-two, four, eight, or sixteen counter.

Both devices have strobed parallel-entry capability so that the counter may be set to any desired output state. A "1" or "0" at a data input will be transferred to the associated output when the strobe input is put at the "0" level. For additional flexibility, both units are provided with a reset input which is common to all four bits. A "0" on the reset lines produces "0" at all four outputs.

The counting operation is performed on the falling (negative going) edge of the input clock pulse.

Triggering requirements are compatible with any of the 8000 Series elements.

FUNCTIONAL DESCRIPTION

1. 82S90 Decade Counter

The 82S90 can be used in three basic modes as follows:

a. BCD Counter. The CP2 input must be connected to the AO output and CP1 receives the count input. The count sequence obtained is BCD in accordance with the truth table.

b. Bi-Quinary Counter. If a symmetrical output is required for divide by 10 operation, the DO output must be connected to the CP1 input and the count input applied to CP2. A symmetrical square wave is then obtained at AO of one-tenth the input frequency present at CP2 in accordance with the truth table.

c. Separate Divide by Two and Five Counters. Because the inherent structure of the counter is that of two separate divide by two and divide by five sections, no other connections are required for this mode of operation. An input presented to CP1 will appear at AO output at half the input frequency. An input presented to CP2 will appear at outputs BO, CO and DO as a binary divide by five count (i.e., from 0 = 000 to 4 = 100). Operation of the DS and RS inputs remain common to all four flip flops as with any other count mode.

2. 82S91 Binary Counter

The 82S90 can be used in two basic count modes as follows:

a. Binary Counter—For this mode of operation AO output must be connected to CP2 input and the count input connected to CP1. Subdivisions of the count input frequency then appear at AO = —2, BO = —4, CO = —8, DO = —16 as shown in the truth table.

b. Separate Divide by Two and Divide by Eight Counters—In similar manner to the 82S90 the 82S91 inherent structure allows separate use of the first and last three stages. In the first stage the input count frequency presented to CP2 appears at outputs BO = —2, CO = —4 and DO = —8 simultaneously. Operation of the DS and RS inputs remains common to all stages.

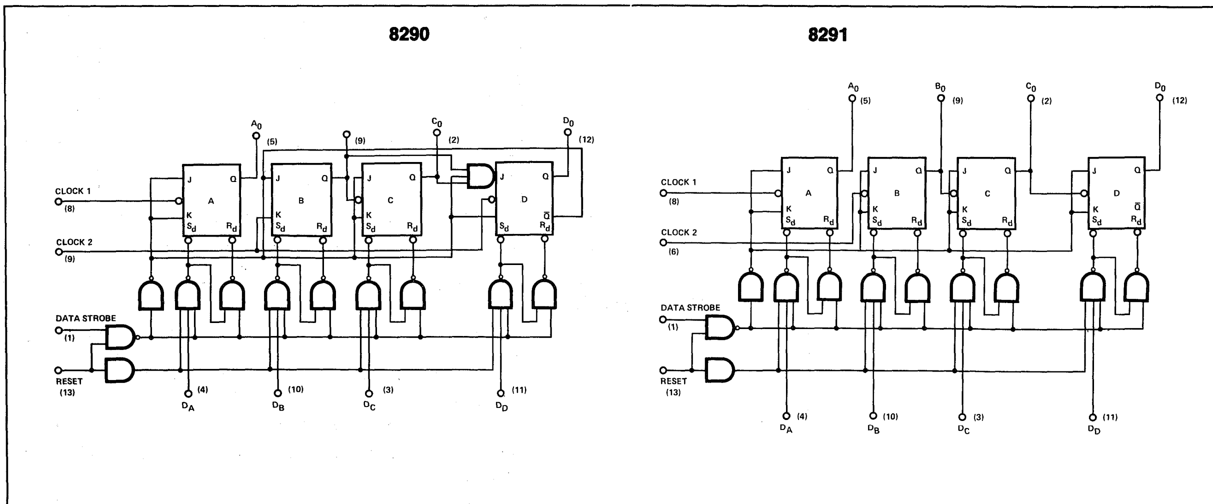
3. Operation of the DS Data Strobe and RS Reset Inputs:

a. Data Strobe DS Input When DS = 0 the four stages of the 82S90/91 can be used as four separate latches with the outputs AO - DO following the data presented to the inputs DA - DD regardless of clock inputs.

With DS = 1 the four stages remain unchanged until the next clock inputs, which activate counting in accordance with the various modes described previously. The Reset RS inputs when low overrides DS as described below.

b. Reset RS Input With RS = 0 the clock inputs CP1/CP2 and DS input are overriden, all stages of the 82S90/91 are cleared and zeros appear at the counter outputs AO - DO. When RS = 1, operation is controlled by DS or DP1/CP2 clock inputs as described.

LOGIC DIAGRAM



V_{CC} = (14)
GND = (7)
( ) = denotes pin numbers

TRUTH TABLE

	8290								8291			
BI-QUINARY(5-2)					DECADE (BCD)				BINARY			
INPUT	B_O	C_O	D_O	D_O	A_O	B_O	C_O	D_O	A_O	B_O	C_O	D_O
0	0	0	0	0	0	0	0	0	0	0	0	0
1	1	0	0	0	1	0	0	0	1	0	0	0
2	0	1	0	0	0	1	0	0	0	1	0	0
3	1	1	0	0	1	1	0	0	1	1	0	0
4	0	0	1	0	0	0	1	0	0	0	1	0
5	0	0	0	1	1	0	1	0	1	0	1	0
6	1	0	0	1	0	1	1	0	0	1	1	0
7	0	1	0	1	1	1	1	0	1	1	1	0
8	1	1	0	0	0	0	0	1	0	0	0	1
9	0	0	1	1	1	0	0	1	1	0	0	1
10									0	1	0	1
11									1	1	0	1
12									0	0	1	1
13									1	0	1	1
14									0	1	1	1
15									1	1	1	1

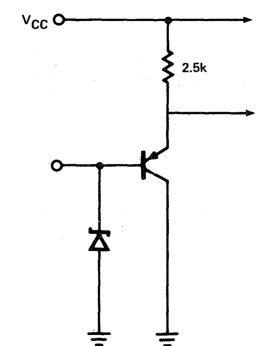
SWITCHING CHARACTERISTICS $T_A = 25°C$, $V_{CC} = 5V$

PARAMETER		TEST CONDITION	8290/8291 MIN	TYP	MAX	82S90/82S91 MIN	TYP	MAX	UNIT
Propagation delay time									
t_{on}	Turn-on time								
	Clock mode	Bit A		12	25		9	12	ns
		Bits B,C,D		15	30		10	13	
	Strobed data	All Bits		31	42		15	22	ns
t_{off}	Turn-off time								
	Clock mode	Bit A		12	23		5	8	ns
		Bits B,C,D		15	25		6	10	
	Strobed data	All Bits		33	42		13	20	ns
t_w	Input pulse width								
	Strobe			15	25		5	10	ns
	Reset	Clock 2 = A_{out}		25	40		7	15	ns
$t_{release}$	Release time								
	Strobe/reset	Clock 2 = A_{out}		20	30		10	15	ns
Toggle rate			40	60					MHz
Switching test									
	Clock mode[1]				75				ns

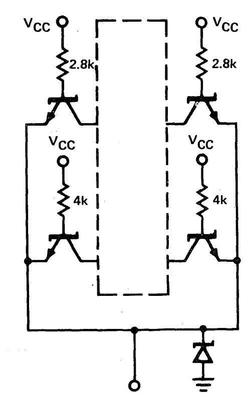
NOTES:
1. This test guarantees the device will reliably trigger on a pulse with 75ns fall-time.

INPUT AND OUTPUT STRUCTURES

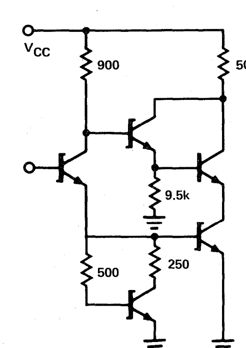
82S90,82S91
DATA, STROBE and RESET INPUTS



82S90,82S91
CLOCK INPUTS



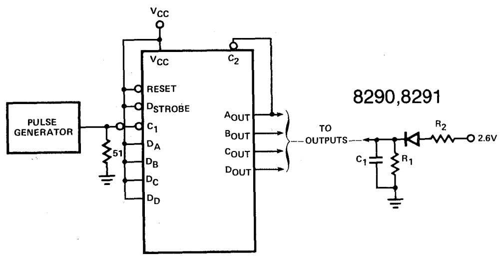
82S90,82S91
OUTPUTS



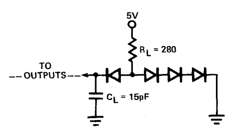
LOGIC

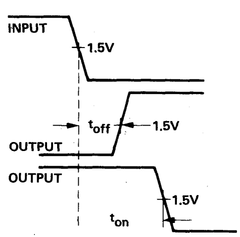
AC TEST FIGURES AND WAVEFORMS

CLOCK MODE t_{on}/t_{off} DELAY



8290,82S91

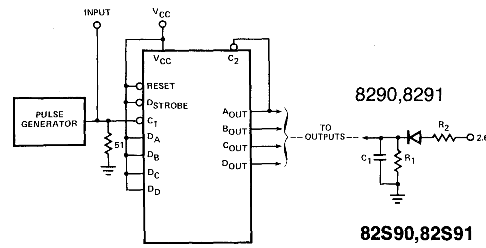




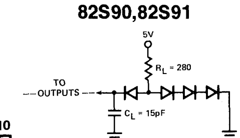
Note:
t_{on} and t_{off} are measured from the clock input of each binary to the O output of that binary.

Input pulse:
Amplitude = 2.6V
PW = 30ns, 50% to 50%
$t_r = t_f = 5ns$
PRR = 1MHz

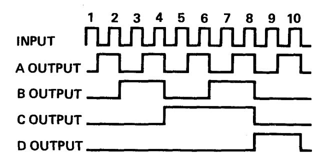
TOGGLE RATE



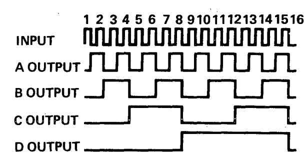
82S90,82S91



8290/82S91

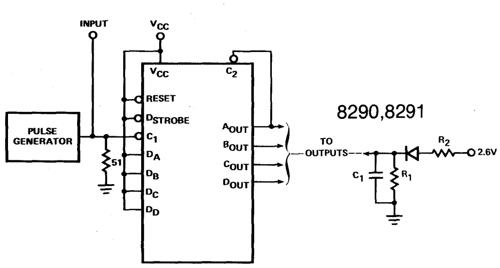


8291,82S91

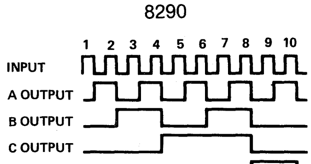


Input pulse:
Amplitude = 2.6V
$t_r = t_f$ = 5ns max.
PRR = 40 MHz, 50% duty cycle.

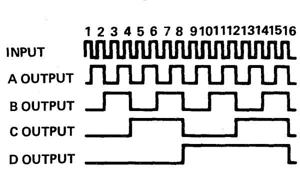
CLOCK MODE SWITCHING TEST



8290

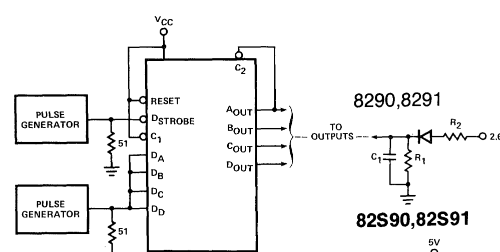


8291

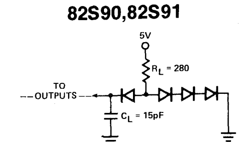


Input pulse:
Amplitude = 3.4V
PW = 100ns, 50% to 50%
PRR = 2.5MHz
t_r = 20ns, t_f = 75ns

STROBED DATA t_{on}/t_{off} DELAY

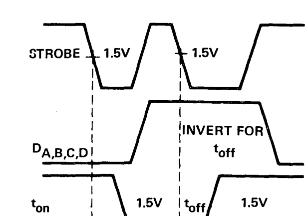


82S90,82S91



LOAD CIRCUIT 1

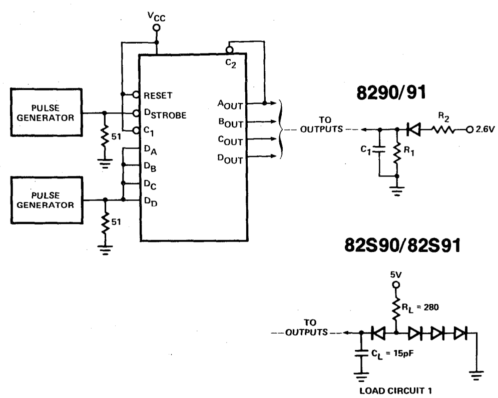
Strobe,
PA = 2.6V
PW = 300ns, 50% to 50%
PRR = 1MHz
$t_r = t_f$ = 5ns

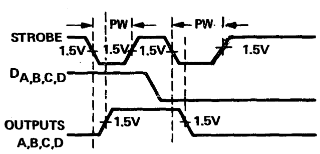


Data,
PA = 2.6V
PW = 500ns, 50% to 50%
PRR = 500kHz
$t_r = t_f$ = 5ns

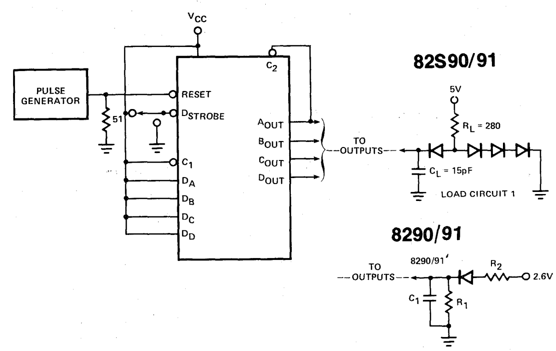
AC TEST FIGURE AND WAVEFORMS (CONT'D.)

MINIMUM STROBE PULSE WIDTH





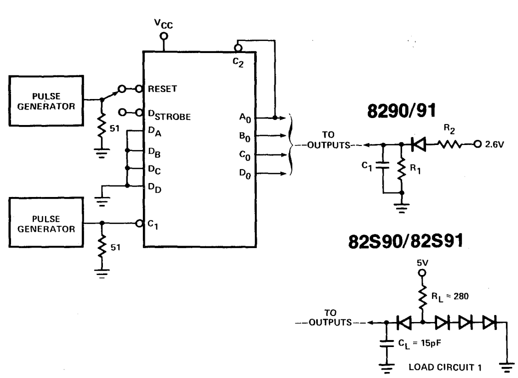
Input pulse:
Amplitude = 2.6V
$t_r = t_f = 5ns$

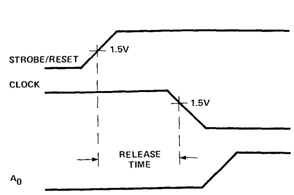


INPUT PULSE: Amplitude = 2.6V $t_r = t_f = 5ns$.

Note: Outputs must be previously brought high by placing a "0" on the D strobe input. A pulse generator may be substituted for the switch.

STROBE/RESET RELEASE TIME





CLOCK, STROBE/RESET:
AMPLITUDE = 2.6V
PRR = 1MHz, 50% DUTY CYCLE
$t_r = t_f = 5$ ns MAX.

NOTES
1. All resistor values are in ohms.
2. All capacitance values are in picofarads and include jig and probe capacitance.
3. All diodes are 1N916.
4. R1 = 20k, R2 = 146Ω, C1 = 30pF.

LOGIC

PRESETTABLE LOW POWER DECADE/BINARY COUNTER — 8292/93

8292-A,F,W•8293-A,F,W

DESCRIPTION

The 8292 Decade Counter and 8293 Binary Counter are low power devices providing a wide variety of counter/storage register applications with a minimum number of packages.

The 8292 Decade Counter can be connected in the familiar BCD counting mode, in a divide-by-two and divide-by-five configuration or in the Bi-Quinary mode. The Bi-Quinary mode produces a square wave output which is particularly useful in frequency synthesizer applications.

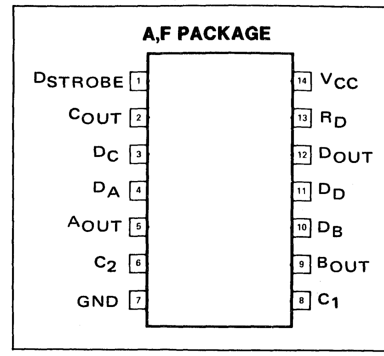
The 8293 Binary Counter may be connected as a divide-by-two, four, eight, or sixteen counter.

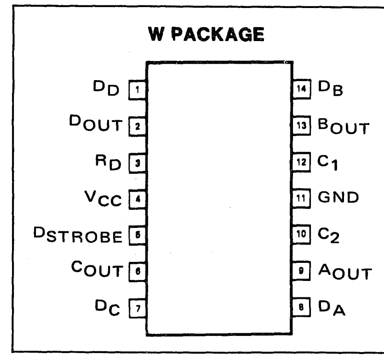
Both devices have strobed parallel-entry capability so that the counter may be set to any desired output state, A "1" or "0" at a data input will be transferred to the associated output when the strobe input is put at the "0" level. For additional flexibility, both units are provided with a reset input which is common to all four bits. A "0" on the reset line produces "0" at all four outputs.

The counting operation is performed on the falling (negative-going) edge of the input clock pulse.

Triggering requirements are compatible with any of the 8000 Series elements.

PIN CONFIGURATION





TRUTH TABLE

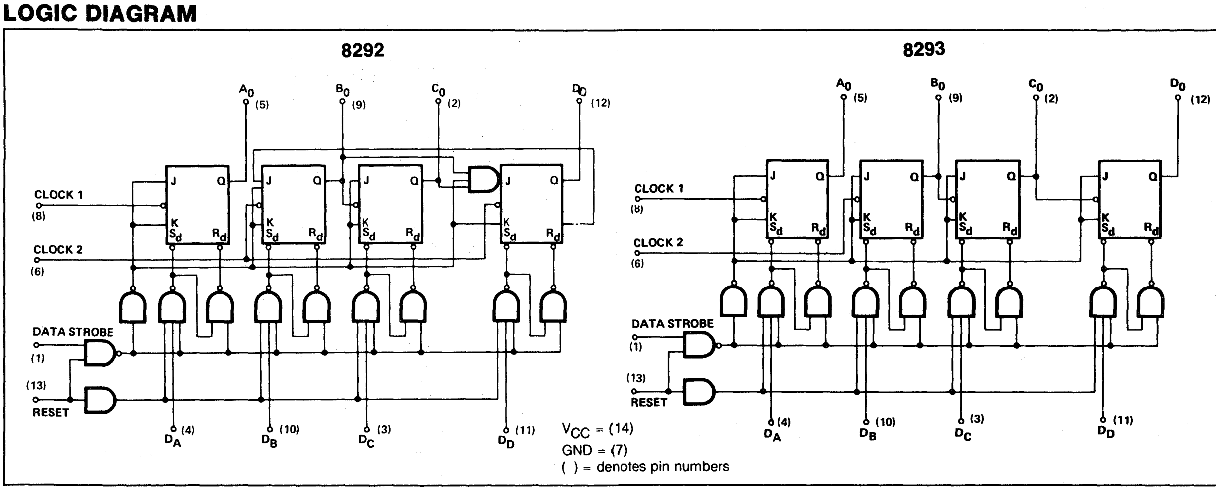
8292									8293			
BI QUINARY (5-2)					DECADE(BCD)				BINARY			
Input	B_0	C_0	D_0	A_0	A_0	B_0	C_0	D_0	A_0	B_0	C_0	D_0
0	0	0	0	0	0	0	0	0	0	0	0	0
1	1	0	0	0	1	0	0	0	1	0	0	0
2	0	1	0	0	0	1	0	0	0	1	0	0
3	1	1	0	0	1	1	0	0	1	1	0	0
4	0	0	1	0	0	0	1	0	0	0	1	0
5	0	0	0	1	1	0	1	0	1	0	1	0
6	1	0	0	1	0	1	1	0	0	1	1	0
7	0	1	0	1	1	1	1	0	1	1	1	0
8	1	1	0	1	0	0	0	1	0	0	0	1
9	0	0	1	1	1	0	0	1	1	0	0	1
10									0	1	0	1
11									1	1	0	1
12									0	0	1	1
13									1	0	1	1
14									0	1	1	1
15									1	1	1	1

SWITCHING CHARACTERISTICS $T_A = 25°C$, $V_{CC} = 5V$

PARAMETER		TEST CONDITIONS	LIMITS MIN	TYP	MAX	UNIT
Propagation delay time						
t_{on}	Turn-on time					
	Clock mode	All bits		37	55	ns
	Strobed data			80	100	
t_{off}	Turn-off time					
	Clock mode	All bits		32	55	ns
	Strobed data			80	100	
t_W	Input pulse width	V_{IN} = 0.8V: reset, clock 1 = 2V: clock 2 = A_{out}		60	75	ns
	Strobe					
	Reset	V_{in}, reset clock 1 = 2V: clock 2 = A_{out}		45	60	
$t_{release}$	Release time					
	Strobe/reset	clock 2 = A_{out}		80		
Toggle rate			5	10		MHz

NOTES:
1. This test guarantees the device will reliably trigger on a pulse with 75ns fall-time.

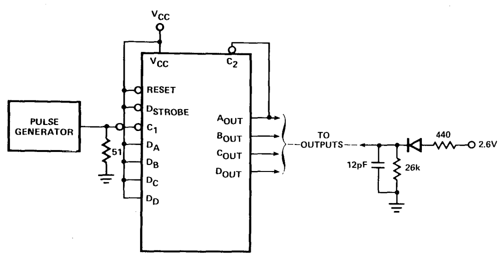
LOGIC DIAGRAM

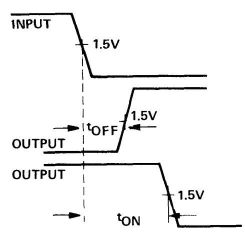


LOGIC

AC TEST FIGURES AND WAVEFORMS

CLOCK MODE t_{on}/t_{off} DELAY

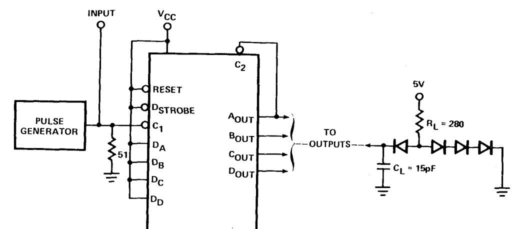




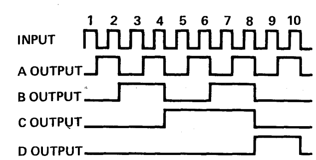
Input pulse:
Amplitude = 2.6V
P.W. = 30ns, 50% to 50%
$t_r = t_f$ = 5ns
PRR = 1MHz

NOTE:
1. t_{on} and t_{off} are measured from the clock input of each binary to the Q output of that binary.

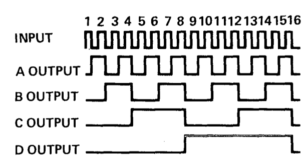
CLOCK MODE SWITCHING TEST



8292

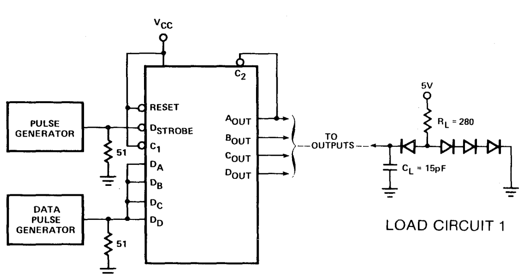


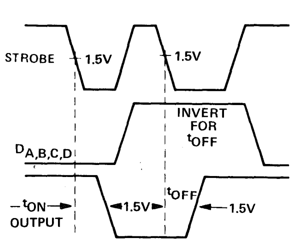
8293



Input pulse:
Amplitude = 3.4V
P.W. = 100ns, 50% to 50%
PRR = 2.5MHz
t_r = 20ns
t_f = 75ns

STROBED DATA t_{on}/t_{off} DELAY

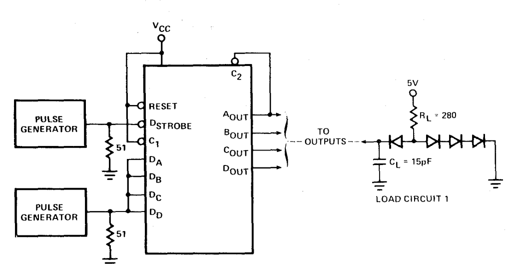


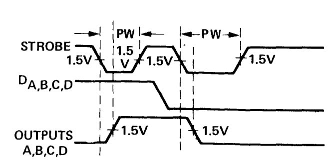


Strobe,
P.A. = 2.6V
P.W. = 300ns, 50% to 50%
PRR = 1MHz
$t_r = t_f$ = 5ns

Data,
P.A. = 2.6V
P.W. = 500ns, 50% to 50%
PRR = 500KHz
$t_r = t_f$ = 5ns

MINIMUM STROBE PULSE WIDTH

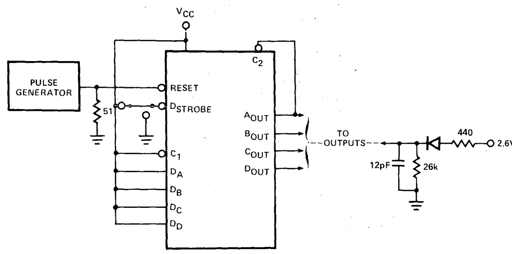


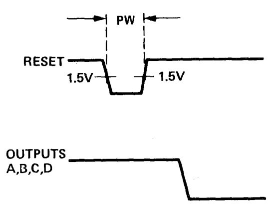


Input pulse:
Amplitude = 2.6V
$t_r = t_f$ = 5ns max.

AC TEST FIGURES AND WAVEFORMS (CONT'D.)

MINIMUM RESET PULSE WIDTH

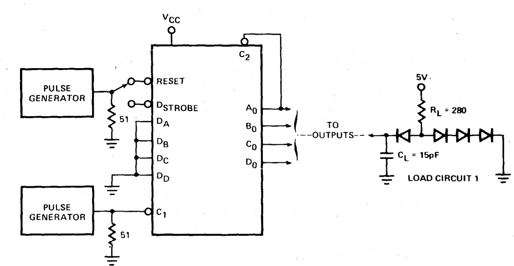


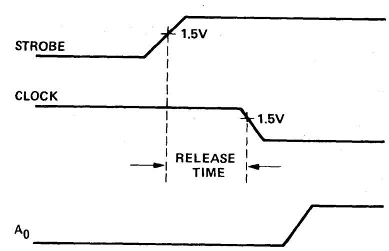


Input pulse:
Amplitude 2.6V
$t_r = t_f$ = 5ns max.

NOTE: outputs must be previously brought high by placing a "Q" on the D strobe light. A pulse generator may be substituted for the switch.

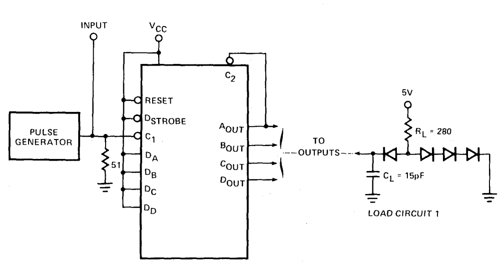
STROBE/RESET RELEASE TIME



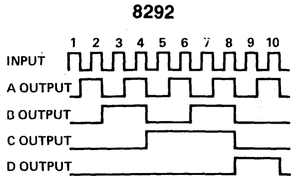


Clock, strobe/reset:
Amplitude = 2.6V
PRR = 1MHz, 50% duty cycle
$t_r = t_f$ = 5ns max.

TOGGLE RATE

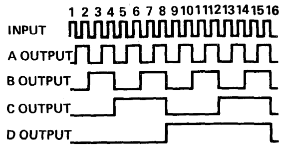


8292



Input pulse:
Amplitude = 2.6V
PRR = 5MHz, 50% duty cycle
$t_r = t_f$ = 5ns max.

8293



NOTES:
1. All resistor values are in ohms.
2. All capacitance values are in picofarads and include jig and probe capacitance.
3. All diodes are 1N916.

DESCRIPTION

The 10,000 series of monolithic integrated logic circuits presents the system designer with an integrated circuit family designed to permit system implementation with a relatively small number of individual types. This approach offers cost savings, reduced power supply requirements, small physical size and high reliability.

ECL II circuits feature very fast propagation times relative to rise and fall times. This and the constant current feature impose fewer restrictions on system design, layout and fabrication than other high-speed families.

FEATURES

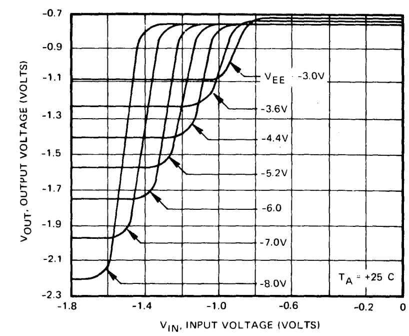
- **Full replacements for Motorola 10,000 series parts**
- **Excellent noise immunity**
- **Simultaneous OR/NOR outputs**
- **High fan-in and fan-out**
- **Internal temperature compensation**

DEFINITIONS

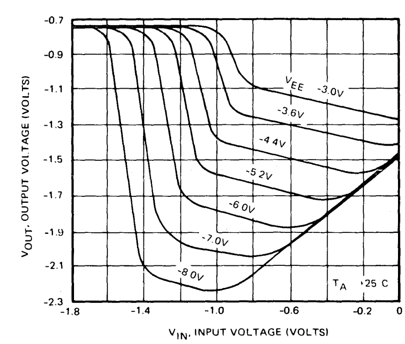
I_{in}	Current drawn by the input of the test unit when a maximum logic "1" ($V_{IH\ max}$) is applied at that input
I_{out}	Output current
I_R	Reverse current drawn from a transistor input of the test unit when V_{EE} is applied at that input
V_{BB}	Bias reference supply voltage (-1.29 V nominal at 25°C)
V_{BE}	Base-to-emitter voltage drop of a transistor
V_{CB}	Collector-to-base voltage drop of a transistor
V_{CC}	Most positive power supply voltage for a circuit
V_{EE}	Most negative power supply voltage for a circuit
V_{in}	Input voltage
$V_{IH\ max}$	Maximum input logic "1" level voltage
$V_{IH\ min}$	Minimum input logic "1" level (threshold) voltage
$V_{IL\ max}$	Maximum input logic "0" level (threshold) voltage
$V_{IL\ min}$	Minimum input logic "0" level voltage
$V_{OH\ max}$	Maximum output "1" or high-level voltage
$V_{OH\ min}$	Minimum output "1" high-level voltage
$V_{OL\ max}$	Maximum output "0" or low-level voltage
$V_{OL\ min}$	Minimum output "0" or low-level voltage
V_{out}	Output voltage

TYPICAL CHARACTERISTIC CURVES

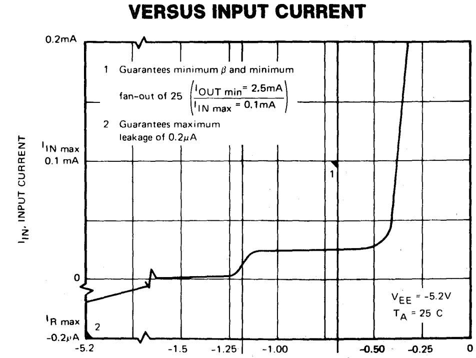
TYPICAL "OR" TRANSFER CHARACTERISTICS

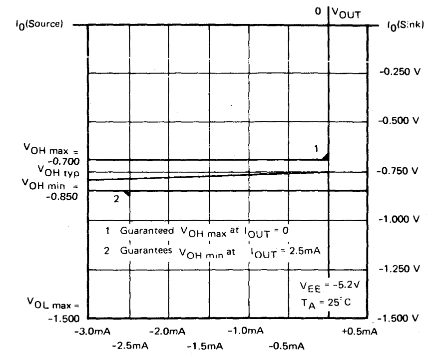


TYPICAL "NOR" TRANSFER CHARACTERISTICS



TYPICAL INPUT VOLTAGE VERSUS INPUT CURRENT





25°C LOGIC LEVELS

General Conditions: V_{EE} = -5.2V, V_{CC} = Gnd

INPUTS	OUTPUTS	10,100 10,200	10,500 10,600
V_{IL} min		-1.850	-1.850
V_{IH} max		-0.810	-0.720
	V_{OL} min	-1.850	-1.850
	V_{OL} max	-1.650	-1.620
	V_{OH} min	-0.960	-0.930
	V_{OH} max	-0.980	-0.950
V_{ILA} max		-1.475	-1.475
V_{IHA} min		-1.105	-1.105
	V_{OLA} max	-1.630	-1.600
	V_{OHA} min	-0.980	-0.950
With suitable inputs:			
Typical Output HIGH State		-0.900	-0.825
Typical Output LOW State		-1.750	-1.725
Typical V_{BB} (Switching Threshold)		-1.290	-1.290

Stabilized temperature, with ≥ 500 ifpm air flow.
DIL package outputs terminated through 50Ω resistor to -2.0V.

TEMPERATURE LOGIC LEVELS

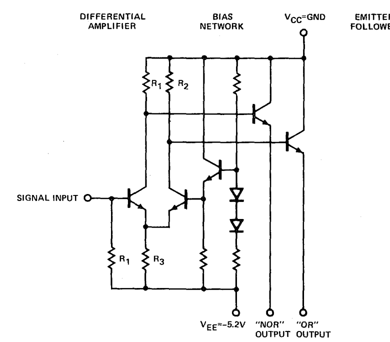
PARAMETER	-30°C	+85°C
V_{IH} max, V_{OH} max	-0.890	-0.700
V_{OH} min	-1.060	-0.890
V_{OHA} min	-1.080	-0.910
V_{IHA} min	-1.205	-1.035
V_{ILA} max	-1.500	-1.440
V_{OLA} max	-1.655	-1.595
V_{OL} max	-1.675	-1.615
V_{IL} min, V_{OL} min	-1.890	-1.825

*Outputs loaded 50Ω to -2.0V

MAXIMUM RATINGS

	PARAMETER	RATING	UNIT
Ratings above which device life may be impaired			
V_{EE}	Power Supply Voltage (V_{CC}=0)	-8	V_{DC}
V_{IN}	Input Voltage (V_{CC}=0)	0 to V_{EE}	V_{DC}
I_O	Output Source Current	0 to +20	mAdc
T_{stg}	Storage Temperature Range	-55 to +125	°C
Recommended maximum ratings above which performance may be degraded:			
T_A	Operating Temperature Range	-30 to+85	°C

BASIC ECL GATE CIRCUIT



Typical values:
Logical "1" = -0.9V
Logical "0" = -1.75V
For Logical "1" Input, "NOR" Output = -0.90V
"OR" Output = -1.75V
For Logical "0" Input, "NOR" Output = -1.75
"OR" Output = -0.90V

The 10,000 series line of monolithic integrated logic circuits was designed as a non-saturating form of logic which eliminates transistor storage time as a speed limiting characteristic.

The typical 10,000 series circuit comprises a differential-amplifier input with internal bias reference and with emitter-follower output to restore dc levels. High fan-out operation is possible because of high input impedance of the differential amplifier and low output impedance of the emitter followers. Power supply noise is virtually eliminated by the nearly constant current drain of the differential amplifier, even during transition time. Basic gate design provides for simultaneous output of both the function and its complement.

As shown in the schematic above, it is recommended that -5.2V be applied at V_{EE} with V_{CC} = Gnd.

The nominal output logic swing of 0.85V varies from a low state of V_L = -1.75V to a high state of V_H = -0.90V.

An internal voltage of -1.29V is applied to the "bias input" of the differential amplifier and the logic signals are applied to the "signal input". If a logical "0" is applied, the current through R_3 is supplied by the internally biased transistor. A drop of 0.85V occurs across R_2. The OR output then is -1.75V, one V_{BE} drop below 0..85V. Since no current flows in the "signal input transistor, the NOR output is a V_{BE} drop below ground, -0.90V. When a logical "1" level is applied to the "signal input", the current through R2 is switched to the "signal input" transistor and a drop of 0.85V occurs across R_1. The OR output then goes to -0.90V, and the NOR output goes to -1.75V.

NOTE: Unused inputs should be connected to V_{EE}.

The voltage applied to the bias input is obtained from an internal regulated, temperature-compensated bias network. The temperature characteristics of the bias network compensate for variations in circuit operating point over the temperature range or supply voltage changes, and insure that the threshold point is in the center of the transfer characteristic curves.

Test Temperature	Test Voltage Values (V) V_{IH} MAX	V_{IL} MIN	V_{IHA} MIN	V_{ILA} MAX	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

ECL DC ELECTRICAL CHARACTERISTICS - See Notes Page 12

	INPUT CURRENT									OUTPUT VOLTAGE											
PARAMETER	I_E (MA) SUPPLY CURRENT			I_{IL} (μA) LOW LEVEL			I_{IH} (μA) HIGH LEVEL			V_{OL} (V) LOW LEVEL			V_{OH} (V) HIGH LEVEL			V_{OLA} (V) THRESHOLD LOW LEVEL			V_{OHA} (V) THRESHOLD HIGH LEVEL		
TEST CONDITION*				$V_{IN}=V_{IL}$MIN			$V_{IH}=V_{IH}$ MAX			OUTPUT=50Ω LOAD TO-2V $V_{IN}=V_{IL}$MIN OR V_{IH}MAX			OUTPUT=50Ω LOAD TO-2V $V_{IN}=V_{IL}$MIN OR V_{IH} MAX			OUTPUT=50Ω LOAD TO-2V $V_{IN}=V_{ILA}$MAX OR V_{IHA} MIN			OUTPUT=50Ω LOAD TO-2V $V_{IH}=V_{ILA}$MIN OR V_{IHA}MIN		
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
10100																					
-30°C		N/A			N/A			N/A		-1.890		-1.675	-1.060		-0.890			-1.655	-1.080		
+25°C		20	26	0.5					245	-1.850		-1.650	-0.960		-0.810			-1.630	-0.980		
+85°C		N/A			N/A					-1.825		-1.615	-0.890		-0.700			-1.595	-0.910		
								Pin 9													
-30°C								N/A													
+25°C									470												
+85°C								N/A													
10101								Pin 4													
-30°C		N/A			N/A			N/A		-1.890		-1.675	-1.060		-0.890			-1.655	-1.080		
+25°C		20	26	0.5					265	-1.850		-1.650	-0.960		-0.810			-1.630	-0.980		
+85°C		N/A			N/A			N/A		-1.825		-1.615	-0.890		-0.700			-1.595	-0.910		
								Pin 12													
-30°C								N/A													
+25°C									535												
+85°C								N/A													
10102																					
-30°C		N/A			N/A			N/A		-1.890		-1.675	-1.060		-0.890			-1.655	-1.080		
+25°C		20	26	0.5					265	-1.850		-1.650	-0.960		-0.810			-1.630	-0.980		
+85°C		N/A			N/A			N/A		-1.825		-1.615	-0.890		-0.700			-1.595	-0.910		
10103																					
-30°C		N/A			N/A			N/A		-1.890		-1.675	-1.060		-0.890			-1.655	-1.080		
+25°C		20	26	0.5					245	-1.850		-1.650	-0.960		-0.810			-1.630	-0.980		
+85°C		N/A			N/A			N/A		-1.825		-1.615	-0.890		-0.700			-1.595	-0.910		
10104								Pin 12													
-30°C		N/A			N/A			N/A		-1.890		-1.675	-1.060		-0.890			-1.655	-1.080		
+25°C		28	35	0.5				265		-1.850		-1.650	-0.960		-0.810			-1.630	-0.980		
+85°C		N/A			N/A			N/A		-1.825		-1.615	-0.890		-0.700			-1.595	-0.910		
								Pin 13													
								N/A													
-30°C									220												
+25°C								N/A													
+85°C																					
10105																					
-30°C		N/A			N/A			N/A		-1.890		-1.675	-1.060		-0.890			-1.655	-1.080		
+25°C		15	21	0.5					265	-1.850		-1.650	-0.960		-0.810			-1.630	-0.980		
+85°C		N/A			N/A			N/A		-1.825		-1.615	-0.890		-0.700			-1.595	-0.910		
10106																					
-30°C		N/A			N/A			N/A		-1.890		-1.675	-1.060		-0.890			-1.655	-1.080		
+25°C		15	21	0.5					265	-1.860		-1.650	-0.960		-0.810			-1.630	-0.980		
+85°C		N/A			N/A			N/A		-1.825		-1.615	-0.890		-0.700			-1.595	-0.910		
10107									Pins 4,9,14												
-30°C		N/A			N/A			N/A		-1.890		-1.675	-1.060		-0.890			-1.655	-1.080		
+25°C			28	0.5					265	-1.850		-1.650	-0.960		-0.810			-1.630	-0.980		
+85°C		N/A			NA			N/A		-1.825		-1.615	-0.890		-0.700			-1.595	-0.910		
									Pins 5,7,15												
-30°C								N/A													
+25°C									220												
+85°C								N/A													

LOGIC

ECL DC ELECTRICAL CHARACTERISTICS — See Notes Page 12

	INPUT CURRENT									OUTPUT VOLTAGE											
PARAMETER	I_E (mA) SUPPLY CURRENT			I_{IL} (μA) LOW LEVEL			I_{IH} (μA) HIGH LEVEL			V_{OL} (V) LOW LEVEL			V_{OH} (V) HIGH LEVEL			V_{OLA} (V) THRESHOLD LOW LEVEL			V_{OHA} (V) THRESHOLD HIGH LEVEL		
TEST CONDITION*				$V_{IN}=V_{IL}$MIN			$V_{IH}=V_{IH}$ MAX			OUTPUT = 50Ω LOAD TO-2V $V_{IN}=V_{IL}$MIN OR V_{IH}MAX			OUTPUT = 50Ω LOAD TO-2V $V_{IN}=V_{IL}$MIN OR V_{IH} MAX			OUTPUT = 50Ω LOAD TO-2V $V_{IN}=V_{ILA}$MAX OR V_{IHA} MIN			OUTPUT = 50Ω LOAD TO-2V $V_{IH}=V_{ILA}$MIN OR V_{IHA}MIN		
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
10108										Pin 2											
-30°C		N/A			N/A			N/A		-2.000		-1.675	-1.060		-0.890			-1.655	-1.080		
+25°C		28	36	0.5					265	-1.990		-1.650	-0.960		-0.810			-1.630	-0.980		
+85°C		N/A		N/A			N/A		-1.920		-1.615	-0.890	-0.700					-1.595	-0.910		
										Pin 3											
-30°C										-1.890	-1.675										
+25°C										-1.850	-1.650										
+85°C										-1.825	-1.615										
10109																					
-30°C		N/A			N/A			N/A		-1.890		-1.675	-1.060		-0.890			-1.655	-1.080		
+25°C		10	14	0.5					265	-1.850		-1.650	-0.960		-0.810			-1.630	-0.980		
+85°C		N/A			N/A			N/A		-1.825		-1.615	-0.890		-0.700			-1.595	-0.910		
10110																					
-30°C		N/A			N/A			N/A		-1.890		-1.675	-1.060		-0.890			-1.655	-1.080		
+25°C		30	38	0.5					425	-1.850		-1.650	-0.960		-0.810			-1.630	-0.980		
+85°C		N/A			N/A			N/A		-1.825		-1.615	-0.890		-0.700			-1.595	-0.910		
10111																					
-30°C		N/A			N/A			N/A		-1.890		-1.675	-1.060		-0.890			-1.655	-1.080		
+25°C			38	0.5					425	-1.850		-1.650	-0.960		-0.810			-1.630	-0.980		
+85°C		N/A			N/A			N/A		-1.825		-1.615	-0.890		-0.700			-1.595	-0.910		
10112																					
-30°C		N/A			N/A			N/A		-1.890		-1.675	-1.060		-0.890			-1.655	-1.080		
+25°C				0.5					420	-1.850		-1.650	-0.960		-0.810			-1.630	-0.980		
+85°C		N/A			N/A			N/A		-1.825		-1.615	-0.890		-0.700			-1.595	-0.910		
10113								N/A													
-30°C		N/A			N/A		Pin 6		220	-1.890		-1.675	-1.060		-0.890			-1.655	-1.080		
+25°C			42	0.5			Pin 7		265	-1.850		-1.650	-0.960		-0.810			-1.630	-0.980		
+85°C		N/A			N/A			N/A		-1.825		-1.615	-0.890		-0.700			-1.595	-0.910		
								Pin 9													
								N/A													
									545												
								N/A													
10114																					
-30°C		N/A			N/A			N/A		-1.890		-1.675	-1.060		-0.890			-1.655	-1.080		
+25°C		28	35			*1.0			45	-1.850		-1.650	-0.960		-0.810			-1.630	-0.980		
+85°C		N/A						N/A		-1.825		-1.615	-0.890		-0.700			-1.595	-0.910		
10115																					
-30°C		N/A						N/A		-1.890		-1.675	-1.060		-0.890			-1.655	-1.080		
+25°C			26			*1.0			95	-1.850		-1.650	-0.960		-0.810			-1.630	-0.980		
+85°C		N/A						N/A		-1.825		-1.615	-0.890		-0.700			-1.595	-0.910		
10116																					
-30°C		N/A						N/A		-1.890		-1.675	-1.060		-0.890			-1.655	-1.080		
+25°C		16	21			*1.0			95	-1.850		-1.675	-1.060		-0.890			-1.655	-1.080		
+85°C		N/A						N/A		-1.825		-1.615	-0.890		-0.700			-1.595	-0.910		
10117								Pin 4													
-30°C		N/A			N/A			N/A		-1.890		-1.675	-1.060		-0.890			-1.655	-1.080		
+25°C		20	26	0.5					265	-1.850		-1.650	-1.650		-0.960			-1.630	-0.980		
+85°C		N/A			N/A			N/A		-1.825		-1.615	-0.890		-0.700			-1.595	-0.910		
								Pin 9													
								N/A													
									350												
								N/A													
10118								Pin 6,7													
-30°C		N/A			N/A			N/A		-1.890		-1.675	-1.060		-0,890			-1.655	-1.080		
+25°C		20	26	0.5					265	-1.850		-1.650	-0.960		-0.810			-1.630	-0.980		
+85°C		N/A			N/A			N/A		-1.825		-1.615	-0.890		-0.700			-1.595	-0.910		
								N/A													
									370												
								N/A													

*I_{CBO}

ECL DC ELECTRICAL CHARACTERISTICS — See Notes Page 12

	INPUT CURRENT									OUTPUT VOLTAGE											
PARAMETER	I_E (mA) SUPPLY CURRENT			I_{IL} (μA) LOW LEVEL			I_{IH} (μA) HIGH LEVEL			V_{OL} (V) LOW LEVEL			V_{OH} (V) HIGH LEVEL			V_{OLA} (V) THRESHOLD LOW LEVEL			V_{OHA} (V) THRESHOLD HIGH LEVEL		
TEST CONDITION*				$V_{IN}=V_{IL}$MIN			$V_{IH}=V_{IH}$ MAX			OUTPUT=50Ω LOAD TO-2V $V_{IN}=V_{IL}$MIN OR V_{IH}MAX			OUTPUT=50Ω LOAD TO-2V $V_{IN}=V_{IL}$MIN OR V_{IH} MAX			OUTPUT=50Ω LOAD TO-2V $V_{IN}=V_{ILA}$MAX OR V_{IHA} MIN			OUTPUT=50Ω LOAD TO-2V $V_{IH}=V_{ILA}$MIN OR V_{IHA}MIN		
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
10119								Pin 7,9													
-30°C		N/A			N/A			N/A		-1.890		-1.675	-1.060		-0.890			-1.655	-1.080		
+25°C		20	26	0.5					265	-1.850		-1.650	-0.960		-0.810			-1.630	-0.980		
+85°C		N/A			N/A			N/A		-1.825		-1.615	-0.890		-0.700			-1.595	-0.910		
								Pin 10													
								N/A													
									370												
								N/A													
10121								Pin 7,9													
-30°C		N/A			N/A			N/A		-1.890		-1.675	-1.060		-0.780			-1.655	-1.080		
+25°C		20	26	0.5					265	-1.850		-1.650	-0.960		-0.700			-1.630	-0.980		
+85°C		N/A			N/A			N/A		-1.825		-1.615	-0.890		-0.590			-1.595	-0.910		
								Pin 10													
								N/A													
									370												
								N/A													
											V_{IN}=4.0Vdc or 0.4Vdc			V_{IN}=0.4Vdc or 4.0Vdc			V_{IN}=1.8Vdc or 1.1Vdc			V_{IN}=1.8Vdc or 1.1Vdc	
10124																					
-30°C		N/A								-1.890		-1.675	-1.060		-0.890			-1.655	-1.080		
+25°C		-66			N/A			N/A		-1.850		-1.650	-0.960		-0.810			-1.630	-0.980		
+85°C		N/A								-1.825		-1.615	-0.890		-0.700			-1.595	-0.910		
10125																					
-30°C		N/A						N/A	14			0.5	2.5					0.5	2.5		
+25°C			40		N/A	*1.0			115			0.5	2.5					0.5	2.5		
+85°C		N/A						N/A				0.5	2.5					0.5	2.5		
10129		Pin 8, Pin 5=Gnd			Pin 4,6,7,13			Pin 4,6,7,13		-1.890		-1.675	-1.060		-0.890			-1.655	-1.080		
-30°C		N/A			N/A			N/A		-1.850		-1.650	-0.960		-0.810			-1.630	-0.980		
+25°C			152			-1.0			95	-1.825		-1.615	-0.890		-0.700			-1.595	-0.910		
+85°C		N/A			N/A			N/A													
		Pin 8, Pin 5=V_{EE}			Pin 10,11,12			Pin 10													
-30°C		N/A			N/A			N/A													
+25°C			172	0.5					450												
+85°C		N/A			N/A			N/A													
								Pin 11,12													
								N/A													
									245												
								N/A													
10130								Pin 6,11													
-30°C		N/A			N/A			N/A		-1.890		-1.675	-1.060		-0.890			-1.655	-1.080		
+25°C		28	35	0.5					220	-1.850		-1.650	0.960		-0.810			-1.630	-0.980		
+85°C		N/A			N/A		N/A			-1.825		-1.615	-0.890		-0.700			-1.595	-0.910		
							Pin 9														
								N/A													
									265												
								N/A													
								Pin 4,5,7													
								N/A													
									285												
								N/A													
10131								Pin 4,5			Note 2			Note 2			Note 2			Note 2	
-30°C		N/A			N/A			N/A		-1.890		-1.675	-1.060		-0.890			-1.655	-1.08		
+25°C		45	56	0.5					330	-1.850		-1.650	-0.960		-0.810			-1.630	-0.98		
+85°C		N/A			N/A			N/A		-1.825		-1.615	-0.890		-0.700			-1.595	-0.91		
							Pin 6														
								N/A													
									220												
								N/A													
							Pin 7														
								N/A													
									245												
								N/A													

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LOGIC

ECL DC ELECTRICAL CHARACTERISTICS — See Notes Page 12

	INPUT CURRENT									OUTPUT VOLTAGE											
PARAMETER	I_E (mA) SUPPLY CURRENT			I_{IL} (μA) LOW LEVEL			I_{IH} (μA) HIGH LEVEL			V_{OL} (V) LOW LEVEL			V_{OH} (V) HIGH LEVEL			V_{OLA} (V) THRESHOLD LOW LEVEL			V_{OHA} (V) THRESHOLD HIGH LEVEL		
TEST CONDITION*				$V_{IN}=V_{IL}$ MIN			$V_{IH}=V_{IH}$ MAX			OUTPUT = 50Ω LOAD TO-2V $V_{IN}=V_{IL}$ MIN OR V_{IH} MAX			OUTPUT = 50Ω LOAD TO-2V $V_{IN}=V_{IL}$ MIN OR V_{IH} MAX			OUTPUT = 50Ω LOAD TO-2V $V_{IN}=V_{ILA}$ MAX OR V_{IHA} MIN			OUTPUT = 50Ω LOAD TO-2V $V_{IH}=V_{ILA}$ MIN OR V_{IHA} MIN		
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
							Pin 9														
								N/A													
									265												
								N/A													
10132							Pin 4,5,7														
-30°C		N/A			N/A			N/A		-1.890		-1.675	-1.060		-0.890			-1.655	-1.08		
+25°C			55	0.5					290	-1.850		-1.650	-0.960		-0.810			-1.630	-0.98		
+85°C		N/A			N/A			N/A		-1.825		-1.615	-0.890		-0.700			-1.595	-0.91		
							Pin 6														
								N/A													
									390												
								N/A													
							Pin 10,11														
								N/A													
									220												
								N/A													
10133							Pin 3										Notes 5&6			Notes 5&6	
-30°C		N/A			N/A			N/A		-1.890		-1.675	-1.060		-0.890			-1.655	-1.08		
+25°C			75	0.5					245	-1.850		-1.650	-0.960		-0.810			-1.630	-0.98		
+85°C		N/A			N/A			N/A		-1.825		-1.615	-0.890		-0.700			-1.595	-0.91		
							Pin 4														
								N/A													
									220												
								N/A													
							Pin 5,13														
								N/A													
									350												
								N/A													
10134							Pin 4,5,7														
-30°C		N/A			N/A			N/A		-1.890		-1.675	-1.060		-0.890			-1.655	-1.08		
+25°C			55	0.5					290	-1.850		-1.650	-0.960		-0.810			-1.630	-0.98		
+85°C		N/A			N/A			N/A		-1.825		-1.615	-0.890		-0.700			-1.595	-0.91		
							Pin 6,10														
								N/A													
									265												
								N/A													
10135							Pin 6,7,9,10,11				Note 7			Note 7			Note 7			Note 7	
-30°C		N/A			N/A			N/A		-1.890		-1.675	-1.060		-0,890			-1.655	-1.08		
+25°C			68	0.5					265	-1.850		-1.650	-0.960		-0.810			-1.630	-0.98		
+85°C		N/A			N/A			N/A		-1.825		-1.615	-0.890		-0.700			-1.595	-0.91		
							Pin 4,5,12,13														
								N/A													
									390												
10136							Pin 5,6,11,12				Note 3			Note 3			Note 3			Note 3	
-30°C		N/A			N/A			N/A		-1.890		-1.675	-1.060		-0.890			-1.655	-1.080		
+25°C		120	150	0.5					220	-1.850		-1.650	-0.960		-0.810			-1.630	-0.980		
+85°C		N/A			N/A			N/A		-1.825		-1.615	-0.890		-0.700			-1.595	-0.910		
							Pin 7														
								N/A													
									265												
								N/A													
							Pin 9,10														
								N/A													
									245												
								N/A													
							Pin 13														
								N/A													
									290												
								N/A													

ECL PRODUCT INFORMATION

ECL DC ELECTRICAL CHARACTERISTICS — See Notes Page 12

	INPUT CURRENT									OUTPUT VOLTAGE											
PARAMETER	I_E (mA) SUPPLY CURRENT			I_{IL} (μA) LOW LEVEL			I_{IH} (μA) HIGH LEVEL			V_{OL} (V) LOW LEVEL			V_{OH} (V) HIGH LEVEL			V_{OLA} (V) THRESHOLD LOW LEVEL			V_{OHA} (V) THRESHOLD HIGH LEVEL		
TEST CONDITION*				$V_{IN}=V_{IL}$ MIN			$V_{IH}=V_{IH}$ MAX			OUTPUT=50Ω LOAD TO-2V $V_{IN}=V_{IL}$MIN OR V_{IH}MAX			OUTPUT=50Ω LOAD TO-2V $V_{IN}=V_{IL}$MIN OR V_{IH} MAX			OUTPUT=50Ω LOAD TO-2V $V_{IN}=V_{ILA}$MAX OR V_{IHA} MIN			OUTPUT=50Ω LOAD TO-2V $V_{IH}=V_{ILA}$MIN OR V_{IHA}MIN		
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
10137							Pin 5,6,11,12				Note 3			Note 3			Note 3			Note 3	
-30°C		N/A			N/A			N/A		-1.890		-1.675	-1.060		-0.890			-1.655	-1.080		
+25°C		120	150	0.,5					220	-1.850		-1.650	-0.960		-0.810			-1.630	-0.980		
+85°C		N/A			N/A			N/A		-1.825		-1.615	-0.890		-0.700			-1.595	-0.910		
							Pin 7														
								N/A													
									265												
								N/A													
							Pin 9,10														
								N/A													
									245												
								N/A													
							Pin 13														
								N/A													
									290												
								N/A													
10139																					
-30°C																					
+25°C	SEE BIPOLAR MEMORIES SECTION FOR ELECTRICAL SPECIFICATIONS																				
+85°C																					
10140																					
-30°C																					
+25°C	SEE BIPOLAR MEMORIES SECTION FOR ELECTRICAL SPECIFICATIONS																				
+85°C																					
10141							Pin 5,6														
-30°C		N/A			N/A			N/A		-1.890		-1.675	-1.060		-0.890			-1.655	-1.08		
+25°C		82	102	0.5					220	-1.850		-1.650	-0.960		-0.810			-1.630	-0.98		
+85°C		N/A			N/A			N/A		-1.825		-1.615	-0.890		-0.700			-1.595	-0.91		
							Pin 7														
								N/A													
									245												
								N/A													
							Pin 4														
									265												
								N/A													
10142																					
-30°C																					
+25°C	SEE BIPOLAR MEMORIES SECTION FOR ELECTRICAL SPECIFICATIONS																				
+85°C																					
10145							Pin 3,6,7,9,10														
-30°C		N/A			N/A			N/A		-1.890		-1.675	-1.060		-0.890			-1.675	-1.080		
+25°C		116	145	0.5					200	-1.850		-1.650	-0.960		-0.810			-1.630	-0.980		
+85°C		N/A			N/A			N/A		-1.825		-1.615	-0.890		-0.700			-1.595	-0.910		
							Pin 4,5,11,12														
								N/A													
									220												
								N/A													
							Pin 13														
								N/A													
									470												
								N/A													
10148																					
-30°C																					
+25°C	SEE BIPOLAR MEMORIES SECTION FOR ELECTRICAL SPECIFICATIONS																				
+85°C																					

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ECL PRODUCT INFORMATION

ECL DC ELECTRICAL CHARACTERISTICS

	INPUT CURRENT									OUTPUT VOLTAGE											
PARAMETER	I_E (mA) SUPPLY CURRENT			I_{IL} (μA) LOW LEVEL			I_{IH} (μA) HIGH LEVEL			V_{OL} (V) LOW LEVEL			V_{OH} (V) HIGH LEVEL			V_{OLA} (V) THRESHOLD LOW LEVEL			V_{OHA} (V) THRESHOLD HIGH LEVEL		
TEST CONDITION*				$V_{IN}=V_{IL}$ MIN			$V_{IH}=V_{IH}$ MAX			OUTPUT = 50Ω LOAD TO -2V $V_{IN}=V_{IL}$ MIN OR V_{IH} MAX			OUTPUT = 50Ω LOAD TO -2V $V_{IN}=V_{IL}$ MIN OR V_{IH} MAX			OUTPUT = 50Ω LOAD TO -2V $V_{IN}=V_{ILA}$ MAX OR V_{IHA} MIN			OUTPUT = 50Ω LOAD TO -2V $V_{IH}=V_{ILA}$ MIN OR V_{IHA} MIN		
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
10158							Pin 4,9														
-30°C		N/A			N/A			N/A		-1.890		-1.675	-1.060		-0.890			-1.655	-1.080		
+25°C		32	40	0.5					265	-1.850		-1.650	-0.960		-0.810			-1.630	-0.980		
+85°C		N/A			N/A			N/A		-1.825		-1.615	-0.890		-0.700			-1.595	-0.910		
							Pin 7														
								N/A													
									575												
								N/A													
10159							Pin 4,9														
-30°C		N/A			N/A			N/A		-1.890		-1.675	-1.060		-0,890			-1.655	-1.080		
+25°C		32	40	0.5					265	-1.850		-1.650	-0.960		-0.810			-1.630	-0.980		
+85°C		N/A			N/A			N/A		-1.825		-1.615	-0.890		-0.700			-1.595	-0.910		
							Pin 7														
								N.A													
									575												
								N/A													
10160							Pin 3														
-30°C		N/A			N/A			N/A		-1.890		-1.675	-1.060		-0.890			-1.675	-1.080		
+25°C		62	78	0.5					265	-1.850		-1.650	-0.960		-0.810			-1.630	-0.980		
+85°C		N/A			N/A			N/A		-1.825		-1.615	-0.890		-0.700			-1.595	-0.910		
							Pin 4														
								N/A													
									220												
								N/A													
10161																					
-30°C		N/A			N/A			N/A		-1.890		-1.675	-1.060		-0.890			-1.655	-1.080		
+25°C		57	76	0.5					220	-1.850		-1.650	-0.960		-0810			-1.630	-0.980		
+85°C		N/A			N/A			N/A		-1.825		-1.615	-0.890		-0.700			-1.595	-0.910		
10162																					
-30°C		N/A			N/A			N/A		-1.890		-1.675	-1.060		-0.890			-1.655	-1.080		
+25°C		57	76	0.5					220	-1.850		-1.650	-0.960		-0.810			-1.630	-0.980		
+85°C		N/A			N/A			N/A		-1.825		-1.615	-0.890		-0.700			-1.595	-0.910		
10164																					
-30°C		N/A			N/A			N/A		-1.890		-1.675	-1.060		-0.890			-1.675	-1.080		
+25°C		56	75	0.5					265	-1.850		-1.650	-0.960		-0.810			-1.630	-0.980		
+85°C		N/A			N/A			N/A		-1.825		-1.615	-0.890		-0.700			-1.595	-0.910		
10165							Pin 4														
-30°C		N/A			N/A			N/A		-1.890		-1.675	-1.060		-0.890			-1.655	-1.080		
+25°C		105	131	0.5					245	-1.850		-1.650	-0.960		-0.810			-1.630	-0.980		
+85°C		N/A			N/A			N/A		-1.825		-1.615	-0.890		-0.700			-1.595	-0.910		
							Pin 5														
								N/A													
									220												
								N/A													
10170																					
-30°C		N/A			N/A			N/A		-1.890		-1.675	-1.060		-0.890			-1.655	-1.080		
+25°C		54	68	0.5					265	-1.850		-1.650	-0.960		-0.810			-1.630	-0.980		
+85°C		N/A			N/A			N/A		-1.825		-1.615	-0.890		-0.700			-1.595	-0.910		

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ECL DC ELECTRICAL CHARACTERISTICS — See Notes Page 12

	INPUT CURRENT									OUTPUT VOLTAGE											
PARAMETER	I_E (mA) SUPPLY CURRENT			I_{IL} (µA) LOW LEVEL			I_{IH} (µA) HIGH LEVEL			V_{OL} (V) LOW LEVEL			V_{OH} (V) HIGH LEVEL			V_{OLA} (V) THRESHOLD LOW LEVEL			V_{OHA} (V) THRESHOLD HIGH LEVEL		
TEST CONDITION*				$V_{IN}=V_{IL}$MIN			$V_{IH}=V_{IH}$ MAX			OUTPUT=50Ω LOAD TO-2V $V_{IN}=V_{IL}$MIN OR V_{IH}MAX			OUTPUT=50Ω LOAD TO-2V $V_{IN}=V_{IL}$MIN OR V_{IH} MAX			OUTPUT=50Ω LOAD TO-2V $V_{IN}=V_{ILA}$MAX OR V_{IHA} MIN			OUTPUT=50Ω LOAD TO-2V $V_{IH}=V_{ILA}$MIN OR V_{IHA}MIN		
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
10171																					
-30°C		N/A			N/A			N/A		-1.890		-1.675	-1.060		-0.890			-1.655	-1.080		
+25°C		60	75	0.5					220	-1.850		-1.650	-0.960		-0.810			-1.630	-0.980		
+85°C		N/A			N/A			N/A		-1.825		-1.615	-0.890		-0.700			-1.595	-0.910		
10172																					
-30°C		N/A			N/A			N/A		-1.890		-1.675	-1.060		-0.890			-1.675	-1.080		
+25°C		60	77	0.5					220	-1.850		-1.650	-0.960		-0.810			-1.630	-0.980		
+85°C		N/A			N/A			N/A		-1.825		-1.615	-0.890		-0.700			-1.595	-0.910		
10173							Pin 5,6														
-30°C		N/A			N/A			N/A		-1.890		-1.675	-1.060		-0.890			-1.675	-1.080		
+25°C			66	0.5					295	-1.850		-1.650	-0.960		-0.810			-1.630	-0.980		
+85°C		N/A			N/A			N/A		-1.825		-1.615	-0.890		-0.700			-1.595	-0.91		
							Pin 7,9														
								N/A													
									250												
								N/A													
10174																					
							Pin 4														
-30°C		N/A			N/A			N/A		-1.890		-1.675	-1.060		-0.890			-1.655	-1.080		
+25°C		55	73	0.5					220	-1.850		-1.650	-0.960		-0.810			-1.630	-0.980		
+85°C		N/A			N/A			N/A		-1.825		-1.615	-0.890		-0.700			-1.595	-0.910		
							Pin 14														
								N/A													
									330												
								N/A													
10175							Pin 6,7,10														
-30°C		N/A			N/A			N/A		-1.890		-1.675	-1.060		-0.890			-1.655	-1.080		
+25°C			97	0.5					290	-1.850		-1.650	-0.960		-0.810			-1.630	-0.980		
+85°C		N/A			N/A			N/A		-1.825		-1.615	-0.890		-0.700			-1.595	-0.910		
							Pin 11														
								N/A													
									650												
								N/A													
10176																	Note 7			Note 7	
							Pin 5														
-30°C		N/A			N/A			N/A		-1.890		-1.675	-1.060		-0.890			-1.655	-1.080		
+25°C		88	110	0.5					220	-1.850		-1.650	-0.960		-0.810			-1.630	-0.980		
+85°C		N/A			N/A			N/A		-1.825		-1.615	-0.890		-0.700			-1.595	-0.910		
							Pin 9														
								N/A													
									310												
								N/A													

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	INPUT CURRENT									OUTPUT VOLTAGE											
PARAMETER	I_E (mA) SUPPLY CURRENT			I_{IL} (μA) LOW LEVEL			I_{IH} (μA) HIGH LEVEL			V_{OL} (V) LOW LEVEL			V_{OH} (V) HIGH LEVEL			V_{OLA} (V) THRESHOLD LOW LEVEL			V_{OHA} (V) THRESHOLD HIGH LEVEL		
TEST CONDITION*				$V_{IN}=V_{IL}$MIN			$V_{IH}=V_{IH}$ MAX			OUTPUT=50Ω LOAD TO-2V $V_{IN}=V_{IL}$MIN OR V_{IH}MAX			OUTPUT=50Ω LOAD TO-2V $V_{IN}=V_{IL}$MIN OR V_{IH} MAX			OUTPUT=50Ω LOAD TO-2V $V_{IN}=V_{ILA}$MAX OR V_{IHA} MIN			OUTPUT=50Ω LOAD TO-2V $V_{IH}=V_{ILA}$MIN OR V_{IHA}MIN		
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
10179								Pin 4,7,11													
-30°C		N/A			N/A			N/A		-2.000		-1.675	-1.060		-0.890			-1.655	-1.080		
+25°C		39	72	0.5					270	-1.990		-1.650	-0.960		-0.810			-1.630	-0.980		
+85°C		N/A			N/A			N/A		-1.920		-1.615	-0.890		-0.700			-1.595	-0.910		
								Pin 5,9													
								N/A													
									225												
								N/A													
								Pin 10,13													
								N/A													
									440												
								N/A													
								Pin 12													
								N/A													
									395												
								N/A													
								Pin 14													
								N/A													
									355												
								N/A													
10181								Pin 9,11,19,20													
-30°C		N/A			N/A			N/A		-2.000		-1.675	-1.060		-0.890			-1.655	-1.080		
+25°C			145	0.5					245	-1.990		-1.650	-0.960		-0.810			-1.630	-0.980		
+85°C		N/A			N/A			N/A		-1.920		-1.615	-0.890		-0.700			-1.595	-0.910		
								Pin 10,16,18,21													
								N/A													
									220												
								N/A													
								Pin 13,23													
								N/A													
									200												
								N/A													
								Pin 14,15,17													
								N/A													
									265												
								N/A													
								Pin 22													
								N/A													
									290												
								N/A													
10190											V_{IN}=+0.57 or -0.5			V_{IN}=+0.57 or -0.5			V_{IN}=±0.17			V_{IN}=±0.17	
-30°C		N/A			N/A			N/A		-1.890		-1.675	-1.060		-0.890			-1.655	-1.080		
+25°C		36	45						50	-1.850		-1.650	-0.960		-0.810			-1.630	-0.980		
+85°C		N/A			N/A			N/A		-1.825		-1.615	-0.890		-0.700			-1.595	-0.910		
10191								Pin 7													
-30°C		N/A			N/A			N/A		Note 1		-0.365	0.220		0.400			-0.345	0.200		
+25°C		30	38	0.5					245			-0.330	0.305		0.490			-0.310	0.285		
+85°C		N/A			N/A			N/A				-0.295	0.400		0.585			-0.275	0.380		
								Pin 9													
								N/A													
									265												
								N/A													

ECL PRODUCT INFORMATION
ECL DC ELECTRICAL CHARACTERISTICS

PARAMETER	INPUT CURRENT									OUTPUT VOLTAGE											
	I_E (μA) SUPPLY CURRENT			I_{IL} (μA) LOW LEVEL			I_{IH} (μA) HIGH LEVEL			V_{OL} (V) LOW LEVEL			V_{OH} (V) HIGH LEVEL			V_{OLA} (V) THRESHOLD LOW LEVEL			V_{OHA} (V) THRESHOLD HIGH LEVEL		
TEST CONDITION*				$V_{IN}=V_{IL}$MIN			$V_{IH}=V_{IH}$ MAX			OUTPUT=50Ω LOAD TO 2V $V_{IN}=V_{IL}$MIN OR V_{IL}MAX			OUTPUT=50Ω LOAD TO 2V $V_{IN}=V_{IL}$MIN OR V_{IH} MAX			OUTPUT=50Ω LOAD TO 2V $V_{IN}=V_{ILA}$MAX OR V_{IHA} MIN			OUTPUT=50Ω LOAD TO 2V $V_{IH}=V_{ILA}$MIN OR V_{IHA}MIN		
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
10192																					
-30°C		N/A			N/A			N/A													
+25°C	76	95	118	0.5					320												
+85°C		N/A			N/A			N/A													
10210																					
-30°C		N/A					N/A														
+25°C			38						425												
+85°C		N/A					N/A														
10211																					
-30°C		N/A							N/A												
+25°C			38						425												
+85°C		N/A						N/A													
10212																					
-30°C		N/A						N/A													
+25°C			38						425												
+85°C		N/A						N/A													
10216																					
-30°C		N/A						N/A		-1.890		-1.695	-1.060		-0.890			-1.655	-1.080		
+25°C		20	25			*1.0			115	-1.850		-1.650	-0.960		-0.810			-1.630	-0.980		
+85°C		N/A						N/A		-1.825		-1.615	-0.890		-0.700			-1.595	-0.910		
10231								Pin 4,5			Note 2			Note 2			Note 2			Note 2	
-30°C		N/A			N/A			N/A		-1.890		-1.695	-1.060		-0.890			-1.655	-1.080		
+25°C		52	65	0.5					410	-1.850		-1.650	-0.960		-0.810			-1.630	-0.980		
+85°C		N/A			N/A			N/A		-1.825		-1.615	-0.890		-0.700			-1.595	-0.910		
								Pin 6,7													
								N/A													
									220												
								N/A													
								Pin 9													
								N/A													
									290												
								N/A													

* For more test information see notes on individual data sheets.

NOTE:

1. V_{OL} (min) is determined by load network (approx. -0.500V with 845Ω to V_{EE} and 90Ω to ground.
2. Output level to be measured after a clock pulse has been applied to the $\overline{C}_F$ input (Pin 6) V_{IH} max V_{ILMin}
3. Measure output before and after clock pulse V_{IL} VIH appears at clock input (Pin 13).
4. For additional electrical specifications see data sheet.
5. Before test set Q, Q_2 outputs to logic low.
6. Before test set all Q outputs to a logic high.
7. Output levels to be measured after a clock pulse has been applied to C input (Pin 9).

* I_{CBO}

** Output=25Ω for 10123.

ECL AC CHARACTERISTICS (50Ω Load) — See Notes Page 19

PARAMETER		Propagation[2] Delay, (ns)			Rise Time (ns) 20-80%			Fall Time (ns) 20-80%			t setup[5]			t hold[6]		
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
10100			t4+2-,t4-2+			t2+			t2-							
	- 30°C	1.0		3.1	1.1		3.6	1.1		3.6						
	+25°C	1.0	2.0	2.9	1.1	2.0	3.3	1.1	2.0	3.3		N/A			N/A	
	+85°C	1.0		3.3	1.1		3.7	1.1		3.7						
10101			t4+2-,t4-2+ t4+5-,t4-5-			t2+,t5+			t2-,t5-							
	30°C	1.0		3.1	1.1		3.6	1.1		3.6						
	+25°C	1.0	2.0	2.9	1.1		3.3	1.1		3.3		N/A			N/A	
	+85°C	1.0		3.3	1.1		3.7	1.1		3.7						
10102			t12+15-,t12-15+, t12+9+,t12-9-			t15+,t9+			t15-,t9-							
	- 30°C	1.0		3.1	1.1		3.6	1.1		3.6						
	+25°C	1.0	2.0	2.9	1.1		3.3	1.1		3.3		N/A			N/A	
	+85°C	1.0		3.3	1.1		3.7	1.1		3.7						
10103			t12+15+,t12-15- t12+9-,t12-9+			t15+,t9+			t15-,t9-							
	- 30°C	1.0		3.1	1.1		3.6	1.1		3.6						
	+25°C	1.0	2.0	2.9	1.1	2.0	3.3	1.1	2.0	3.3		N/A			N/A	
	+85°C	1.0		3.3	1.1		3.7	1.1		3.7						
10104			t12+14+,t12-15-, t12+9-,t12-9+			t15+,t9+			t15-,9-							
	- 30°C	1.0		4.3	1.5		3.7	1.5		3.7						
	+25°C	1.0	2.2	4.0	1.5	2.0	3.5	1.5	2.0	3.5		N/A			N/A	
	+85°C	1.0		4.2	1.5		3.6	1.5		3.6						
			t13+15+ t13+8-													
	+25°C	1.0	2.7	4.0												
10105			t4+3-,t4-3+, t4+2+,t4-2-			t3+,t2+			t3-,t2-							
	- 30°C	1.0		3.1	1.1		3.6	1.1		3.6						
	+25°C	1.0	2.0	2.9	1.1		3.3	1.1		3.3		N/A			N/A	
	+85°C	1.0		3.3	1.1		3.7	1.1		3.7						
10106			t4+3-,t4-3+			t3+			t3-							
	- 30°C	1.0		3.1	1.1		3.6	1.1		3.6						
	+25°C	1.0	2.0	2.9	1.1		3.3	1.1		3.3		N/A			N/A	
	+85°C	1.0		3.3	1.1		3.7	1.1		3.7						
			Pins 4,9,14													
10107			t++,t+-,t-+,t- -			t+			t-							
	- 30°C	1.0		3.8	1.1		3.5	1.1		3.5						
	+25°C	1.1	2.0	3.7	1.1	2.5	3.5	1.1	2.5	3.5		N/A			N/A	
	+85°C	1.1		4.0	1.1		3.8	1.1		3.8						
	- 30°C															
			Pins 5,7,15													
	+25°C	1.1	2.8	3.7												
	+85°C															
10108			t4+2+,t4-2, t4+3-,t4-3+			t2+,t3+			t2-,t3-							
	- 30°C		N/A			N/A			N/A							
	+25°C	1.4	2.3	3.4	1.1	2.2	4.0	1.1	2.2	4.0		N/A			N/A	
	+85°C		N/A			N/A			N/A							

ECL AC CHARACTERISTICS (50Ω Load) — See Notes Page 19

PARAMETER	Propagation [2] Delay, (ns)			Rise Time (ns) 20-80%			Fall Time (ns) 20-80%			t setup [5]			t hold [6]		
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
		t5+2+,t5-2-, t5+3-,t5-3+													
- 30°C		N/A													
+25°C	1.4	2.8	3.7												
+85°		N/A													
10109		t4+2+,t4-2-, t4+3-,t4-3+			t2+,t3+			t2-,t3-							
- 30°C	1.0		3.1	1.1		3.6	1.1		3.6						
+25°C	1.0	2.0	2.9	1.1		3.3	1.1		3.3		N/A			N/A	
+85°C	1.0		3.3	1.1		3.7	1.1		3.7						
10110		t5+2+,t5-2-, t5+3+,t5-3-, t5+4,t5-4-			t2+,t3+,t4+			t2-,t3-,t4-							
- 30°C	1.4		3.5	1.0		3.5	1.0		3.5						
+25°C	1.4	2.4	3.5	1.1	2.2	3.5	1.1	2.2	3.5		N/A			N/A	
+85°C	1.5		3.8	1.2		3.8	1.2		3.8						
10111		t5+2-,t5-2t, t5+3-,t5-3t, t5+4-,t5-4t			t2+,t3+,t4+			t2-,t3-,t4-							
- 30°C	1.4		3.5	1.0		3.5	1.0		3.5						
+25°C	1.4	2.4	3.5	1.1	2.2	3.5	1.1	2.2	3.5		N/A			N/A	
+85°C	1.5		3.8	1.2		3.8	1.2		3.8						
10112		t5+2+,t5-2-, t5+3-,t5+3+, t5+4-,t5-4+			t2+,t3+,t4+			t2-,t3-t4-							
+25°C	1.4	2.4	3.5	1.1	2.2	3.5	1.1	2.2	3.5		N/A			N/A	
10113		t4+2+,t4-2-			t+			t-							
- 30°C															
+25°C		3.0			2.0			2.0			N/A			N/A	
+85°C															
	t9+2-,t9-2+														
- 30°C															
+25°C		3.4													
+80°C															
10114		t4+2+,t4-2-,3 t4+3-,t4-3+			t2+,t3+			t2-3-							
- 30°C	1.0		4.4	1.5		3.8	1.5		3.8						
+25°C	1.0	2.5	4.0	1.5	2.1	3.5	1.5	2.1	3.5		N/A			N/A	
+85°C	0.9		4.3	1.5		3.7	1.5		3.7						
10115		t4+2-,t4-2+			t2+			t2-							
- 30°C	1.0		3.1	1.1		3.6	1.1		3.6						
+25°C	1.0		2.9	1.1		3.3	1.1		3.3		N/A			N/A	
+85°C	1.0		3.3	1.1		3.7	1.1		3.7						
10116		t4+2+,t4-2-, t4+3,t4-3+			t2+,t3+			t2-,t3-							
- 30°C	1.0		3.1	1.1		3.6	1.1		3.6						
+25°C	1.0	2.0	2.9	1.1	2.0	3.3	1.1	2.0	3.3		N/A			N/A	
+85°C	1.0		3.3	1.1		3.7	1.1		3.7						
10117		t4+2+,t4-2-, t4+3-,t4-3+			t2+,t3+			t2-3-							
- 30°C	1.4		3.9	0.9		4.1	0.9		4.1						
+25°C	1.4	2.3	3.4	1.1	2.2	4.0	1.1	2.2	4.0		N/A			N/A	
+85°C	1.4		3.8	1.1		4.6	1.1		4.6						

ECL AC CHARACTERISTICS (50Ω Load)—SEE NOTES PAGE 19

PARAMETER	Propagation[2] Delay, (ns) MIN	TYP	MAX	Rise Time (ns) 20-80% MIN	TYP	MAX	Fall Time (ns) 20-80% MIN	TYP	MAX	t setup[5] MIN	TYP	MAX	t hold[6] MIN	TYP	MAX
10118		t6+2+,t6-2-			t+			t-							
- 30°C	1.4		3.9	0.8		4.1	0.8		4.1						
+25°C	1.4	2.3	3.4	1.5	2.5	4.0	1.5	2.5	4.0		N/A			N/A	
+85°C	1.4		3.8	1.5		4.6	1.5		4.6						
10119		t3+2+,t3-2-			t+			t-							
- 30°C	1.4		3.9	0.8		4.1	0.8		4.1						
+25°C	1.4	2.3	3.4	1.5	2.5	4.0	1.5	2.5	4.0		N/A			N/A	
+85°C	3.4	1.4	3.8	1.5		4.6	1.5		4.6						
10121		t4+3-,t4-3+, t4+2+,t4-2-			t3+,t2+			t3-,t2-							
- 30°C	1.4		3.9	0.9		4.1	0.9		4.1						
+25°C	1.4	2.3	3.4	1.1	2.5	4.0	1.1	2.5	4.0		N/A			N/A	
+85°C	1.4		3.8	1.1		4.6	1.1		4.6						
10124 (Note 4)		t6+1+,t6-1- t7+1+,t7-1-, t7+3+,t7-3+			t1+			t1-							
- 30°C	1.0		6.8	1.1		4.2	1.1		4.2						
+25°C	1.5		6.0	1.1		3.9	1.1		3.9		N/A			N/A	
+85°C	1.0		6.8	1.1		4.3	1.1		4.3						
10125		t6+5-,t6-5+ t2+t4-,t2-4+			t4+			t4-							
- 30°C	1.0	4.5	6.0			3.3			3.3		N/A			N/A	
+25+85	1.0		6.0			3.3			3.3						
Data Input		t7+t4+			t+			t-							
10129 +25°C	6.6	12.0	27.0	1.5		4.3	1.5		4.3	25.0			0		
Data Input		t7-14-													
	3.7	10.0	15.0												
Clock Input		t11-14+													
	2.7	5.0	11.0												
Strobe Input		t12±14±													
	1.6	4.0	7.0												
Reset Input		t10+14-													
	2.0	5.0	8.0												
Hysteresis Mode		t7+14+													
		18.0													
Hysteresis Mode		t7-14-													
		10.0													
10130		t7+2+			t2+			t2-							
- 30°C	1.0		3.6	1.0		3.6	1.0		3.6						
+25°C	1.0	2.5	3.5	1.0	2.7	3.5	1.0	2.7	3.5		N/A			N/A	
+85°C	1.0		3.8	1.1		3.8	1.1		3.8						
		t5+2+,t4+2-													
- 30°C	1.0		3.6												
+25°C	1.0	2.7	3.5												
+85°C	1.1		3.9												
		t6-2+													
- 30°C	1.0		4.3												
+25°C	1.0		4.0												
+85°C	1.0		4.1												
10131 Clock Input		t9+2-,t9+2+, t6+2+,t6+2-			t2+			t2-							
- 30°C	1.4		4.6	1.0		4.6	1.0		4.6						
+25°C	1.5	3.0	4.5	1.1	2.5	4.5	1.1	2.5	4.5	2.5			1.5		
+85°C	1.5		5.0	1.1		4.9	1.1		4.9						

ECL AC CHARACTERISTICS (50Ω Load) — See Notes Page 19

PARAMETER	Propagation [2] Delay, (ns)			Rise Time (ns) 20-80%			Fall Time (ns) 20-80%			t setup [5]			t hold [6]		
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
Set Input		t5+2+,t12+5+,													
		t5+3-,t12+14-													
- 30°C	1.1		4.4												
+25°C	1.2	2.8	4.3												
+85°C	1.2		4.8												
Reset Input		t4+2,t13+15-													
		t4+3+,t13+14+													
- 30°C	1.1		4.4												
+25°C	1.2	2.8	4.3												
+85°C	1.2		4.8												
10132 +25°C															
Data		t4+2+			t2+			t2-			Data			Data	
	1.0	2.5	3.3	1.5		3.5	1.5		3.5	2.5			1.5		
Reset		t6+2-									Select			Select	
	1.0	3.0	3.8							3.5			1.0		
Clock		t7-2+													
	1.0	4.0	5.7												
Select		t11+2+													
	1.0	3.7	4.6												
10133		t3+2+			t2+			t2-							
- 30°C	1.0		5.6	1.0		3.6	1.0		3.6						
+25°C	1.0		5.4	1.1		3.5	1.1		3.5		N/A			N/A	
+85°C	1.1		5.9	1.1		3.8	1.1		3.8						
		t4+2+													
- 30°C	1.0		5.4												
+25°C	1.0		5.4												
+85°C	1.2		6.0												
		t5-2+													
- 30°C	1.0		3.2												
+25°C	1.0		3.1												
+85°C	1.0		3.4												
10134 +25°C					t2+			t2-			Data			Data	
Data		t4+2+		1.5	2.0	3.5	1.5	2.0	3.5	2.5	1.5		1.5	0.0	
	1.0	2.5	3.3								Select			Select	
Clock		t10-2+													
	1.0	4.0	5.7							3.5	2.5		1.0	0.5	
Select		t6+2+													
	1.0	3.5	4.6												
10135 +25°C		t9+2+,t9+2-			t2+,t3+			t2-,t3-							
Clock Input	1.0	3.0	4.5	1.1	2.0	4.5	1.0	2.0	4.5	2.5	1.0		1.5	1.0	
Set Input		t5+2+,t12+5+,													
		t5+3-,t12+4+													
	1.0	3.0	5.0												
Reset Input		t4+2-,t4+3+,													
		t13+15-,t13+14+													
	1.0	3.0	5.0												
10136															
Clock Input		t13+14+,t13+14-,			t4+,t14+			t4-,t14-			Data Inputs			Data Inputs	
											t12+13+,t12-13-			t12+13+,t12-13-	
- 30	0.8		4.8	4		0.9	4		0.9		+25°C			+25°C	
+25	1.0	3.3	4.5	3.3	1.1	2.0	3.3	1.1	2.0	3.5	2.1			-1.0	-1.9
+85	1.4		5.0	3.3	1.1	3.5	3.3	1.1	3.5		Select Inputs			Select Inputs	
Clock Input		t13+4+,t13+4-									t9+13+,t7+13+			+9+13+,t7+13+	
- 30	2.0		10.9								+25°C			+25°C	
+25	2.5	7.0	10.5							7.5	5.4			-2.5	-5.4
+85	2.4		11.5												

LOGIC

ECL PRODUCT INFORMATION

ECL AC CHARACTERISTICS (50Ω Load) — See Notes Page 19

PARAMETER	Propagation [2] Delay, (ns)			Rise Time (ns) 20-80%			Fall Time (ns) 20-80%			t_{setup} [5]			t_{hold} [6]		
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
											Carry In Input			Carry In Input	
Carry In to		t10-4+,t10+4+									t10-13+,t13+10+			+25°C	
Carry Out															
Note 7 - 30	1.6		7.4								+25°C			t10-13+	
+25	1.6	5.0	6.9							-1.0	-1.9		-1.6		-2.4
+85	1.9		7.5												
														t13+,t10+	
													3.1	2.2	
10137															
Clock Input		t13+14+,t13+14-,			t4+,t14+			t4-,t14-			Data Inputs			Data Inputs	
											t12+13+,t12-13-			t12+13+,t12-13-	
- 30	0.8		4.8	4		0.9	4		0.9		+25°C			+25°C	
+25	1.0	3.3	4.5	3.3	1.1	2.0	3.3	1.1	2.0	3.5	2.1			-1.0	-1.9
+85	1.4		5.0	3.3	1.1	3.5	3.3	1.1	3.5		Select Inputs			Select Inputs	
Clock Input		t13+4+,t13+4-									t9+13+,t7+13+			+9+13+,t7+13+	
- 30	2.0		10.9								+25°C			+25°C	
+25	2.5	7.0	10.5						7.5	5.4			-2.5	-5.4	
+85	2.4		11.5								Carry In Input			Carry In Input	
Carry In to		t10-4+,t10+4+									t10-13+,t13+10+			+25°C	
Carry Out															
Note 8 - 30	1.6		7.4								+25°C			t10-13+	
+25	1.6	5.0	6.9							-1.0	-1.9		-1.6		-2.4
+85	1.9		7.5											t13+,t10+	
														3.1 2.2	
10141		t4+3+			t3+			-3-			t12+4+			t4+12+	
- 30	0.9		3.9	1.0		3.4	1.0		3.4		N/A				N/A
+25	1.0	2.9	3.8	1.1	1.7	3.3	1.1	1.7	3.3	2.5			1.5		
+85	1.2		4.2	1.1		3.6	1.1		3.6		N/A				N/A
10145	SEE DATA SHEET FOR ELECTRICAL SPECIFICATIONS														
10158		t3+2+,t3-2-			t+			t-							
- 30°C	1.1		3.8	1.0		4.1	1.0		4.1						
+25°C	1.2	2.2	3.3	1.0	2.5	3.8	1.0	2.5	3.8		N/A				N/A
+85°C	1.1		3.8	1.1		4.1	1.1		4.1						
		t9+2+,t9-2-													
- 30°C	1.4		5.0												
+25°C	1.5	3.0	4.5												
+85°C	1.4		5.0												
10159		t3+2-,t3-2+			t+			t-							
- 30°C	1.1		3.8	1.0		4.1	1.0		4.1						
+25°C	1.2	2.2	3.3	1.0	2.5	3.8	1.0	2.5	3.8		N/A				N/A
+85°C	1.1		3.8	1.1		4:1	1.1		4.1						
		t9+2+,t9-2- t7+2-,t7-2+													
- 30°C	1.4		5.0												
+25°C	1.5	3.0	4.5												
+85°C	1.4		5.0												
10160		t3+2+,t3+2-, t3-2-,t3-2+, t4+2+,t4+2-, t4-2-,t4-2+			t2+			t2-							
- 30°C	1.8		8.1	1.1		3.5	1.1		3.5						
+25°C	2.0	5.0	7.5	1.1	2.0	3.3	1.1	2.0	3.3		N/A				N/A
+85°C	2.0		8.0	1.1		3.5	1.1		3.5						

ECL PRODUCT INFORMATION

ECL AC CHARACTERISTICS (50Ω Load) — See Notes Page 19

PARAMETER	Propagation [2] Delay, (ns)			Rise Time (ns) 20-80%			Fall Time (ns) 20-80%			t_{setup} [5]			t_{hold} [6]		
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
10161		t14+13-,t14-13+			t13+			t13-							
- 30°C	1.5		6.0	1.1		3.3	1.1		3.3						
+25°C	1.5	4.0	6.0	1.1	2.0	3.3	1.1	2.0	3.3		N/A				N/A
+85°C	1.5		6.0	1.1		3.3	1.1		3.3						
10162		t14+13+,t14-13-			t+			t-							
- 30°C	2.5		6.2	1.0		3.3	1.0		3.3						
+25°C	1.5	4.0	6.0	1.1	2.0	3.3	1.1	2.0	3.3		N/A				N/A
+85°C	1.5		6.4	1.1		3.5	1.1		3.5						
10164		t4+15+,t4-15-			t+			t-							
- 30°C	1.5		4.7	0.9		3.3	0.9		3.3						
+25°C	1.5	3.0	4.5	1.1	2.0	3.3	1.1	2.0	3.3		N/A			N/A	
+85°C	1.6		4.8	1.2		3.6	1.2		3.6						
		t7+15+,t7-15-													
- 30°C	1.9		6.3												
+25°C	2.0	4.0	6.0												
+85°C	2.2		6.5												
		t2+15+,t2-15+													
- 30°C	0.9		3.3												
+25°C	1.0	2.0	2.9												
+85°C	1.0		3.1												
10165 +25°C															
Data Input		t5+14+,t5-14-, t7+3+,t11+15+, t13+2+			t3+			t3-			t_{setup} H			t_{hold} H	
		7.0	10.0		2.0	3.3		2.0	3.3		3.4	4.5		-2.3	-.5
Clock Input		t4-3+10,t4-3-11 t4-14+10,t4-14-11									t_{setup} L			t_{hold} L	
											3.0	4.5		-2.7	-.5
		3.0	5												
10170		t3+2+,t3+2-, t3-2-,t3-2+			t2+			t2-,t15+,+15							
- 30°C	1.5		6.5								N/A			N/A	
+25°C	2.0	4.0	6.0	1.1	2.0	3.3	1.1	2.0	3.3						
+85°C	1.5		6.5												
		t3+15+,t3+15-, t3-15-,t3-15+													
- 30°C	2.0		10.0												
+25°C	3.0	6.0	9.0												
+85°C	5.0		10.0												
		t13+15+,t13+15-, t13-15-,t13-15+													
- 30°C	0.9		3.3												
+25°C	1.0	2.0	3.0												
+85°C	0.9		3.3												
10171		t9+13+,t9-13-			t13+			t13-							
- 30°C	1.5		6.2	1.0		3.3	1.0		3.3						
+25°C	1.5	4.0	6.0	1.1	2.0	3.3	1.1	2.0	3.3		N/A			N/A	
+85°C	1.5		6.4	1.1		3.4	1.1		3.4						
10172		t9+13-,t9-13+			t+			t-							
- 30°C	1.5		6.2	1.0		3.3	1.0		3.3						
+25°C	1.5	4.0	6.0	1.1	2.0	3.3	1.1	2.0	3.3		N/A			N/A	
+85°C	1.5		6.4	1.1		3.4	1.1		3.4						
10173		t6+1+,t6-1-,			t+			t-							
Data Input		t5+1+,t5-1-													
- 30°C	0.8		3.7	1.2		4.0	1.2		4.0						
+25°C	1.0	2.5	3.5	1.5		3.5	1.5		3.5		N/A			N/A	
+85°C	1.1		5.3	1.4		4.0	1.4		4.0						

ECL AC CHARACTERISTICS (50Ω Load) — See Notes Page 19

PARAMETER	Propagation [2] Delay, (ns)			Rise Time (ns) 20-80%			Fall Time (ns) 20-80%			t setup [5]			t hold [6]		
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
Clock Input		t7-1+,t7-1-													
- 30°C	1.6		7.2												
+25°C	1.6		6.8												
+85°C	1.4		6.8												
Select		t9+1+,t9+1-, t9-1+,t9-1-													
- 30°C	1.1		6.2												
+25°C	1.3		5.7												
+85°C	1.2		6.7												
10174		t13+15+,t13-15-			t+			t-							
- 30°C	1.4		4.8	1.0		3.4	1.0		3.4						
+25°C	1.5	3.5	4.5	1.1	2.0	3.3	1.1	2.0	3.3		N/A			N/A	
+85°C	1.4		4.8	1.1		3.6	1.1		3.6						
		t7+15-,t7-15+													
- 30°C	1.9		6.4												
+25°C	2.0	5.0	6.0												
+85°C	2.1		6.4												
		t14+15-,t14-15+													
- 30°C	1.0		3.1												
+25°C	1.0	2.0	2.9												
+85°C	0.9		3.2												
10174 +25°C		t13+15+,t13-15-			t+			t-							
		3.5			2.0			2.0			N/A			N/A	
		t7+15-,t7-15+													
		5.0													
		t15+5-,t14-5+													
		2.0													
10175															
Data Input		t10+14+,t10-14-			t+			t-							
- 30°C	1.0		3.6	1.0		3.6	1.0		3.6						
+25°C	1.0		3.5	1.1		3.5	1.1		3.5	N/A			N/A		
+85°C	1.0		3.6	1.1		3.7	1.1		3.6						
Clock Input		t6-14+,t6-14-													
- 30°C	1.0		4.7												
+25°C	1.0		4.3												
+85°C	1.0		4.4												
Reset Input		t11+4-,t11+14-													
(Note 10 - 30°C	0.9		4.0												
+25°C	1.0		3.9												
+85°C	1.0		4.2												
10176		t9+2+,t9+2-			t2+			t2-							
- 30°C	1.4		4.6	1.0		4.2	1.0		4.1						
+25°C	1.5		4.5	1.1	2.0	4.0	1.1	2.0	4.0	2.5	1.5		1.5	-0.5	
+85°C	1.5		5.0	1.1		4.4	1.1		4.4						
10179 +25°C		t11+6+,t11-6-			t6+			t6-							
	1.0		5.5	1.1	3.5	3.5	1.1	3.5	3.5		N/A			N/A	
10181	SEE DATA SHEET FOR ELECTRICAL SPECIFICATIONS														
10190 +25°C		t4+2-,t4-2+			t2+			t2-							
	1.5	2.5	3.5	1.5	2.5	3.5	1.5	2.5	3.5		N/A			N/A	
10191		t7+2+,t7-2-			t2+			t2-							
	1.4	2.2	3.3	1.5	2.5	3.5	1.5	2.5	3.5		N/A			N/A	
		t9+2-,t9-2+													
	1.7	2.8	4.0												

ECL PRODUCT INFORMATION

ECL AC CHARACTERISTICS (50Ω Load) — See Notes Page 19

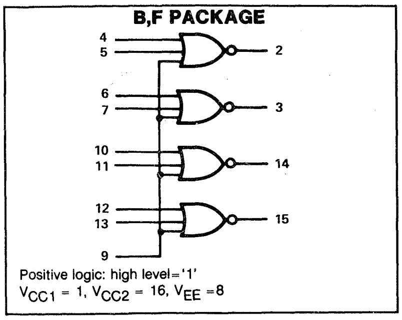
PARAMETER	Propagation [2] Delay, (ns)			Rise Time (ns) 20-80%			Fall Time (ns) 20-80%			t setup [5]			t hold [6]		
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
10192 +25°C Data Inputs		t6+1+,t6+2-, t6-1-,t6-2+			t+			t-							
	1.5	2.8	4.5		1.5	3.0		1.5	3.0		N/A			N/A	
Enable Inputs		t7+1+,t7-1-, t7+2+1t7-2-													
	2.0	4.0	6.0												
10210 +25°C		1.7													
10211 +25°C		1.7													
10212 +25°C		1.7													
10216 +25°C		NOTE 12 t4+2+,t4-2-, t4+3-,t4-3+			t2+,t3+			t2-,t3-							
	1.0		2.5	1.0	1.5	2.5	1.0	1.5	2.5		N/A			N/A	
10231		t9-2-,t9+2+, t6+2+,t6+2-			t2+			t2-							
-30°C	1.4		3.4	0.9		3.3	0.9		3.3						
+25°C	1.5	2.0	3.3	1.0	1.3	3.1	1.0	1.3	3.1	1.0			0.75		
+85°C	1.5		3.7	1.0		3.5	1.0		3.5						
Set Input		t5+2+,t12+15+, t5+3-,t12+14-													
-30°C	1.0		3.4												
+25°C	1.1	2.0	3.3												
+85°C	1.1		3.7												
Reset Input		t4+2-,t13+15-, t4+3+,t13+14+													
-30°C	1.0		3.4												
+25°C	1.0	2.0	3.3												
+85°C	1.1		3.7												

ECL AC CHARACTERISTICS NOTES

1. Unused outputs connected to a 50Ω resistor to ground.
2. In making propagation delay measurement, input pulse is applied at first pin listed (for example, 6+1+) output pulse is measured at second pin listed.
3. Delay is 2.0ns with differential input.
4. (+3.5Vdc to 50%) See switching time test circuit propagation delay for this circuit is specified from +1.5Vdc in to the 50% point on the output waveform. The +3.5Vdc is shown here because all logic and supply levels are shifted 2 volts positive.
5. t_{setup} is the minimum time before the positive transition of the clock pulse (C) that information must be present at the data input. (D).
6. t_{hold} is the minimum time after the positive transition of the clock pulse (C) that information must remain unchanged at the data input (D).
7. Before test set all Q outputs to a logic high.
8. Before test set Q_1, Q_2 outputs to logic low.
9. Output latched to low state prior to test.
10. Output latched to high state prior to test.
11. 1.8 refers to single-ended drive; differential drive results in 1.5ns delay.
12. Individually test each input, apply $V_{IH\,max}$ to pin under test.

10100-B,F

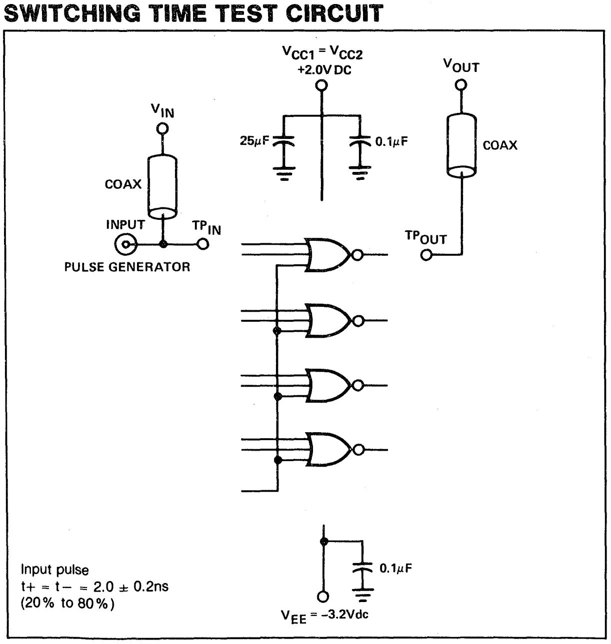
LOGIC DIAGRAM



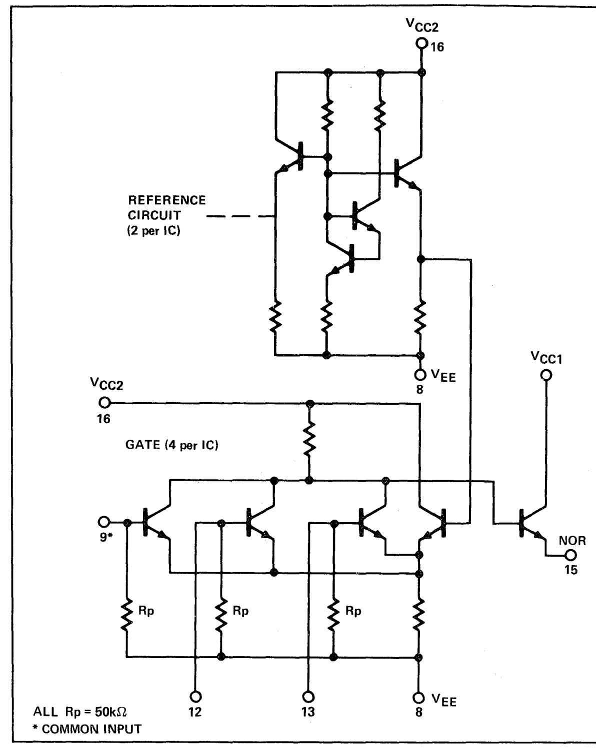
FEATURES

- **Fast propagation delay = 20ns TYP**
- **Common input for gating**
- **Low power dissipation = 100mW/package type (no load)**
- **High fanout capability — can drive 50Ω lines**
- **High Z inputs — internal 50kΩ pulldowns**
- **High immunity from power supply variations: V_{EE} = −5.2 V±5% recommended**
- **Open emitter logic and bussing capability**

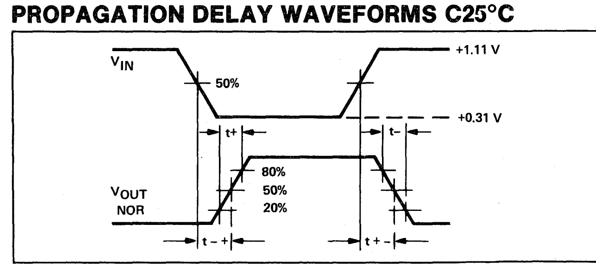
SWITCHING TIME TEST CIRCUIT



CIRCUIT SCHEMATIC



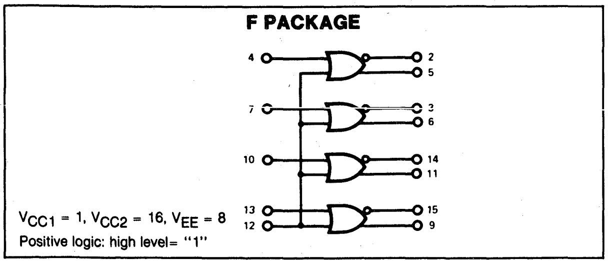
PROPAGATION DELAY WAVEFORMS C25°C



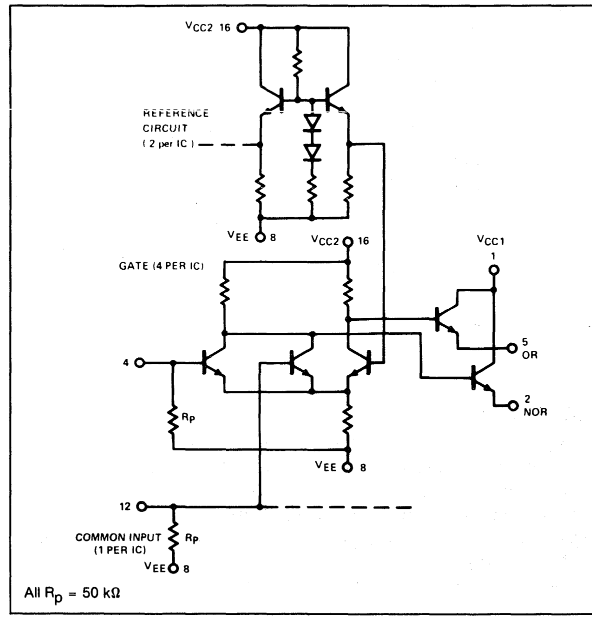
NOTES:

1. Each ECL 10,000 series device has been designed to meet the DC specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Voltage levels will shift approximately 3 mV with an air flow of 200 linear fpm. Outputs are terminated through a 50-ohm resistor to 2.0 volts.
2. For AC tests, all input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be <¼ inch from TP_{in} to input pin and TP_{out} to output pin. A 50-ohm termination to ground is located in each scope input. Unused outputs are connected to a 50-ohm resistor to ground.
3. Test procedures are shown for only one input or set of input conditions. Other inputs are tested in the same manner.
4. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.

LOGIC DIAGRAM



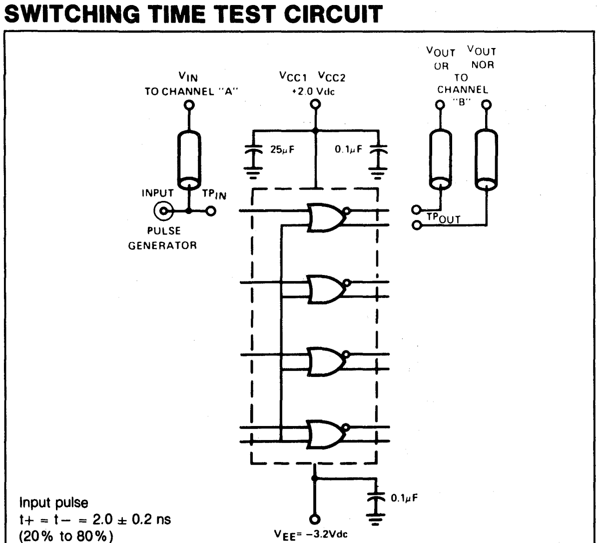
CIRCUIT SCHEMATIC



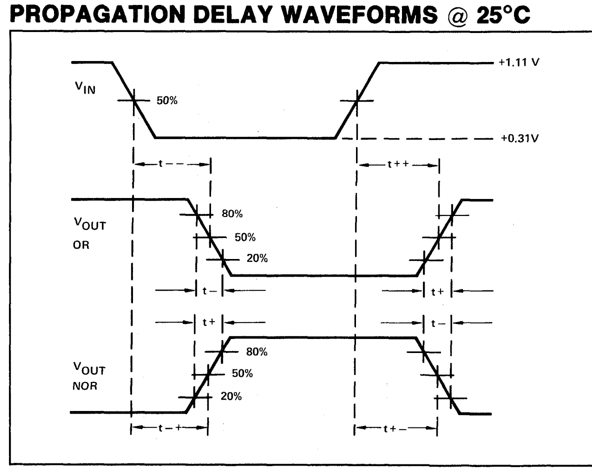
FEATURES

- **Fast propagation delay = 20 ns TYP**
- **Complementary OR/NOR outputs — excellent for driving twisted pairs**
- **Common input for gating**
- **Low power dissipation = 100 mW/package TYP (no load)**
- **High fanout capability — can drive 50 ohm lines**
- **High Z inputs — internal 50kΩ pulldowns**
- **High immunity from power supply variations: V_{EE} = −5.2 ±5% recommended**
- **Open emitter logic and bussing capability**

SWITCHING TIME TEST CIRCUIT



PROPAGATION DELAY WAVEFORMS @ 25°C

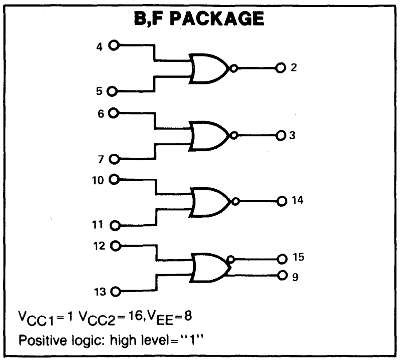


NOTES:

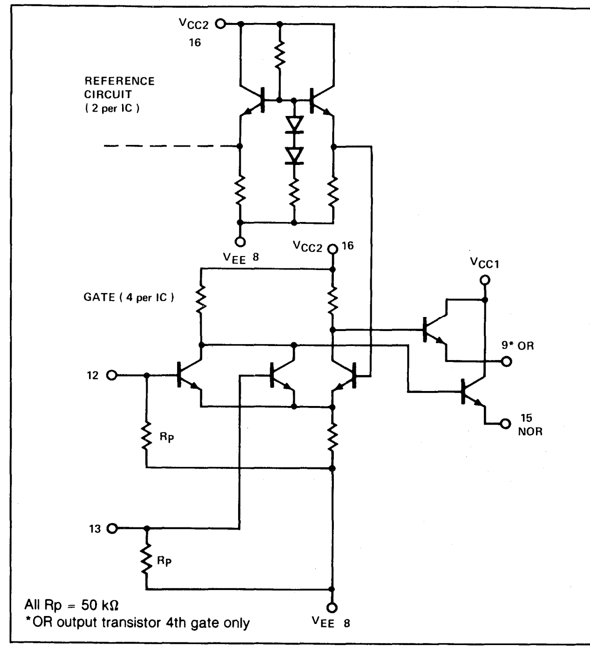
1. Each ECL 10,000 series device has been designed to meet the DC specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Voltage levels will shift approximately 4 mV with an air flow of 200 linear fpm. Outputs are terminated through a 50-ohm resistor to 2.0 volts.
2. For AC tests, all input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be <¼ inch from TP_{in} to input pin and TP_{out} to output pin. A 50-ohm termination to ground is located in each scope input. Unused outputs are connected to a 50-ohm resistor to ground.
3. Test procedures are shown for only one input or set of input conditions. Other inputs are tested in the same manner.
4. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.

10102-B,F

LOGIC DIAGRAM



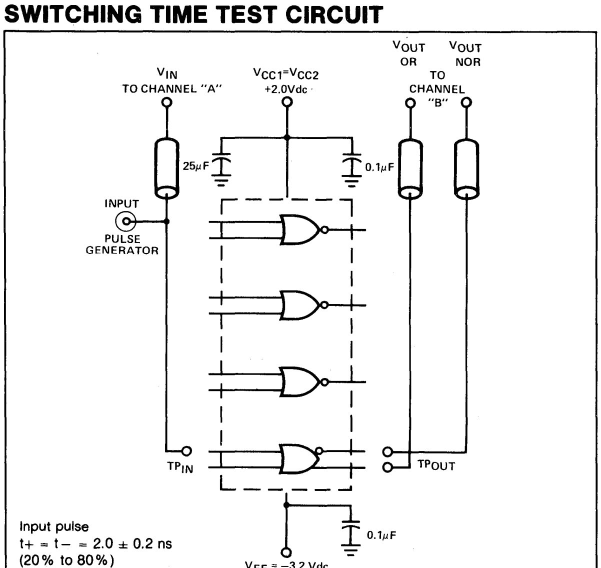
CIRCUIT SCHEMATIC



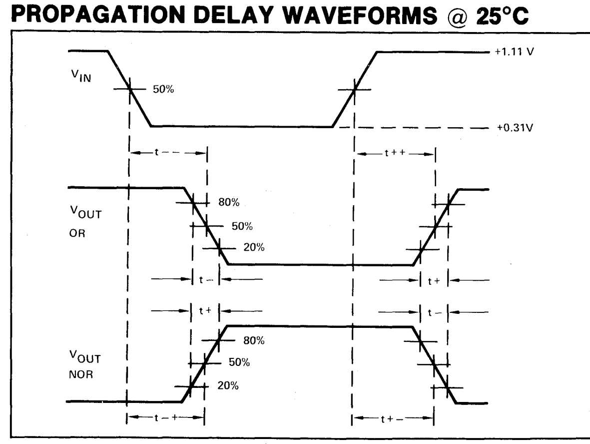
FEATURES

- **Fast propagation delay = 2.0 ns TYP**
- **Low power dissipation = 100 mW/package (no load)**
- **High fanout capability — can drive 50Ω lines**
- **High Z inputs — internal 50 kΩ pulldowns**
- **High immunity from power supply variations: V_{EE} = −5.2 V ±5% recommended**
- **Open emitter logic and bussing capability**

SWITCHING TIME TEST CIRCUIT



PROPAGATION DELAY WAVEFORMS @ 25°C

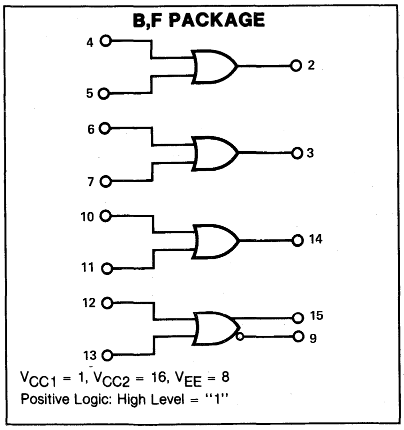


NOTES:

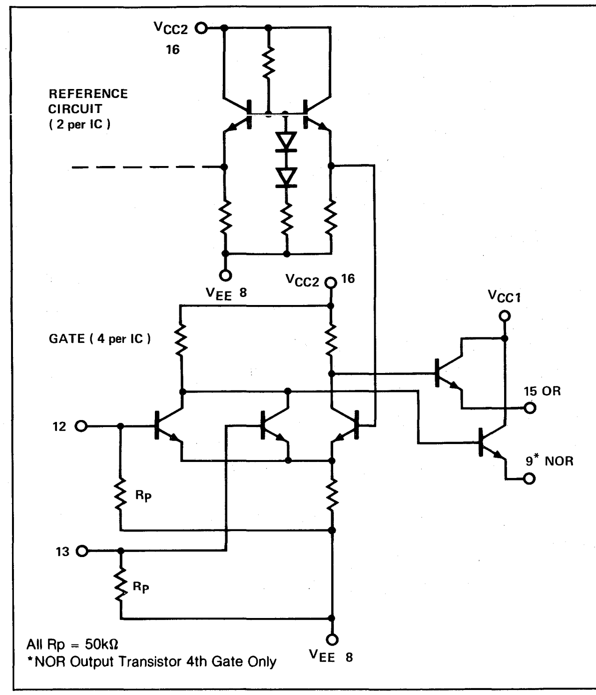
1. Each ECL 10,000 series device has been designed to meet the DC specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Voltage levels will shift approximately 3 mV with an air flow of 200 linear fpm. Outputs are terminated through a 50-ohm resistor to 2.0 volts.
2. For AC tests, all input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be <¼ inch from TP_{in} to input pin and TP_{out} to output pin. A 50-ohm termination to ground is located in each scope input. Unused outputs are connected to a 50-ohm resistor to ground.
3. Test procedures are shown for only one input or set of input conditions. Other inputs are tested in the same manner.
4. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.

10103-B,F

LOGIC DIAGRAM



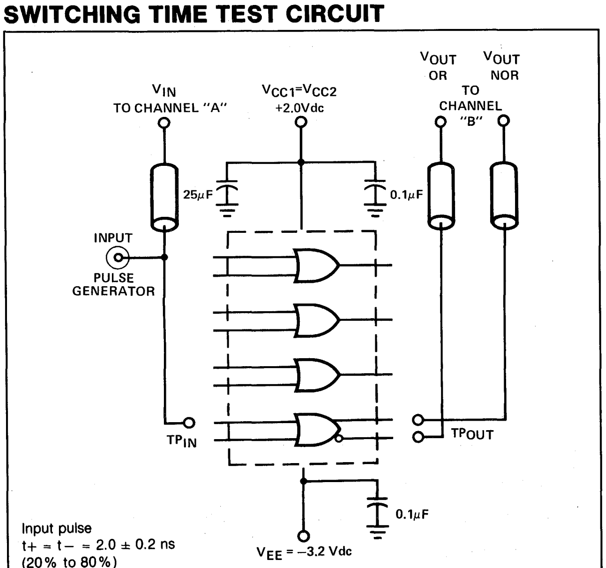
CIRCUIT SCHEMATIC



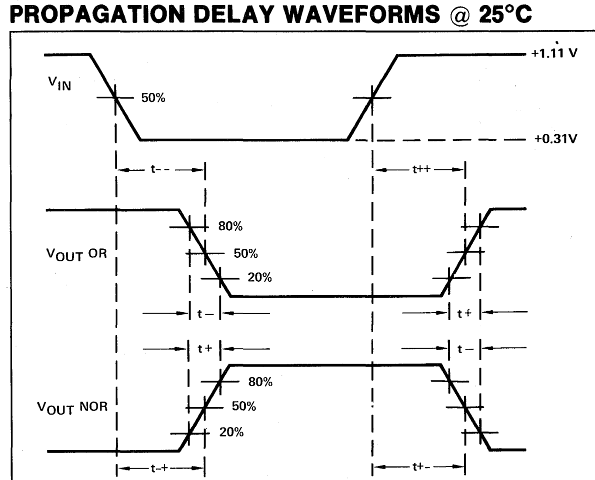
FEATURES

- **Fast propagation delay = 2.0 ns TYP**
- **Power dissipation = 100mW/package TYP**
- **Very high fanout capability — can drive 50Ω lines**
- **High Z inputs with 50kΩ pull-down resistors**
- **High noise immunity from power supply variations: V_{EE} = 5.2V ± 5%**
- **Open emitter logic and bussing capability**

SWITCHING TIME TEST CIRCUIT



PROPAGATION DELAY WAVEFORMS @ 25°C

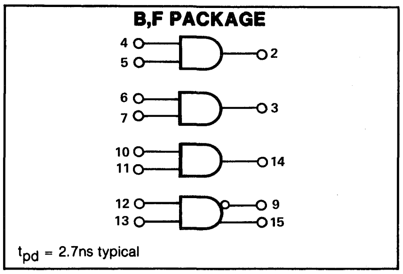


NOTES:

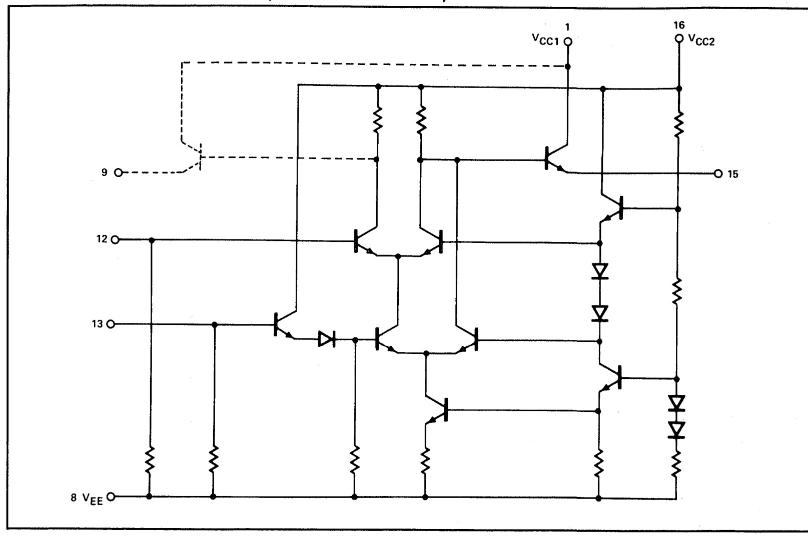
1. Each ECL 10,000 series device has been designed to meet the DC specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Voltage levels will shift approximately 3 mV with an air flow of 200 linear fpm. Outputs are terminated through a 50-ohm resistor to 2.0 volts.
2. For AC tests, all input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be <¼ inch from TP_{in} to input pin and TP_{out} to output pin. A 50-ohm termination to ground is located in each scope input. Unused outputs are connected to a 50-ohm resistor to ground.
3. Test procedures are shown for only one input or set of input conditions. Other inputs are tested in the same manner.
4. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.

10104-B,F

LOGIC DIAGRAM



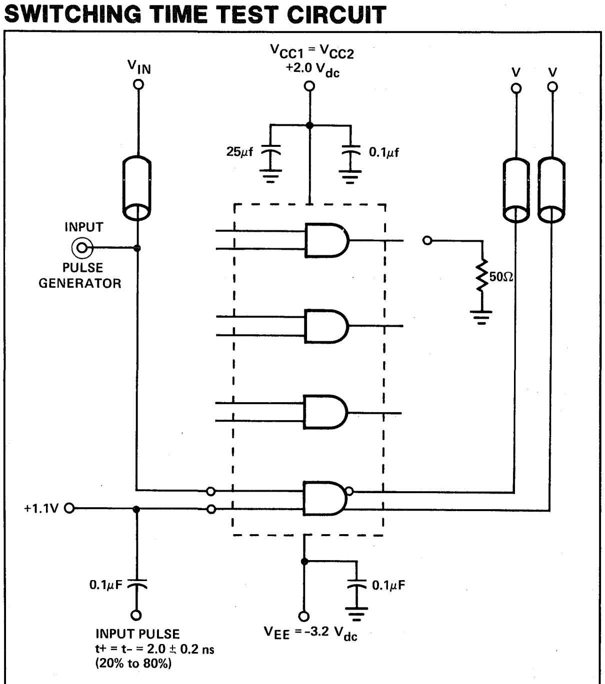
CIRCUIT SCHEMATIC (¼ of Circuit Shown)



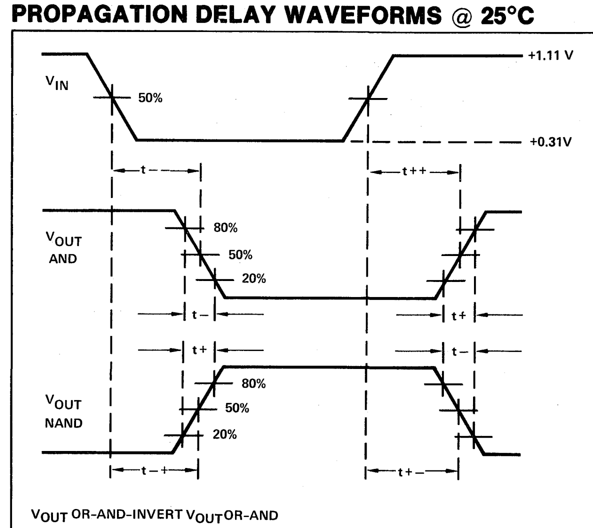
FEATURES

- **High speed propagation delay = 2.7ns typical**
- **Low power dissipation = 40mW/gate typical**
- **High fanout capability, can drive 50Ω lines**
- **High Z inputs, internal 50KΩ pulldown resistors**
- **Open emitter outputs for bussing applications**

SWITCHING TIME TEST CIRCUIT



PROPAGATION DELAY WAVEFORMS @ 25°C

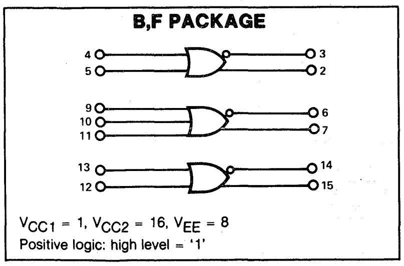


NOTES:

1. Each ECL 10,000 series device has been designed to meet the DC specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Voltage levels will shift approximately 4 mV with an air flow of 200 linear fpm. Outputs are terminated through a 50-ohm resistor to 2.0 volts.
2. For AC tests, all input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be <¼ inch from TP_{in} to input pin and TP_{out} to output pin. A 50-ohm termination to ground is located in each scope input. Unused outputs are connected to a 50-ohm resistor to ground.
3. Test procedures are shown for only one input or set of input conditions. Other inputs are tested in the same manner.
4. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.

10105-B,F

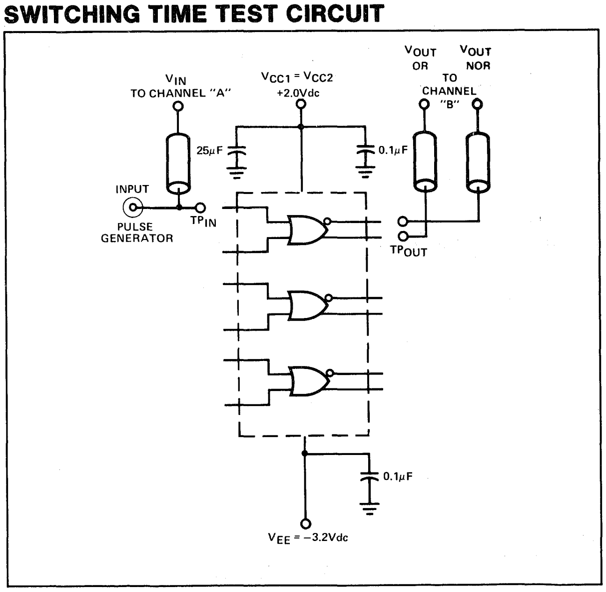
LOGIC DIAGRAM



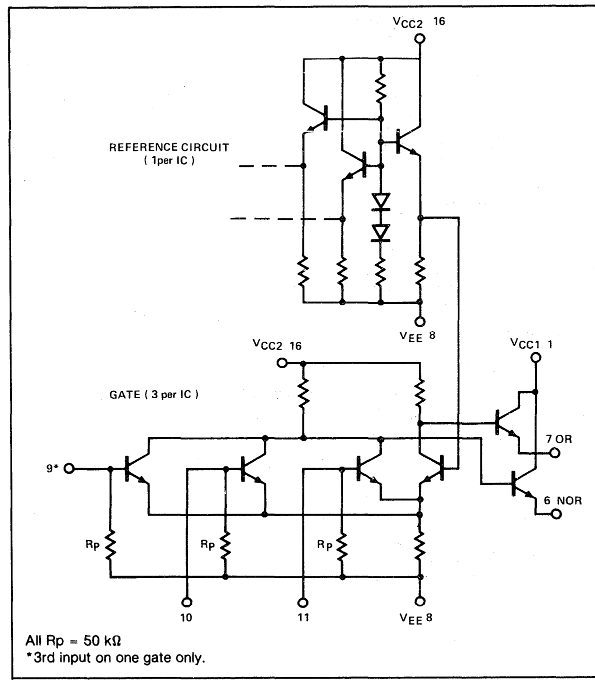
FEATURES

- **Fast propagation delay = 2.0 ns TYP**
- **Power dissipation = 75 mW/package TYP (no load)**
- **Very high fanout capability — can drive 50 Ω lines**
- **High Z inputs — internal 50kΩ pulldowns**
- **High immunity from power supply variations: V_{EE} = −5.2V ±5% recommended**
- **Complementary OR/NOR outputs**
- **Open emitter logic and bussing capability**

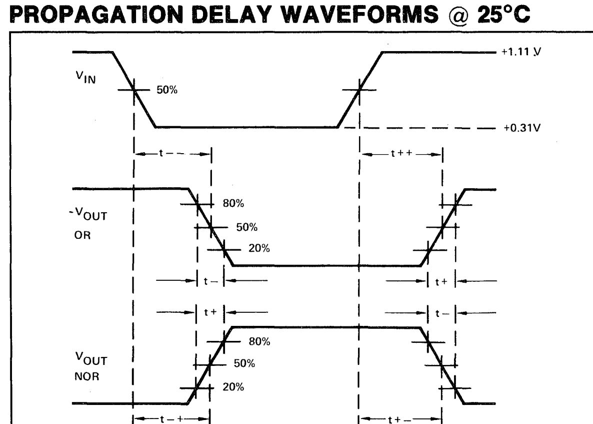
SWITCHING TIME TEST CIRCUIT



CIRCUIT SCHEMATIC



PROPAGATION DELAY WAVEFORMS @ 25°C



NOTES:

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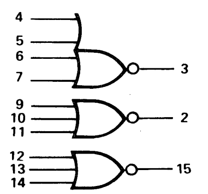
2. For AC tests, all input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be <¼ inch from TP_{in} to input pin and TP_{out} to output pin. A 50-ohm termination to ground is located in each scope input. Unused outputs are connected to a 50-ohm resistor to ground.
3. Test procedures are shown for only one input or set of input conditions. Other inputs are tested in the same manner.
4. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.

LOGIC

10106-B,F

LOGIC DIAGRAM

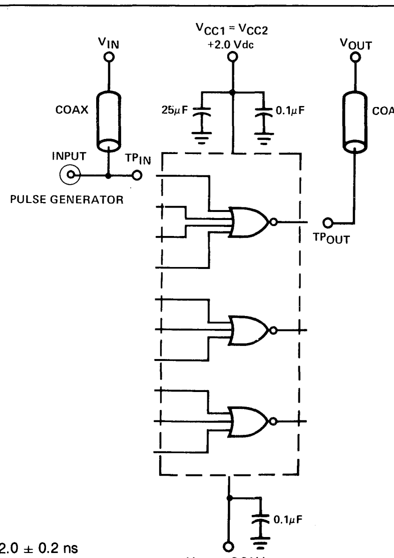


V_{CC1} = 1, V_{CC2} = 16, V_{EE} = 8
Positive logic: high level = '1'

FEATURES

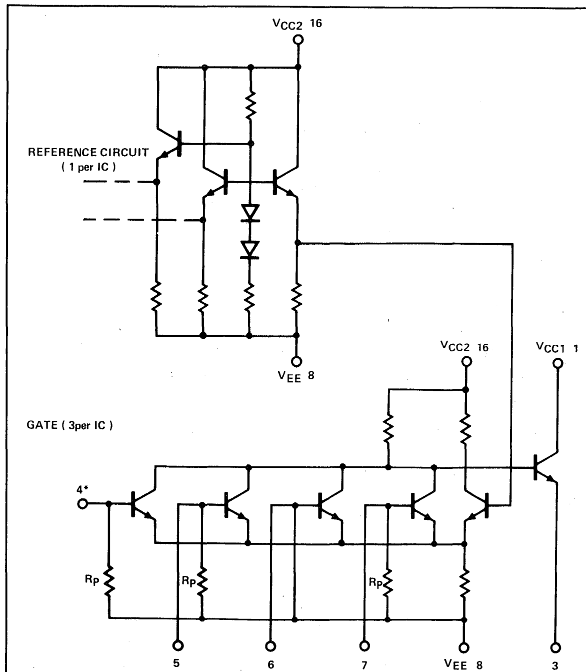
- **Fast propagation delay = 2.0 ns TYP**
- **Low power dissipation = 75 mW/package TYP (no load)**
- **Very high fanout capability — can drive 50 Ω lines**
- **High Z inputs — internal 50 kΩ pulldowns**
- **High immunity from power supply variations: V_{EE} = −5.2 V ±5% recommended**
- **Open emitter logic and bussing capability**

SWITCHING TIME TEST CIRCUIT



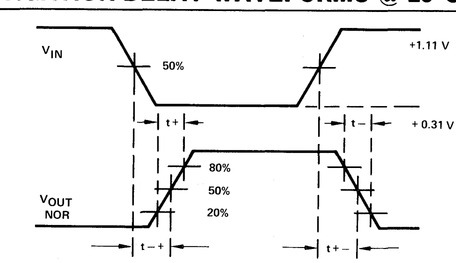
Input pulse
t+ = t− = 2.0 ± 0.2 ns
(20% to 80%)

CIRCUIT SCHEMATIC



All Rp = 50 kΩ.
*4th input on one gate only.

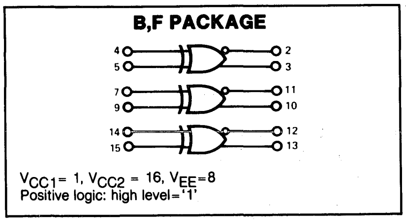
PROPAGATION DELAY WAVEFORMS @ 25°C



NOTES:

1. Each ECL 10,000 series device has been designed to meet the DC specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Voltage levels will shift approximately 3 mV with an air flow of 200 linear fpm. Outputs are terminated through a 50-ohm resistor to 2.0 volts.
2. For AC tests, all input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be <¼ inch from TP_{in} to input pin and TP_{out} to output pin. A 50-ohm termination to ground is located in each scope input. Unused outputs are connected to a 50-ohm resistor to ground.
3. Test procedures are shown for only one input or set of input conditions. Other inputs are tested in the same manner.
4. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.

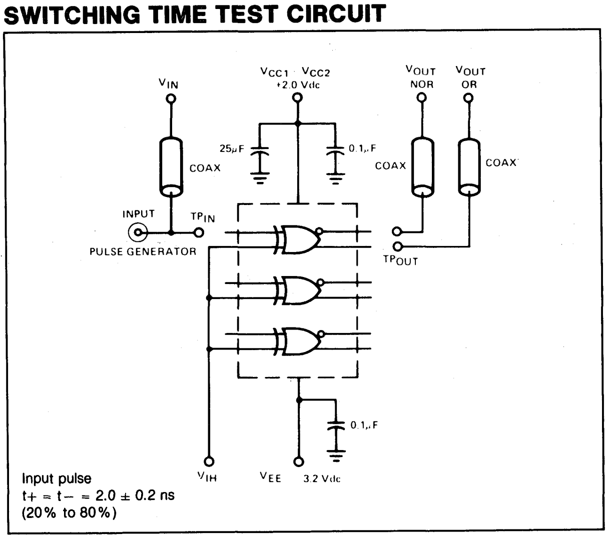
LOGIC DIAGRAM



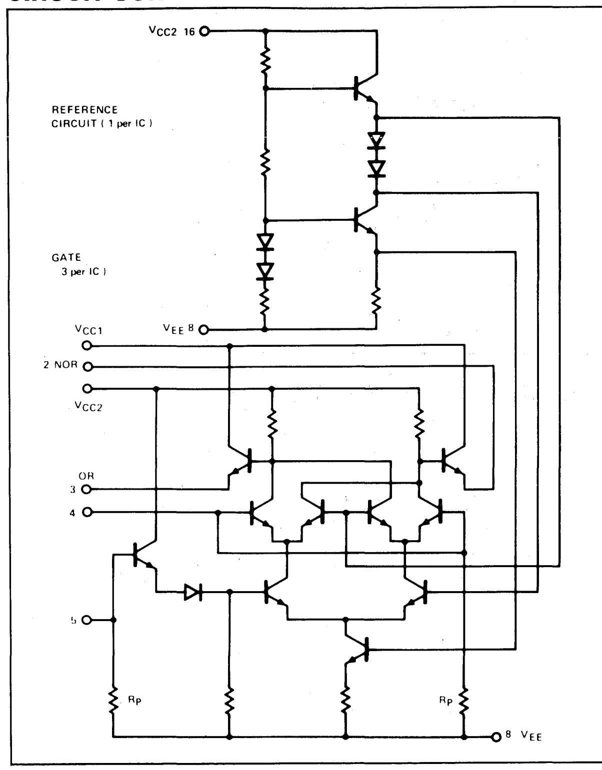
FEATURES

- **Fast propogation delay**
  - **2.0 ns TYP (inputs 4,9,14)**
  - **2.8 ns TYP (inputs 5,7,15)**
- **Low power dissipation=115 mW/package TYP (no load)**
- **Very high fanout capability — can drive six 50 Ω lines**
- **High Z inputs — internal 50kΩ pulldowns**
- **High immunity from power supply variations: V_{EE} = −5.2V ± 5% recommended**
- **Complementary OR/NOR outputs**
- **Open emitters for bussing and logic capability**

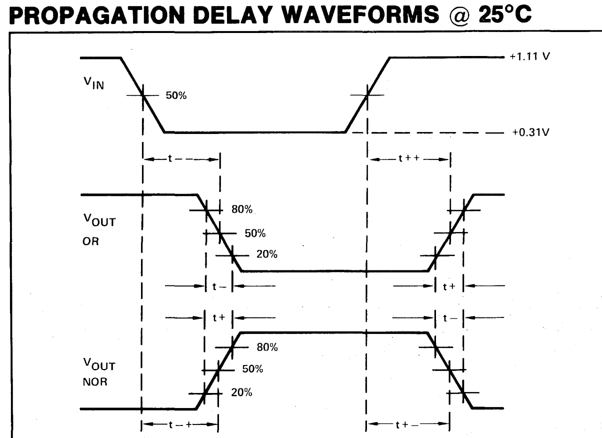
SWITCHING TIME TEST CIRCUIT



CIRCUIT SCHEMATIC



PROPAGATION DELAY WAVEFORMS @ 25°C



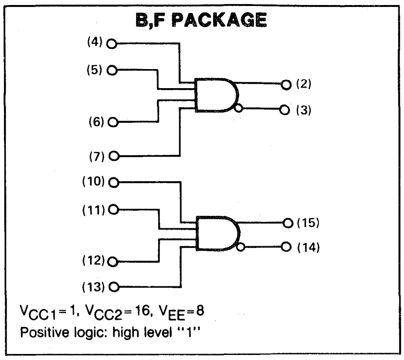
NOTES:

1. Each ECL 10,000 series device has been designed to meet the DC specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Voltage levels will shift approximately 4 mV with an air flow of 200 linear fpm. Outputs are terminated through a 50-ohm resistor to 2.0 volts.
2. For AC tests, all input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be <¼ inch from TP_{in} to input pin and TP_{out} to output pin. A 50-ohm termination to ground is located in each scope input. Unused outputs are connected to a 50-ohm resistor to ground.
3. Test procedures are shown for only one input or set of input conditions. Other inputs are tested in the same manner.
4. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.

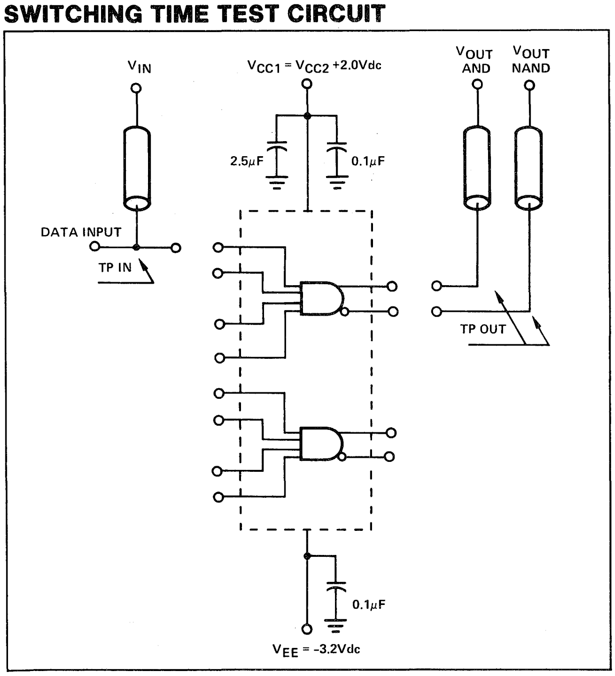
DUAL 4-INPUT AND/NAND GATE 10108

10108-B,F

LOGIC DIAGRAM



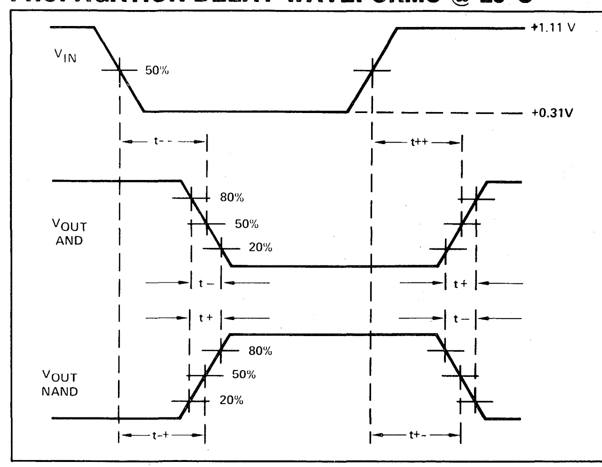
SWITCHING TIME TEST CIRCUIT



FEATURES

- **High speed propagation delay**
  2.3ns typical for AND
  2.8ns typical for NAND
- **Low power — 145mW/package typical**
- **High fanout — can drive 50 lines**
- **High Z inputs with 50kΩ pull down resistors**
- **Open emitter outputs for bussing applications**
- **Useful AND/NAND function**

PROPAGATION DELAY WAVEFORMS @ 25°C



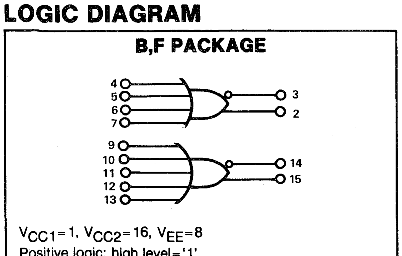
NOTES:

1. Each ECL 10,000 series device has been designed to meet the DC specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Voltage levels will shift approximately 4 mV with an air flow of 200 linear fpm. Outputs are terminated through a 50-ohm resistor to 2.0 volts.
2. For AC tests, all input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be <¼ inch from TP_{in} to input pin and TP_{out} to output pin. A 50-ohm termination to ground is located in each scope input. Unused outputs are connected to a 50-ohm resistor to ground.
3. Test procedures are shown for only one input or set of input conditions. Other inputs are tested in the same manner.
4. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.

DUAL 4-5 INPUT OR/NOR GATE 10109

10109B,F

LOGIC DIAGRAM

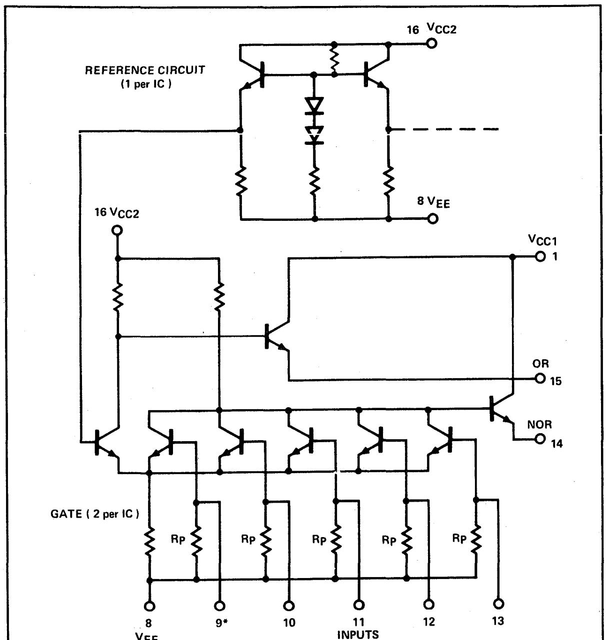


FEATURES

- **Fast propagation delay=2.0 ns TYP**
- **Low power dissipation=50mW/package TYP (no load)**
- **High fanout capability — can drive 50kΩ lines**
- **High Z inputs — internal 50kΩ pulldowns**
- **High immunity from power supply variations: V_{EE} = −5.2V ±5% recommended**
- **Complementary OR/NOR outputs**
- **Open emitters for bussing and logic capability**

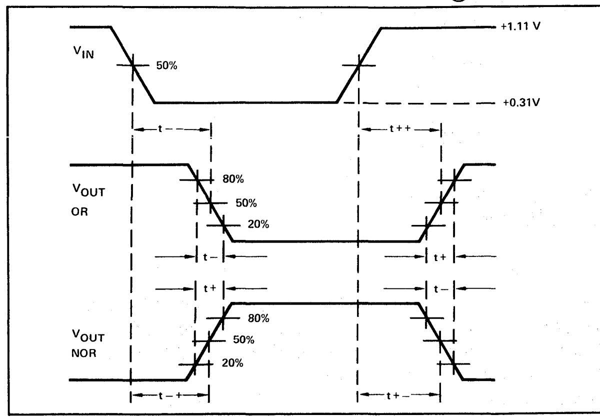
10109B,F

SWITCHING TIME TEST CIRCUIT



Input pulse
t+ = t- = 2.0 ± 0.2ns
(20% to 80%)

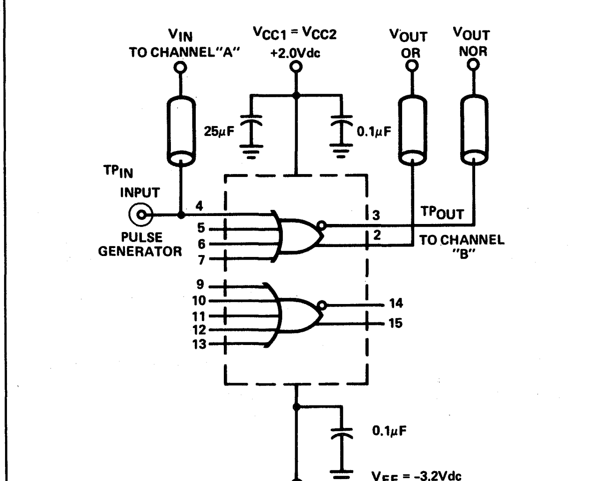
PROPAGATION DELAY WAVEFORMS @ 25°C



NOTES:

1. Each ECL 10,000 series device has been designed to meet the DC specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Voltage levels will shift approximately 2 mV with an air flow of 200 linear fpm. Outputs are terminated through a 50-ohm resistor to − 2.0 volts.
2. For AC tests, all input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be <¼ inch from TP_{in} to input pin and TP_{out} to output pin. A 50-ohm termination to ground is located in each scope input. Unused outputs are connected to a 50-ohm resistor to ground.
3. Test procedures are shown for only one input or set of input conditions. Other inputs are tested in the same manner.
4. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.

CIRCUIT SCHEMATIC

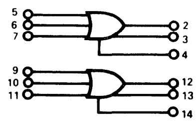


All Rp = 50kΩ.
*5th input on one gate only.

10110B,F

LOGIC DIAGRAM

B,F PACKAGE

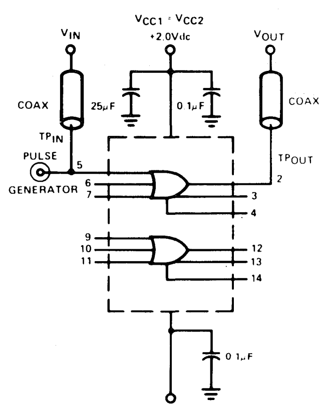


V_{CC1} = 1, 15, V_{CC2} = 16, V_{EE} = 8
Positive logic: high level = '1'

FEATURES

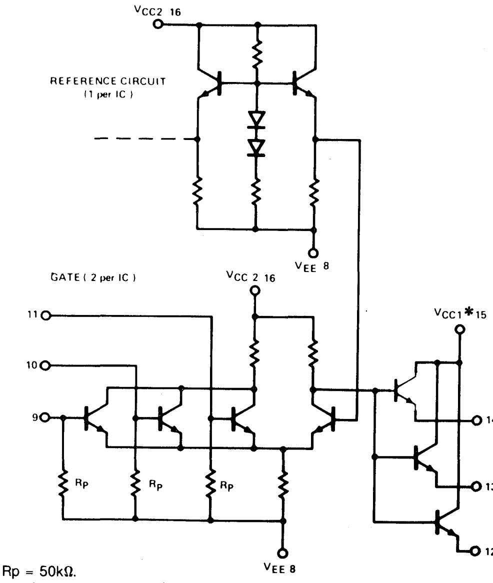
- **Fast propagation delay = 2.4 ns TYP (all outputs loaded)**
- **Power dissipation = 150mW/package TYP (no load)**
- **Very high fanout capability — can drive six 50kΩ lines**
- **High Z inputs — internal 50kΩ pulldowns**
- **High immunity from power supply variations: V_{EE} = −5.2V ±5% recommended**
- **Open emitters for bussing and logic capability**

SWITCHING TIME TEST CIRCUIT



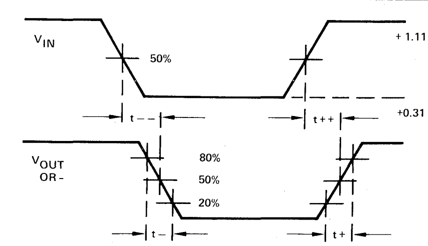
Input pulse
t+ = t- = 2.0 ± 0.2 ns
(20% to 80%)

CIRCUIT SCHEMATIC



All Rp = 50kΩ.
*V_{CC1} for other gate is pin 1.

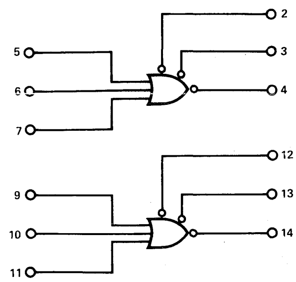
PROPAGATION DELAY WAVEFORMS @ 25°C



NOTES:
1. Each ECL 10,000 series device has been designed to meet the DC specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Voltage levels will shift approximately 5 mV with an air flow of 200 linear fpm. Outputs are terminated through a 50-ohm resistor to 2.0 volts.
2. For AC tests, all input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be <¼ inch from TP_{in} to input pin and TP_{out} to output pin. A 50-ohm termination to ground is located in each scope input. Unused outputs are connected to a 50-ohm resistor to ground.
3. Test procedures are shown for only one input or set of input conditions. Other inputs are tested in the same manner.
4. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.

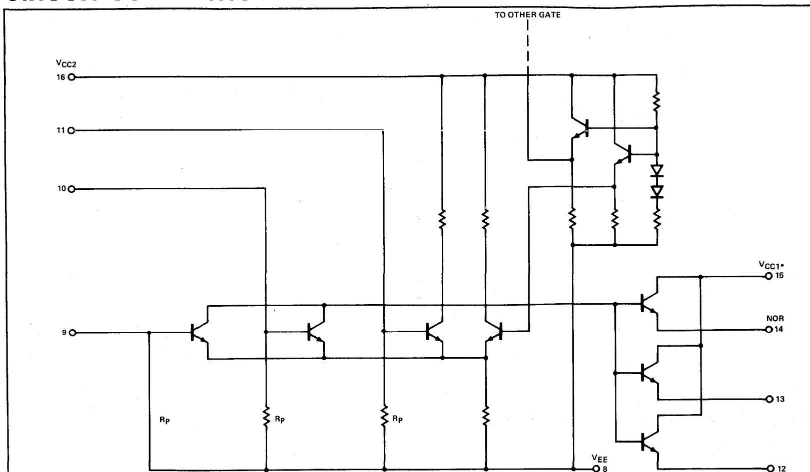
LOGIC DIAGRAM

B,F PACKAGE



V_{CC1} = 1, 15, V_{CC2} = 16, V_{EE} = 8
Positive logic: high level = '1'

CIRCUIT SCHEMATIC

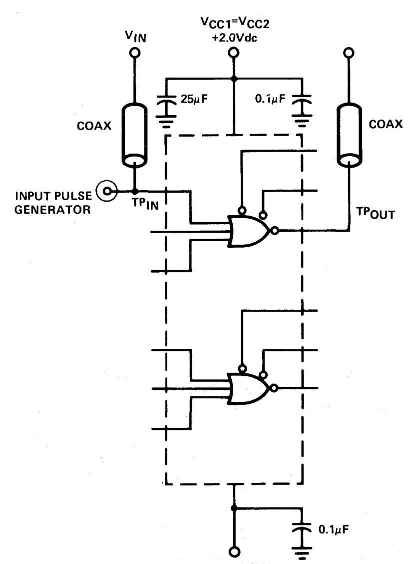


*V_{CC1} for other gate is pin 1. All Rp = 50kΩ.

FEATURES

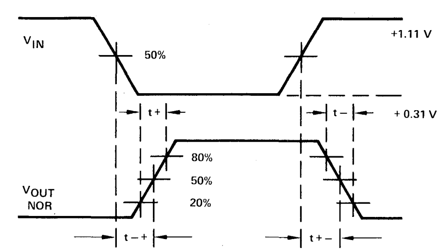
- **Fast propagation delay = 2.4 ns TYP (all outputs loaded)**
- **Power dissipation = 150mW/package TYP (no load)**
- **Very high fanout capability — can drive six 50 μ lines**
- **High Z inputs — internal 50kΩ pulldowns**
- **High immunity from power supply variations: V_{EE} = −5.2V ±5% recommended**
- **Open emitters for bussing and logic capability**

SWITCHING TIME TEST CIRCUIT



Input pulse
t+ = t- = 2.0 ± 0.2 ns
(20% to 80%)

PROPAGATION DELAY WAVEFORMS @ 25°C



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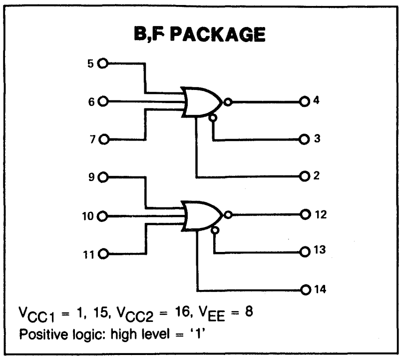
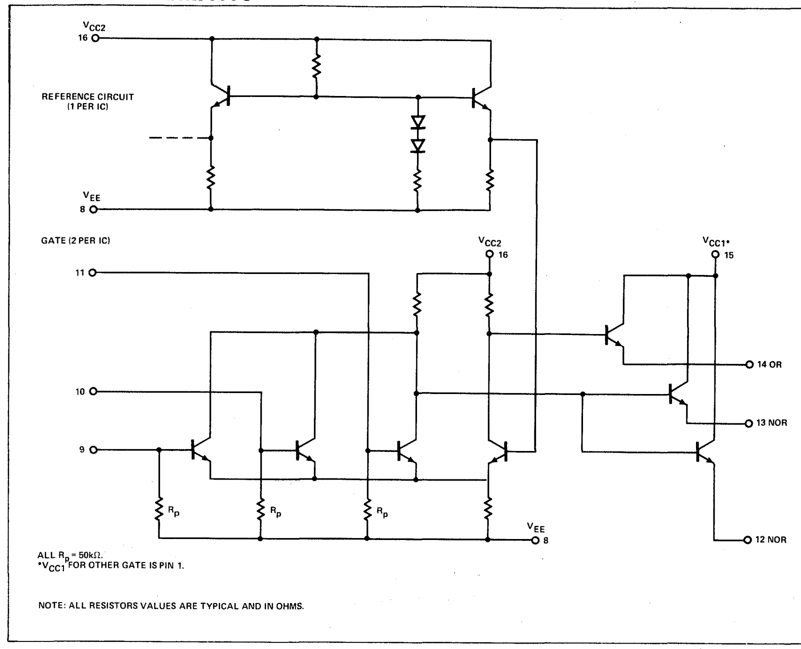
3. Test procedures are shown for only one input or set of input conditions. Other inputs are tested in the same manner.
4. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.

10112B,F

LOGIC DIAGRAM



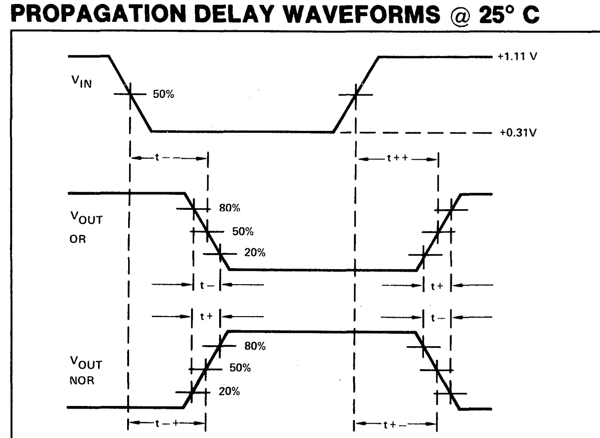
CIRCUIT SCHEMATIC



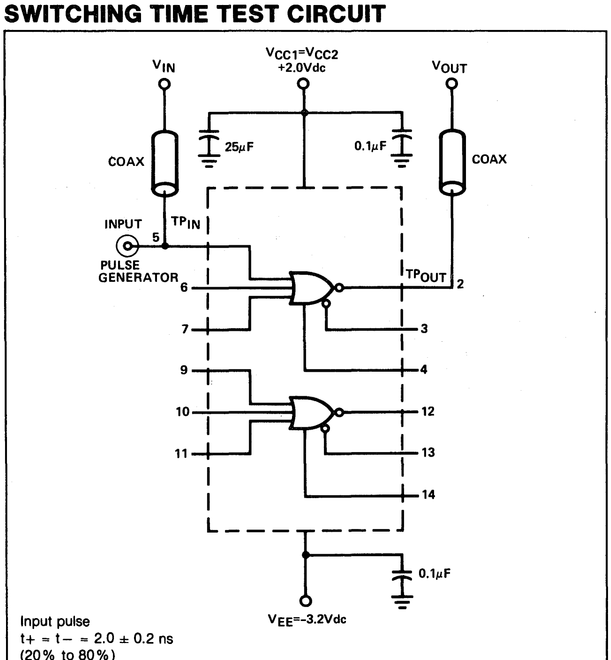
FEATURES

- **Fast propagation delay = 2.4 ns TYP (all outputs loaded)**
- **Power dissipation = 150 mW/package TYP (no load)**
- **Very high fanout capability — can drive six 50 Ω lines**
- **High Z inputs — internal 50kΩ pulldowns**
- **High immunity from power supply variations: V_{EE} = −5.2 V±5% recommended**
- **Open emitters for bussing and logic capability**

PROPAGATION DELAY WAVEFORMS @ 25° C



SWITCHING TIME TEST CIRCUIT



NOTES:

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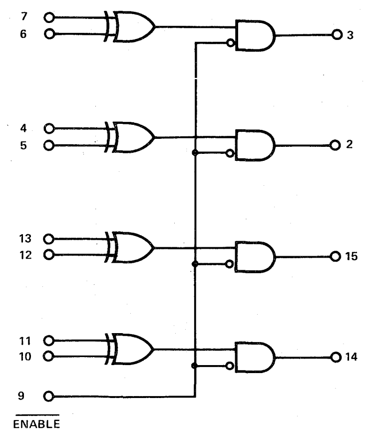
2. For AC tests, all input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be <¼ inch from TP_{in} to input pin and TP_{out} to output pin. A 50-ohm termination to ground is located in each scope input. Unused outputs are connected to a 50-ohm resistor to ground.
3. Test procedures are shown for only one input or set of input conditions. Other inputs are tested in the same manner.
4. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
5. Pin 1 = Pin 15 = Pin 16 = V_{CC} = 0 V, Pin 8 = V_{EE} = −5.2 V.
6. Pin 1 = Pin 15 = Pin 16 = V_{CC} = +2.0 V, Pin 8 = V_{EE} = −3.2 V.

LOGIC DIAGRAM

B,F PACKAGE



V_{CC1} = 1, V_{CC2} = 16, V_{EE} = 8
Positive logic: high level = '1'

FEATURES

- **Performs 4-bit compare function (if outputs are wire- ORed together)**
- **High functional density — four exclusive OR gates/package**
- **Fast propagation delay for exclusive or: 2.5 ns TYP**
- **Low power dissipation: 165 mW/package TYP (no load)**
- **High fanout capability — can drive four 50 Ω lines**
- **High Z inputs — internal 50kΩ pulldowns**
- **High immunity from power supply variations: V_{EE} = −5.2V ±5% recommended**
- **Open emitter logic and bussing capability**
- **Output enable gating makes powerful logic function**

APPLICATIONS

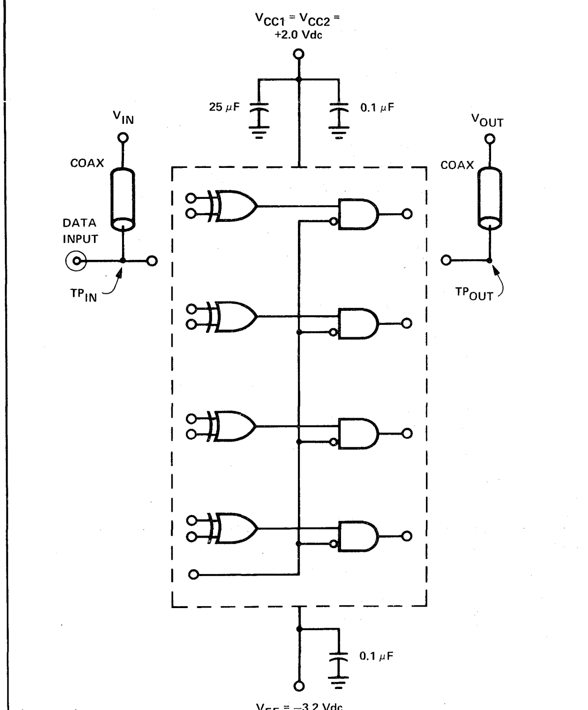
- **QUAD EXCLUSIVE-OR**
  (For parity, error correcting, and other logic functions).
- **FOUR-BIT COMPARATOR**
  (For logic, test equipment, error detection applications).
- **GATED FOUR-BIT COMPARATOR**
  (Enable input permits wire-ORing multiples of four bits)

TRUTH TABLE

$\overline{E9}$	IN 7	IN 6	OUT 3
L	L	L	L
L	L	H	H
L	H	L	H
L	H	H	L
H	φ	φ	L

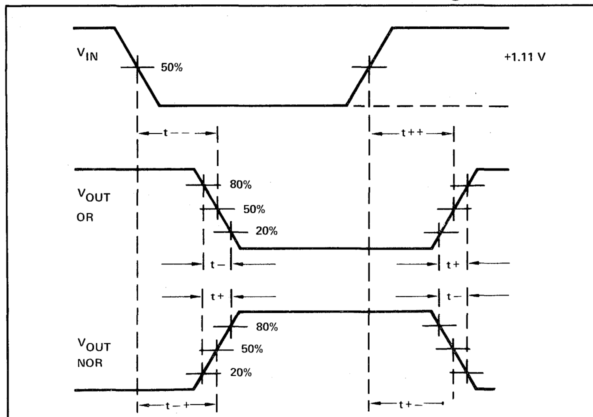
φ = Don't Care.

SWITCHING TIME TEST CIRCUIT



Input pulse
t+ = t− = 2.0 ± 0.2 ns
(20% to 80%)

PROPAGATION DELAY WAVEFORMS @ 25°C

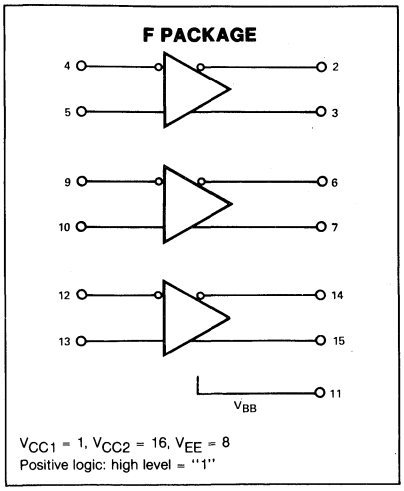


NOTES:

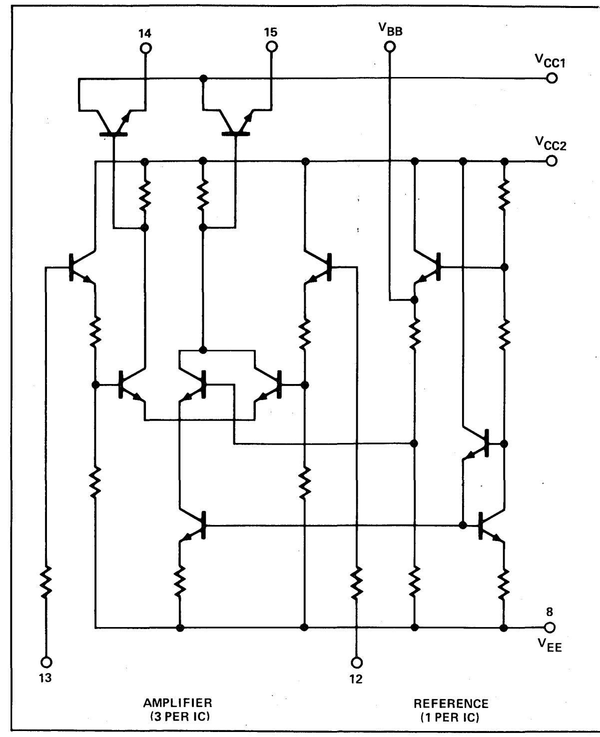
1. Each ECL 10,000 series device has been designed to meet the DC specifications shown in the test table, after thermal equilibruim has been established. The circuit is in a test socket or mounted on a linear printed circuit board and transverse air flow greater than 500 fpm is maintained. Voltage levels will shift approximately 4 mV with an air flow of 200 linear fpm. Outputs are terminated through a 50-ohm resistor to −2.0 volts.
2. For AC tests, all input and output cables to the scope are equal lengths of 50 ohm coaxial cable. Wire length should be <1/4 inch from TP_{in} to input pin and TP_{out} to output pin. A 50-ohm termination to ground is located in each scope input. Unused outputs are connected to a 50-ohm resistor to ground.
3. Test procedures are shown for only one input or set of input conditions. Other inputs are tested in the same manner.
4. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.

10114F

LOGIC DIAGRAM



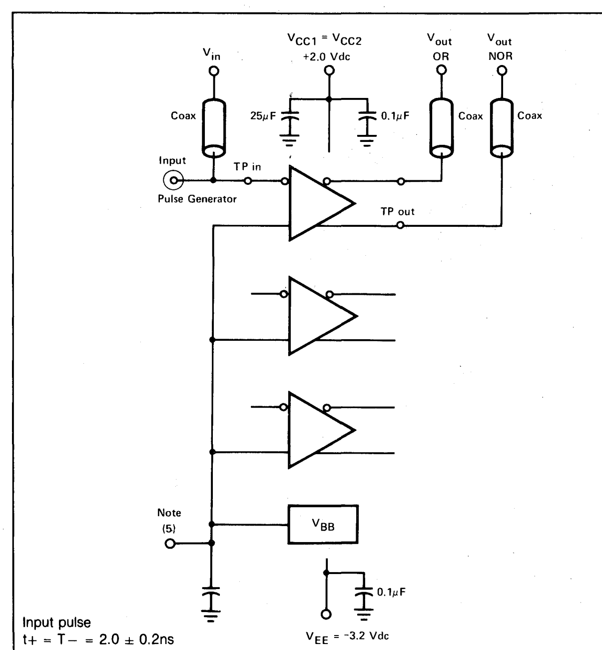
CIRCUIT SCHEMATIC



FEATURES

- **Guaranteed common mode noise rejection of 1 volt**
- **Fast propagation delay = 2.0ns TYP (differential input)**
- **Output level specified — inputs open**
- **High fanout capability — can drive 50Ω lines**
- **Very high input Z — no 50k pulldowns**
- **High immunity from power supply variations: V_{EE} = −5.2V ±5% recommended**
- **Complementary outputs**
- **Open emitter logic and bussing capability**
- **V_{BB} voltage available on pin 11 or**
- **Outputs go to logic "0" level when input left open**

SWITCHING TIME TEST CIRCUIT

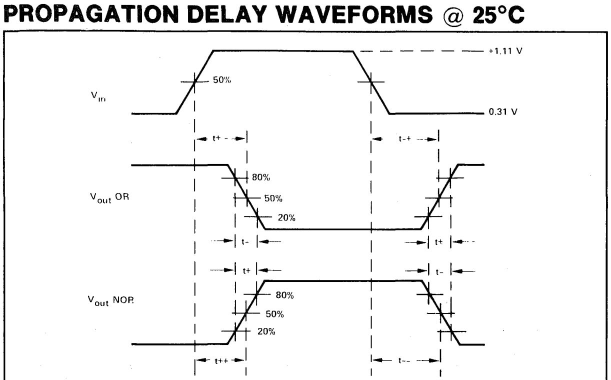


COMMON MODE REJECTION TEST

	TEST CONDITIONS*				V_{OH}		V_{OL}		
	V_{IHH}	V_{ILH}	V_{IHL}	V_{ILL}	MIN	TYP	MIN	TYP	UNIT
-30°C	+0.110	-0.890	-1.890	-2.890	-1.060	-0.890	-1.890	-1.675	V
+25°C	+0.100	-0.850	-1.810	-2.850	-0.960	-0.810	-1.850	-1.650	V
+85°C	+0.300	-0.825	-1.700	-2.825	-0.890	-0.700	-1.825	-1.615	V

*Logic levels shifted positive 1V for test.

PROPAGATION DELAY WAVEFORMS @ 25°C

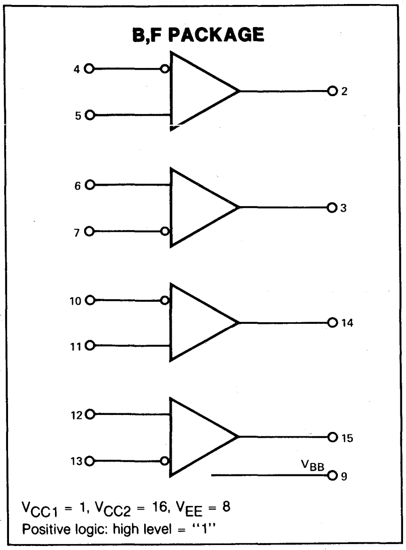


NOTES:

1. Each ECL 10,000 series device has been designed to meet the DC specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Voltage levels will shift approximately 3 mV with an air flow of 200 linear fpm. Outputs are terminated through a 50-ohm resistor to -2.0 volts.
2. For AC tests, all input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be < ¼ inch from TP_{in} to input pin and TP_{out} to output pin. A 50-ohm termination to ground is located in each scope input. Unused outputs are connected to a 50-ohm resistor to ground.
3. Test procedures are shown for only one input or set of input conditions. Other inputs are tested in the same manner.
4. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
5. One input from each gate must be tied to V_{BB} (Pin 11 during testing).

10115B,F

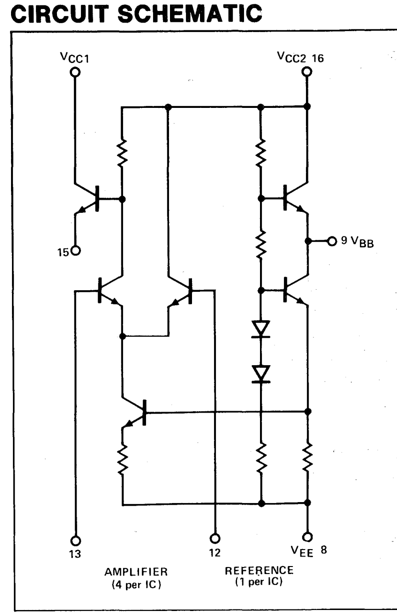
LOGIC DIAGRAM



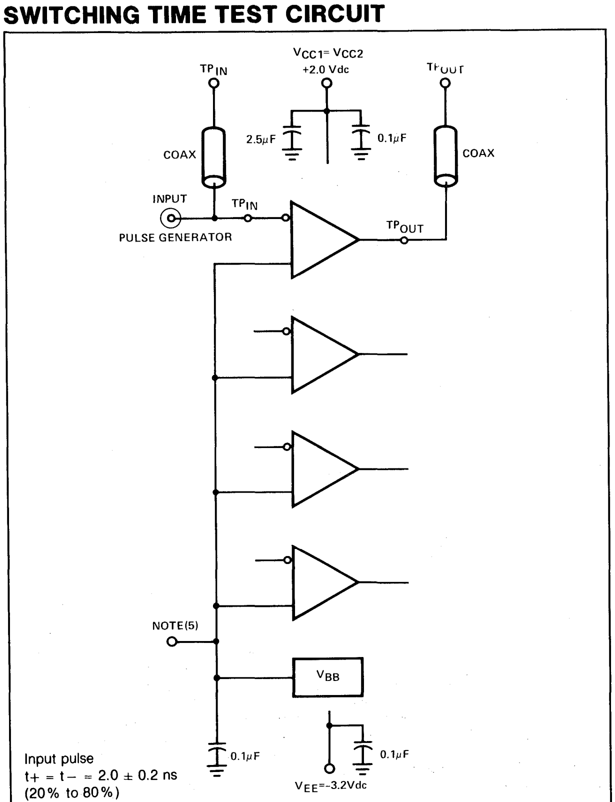
FEATURES

- Good common mode noise rejection
- Fast propagation delay = 2.0 ns TYP
- Low power dissipation = 100mW/package TYP (no load)
- High fanout capability — can drive 50Ω lines
- High system density — four receivers per package
- Very high input Z — no 50 k pulldowns
- High immunity from power supply variations: V_{EE} = −5.2V ±5% recommended
- Open emitter logic and bussing capability
- V_{BB} voltage available on pin 9

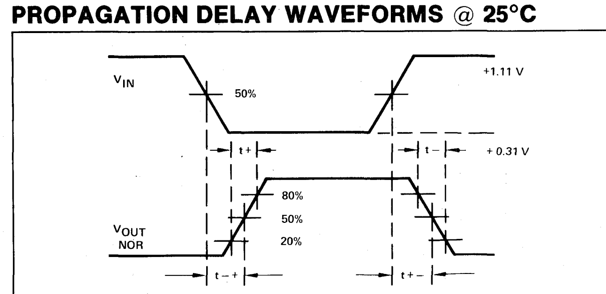
CIRCUIT SCHEMATIC



SWITCHING TIME TEST CIRCUIT



PROPAGATION DELAY WAVEFORMS @ 25°C



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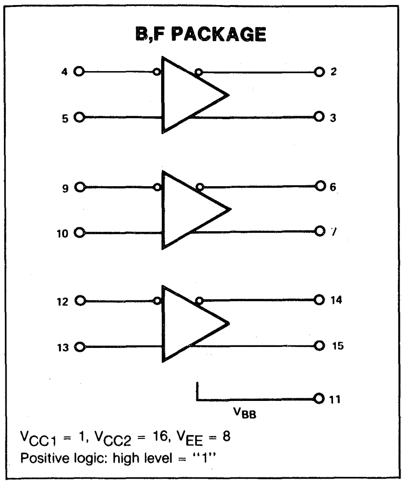
3. Test procedures are shown for only one input or set of input conditions. Other inputs are tested in the same manner.
4. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
5. One input from each gate must be tied to V_{BB} (Pin 9) during testing.

LOGIC DIAGRAM



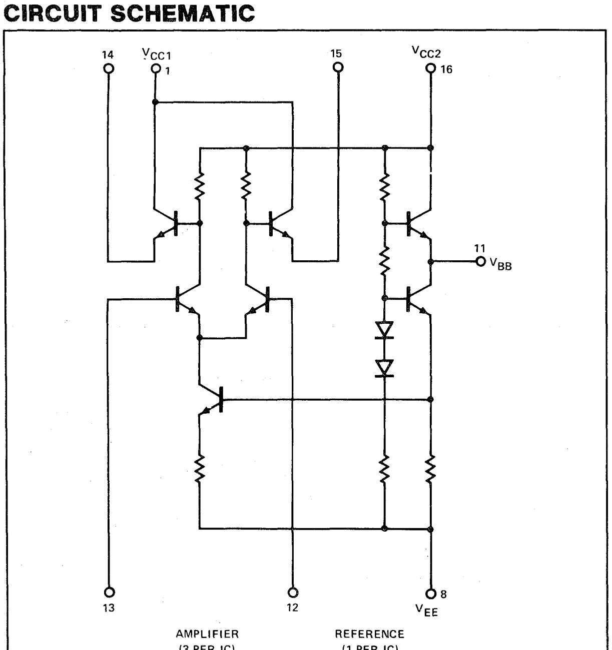
FEATURES

- **Good common mode noise rejection**
- **Fast propagation delay = 2.0 ns TYP**
- **Low power dissipation = 83 mW/package TYP (no load)**
- **High fanout capability — can drive 50Ω lines**
- **Very high input Z — no 50 k pulldowns**
- **High immunity from power supply variations: V_{EE} = −5.2 V ±5% recommended**
- **Complementary outputs**
- **Open emitter logic and bussing capability**
- **V_{BB} voltage available on pin 11**

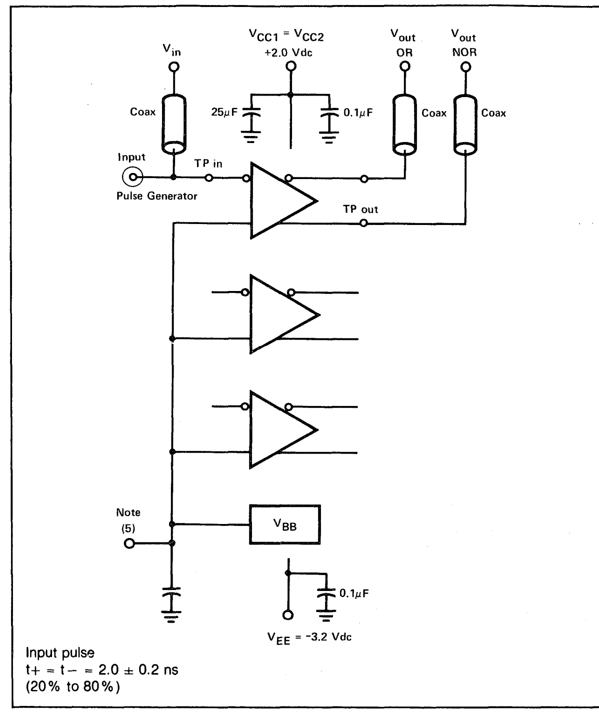
OPERATION NOTE

If any amplifier in a package is not used, one input of that amplifier must be connected to V_{BB} (pin 11) to prevent upsetting the current source bias network.

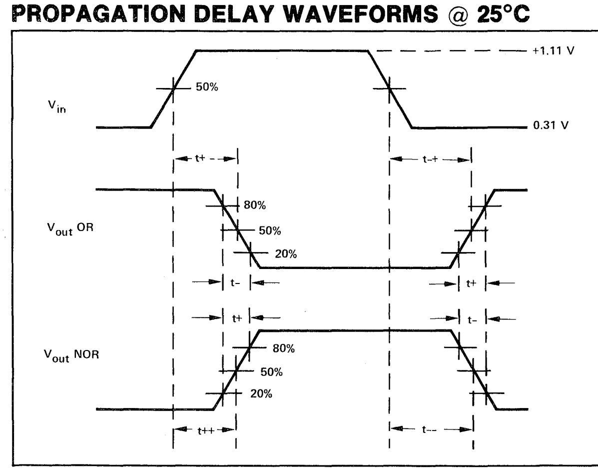
CIRCUIT SCHEMATIC



SWITCHING TIME TEST CIRCUIT



PROPAGATION DELAY WAVEFORMS @ 25°C



NOTES:

1. Each ECL 10,000 series device has been designed to meet the DC specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Voltage levels will shift approximately 3 mV with an air flow of 200 linear fpm. Outputs are terminated through a 50-ohm resistor to 2.0 volts.
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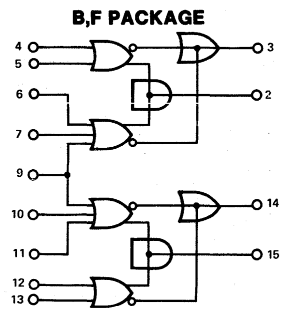
3. Test procedures are shown for only one input or set of input conditions. Other inputs are tested in the same manner.
4. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
5. One input from each gate must be tied to V_{BB} (Pin 11) during testing.

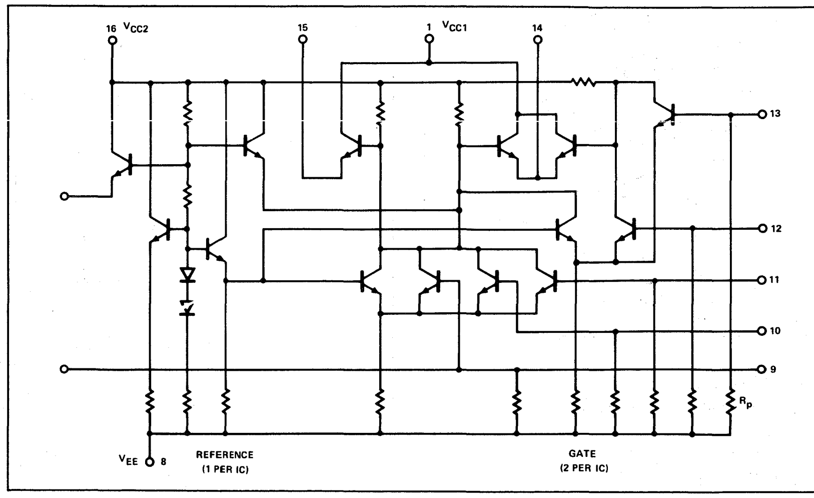
10117-B,F

LOGIC DIAGRAM



V_{CC1} = 1, V_{CC2} = 16, V_{EE} = 8
Positive logic: high level = "1"

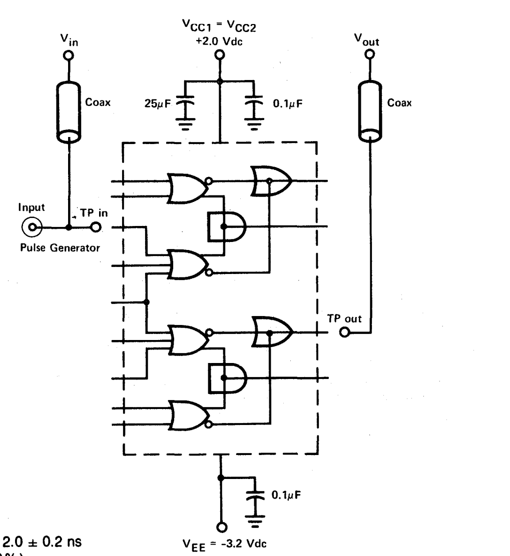
CIRCUIT SCHEMATIC



FEATURES

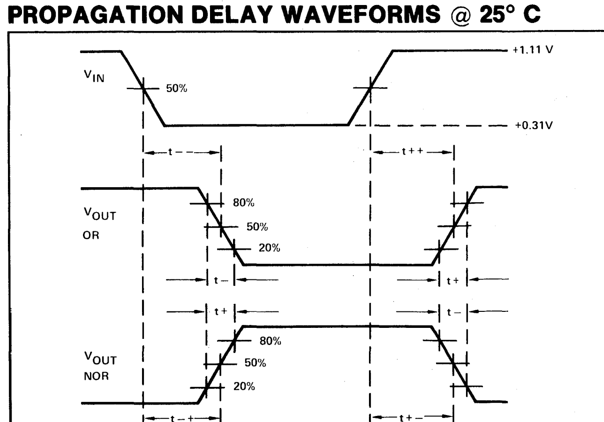
- **Fast propagation delay for two logic levels = 2.3 ns TYP**
- **Power dissipation = 100 mW/package TYP (no load)**
- **Very high fanout capability — can drive 50Ω lines**
- **High Z inputs — 50 kΩ pulldowns**
- **High immunity from power supply variations: V_{EE} = −5.2V ±5% recommended**
- **Open emitters for bussing and logic capability**
- **Outputs may be cross coupled back to inputs to make a latch function**

SWITCHING TIME TEST CIRCUIT



Input pulse
t+ = t− = 2.0 ± 0.2 ns
(20% to 80%)

PROPAGATION DELAY WAVEFORMS @ 25° C



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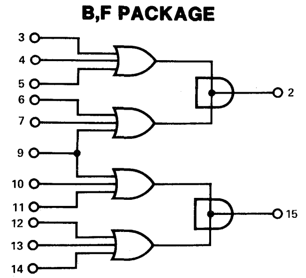
2. For AC tests, all input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be <¼ inch from TP_{in} to input pin and TP_{out} to output pin. A 50-ohm termination to ground is located in each scope input. Unused outputs are connected to a 50-ohm resistor to ground.
3. Test procedures are shown for only one input or set of input conditions. Other inputs are tested in the same manner.
4. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.

LOGIC

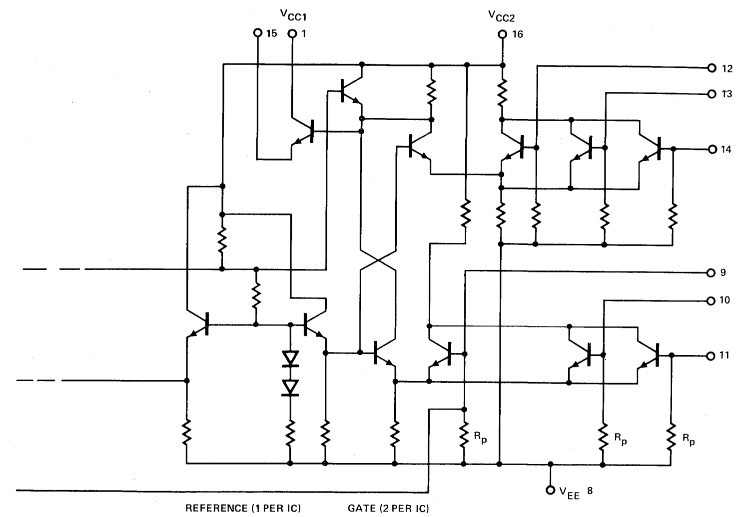
10118B,F

LOGIC DIAGRAM



V_{CC1} = 1, V_{CC2} = 16, V_{EE} = 8
Positive logic: high level = '1'

CIRCUIT SCHEMATIC



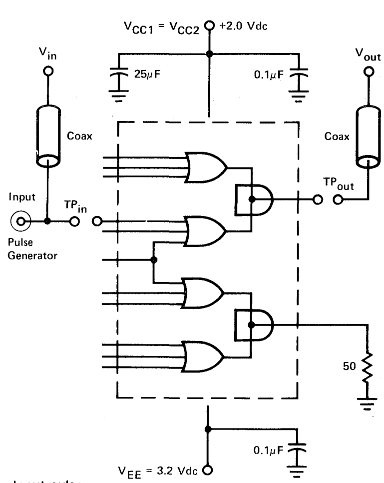
ALL R_p = 50kΩ.

NOTE: ALL RESISTORS VALUES ARE TYPICAL AND IN OHMS.

FEATURES

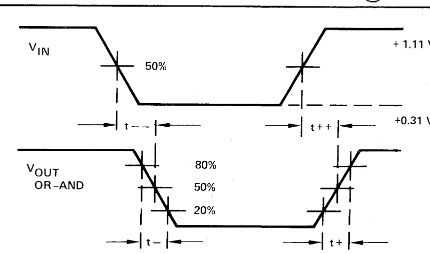
- **Fast propagation delay for 2 logic levels = 2.3 ns TYP**
- **Low power dissipation = 100mW/package TYP (no load)**
- **High fanout capability — can drive 50Ω line**
- **High Z inputs — internal 50kΩ pulldowns**
- **High immunity from power supply variations: V_{CC}= -5.2V ±5% recommended**
- **Open emitter logic and bussing capability**

SWITCHING TIME TEST CIRCUIT



Input pulse
t+ = t− = 2.0 ± 0.2 ns
(20% to 80%)

PROPAGATION DELAY WAVEFORMS @ 25°C



NOTES:

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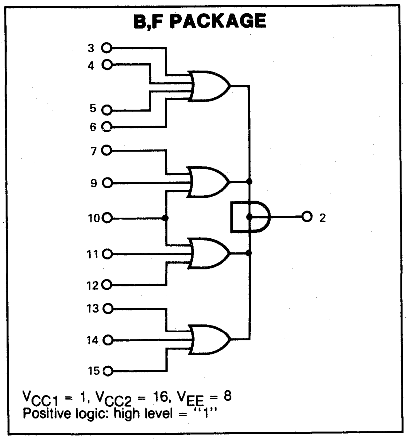
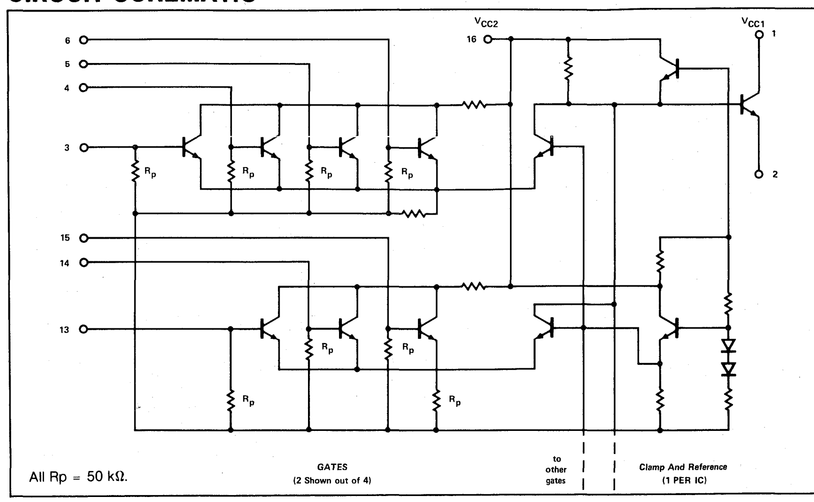
LOGIC DIAGRAM



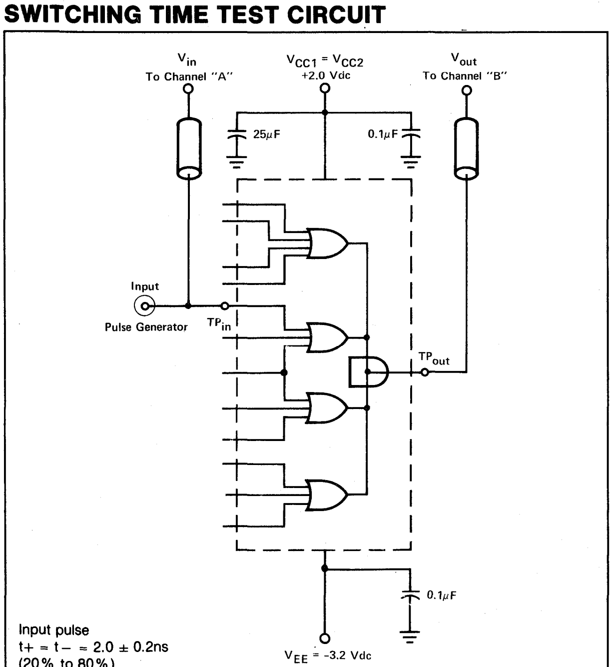
CIRCUIT SCHEMATIC



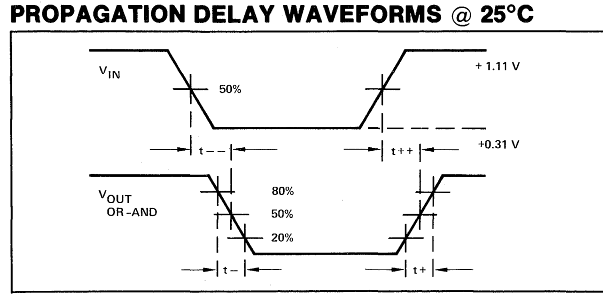
FEATURES

- **Fast propagation delay for 2 logic levels = 2.3 ns TYP**
- **Low power dissipation = 100 mW/package TYP (no load)**
- **High fanout capability — can drive 50Ω line**
- **High Z inputs — internal 50 kΩ pulldowns**
- **High immunity from power supply variations: V_{EE} = −5.2V ±5% recommended**
- **Open emitter logic and bussing capability**

SWITCHING TIME TEST CIRCUIT



PROPAGATION DELAY WAVEFORMS @ 25°C



NOTES:

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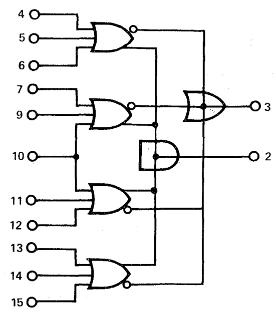
3. Test procedures are shown for only one input or set of input conditions. Other inputs are tested in the same manner.
4. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.

10121B,F

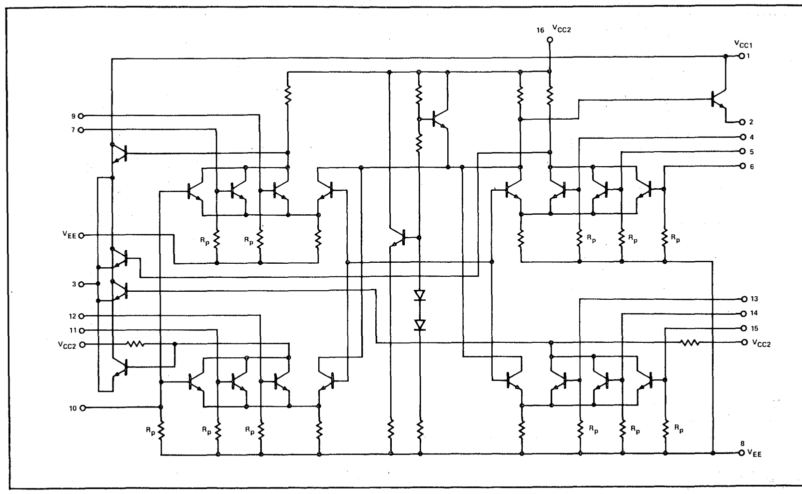
LOGIC DIAGRAM

B,F PACKAGE



V_{CC1} = 1, V_{CC2} = 16, V_{EE} = 8
Positive logic: high level = "1"

CIRCUIT SCHEMATIC



FEATURES

- **Fast propagation delay for 2 logic levels = 2.3 ns TYP**
- **Low power dissipation = 100 mW/package TYP (no load)**
- **High fanout capability — can drive two 50Ω lines**
- **High Z inputs — internal 50 kΩ pulldowns**
- **High immunity from power supply variations: V_{EE} = −5.2V ±5% recommended**
- **Open emitter logic and bussing capability**

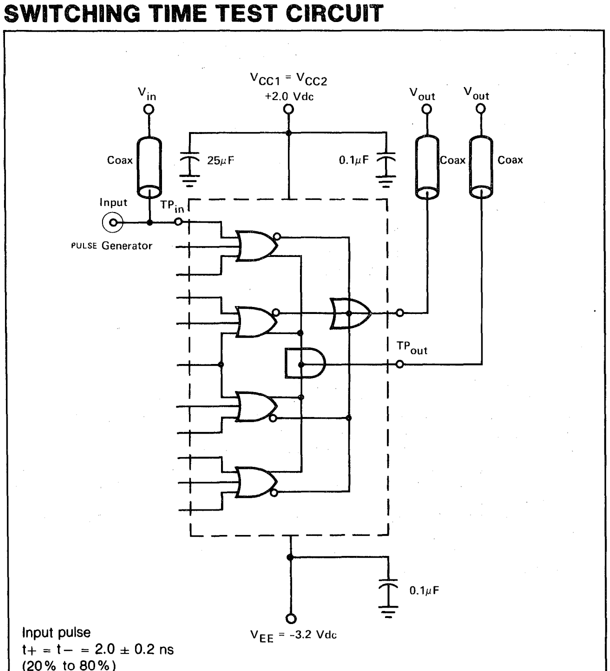
EQUATIONS (Positive Logic)

$2 = (4+5+6) \cdot (7+9+10) \cdot (10+11+12) \cdot (13+14+15)$

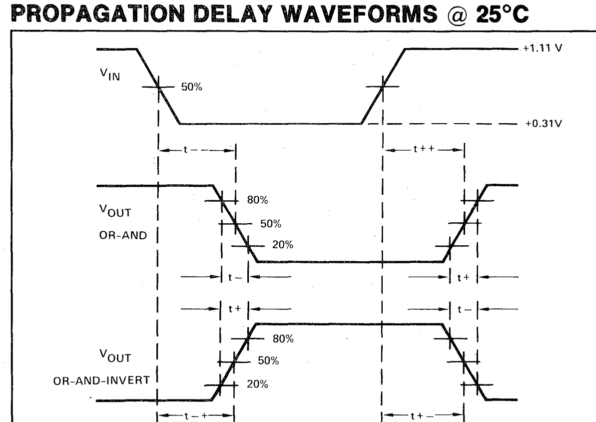
$3 = \overline{(4+5+6)} + \overline{(7+9+10)} + \overline{(10+11+12)} + \overline{(13+14+15)}$

$= \overline{(4+5+6) \cdot (7+9+10) \cdot (10+11+12) \cdot (13+14+15)}$

SWITCHING TIME TEST CIRCUIT



PROPAGATION DELAY WAVEFORMS @ 25°C



NOTES:

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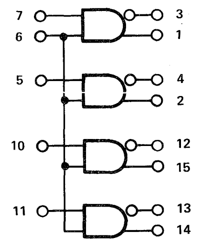
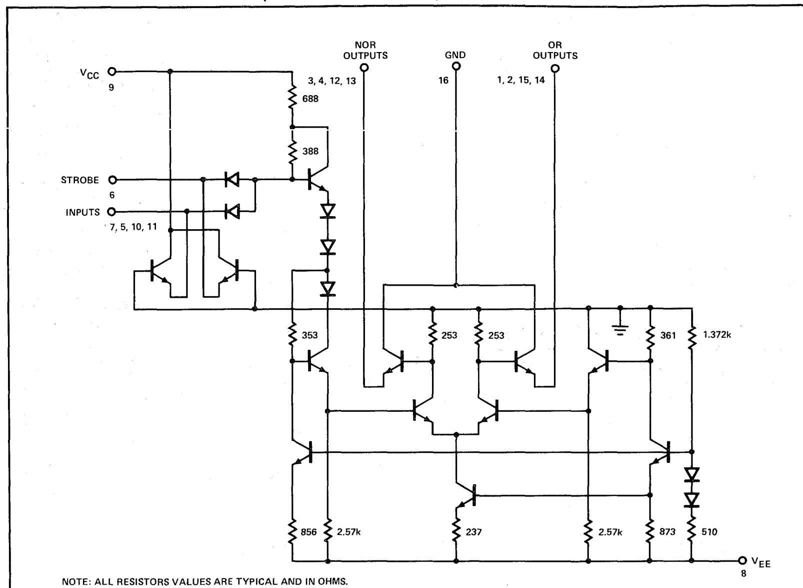
LOGIC DIAGRAM

B,F PACKAGE



V_{CC} = 9 GND = 16 V_{EE} = 8
Positive logic: high level = '1'

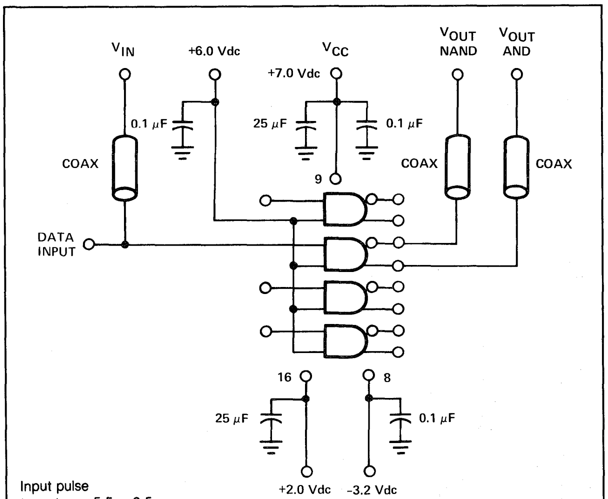
CIRCUIT SCHEMATIC (¼ of Circuit Shown)



FEATURES

- **Fast propagation delay = 5.0ns TYP**
- **Power dissipation = 340mW/package TYP**
- **Very high fanout capability**
  - **— can drive eight 50Ω lines**
  - **— DC output loading factor of 90x8**
- **Complementary outputs**
- **Standard ECL 10,000 series output levels**
- **Open emitter outputs for bussing and logic capability**
- **TTL compatible input strobe**
- **Input-clamp diodes**
- **Four translators per package**

SWITCHING TIME TEST CIRCUIT

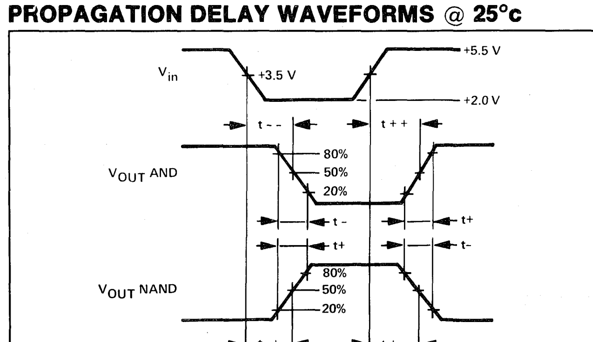


Input pulse
t+ = t− = 5.5 ± 0.5 ns
(100% to 90%)

SWITCHING CHARACTERISTICS — Test Limits 25°C

	PARAMETER		MIN	TYP	MAX	UNIT
I_R	Reverse Current					
		Pin 6			200	μA
		Pin 7			50	μA
I_F	Forward Current					
		Pin 6			-12.8	mA
		Pin 7			- 3.2	mA
BV_{IN}	Input Breakdown Voltage		5.5			V
	Positive Power Supply Drain Current					
		I_{CCH}			16	mA
		I_{CCL}			25	mA

PROPAGATION DELAY WAVEFORMS @ 25°c



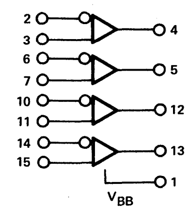
NOTES:

1. Each ECL 10,000 series device has been designed to meet the DC specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 fpm is maintained. Voltage levels will shift approximately 6 mV with an air flow of 200 linear fpm. Outputs are terminated through a 50-ohm resistor to −2.0 volts.
2. For AC tests, all input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be <¼ inch from TP_{in} to input pin and TP_{out} to output pin. A 50-ohm termination to ground is located in each scope input. Unused outputs are connected to a 50-ohm resistor to ground.
3. Test procedures are shown for only one input conditions. Other inputs are tested in the same manner.
4. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.

10125-B,F

LOGIC DIAGRAM

B,F PACKAGE



V_{CC}= 09 GND = 16 V_{EE} = 8
Positive logic: high level = '1'

FEATURES

- **Fast propagation delay = 5.0ns TYP**
- **Power dissipation=360mW/package TYP**
- **Differential inputs, ECL compatible**
- **ECL 10,000 level V_{BB} available**
- **Inverting or non-inverting function**
- **Schottky TTL totem pole outputs**
- **Recommended power supplies:**
  - **$V_{CC}=+5.0V$ DC ±5%**
  - **$V_{EE}=-5.2V$ DC ±5%**
- **Four translators per package**
- **Output levels specified for input voltage range +0.2V to −2.2V**
- **Common mode noise rejection of ±1 volt when used as Differential Line Receiver**

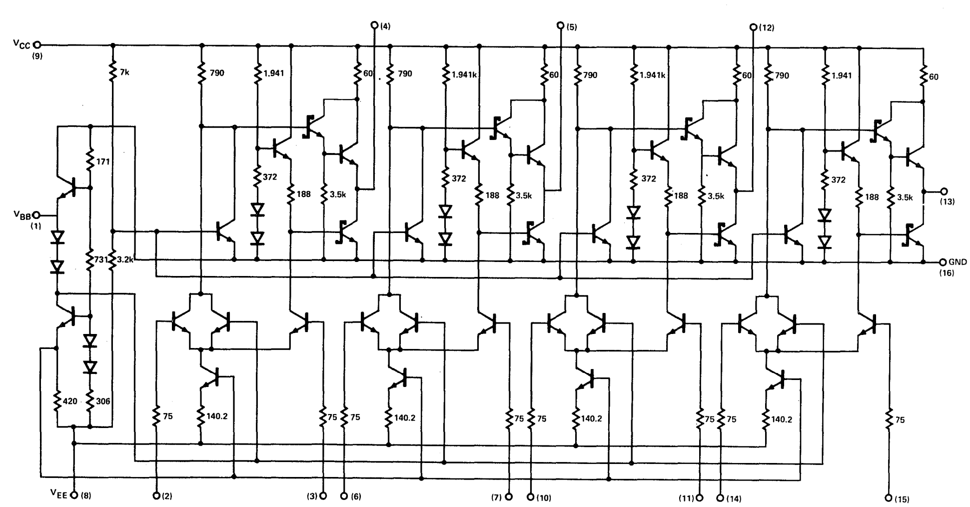
APPLICATIONS

- **Quad differential line receiver**
- **Quad ECL to TTL translator**
- **Quad MOS to TTL sense amp**
- **Quad level detector**

SWITCHING CHARACTERISTICS — Test Limits 25°C

PARAMETER		MIN	TYP	MAX	UNIT
	Positive Power Supply Drain Current				
	I_{CCH}			52	mA
	I_{CCL}			39	mA
I_{CBO}	Input Leakage Current			1.0	uA
I_{OS}	Short Circuit Current	40		100	mA
V_{BB}	Reference Voltage				
	-30°C	-1.420		-1.280	V
	+25°C	-1.350		-1.230	V
	+85°C	-1.295		-1.150	V

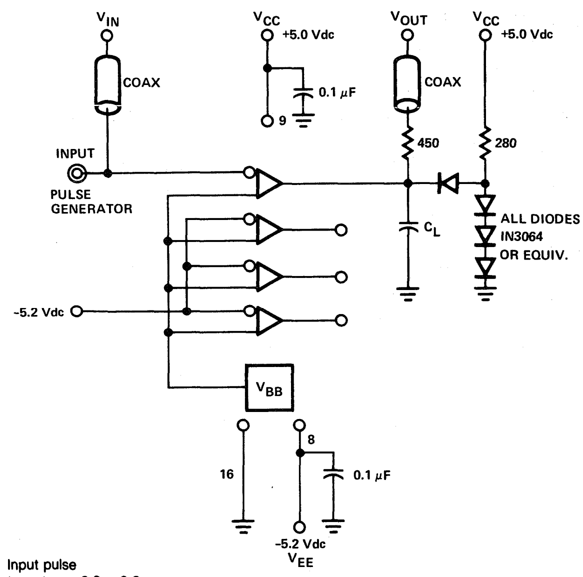
CIRCUIT SCHEMATIC



NOTE: ALL RESISTORS VALUES ARE TYPICAL AND IN OHMS.

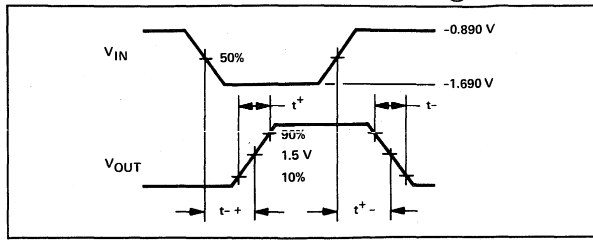
10125-B,F

SWITCHING TIME TEST CIRCUIT



Input pulse
t+ = t− = 2.0 ± 0.2 ns
(20% to 80%)
One input from each gate must be tied to V_{BB}
(Pin 1) during testing.

PROPAGATION DELAY WAVEFORMS @ 25°C



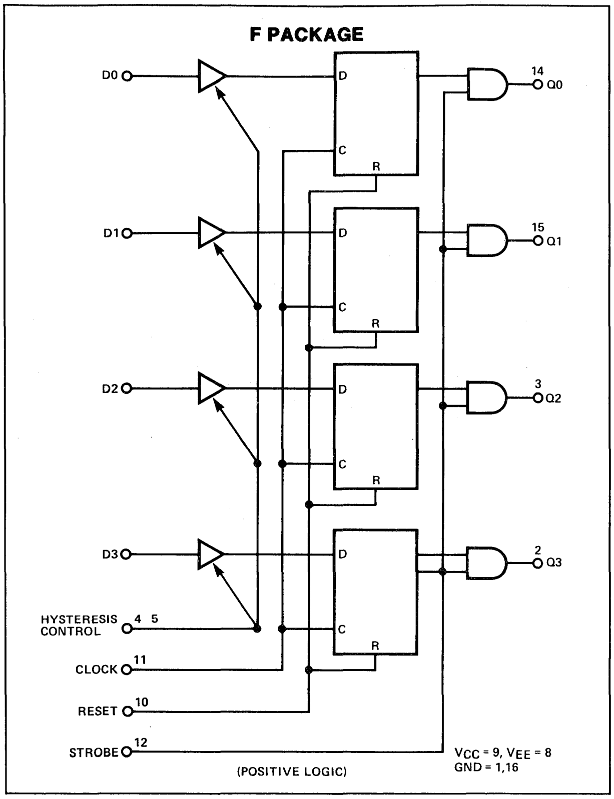
NOTES:

1. Each ECL 10,000 series device has been designed to meet the DC specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 fpm is maintained. The V_{BB} level will shift approximately 5 mV with an air flow of 200 linear fpm.
2. For AC tests, all input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be <¼ inch from TP_{in} to input pin and TP_{out} to output pin. A 50-ohm termination to ground is located in each scope channel input.
3. Test procedures are shown for only one input or set of input conditions. Other inputs are tested in the same manner.
4. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.

LOGIC

10129-F

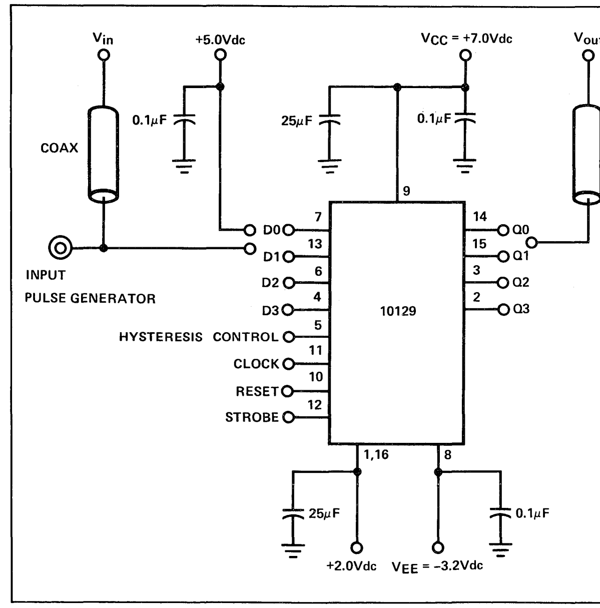
LOGIC DIAGRAM



FEATURES

- **Fast propagation delay —**
  12.0ns typical data to output
  4.0ns typical strobe to output
- **High fanout capability — can drive 50Ω lines**
- **On chip latches**
- **Accepts TTL and IBM data inputs; ECL 10K data outputs**
- **Hysteresis control pin**
- **High input Z — 50kΩ pull-down resistors on ECL inputs (no pulldowns on data inputs)**

SWITCHING TIME TEST CIRCUIT



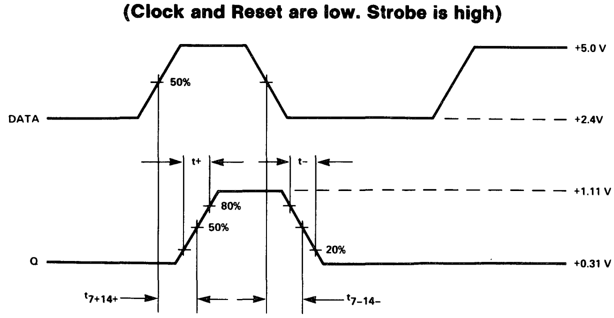
NOTES:
1. Unused outputs connected to ground through a 50Ω resistor.
2. 50Ω termination to ground located in each scope channel input.
3. All input and output cables to the scope are equal lengths of 50Ω coaxial cable and TP_{out} to output pin.

TRUTH TABLE (ø = Don't Care)

STROBE	RESET	C	D	Qn+1
L	ø	ø	ø	L
H	L	H	ø	Qn
H	ø	L	L	L
H	ø	L	H	H
ø	H	H	ø	L

VOLTAGE WAVEFORMS

Figure 1 — DATA TO OUTPUT
(Clock and Reset are low. Strobe is high)



VOLTAGE WAVEFORMS (Cont'd.)

10129-F

Figure 2 — STROBE TO OUTPUT
(Data is high. Clock and Reset are low)

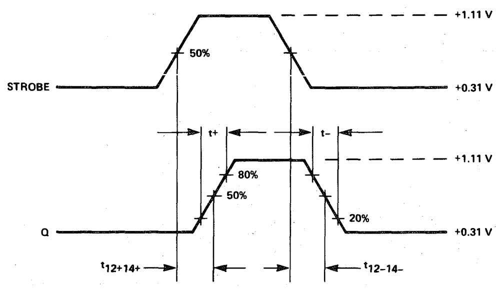


Figure 3 — RESET TO OUTPUT
(Data and Strobe are high)

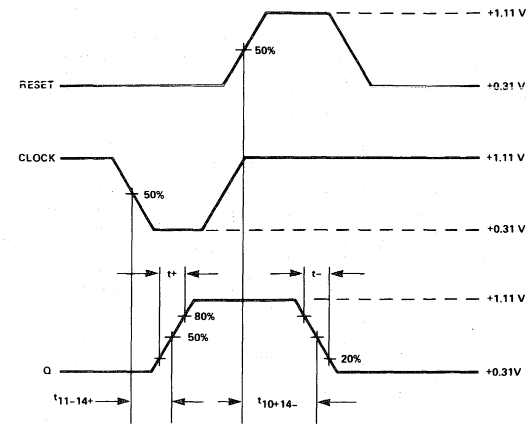


Figure 4 — CLOCK TO OUTPUT
(Reset is low. Strobe is high)

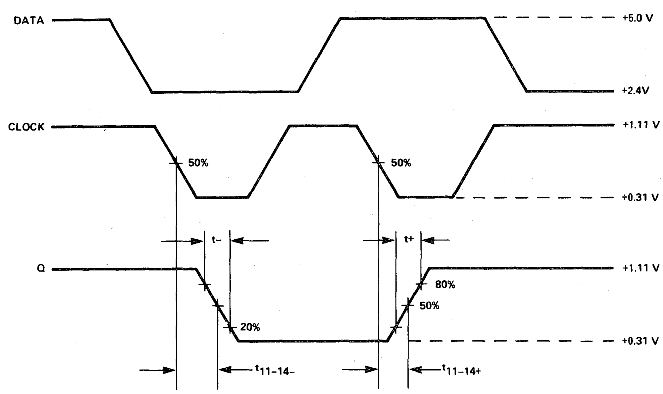
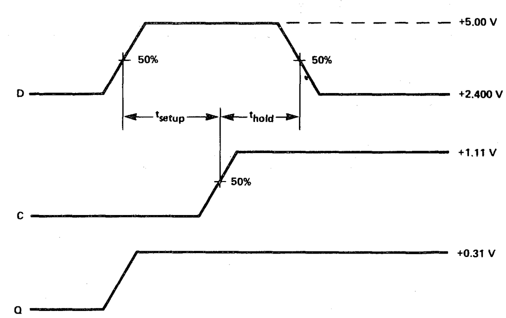


Figure 5 — $T_{SET\ UP}$ AND T_{HOLD}

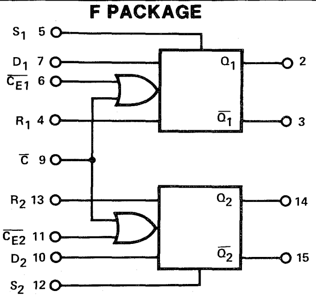


DUAL D-TYPE LATCH 10130

10130F

LOGIC DIAGRAM

F PACKAGE



V_{CC1} = 1, V_{CC2} = 16, V_{EE} = 8
Positive logic: high level = "1"

FEATURES

- **Fast propagation delay = 2.5 ns TYP (data)**
  = 2.8 ns TYP (set, reset)
  = 3.0 ns TYP (clock)
- **Low power dissipation = 140 mW/package TYP (no load)**
- **High fanout capability — can drive 50Ω lines**
- **High Z inputs — internal 50kΩ pulldowns**
- **High immunity from power supply variations: V_{EE} = −5.2V ±5% recommended**
- **Open emitter logic and bussing capability**
- **Pin compatible with 10131**

APPLICATIONS

- **High speed registers**
- **Control latches**
- **Status latches**

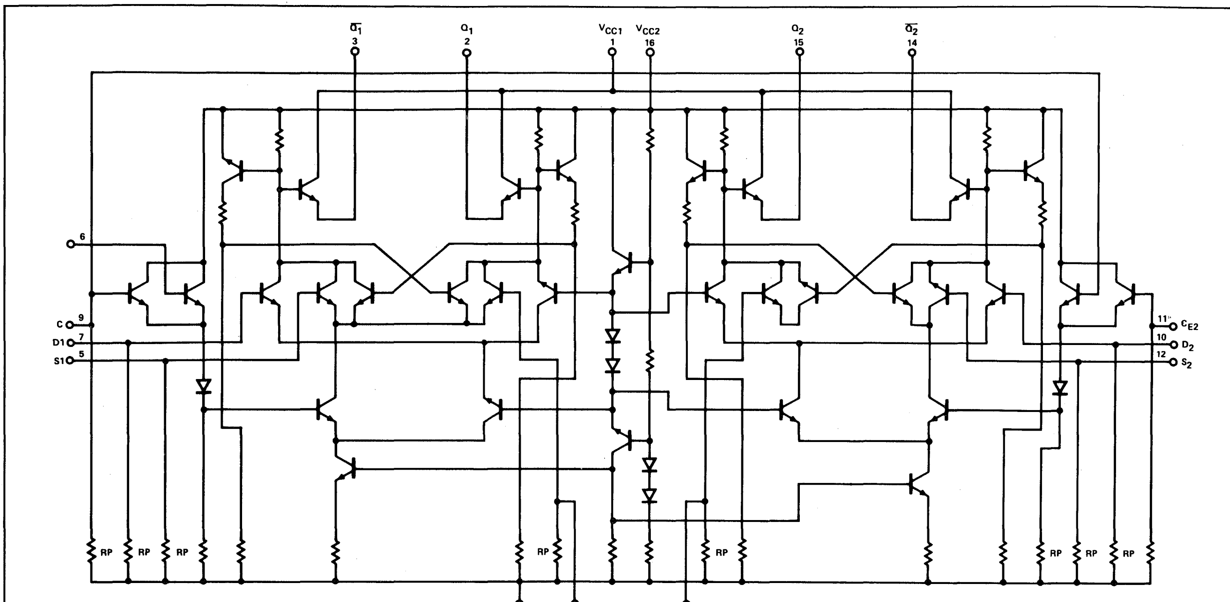
TRUTH TABLE

D	C	S	R	Q_n+1
L	L	ø	ø	1
A	I	ø	ø	H
ø	H	L	L	Q_n
ø	H	H	L	H
ø	H	L	H	L
ø	H	H	H	N.D.

C = $\overline{CE}$ + $\overline{C}$
ø = Don't care
N.D. = Not defined

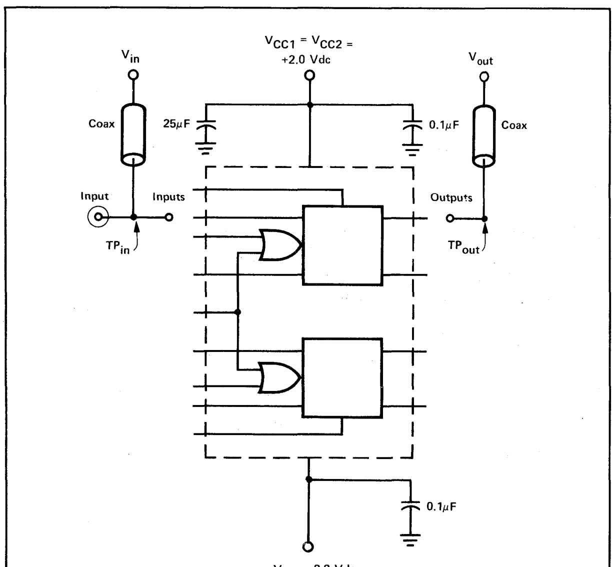
10130F

CIRCUIT SCHEMATIC



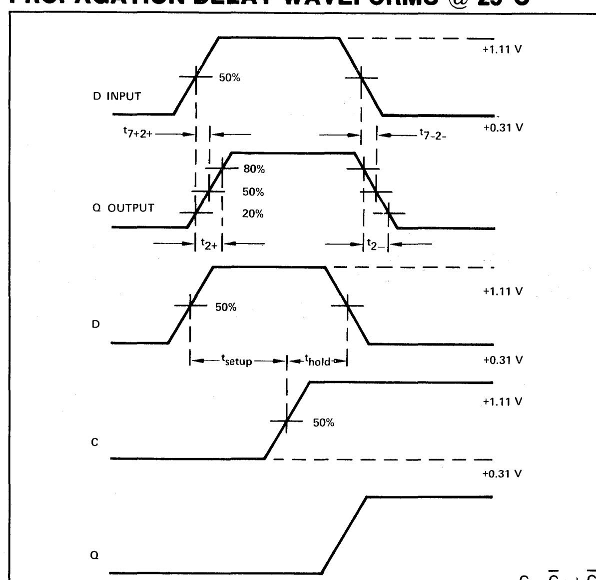
$C = \overline{C}_E + \overline{C}$. All Rp = 50 kΩ.

SWITCHING TIME TEST CIRCUIT



Input pulse
t+ = t− = 2.0 ± 0.2ns
(20 to 80%)

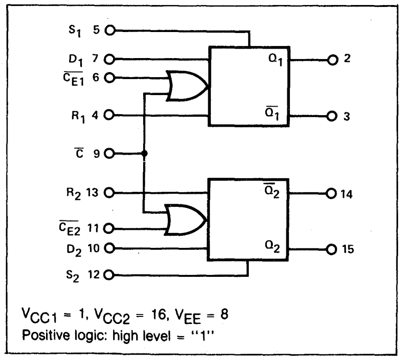
PROPAGATION DELAY WAVEFORMS @ 25°C



NOTES:

1. Each ECL 10,000 series device has been designed to meet the DC specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Voltage levels will shift approximately 4 mV with an air flow of 200 linear fpm. Outputs are terminated through a 50-ohm resistor to 2.0 volts.
2. For AC tests, all input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be <¼ inch from TP_{in} to input pin and TP_{out} to output pin. A 50-ohm termination to ground is located in each scope input. Unused outputs are connected to a 50-ohm resistor to ground.
3. Test procedures are shown for only one input or set of input conditions. Other inputs are tested in the same manner.
4. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.

LOGIC DIAGRAM



FEATURES

- f_{TOG} = 125 MHz MIN
  = 160 MHz TYP
- Fast Propagation delay
  = 2.8ns TYP (set, reset)
  = 3.0ns TYP (clock)
- Low power dissipation = 235 mW/package TYP (no load)
- High fanout capability—can drive 50 lines
- High Z inputs—internal 50 k pull-downs
- High immunity from power supply variations: V_{EE} = -5.2V 5% recommended
- Open emitter logic and bussing capability
- Pin compatible with 10130

APPLICATIONS

- Control logic
- Status logic
- Counters
- Shift register
- Prescalers

TRUTH TABLE

10131F

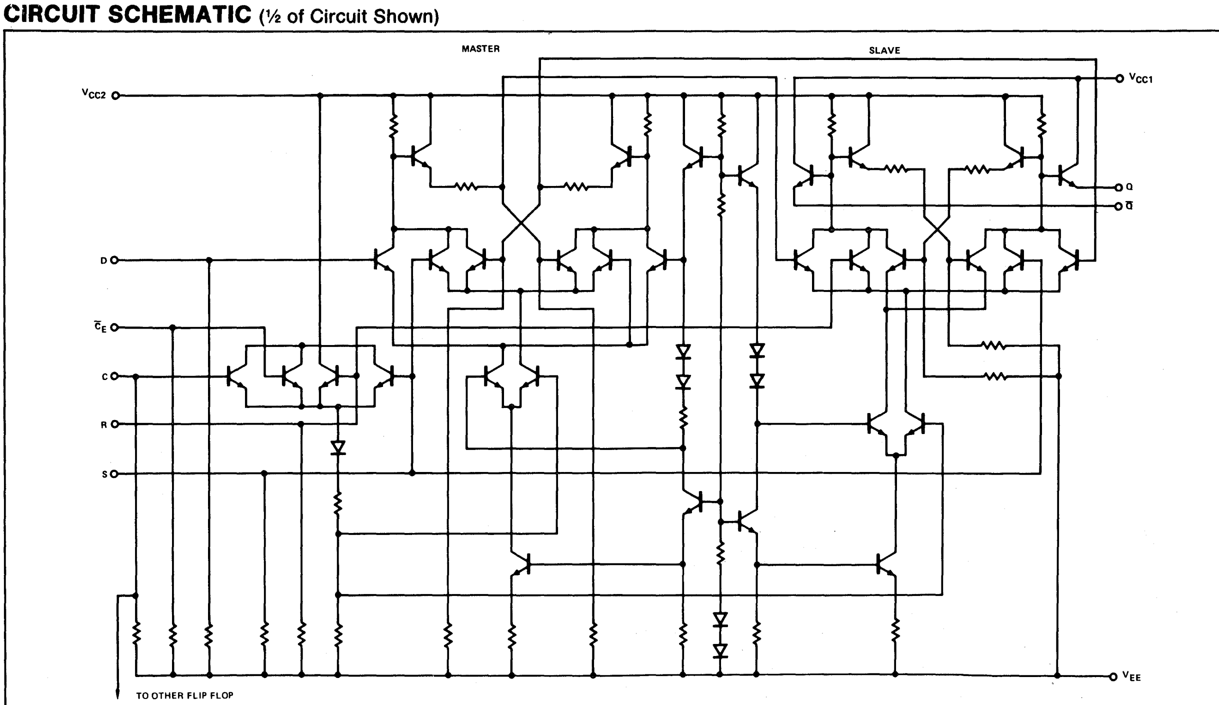
D	C*	S	R	Qn + 1
0	L	L	L	Qn
L	H	L	L	L
H	H	L	L	H
0	0	H	L	H
0	0	L	H	L
0	0	H	H	N.D.

An H represents a transition from L to H between t = and t = n + 1

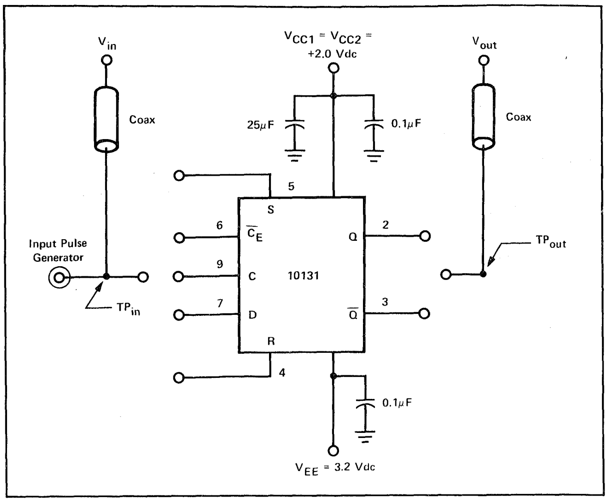
C = C_C + $\overline{CE}$

N.D. = Not Defined

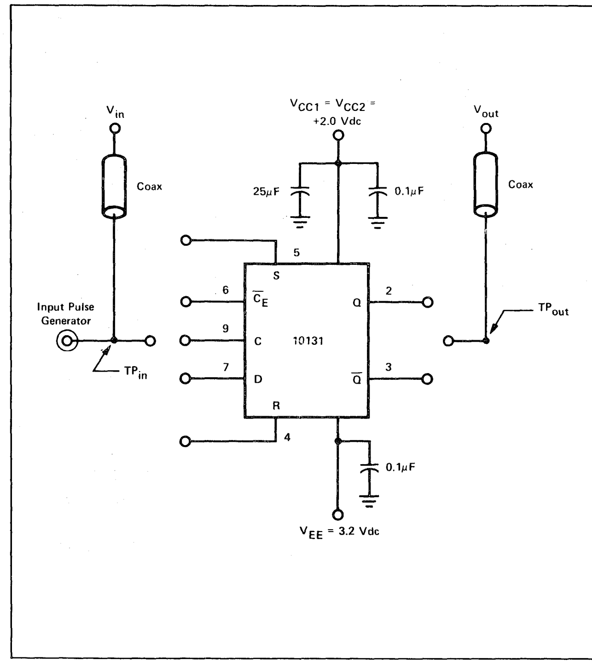
CIRCUIT SCHEMATIC (½ of Circuit Shown)



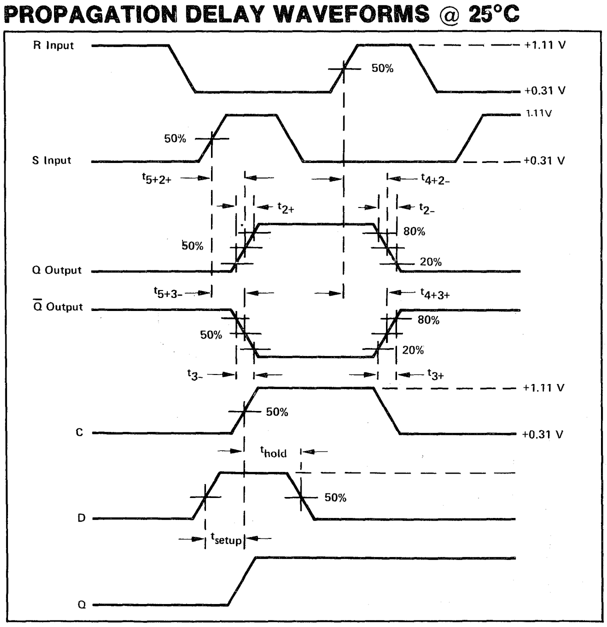
TOGGLE FREQUENCY TEST CIRCUIT



SWITCHING TIME TEST CIRCUIT



PROPAGATION DELAY WAVEFORMS @ 25°C



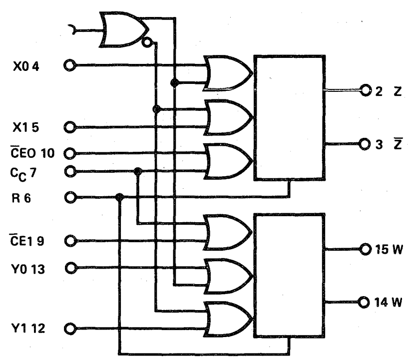
NOTES:

1. Each ECL 10,000 series device has been designed to meet the DC specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Voltage levels will shift approximately 4 mV with an air flow of 200 linear fpm. Outputs are terminated through a 50-ohm resistor to -2.0 volts.
2. For AC tests, all input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be <¼ inch from TP_{in} to input pin and TP_{out} to output pin. A 50-ohm termination to ground is located in each scope input. Unused outputs are connected to a 50-ohm resistor to ground.
3. Test procedures are shown for only one input or set of input conditions. Other inputs are tested in the same manner.
4. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.

10132-F

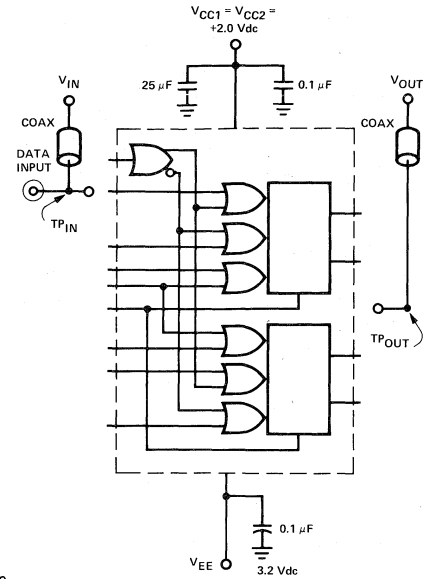
LOGIC DIAGRAM

F PACKAGE



V_{CC1} = 1, V_{CC2} = 16, V_{EE} = 8
Positive logic: high level = '1'

SWITCHING TIME TEST CIRCUIT

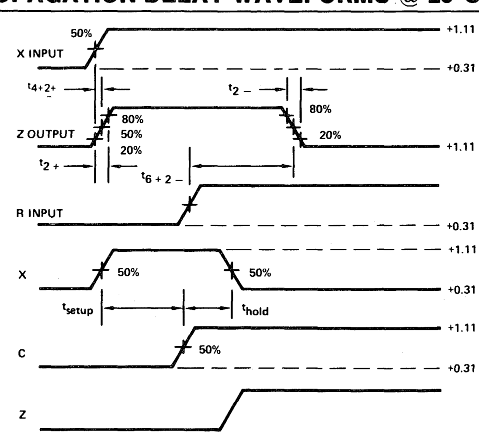


Input pulse
t+ = t− = 2.0 ± 0.2 ns
(20% to 80%)

FEATURES

- **High speed combined multiplexer — latch improves system performance.**
- **Multiplexed inputs to reduce package count**
- **Fast propagation delay = 2.5 ns TYP (data)**
  = 3.7ns TYP (select)
  = 3.0ns TYP (reset)
  = 4.0ns TYP (clock)
- **Low power dissipation = 200 mW/package TYP (no load)**
- **High fanout capability — can drive 50 Ω lines**
- **High Z inputs — internal 50 kΩ pulldowns**
- **High immunity from power supply variations: V_{EE} = −5.2V ±5% recommended**
- **Open emitter logic and bussing capability**

PROPAGATION DELAY WAVEFORMS @ 25°C



APPLICATIONS

- **Combined multiplexer — Register for:**
  high speed central processors
  high speed peripherals
  high speed minicomputers
  high speed accumulators
  communication systems

TRUTH TABLE

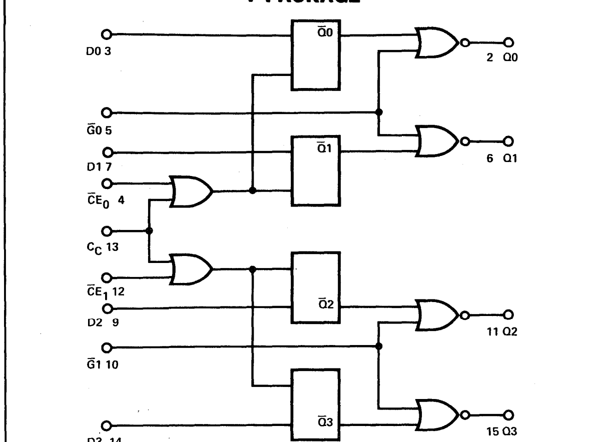
R	X_{in}	C_C	$\overline{CE}$	Z_{n+1}
L	L	L	L	L
L	L	L	H	Z_n
L	L	H	L	Z_n
L	L	H	H	Z_n
L	H	L	L	H
L	H	L	H	Z_n
L	H	H	L	Z_n
L	H	H	H	Z_n
H	φ	H	φ	L

φ = Don't care
$X_{in} = \overline{A} \cdot X0 + A \cdot X1$

NOTES:
1. Each ECL 10,000 series device has been designed to meet the DC specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Voltage levels will shift aproximately 4 mV with an air flow of 200 linear fpm. Outputs are terminated through a 50-ohm resistor to -2.0 volts.
2. For AC tests, all input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be <¼ inch from TP_{in} to input pin and TP_{out} to output pin. A 50-ohm termination to ground is located in each scope input. Unused outputs are connected to a 50-ohm resistor to ground.
3. Test procedures are shown for only one input or set of input conditions. Other inputs are tested in the same manner.
4. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.

10133-F

LOGIC DIAGRAM

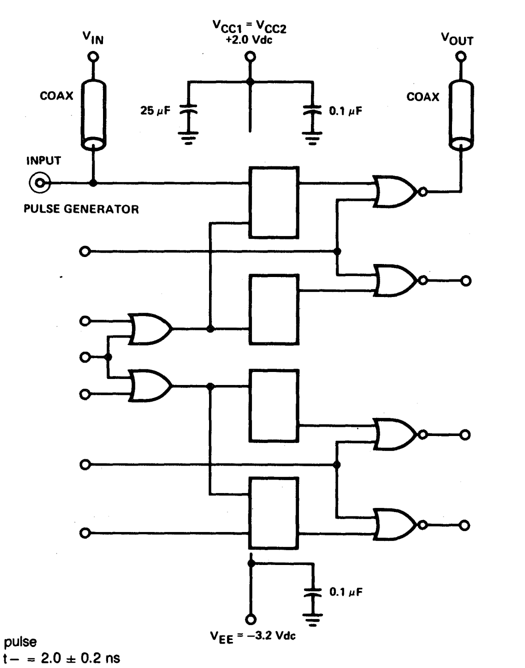


V_{CC1} = 1, V_{CC2} = 16, V_{EE} = 8
Positive logic: high level = '1'

APPLICATIONS

- **Temporary storage element in:**
  high speed central processors
  high speed peripherals and memories
  high speed digital communications
  instrumentation
  test equipment
- **Bus-oriented storage register for:**
  mini-computers
  array processors

SWITCHING TIME TEST CIRCUIT



Input pulse
t+ = t− = 2.0 ± 0.2 ns
(20% to 80%)

FEATURES

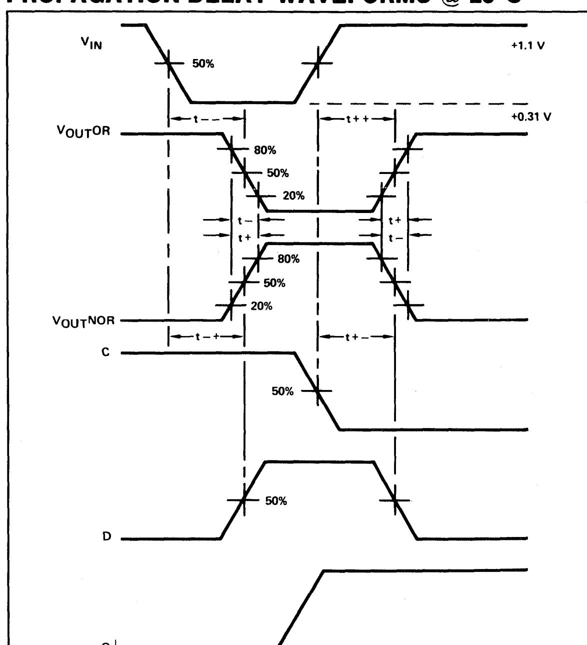
- **Fast propagation delay**
  = 4.0ns TYP clock or data to output
  = 2.0ns TYP enable to output
  = 0.7ns TYP setup and hold times
- **Gated outputs for BUS-oriented applications**
- **High density — four latches plus gating**
- **Low power dissipation = 290 mW/package TYP (no load)**
- **High fanout capability — can drive four 50 Ω lines**
- **High immunity from power supply variations: V_{EE} = −5.2V ±5% recommended**
- **Meets ECL 10,000 series standard interface specifications**

TRUTH TABLE

$\bar{G}$	C	D	Qntl
H	ϕ	ϕ	L
L	L	ϕ	Qn
L	H	L	L
L	H	H	H

C = $\bar{C}_C$ + C_E
ø = Don't Care

PROPAGATION DELAY WAVEFORMS @ 25°C

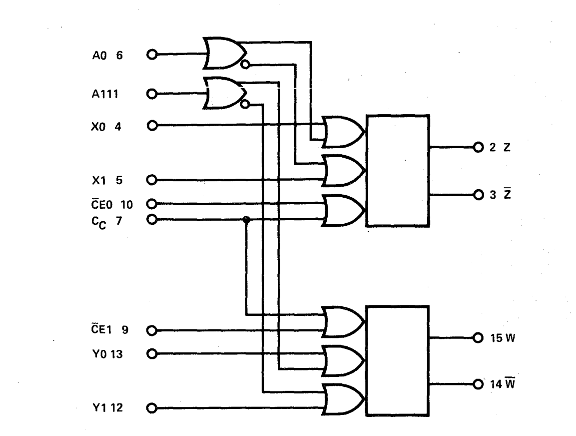


NOTES:

1. For AC tests, all input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be < ¼ inch from TP_{in} to input pin and TP_{out} to output pin. A 50-ohm termination to ground is located in each scope input. Unused outputs are connected to a 50-ohm resistor to ground.
2. Each ECL 10,000 series device has been designed to meet the DC specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 fpm is maintained. Voltage levels will shift approximately 5 mV with an air flow of 200 linear fpm. Outputs are terminated through a 50-ohm resistor to −2.0 volts.

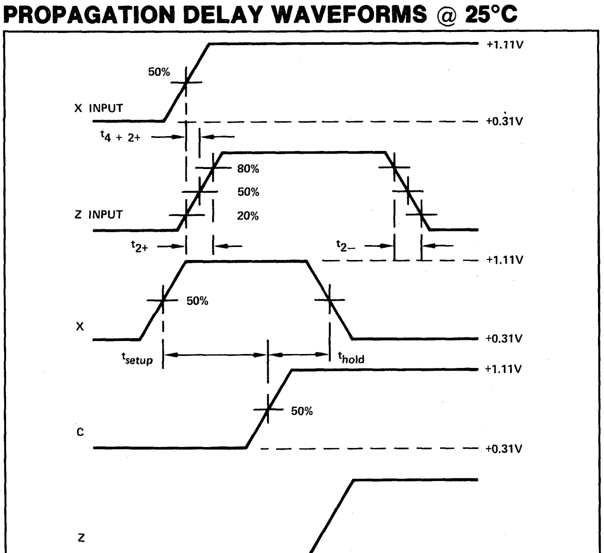
10134-F

LOGIC DIAGRAM



V_{CC1} = 1, V_{CC2} = 16, V_{EE} = 8
Positive logic: high level = '1'

PROPAGATION DELAY WAVEFORMS @ 25°C



NOTES:
1. Each ECL 10,000 series device has been designed to meet the DC specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 fpm is maintained. Voltage levels will shift approximately 4 mV with an air flow of 200 linear fpm. Outputs are terminated through a 50-ohm resistor to 2.0 volts.
2. For AC tests, all input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be <¼ inch from TP_{in} to input pin and TP_{out} to output pin. A 50-ohm termination to ground is located in each scope input. Unused outputs are connected to a 50-ohm resistor to ground.
3. Test procedures are shown for only one input or set of input conditions. Other inputs are tested in the same manner.
4. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.

FEATURES

- **High speed combined multiplexer — latch improves system performance.**
- **Multiplexed inputs to reduce package count**
- **Fast propagation delay = 2.5ns TYP (data)**
  = 3.5ns TYP (select)
  = 4.0ns TYP (clock)
- **Low power dissipation = 225 mW/package TYP (no load)**
- **High fanout capability — can drive 50 Ω lines**
- **High Z inputs — internal 50 kΩ pulldowns**
- **High immunity from power supply variations: V_{EE} = −5.2V ±5% recommended**
- **Open emitter logic and bussing capability**

APPLICATIONS

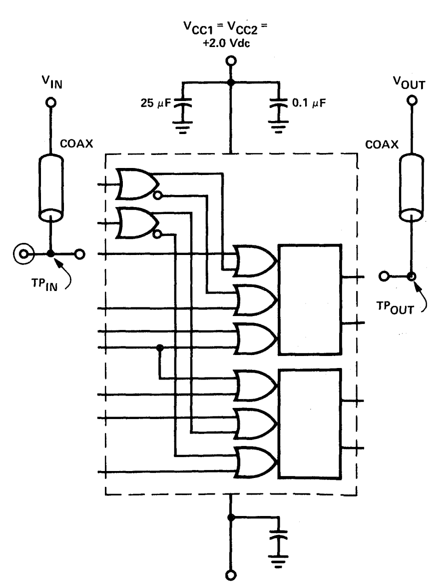
- **Combined multiplexer**
  - **High speed central processors**
  - **High speed peripherals**
  - **High speed minicomputers**
  - **High speed accumulators**
  - **Communication systems**

TRUTH TABLE

C	A0	X0	X1	Z_{n+1}
L	L	L	ϕ	L
L	L	H	ϕ	H
L	H	ϕ	L	L
L	H	ϕ	H	H
H	ϕ	ϕ	ϕ	Z_n

ϕ = don't care
$C = \overline{CE} + C_C$
$X_{in} = \overline{A0} \cdot X0 + A0 \cdot X1$

SWITCHING TIME TEST CIRCUIT

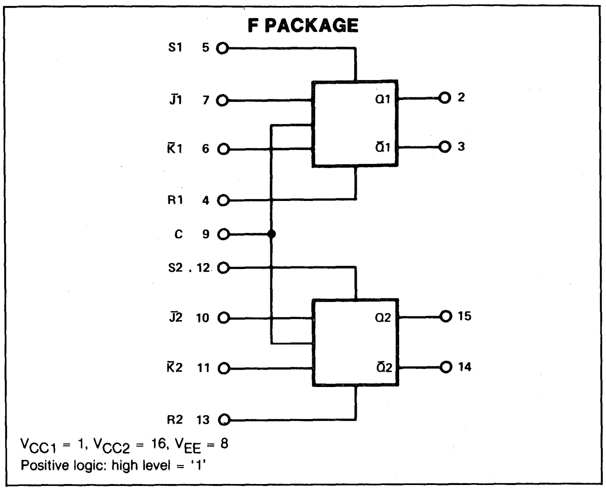


Input pulse
t+ = t− = 2.0 ± 0.2 ns
(20% to 80%)

LOGIC

10135-F

LOGIC DIAGRAM



FEATURES

- f_{TOG} = 140MHz TYP
- Fast propagation delay
  - = 3.0ns TYP (set, reset)
  - = 3.0ns TYP (clock)
- Low power dissipation = 235mW/package TYP (no load)
- High fanout capability — can drive 50Ω lines
- High Z inputs — internal 50kΩ pulldowns
- High immunity from power supply variations
- Open emitter logic and bussing capability

APPLICATIONS

- Control logic
- Status logic
- Counters
- Shift register

R-S TRUTH TABLE

R	S	Q_n+1
L	L	Q_n
L	H	H
H	L	L
H	H	N.D.

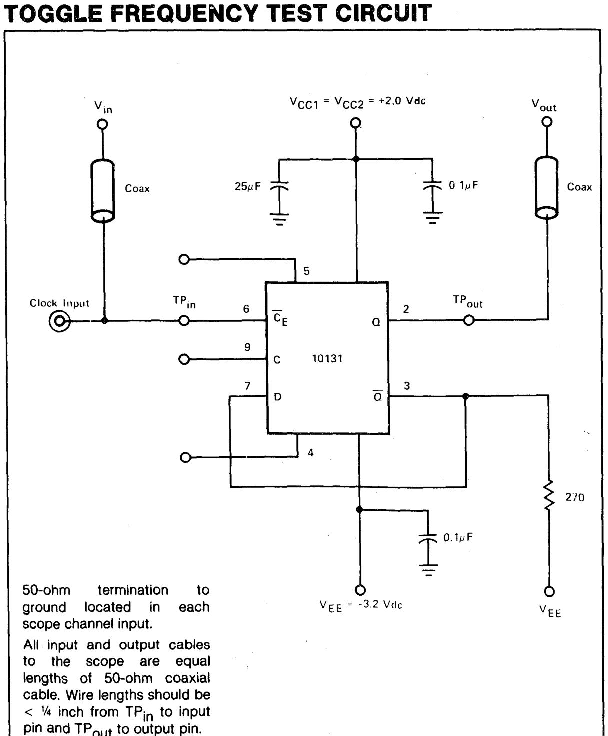
N.D. = not defined

CLOCK J-K TRUTH TABLE*

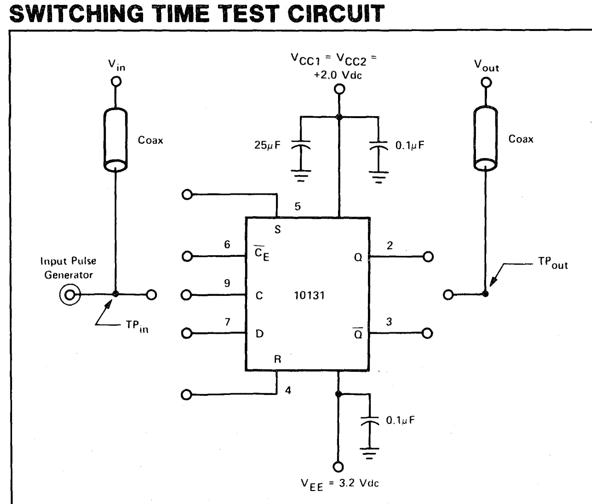
$\overline{J}$	$\overline{K}$	$\overline{Q}_n+1$
L	L	Q_n
H	L	L
L	H	H
H	H	Q_n

*Output states change on positive transition of clock for $\overline{J}$-$\overline{K}$ input condition present.

TOGGLE FREQUENCY TEST CIRCUIT

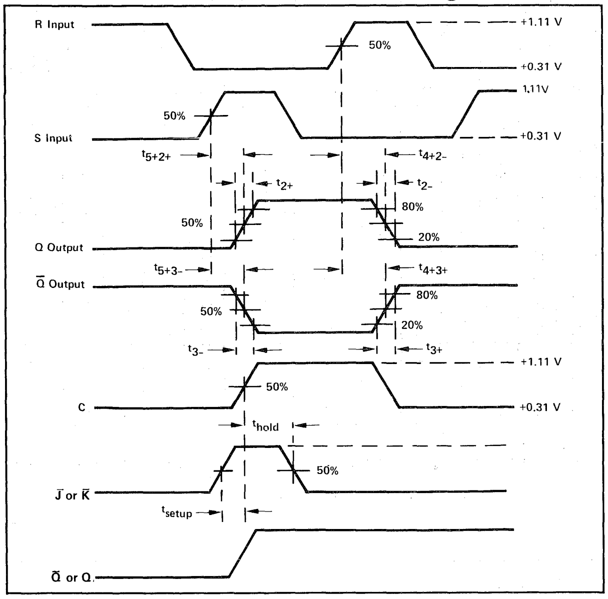


SWITCHING TIME TEST CIRCUIT



10135-F

PROPAGATION DELAY WAVEFORMS @ 25°C



NOTES:
1. Each ECL 10,000 series device has been designed to meet the DC specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Voltage levels will shift approximately 5 mV with an air flow of 200 linear fpm. Outputs are terminated through a 50-ohm resistor to 2.0 volts.
2. For AC tests, all input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be < ¼ inch from TP_{in} to input pin and TP_{out} to output pin. A 50-ohm termination to ground is located in each scope input. Unused outputs are connected to a 50-ohm resistor to ground.
3. Test procedures are shown for only one input or set of input conditions. Other inputs are tested in the same manner.
4. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.

UNIVERSAL HEXADECIMAL COUNTER 10136
UNIVERSAL DECIMAL COUNTER 10137

10136-F, 10137-F

Description

The 10136 and 10137 are high speed synchronous counters that can count up, count down, preset, or stop count at rates exceeding 100MHz.

The 10136 is a 16-state (Hexadecimal) counter and the 10137 is a 10-state (Decade) counter.

The flexibility of these devices allows the designer to use one basic counter design for all applications. The synchronous count feature makes these MSI parts suitable for either computers or instrumentation.

The carry input enables the counter, and prevents it from changing state when the clock goes high. The inputs S1 and S2 control the state of the counter: stop count, increment (count up), decrement (count down), and preset (program) count. The other inputs are clock, and the four D inputs for presetting the counter.

The counter changes state only on the positive-going edge of the clock. Any other input may change at any time except during the positive transition of the clock. The next state of the counter is determined by the configuration of the inputs only during the positive transition of the clock.

In addition to the four Q's outputs there is a carry out which goes low on the terminal count. In the preset mode the carry out on the 10136 will stay low but the carry out on the 10137 will depend on the condition of Q_1 and/or Q_2.

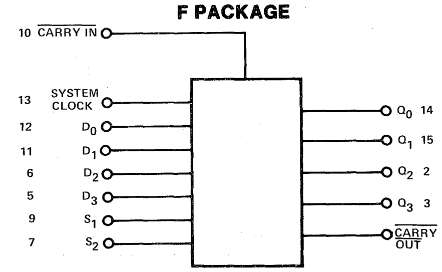
APPLICATIONS

Either the binary counter (10136) or the decade counter (10137) can be useful in high speed central processors and peripheral controllers, mini-computers, high speed digital communication equipment, and instrumentation.

When used as a prescaler, it is possible to extend the input frequency of the 10136, 37 to over 200MHz with the 10231.

BLOCK DIAGRAM

F PACKAGE



V_{CC1} = 1, V_{CC2} = 16, V_{EE} = 8
Positive logic: high level = '1'

FUNCTION SELECT TABLE

S1	S2	OPERATING MODE
L	L	Preset (Program)
L	H	Increment (Count Up)
H	L	Decrement (Count Down)
H	H	Hold (Stop Count)

SEQUENTIAL TRUTH TABLE[1] — 10136

INPUTS								OUTPUTS				
S1	S2	D0	D1	D2	D3	$\overline{\text{Carry}}$ IN	Clock 2	Q0	Q1	Q2	Q3	$\overline{\text{Carry}}$ Out
L	L	L	L	H	H	φ	H	L	L	H	H	L
L	H	φ	φ	φ	φ	L	H	H	L	H	H	H
L	H	φ	φ	φ	φ	L	H	L	H	H	H	H
L	H	φ	φ	φ	φ	L	H	H	H	H	H	L
L	H	φ	φ	φ	φ	H	L	H	H	H	H	H
L	H	φ	φ	φ	φ	H	H	H	H	H	H	H
H	H	φ	φ	φ	φ	φ	H	H	H	H	H	H
L	L	H	H	L	L	φ	H	H	H	L	L	L
H	L	φ	φ	φ	φ	L	H	L	H	L	L	H
H	L	φ	φ	φ	φ	L	H	H	L	L	L	H
H	L	φ	φ	φ	φ	L	H	L	L	L	L	L
H	L	φ	φ	φ	φ	L	H	H	H	H	H	H

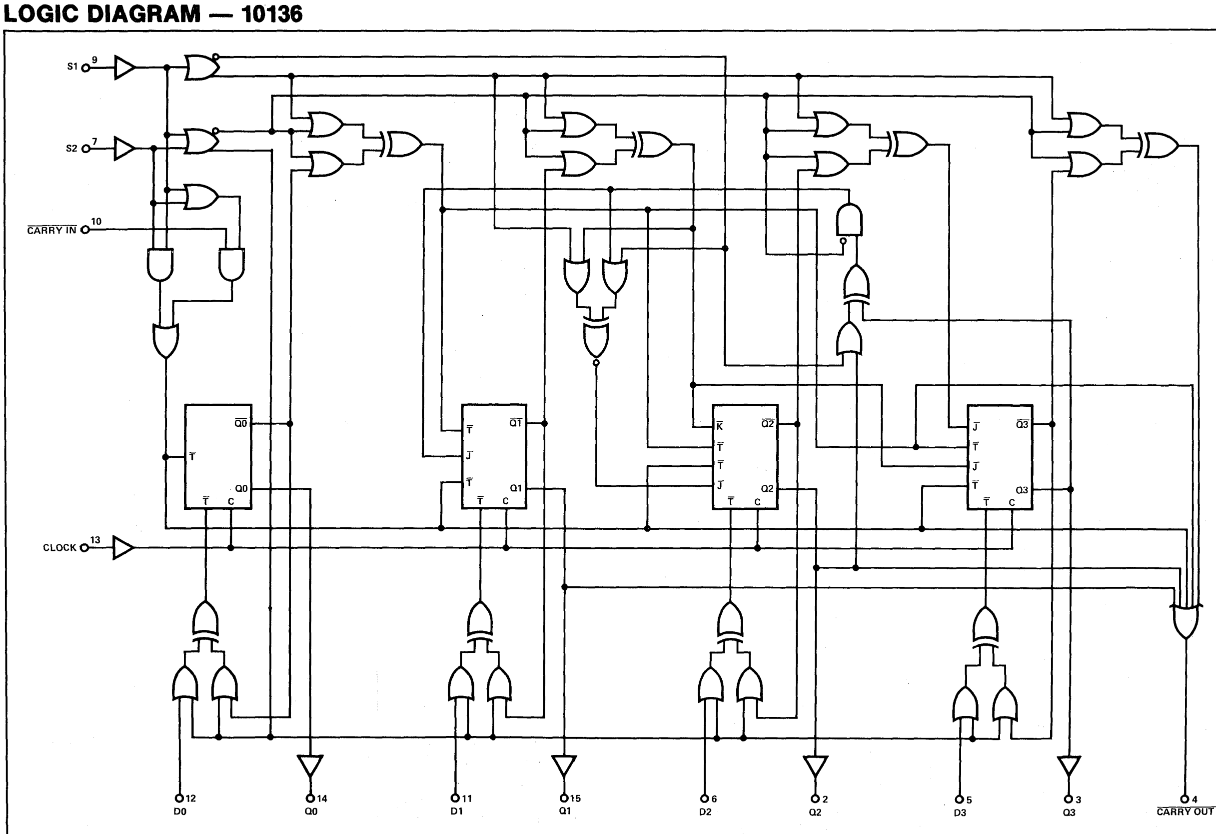
φ = Don't care.
1 = Truth table shows logic states assuming inputs vary in sequence shown from top to bottom.
2 = A clock H is defined as a clock input transition from a low to a high logic level.

SEQUENTIAL TRUTH TABLE[1] — 10137

INPUTS								OUTPUTS				
S1	S2	D0	D1	D2	D3	$\overline{\text{Carry}}$ IN	Clock 2	Q0	Q1	Q2	Q3	$\overline{\text{Carry}}$ Out
L	L	H	H	H	L	φ	H	H	H	H	L	H
L	H	φ	φ	φ	φ	L	H	L	L	L	H	H
L	H	φ	φ	φ	φ	L	H	H	L	L	H	L
L	H	φ	φ	φ	φ	L	H	L	L	L	L	H
L	H	φ	φ	φ	φ	L	H	H	L	L	L	H
L	H	φ	φ	φ	φ	H	H	H	L	L	L	H
L	H	φ	φ	φ	φ	H	H	H	L	L	L	H
H	H	φ	φ	φ	φ	φ	H	H	L	L	L	H
L	L	H	H	L	L	φ	H	H	H	L	L	H
H	L	φ	φ	φ	φ	L	H	L	H	L	L	H
H	L	φ	φ	φ	φ	L	H	H	L	L	L	H
H	L	φ	φ	φ	φ	L	H	L	L	L	L	L

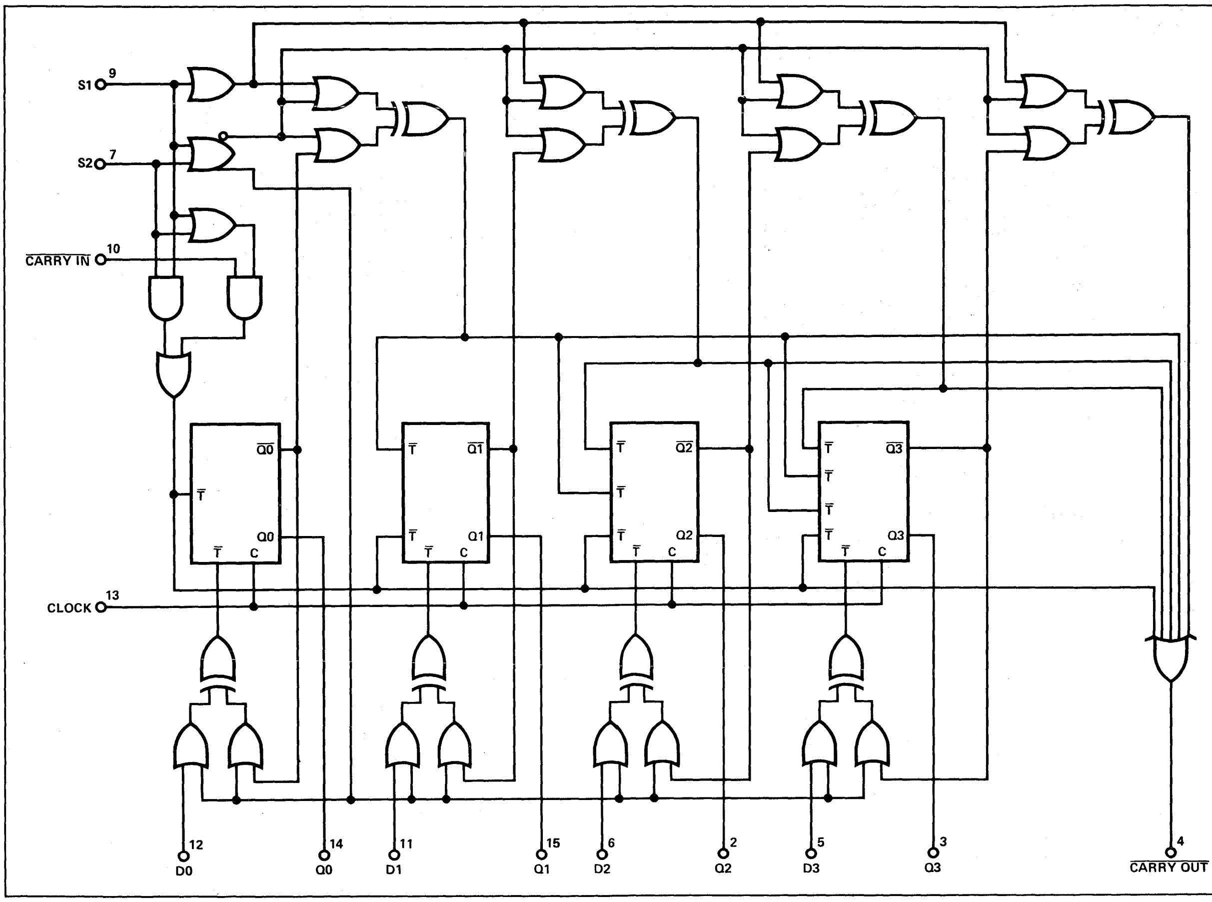
φ = Don't care.
1 = Truth table shows logic states assuming inputs vary in sequence shown from top to bottom.
2 = A clock H is defined as a clock input transition from a low to a high logic level.

LOGIC DIAGRAM — 10136

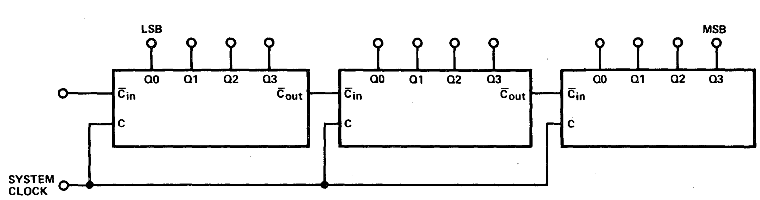


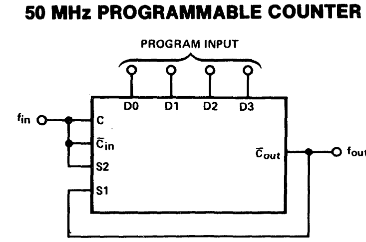
10136-F, 10137-F

LOGIC DIAGRAM — 10137



UNIVERSAL COUNTER APPLICATIONS

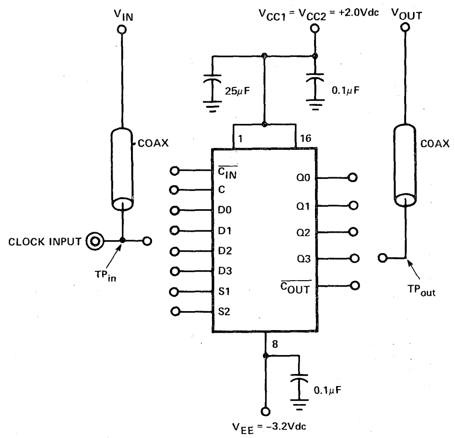




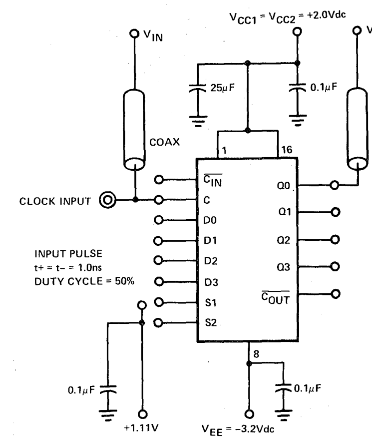
LOGIC

TEST CIRCUIT

SWITCHING TIME

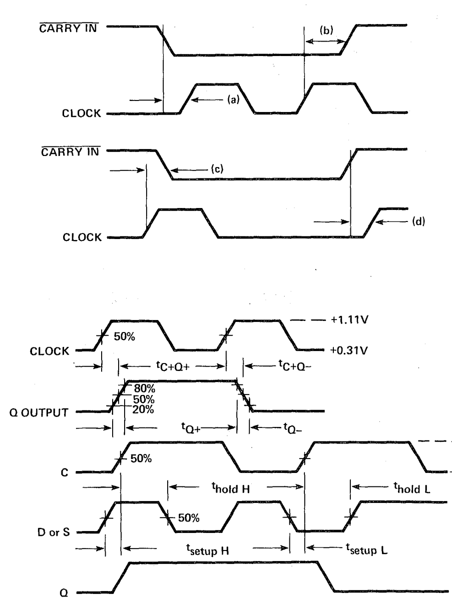


COUNT FREQUENCY



1. 50-ohm termination to ground located in each scope channel input.
2. All input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be ¼ inch from TP_{in} to input pin and TP_{out} to output pin.
3. Unused outputs are connected to a 50-ohm resistor to ground.

PROPAGATION DELAY WAVEFORMS @ 25°C



50-ohm termination to ground located in each channel input.

(a) is the minimum time to wait after the counter has been enabled to clock it

(b) is the minimum time before the counter has been disabled that it may be clocked

(c) is the minimum time before the counter is enabled that a clock pulse may be applied with no effect on the state of the counter.

(d) is the minimum time to wait after the counter is disabled that a clock pulse may be applied with no effect in the state of the counter

(c) and (d) may be negative numbers.

NOTE:

t_{setup} is the minimum time before the positive transition of the clock pulse (C) that information must be present at the input D or S. t_{hold} is the minimum time after the positive transition of the clock pulse (C) that information must remain unchanged at the input D or S.

10141-F

DESCRIPTION

The 10141 is a four-bit shift register that features four separate input terminals for parallel data entry and one each input terminal for serial shift left and serial shift right data entry. The device also provides an output terminal for each stage, thus allowing any combination of serial in/parallel in-serial out/parallel out operation modes to be used.

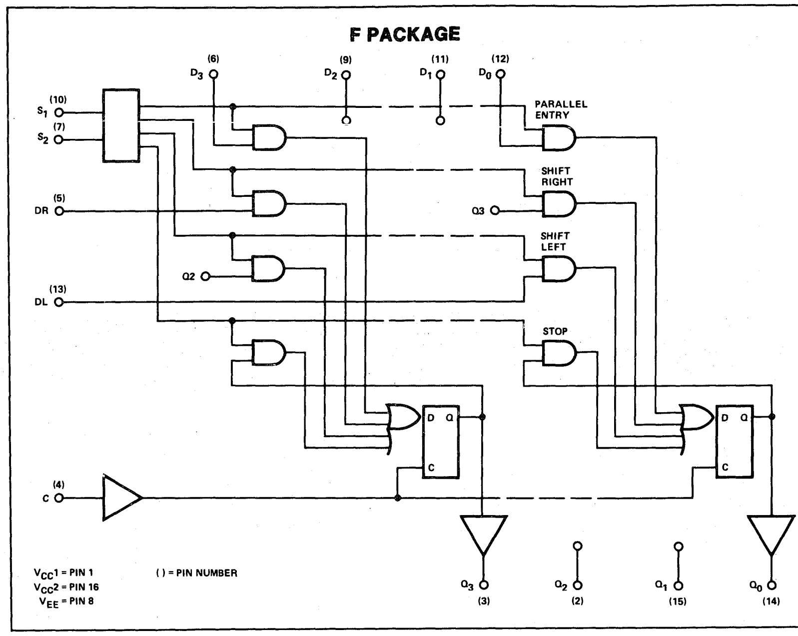
Two additional inputs are provided to control the four different operating modes of the device; parallel data entry, shift left, shift right, and stop. All shift operations occur on the positive-going edge of the clock input.

When operation of the device is restricted to one or two modes, the unused input/output pins can be left open since 50kΩ pulldown resistors are included on all input pins and all outputs are open-emitter. In addition, all outputs have 50Ω drive capability.

FEATURES

- **High speed shift frequency = 200 MHz (TYP)**
- **Low power 425 mW no load (TYP)**
- **High fanout — 50Ω drive capability**
- **High Z inputs with 50kΩ pulldown resistors**
- **Open emitter outputs for bussing applications**
- **Four operating modes**
- **Serial and parallel data entry**

LOGIC DIAGRAM

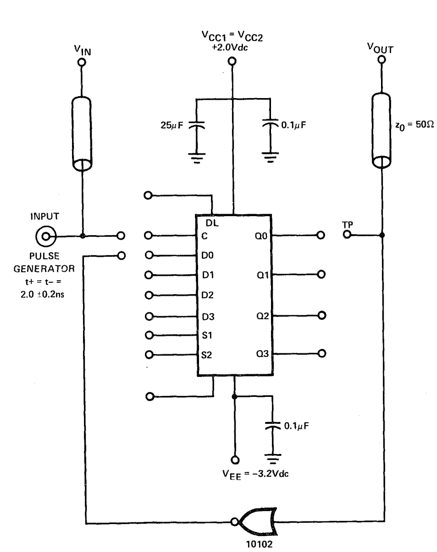


TRUTH TABLE

CONTROL		OPERATING	OUTPUTS			
S_1	S_2	MODE	$Q_{0(N+1)}$	$Q_{1(H+1)}$	$Q_{2(N+1)}$	$Q_{3(N+1)}$
L	L	Parallel Entry	D_{ON}	D_{IN}	D_{2N}	D_{3N}
L	H	Shift Right	Q_{IN}	Q_{2N}	Q_{3N}	D_{RN}
H	L	Shift Left	D_{LN}	Q_{ON}	Q_{IN}	Q_{2N}
H	H	Stop Shift	Q_{ON}	Q_{IN}	Q_{2N}	Q_{3N}

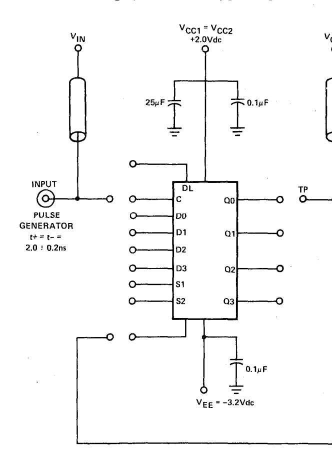
TEST CIRCUIT

SWITCHING TIME



INPUT/OUTPUT CABLES ARE EQUAL LENGTH, 50Ω COAX. WIRE LENGTH TO INPUT/OUTPUT PLUG SHOULD BE <1/4 IN. FROM TEST POINT.

SHIFT FREQUENCY

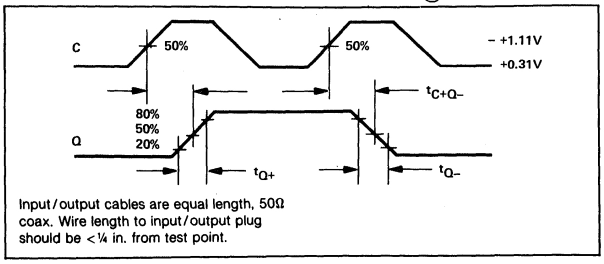


TEST PROCEDURE
1. SET D_1, D_2, D_3 TO L (+0.31VDC) SET D_0 TO H (+1.11VDC)
2. APPLY CLOCK PULSE +1.11 / +0.31
3. MAINTAIN CLOCK LOW SET S_1 TO L (+0.31VDC) SET S_2 TO H (+1.11VDC)
4. MEASURE FREQUENCY

LOGIC

10141-F

PROPAGATION DELAY WAVEFORM @ 25°C



ECL 16x4 RAM 10145

10145-F,I

DESCRIPTION

The 10145 is an ECL 64-bit read-write random access memory organized as 16 words of 4 bits each. Words are selected through fully decoded and buffered inputs when the chip enable (CE) is low. Data is written into the selected word by bringing the READ/WRITE input low. Cut-puts are low during write.

On-chip input pulldown resistors allow any unused inputs to be left open. Open emitter outputs allow corresponding bits of different devices to be tied together to form a "Wire OR" logic connection.

The 10145 utilizes separate internal metal systems and wire bonds for V_{CC1} and V_{CC2}. The exceptionally high speed of the 10145 makes it particularly suited for register file and scratch pad applications.

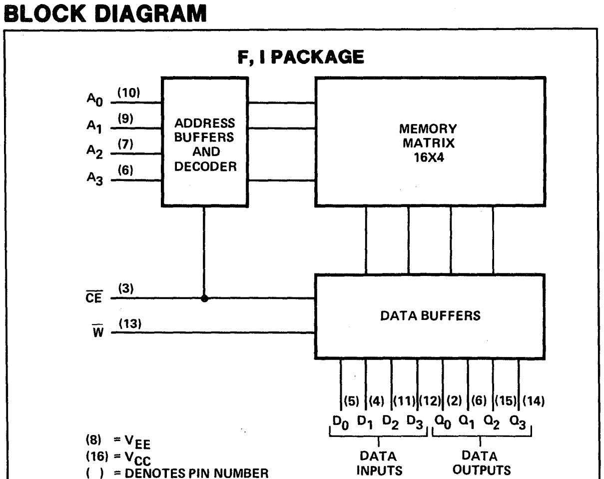
FEATURES

- **8.5 ns address access time (TYP)**
- **Input pulldown resistors**
- **Open emitter outputs and chip enable input for memory expansion**
- **50 Ohm output specification**
- **Single −5.2V power supply**
- **Full decoded inputs**
- **Fully compatible with Signetics 10,000 series family of integrated circuits**

APPLICATIONS

- **Scratch pad memories**
- **Buffer memories**
- **Register files**
- **Control stores**

BLOCK DIAGRAM



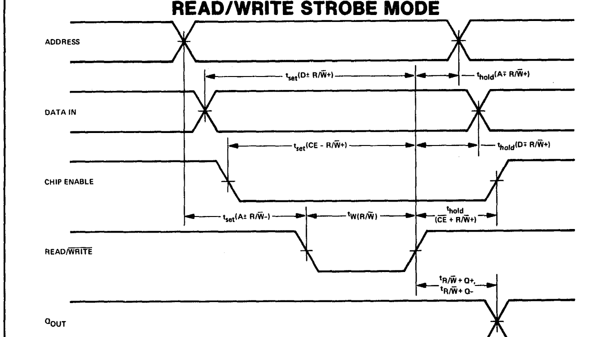
10145-F,I

SWITCHING CHARACTERISTICS $V_{EE}=-3.2V$, $V_{CC}=2V$, $R_L=50\Omega$ TO GND

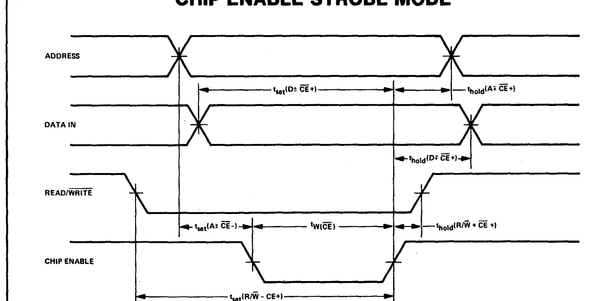
PARAMETER		MIN	TYP	MAX	UNITS
$t_{\overline{CE}-Q+}, t_{\overline{CE}+Q-}$	Access Time — Chip Enable to Output		5.0	7.5	ns
t_{A+Q+}, t_{A-Q+} t_{A+Q-}, t_{A-Q-}	Address to Output		8.5	13.0	ns
	Write Strobe Mode				
$t_{SET(D\pm\ R/\overline{W}+)}$	Data Set-up	11.0	7.5		ns
$t_{SET(CE-\ R/\overline{W}+)}$	Chip Enable Set-up	16.5	11.0		ns
$t_{SET(A\pm\ R/\overline{W}-)}$	Address	5.3	3.5		ns
$t_{HOLD(D\mp\ R/\overline{W}+)}$	Data Hold	4.5	3.0		ns
$t_{HOLD(\overline{CE}+\ R/\overline{W}+)}$	Chip Enable Hold	4.5	3.0		ns
$t_{HOLD(A\mp\ R/\overline{W}+)}$	Address Hold	5.3	3.5		ns
$t_{R/\overline{W}+\ Q+}, t_{R/\overline{W}+\ Q-}$	Recovery Time		7.5	11.0	ns
$t_{W(R/\overline{W})}$	Write Pulse Width	11.0	7.5		ns
	Chip Enable Strobe Mode				
$t_{SET(D\pm\ \overline{CE}+)}$	Data Set-up	11.0	7.5		ns
$t_{SET(R/\overline{W}-\ \overline{CE}+)}$	Read/Write Set-up	16.5	11.0		ns
$t_{SET(A\pm\overline{CE}-)}$	Address Set-up	4.5	3.0		ns
$t_{HOLD(D\mp\overline{CE}+)}$	Data Hold	4.5	3.0		ns
$t_{HOLD(R/\overline{W}+\ \overline{CE}+)}$	Read/Write Hold	4.5	3.0		ns
$t_{HOLD(A\mp\ CE+)}$	Address Hold	4.5	3.0		ns
$t_{W(\overline{CE})}$	Chip Enable Pulse Width	11.0	7.5		ns
t_+	Rise Time (20%—80%)	1.1	2.5	4.0	ns
t_-	Fall Time (20%—80%)	1.1	2.5	4.0	ns

TIMING DIAGRAMS

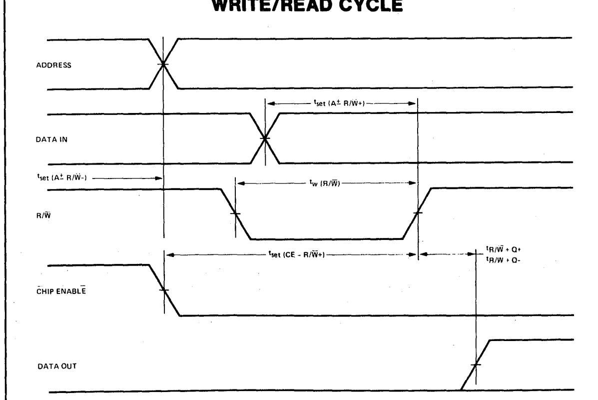
WRITE CYCLE READ/WRITE STROBE MODE



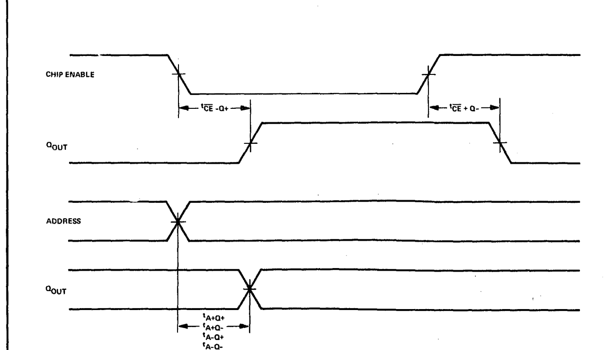
WRITE CYCLE CHIP ENABLE STROBE MODE



WRITE/READ CYCLE



READ CYCLE



LOGIC

10158F. 10159F

FEATURES

- High speed: propagation delay
  = 2.2 nS TYP data to output
  = 3.0 nS TYP select to output
- Output enable on 10159 for output bussing
- Low power: 162 mW/Package TYP
- Drives 50Ω line
- Standard ECL 10,000 series interface
- Open-emitter outputs

TRUTH TABLE (10158)

INPUTS			OUTPUTS
Dno	Dni	S	Zn
L	X	L	L
H	X	L	H
X	L	H	L
X	H	H	H

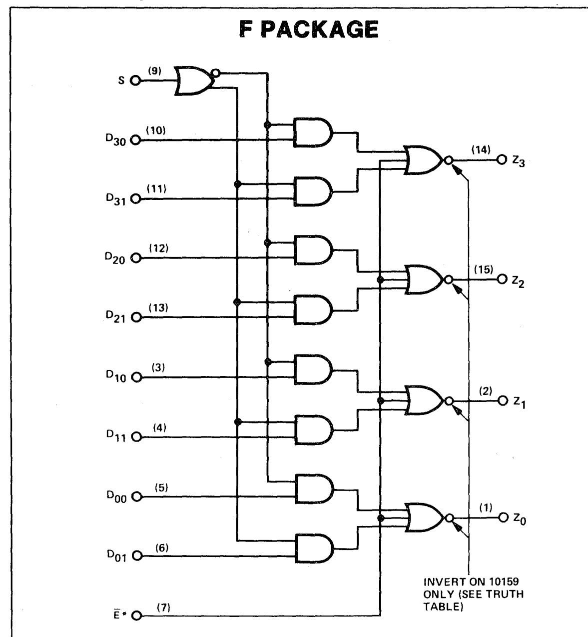
X = Don't Care

TRUTH TABLE (10159)

INPUTS				OUTPUTS
Dno	Dni	S	E	Zn
X	X	X	H	L
L	X	L	L	H
H	X	L	L	L
X	L	H	L	H
X	H	H	L	L

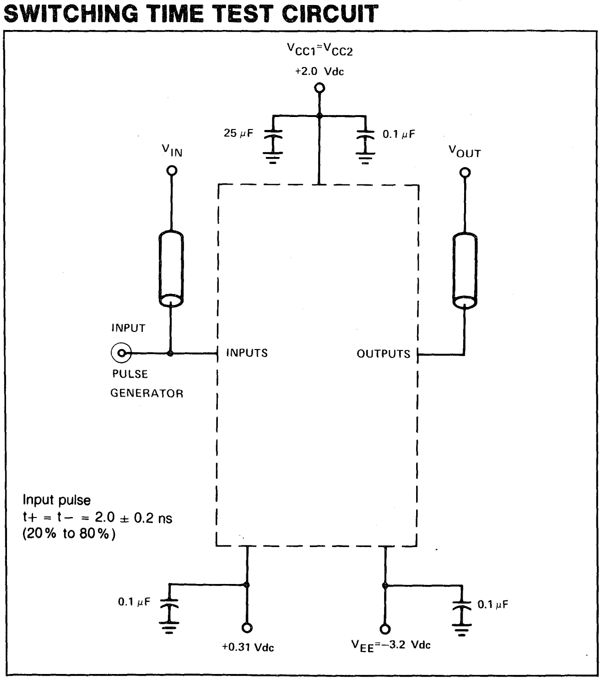
X = Don't Care

LOGIC DIAGRAM

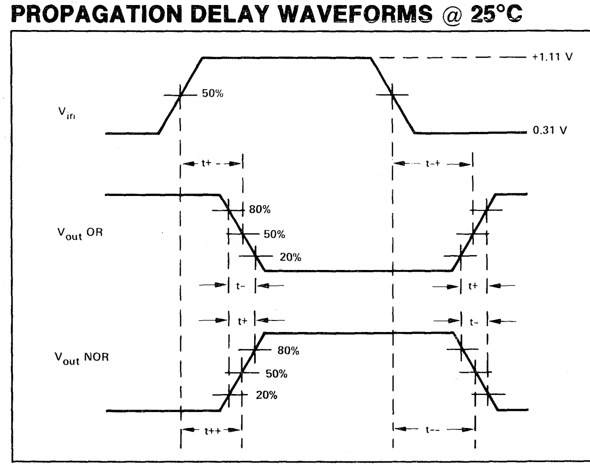


*10159 only (pin 7 open on 10158)
$V_{CC1} = V_{CC2} = 16$ $V_{EE} = 8$
Positive logic high level = "1"

SWITCHING TIME TEST CIRCUIT



PROPAGATION DELAY WAVEFORMS @ 25°C



NOTES:

1. Each ECL 10,000 series device has been designed to meet the DC specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Voltage levels will shift approximately 3 mV with an air flow of 200 linear fpm. Outputs are terminated through a 50-ohm resistor to −2.0 volts.
2. For AC tests, all input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be <¼ inch from TP_{in} to input pin and TP_{out} to output pin. A 50-ohm termination to ground is located in each scope input. Unused outputs are connected to a 50-ohm resistor to ground.
3. Test procedures are shown for only one input or set of input conditions. Other inputs are tested in the same manner.
4. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
5. One input from each gate must be tied to V_{BB} (Pin 11) during testing.

10160-F

FEATURES

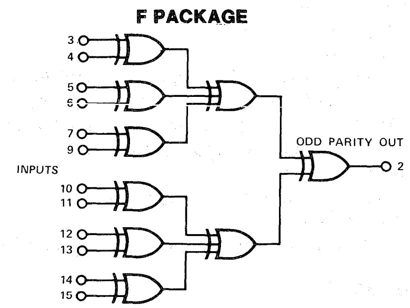
- High functional density on one chip reduces package count and saves system power
- Fast propagation delay = 4.0ns TYP
- Low power dissipation = 325mW/package type (no load)
- High fanout capability — can drive 50Ω lines
- High Z inputs — internal 50kΩ pulldowns
- Controlled output rise and fall times -2.0ns TYP (20% to 80%) (Output loaded)
- High immunity from power supply variations: $V_{EE} = -5.2V \pm 5\%$ recommended
- Open emitter logic and bussing capability

APPLICATIONS

DETECTION OR GENERATION OF PARITY IN:

- High speed central processors
- High speed peripherals
- High speed minicomputers
- Communication systems
- Instrumentation

LOGIC DIAGRAM

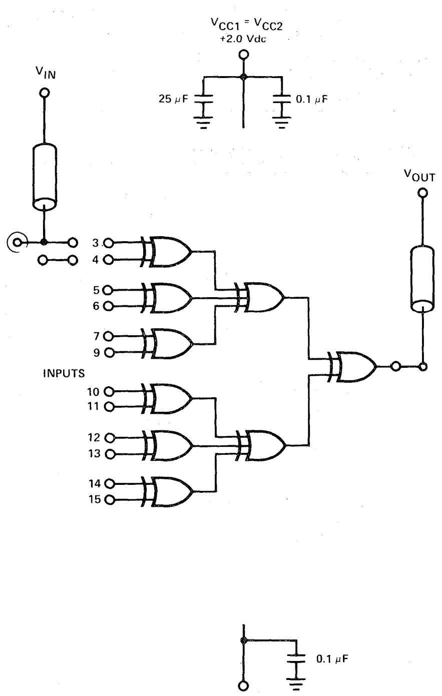


V_{CC1} = 1, V_{CC2} = 16, V_{EE} = 8
Positive logic: high level = '1'

TRUTH TABLE

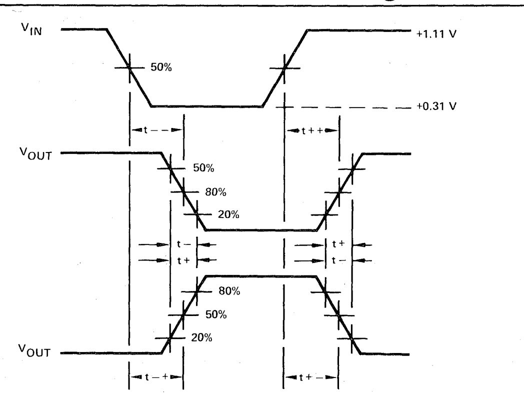
INPUT	OUTPUT
Sum of High Level Inputs	Pin 2
Even	Low
Odd	High

SWITCHING TIME TEST CIRCUIT



Input pulse
t+ = t− = 2.0 ± 0.2 ns
(20% to 80%)

PROPAGATION DELAY WAVEFORMS @ 25°C



NOTES:

1. Each ECL 10,000 series device has been designed to meet the DC specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Voltage levels will shift approximately 5 mV with an air flow of 200 linear fpm. Outputs are terminated through a 50-ohm resistor to -2.0 volts.
2. For AC tests, all input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be <¼ inch from TP_{in} to input pin and TP_{out} to output pin. A 50-ohm termination to ground is located in each scope input. Unused outputs are connected to a 50-ohm resistor to ground.
3. Test procedures are shown for only one input or set of input conditions. Other inputs are tested in the same manner.
4. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.

10161-F

FEATURES

- **Fast propagation delay**
  - **= 4.0ns TYP address to output**
  - **= 4.5ns TYP enable to output**
- **Low power dissipation = 295 mW/package TYP (no load)**
- **High fanout capability — can drive eight 50 Ω lines**
- **True parallel decoder — eliminates unequal delay times**
- **High immunity from power supply variations: V_{EE} = −5.2V ±5% recommended**
- **High Z inputs — internal 50 kΩ pulldowns**
- **Open emitter outputs**
- **Meets ECL 10,000 series standard interface specifications**

APPLICATIONS

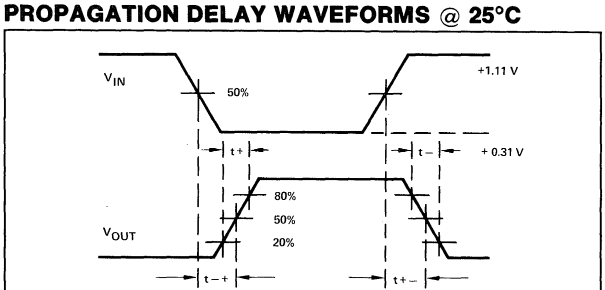
- **1-of-8 decoder**
- **1-line to 8-line demultiplexer**

TRUTH TABLE

Enable INPUTS		INPUTS			OUTPUTS							
$\overline{E1}$	$\overline{E0}$	A2	A1	A0	D0	D1	D2	D3	D4	D5	D6	D7
L	L	L	L	L	L	H	H	H	H	H	H	H
L	L	L	L	H	H	L	H	H	H	H	H	H
L	L	L	H	L	H	H	L	H	H	H	H	H
L	L	L	H	H	H	H	H	L	H	H	H	H
L	L	H	L	L	H	H	H	H	L	H	H	H
L	L	H	L	H	H	H	H	H	H	L	H	H
L	L	H	H	L	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	L	H	H	L
H	L	ø	ø	ø	H	H	H	H	H	H	H	H
L	H	ø	ø	ø	H	H	H	H	H	H	H	H
H	H	ø	ø	ø	H	H	H	H	H	H	H	H

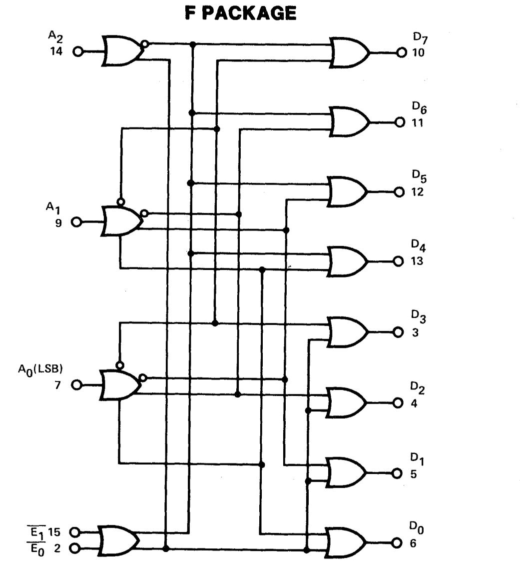
ø = don't care.

PROPAGATION DELAY WAVEFORMS @ 25°C



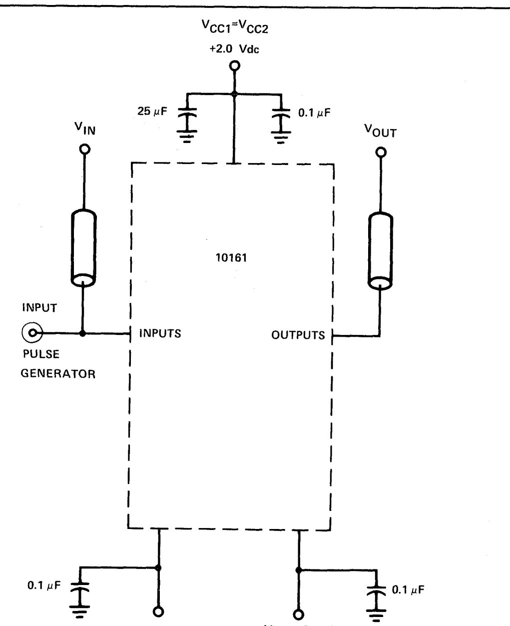
NOTES:
1. Each ECL 10,000 series device has been designed to meet the DC specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Voltage levels will shift approximately 5 mV with an air flow of 200 linear fpm. Outputs are terminated through a 50-ohm resistor to -2.0 volts.
2. For AC tests, all input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be <¼ inch from TP_{in} to input pin and TP_{out} to output pin. A 50-ohm termination to ground is located in each scope input. Unused outputs are connected to a 50-ohm resistor to ground.
3. Test procedures are shown for only one input or set of input conditions. Other inputs are tested in the same manner.
4. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.

LOGIC DIAGRAM



(Internal connections are emitter-dot OR)
V_{CC1} = 1, V_{CC2} = 16, V_{EE} = 8
Positive logic: high level = '1'

SWITCHING TIME TEST CIRCUIT



Input pulse
t+ = t− = 2.0 ± 0.2 ns
(20% to 80%)

FEATURES:

- **Fast propagation delay**
  - **= 4.0ns TYP address to output**
  - **= 4.5ns TYP enable to output**
- **Low power dissipation = 295 mW/package TYP (no load)**
- **High fanout capability — can drive eight 50 Ω lines**
- **True parallel decoder — eliminates unequal delay times**
- **High immunity from power supply variations: V_{EE} = −5.2V±5% recommended**
- **High Z inputs — internal 50 kΩ pulldowns**
- **Open emitter outputs**
- **Meets ECL 10,000 series standard interface specifications**

APPLICATIONS

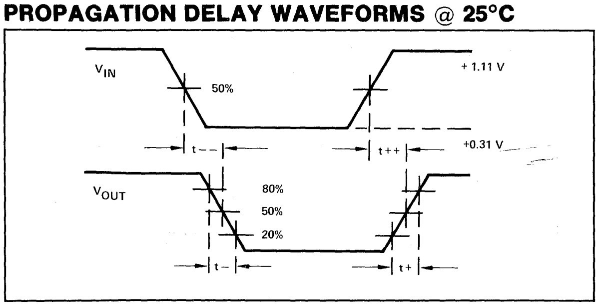
- **1-of-8 Decoder**
- **1-line to 8-line demultiplexer**

TRUTH TABLE

INPUTS					OUTPUTS							
$\overline{E1}$	$\overline{E0}$	A2	A1	A0	D0	D1	D2	D3	D4	D5	D6	D7
L	L	L	L	L	H	L	L	L	L	L	L	L
L	L	L	L	H	L	H	L	L	L	L	L	L
L	L	L	H	L	L	L	H	L	L	L	L	L
L	L	L	H	H	L	L	L	H	L	L	L	L
L	L	H	L	L	L	L	L	L	H	L	L	L
L	L	H	L	H	L	L	L	L	L	H	L	L
L	L	H	H	L	L	L	L	L	L	L	H	L
L	L	H	H	H	L	L	L	L	L	L	L	H
H	L	ø	ø	ø	L	L	L	L	L	L	L	L
L	H	ø	ø	ø	L	L	L	L	L	L	L	L
H	H	ø	ø	ø	L	L	L	L	L	L	L	L

ø = don't care

PROPAGATION DELAY WAVEFORMS @ 25°C

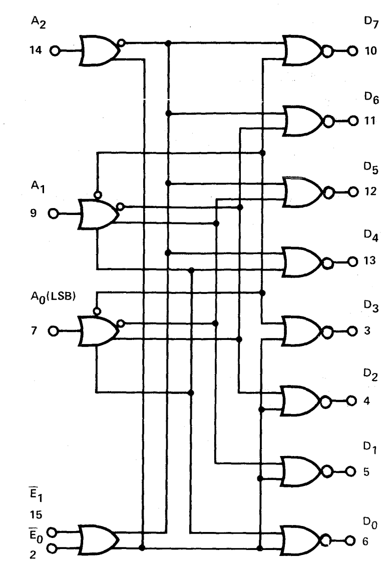


NOTES:

1. Each ECL 10,000 series device has been designed to meet the DC specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Voltage levels will shift approximately 6 mV with an air flow of 200 linear fpm. Outputs are terminated through a 50-ohm resistor to -2.0 volts.
2. For AC tests, all input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be <¼ inch from TP_{in} to input pin and TP_{out} to output pin. A 50-ohm termination to ground is located in each scope input. Unused outputs are connected to a 50-ohm resistor to ground.
3. Test procedures are shown for only one input or set of input conditions. Other inputs are tested in the same manner.
4. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.

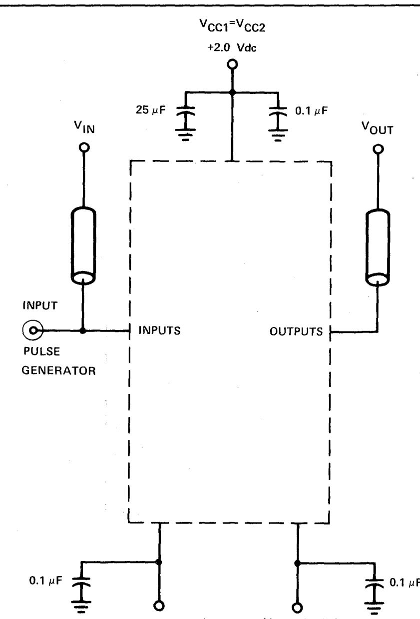
LOGIC DIAGRAM

F PACKAGE



(Internal connections are emitter-dot OR)
V_{CC1} = 1, V_{CC2} = 16, V_{EE} = 8
Positive logic: high level = '1'

SWITCHING TIME TEST CIRCUIT



Input pulse
t+ = t− = 2.0 ± 0.2 ns
(20% to 80%)

10164-F

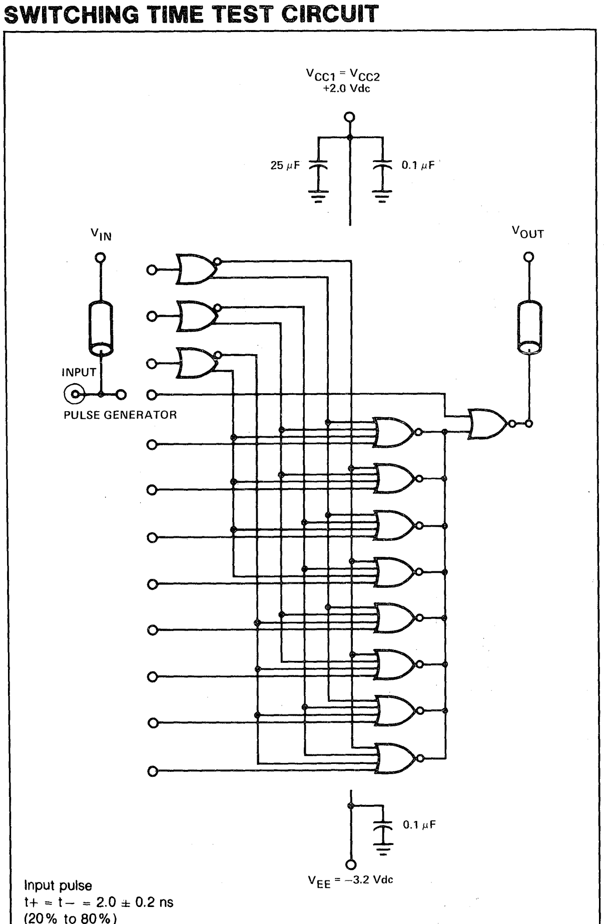
FEATURES

- Fast propagation delay
  - = 3.5ns TYP data to output
  - = 5.0ns TYP address to output
  - = 2.0ns TYP enable to output
- Output enable to permit output bussing
- Low power dissipation = 290 mW/package TYP (no load)
- High fanout capability — can drive a 50 Ω line
- High immunity from power supply variations: $V_{EE} = -5.2V \pm 5\%$ recommended
- Meets ECL 10,000 series standard interface specifications

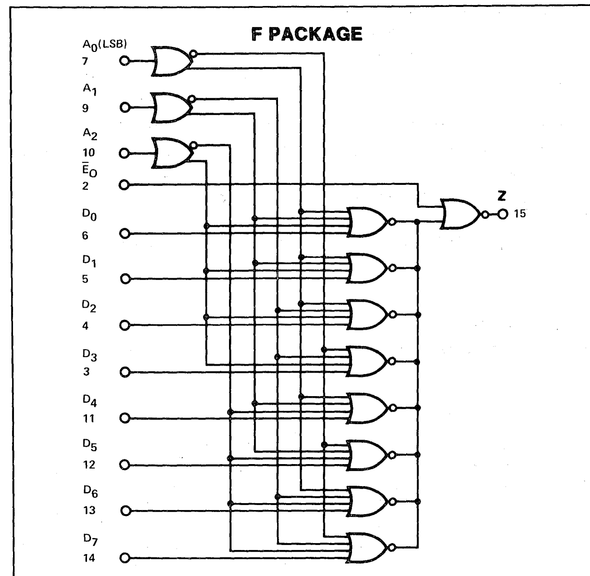
APPLICATIONS

- 8-to-1 multiplexer
- 8-to-1 data selector
- Parallel to serial conversion
- Barrel shift logic

SWITCHING TIME TEST CIRCUIT



LOGIC DIAGRAM



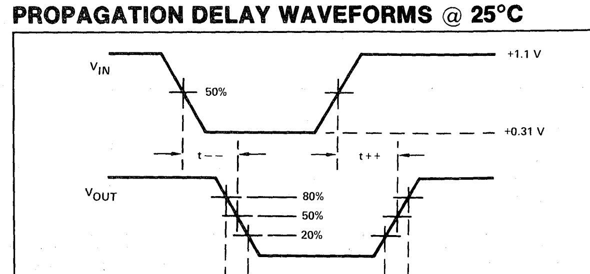
$V_{CC1} = 1$, $V_{CC2} = 16$, $V_{EE} = 8$
Positive logic: high level = '1'

TRUTH TABLE

ENABLE	ADDRESS INPUTS A2	A1	A0	Z
L	L	L	L	D0
L	L	L	H	D1
L	L	H	L	D2
L	L	H	H	D3
L	H	L	L	D4
L	H	L	H	D5
L	H	H	L	D6
L	H	H	H	D7
H	ø	ø	ø	L

ø = don't care.

PROPAGATION DELAY WAVEFORMS @ 25°C



NOTES:

1. Each ECL 10,000 series device has been designed to meet the DC specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Voltage levels will shift approximately 5 mV with an air flow of 200 linear fpm. Outputs are terminated through a 50-ohm resistor to -2.0 volts.
2. For AC tests, all input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be < ¼ inch from TP_{in} to input pin and TP_{out} to output pin. A 50-ohm termination to ground is located in each scope input. Unused outputs are connected to a 50-ohm resistor to ground.
3. Test procedures are shown for only one input or set of input conditions. Other inputs are tested in the same manner.
4. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.

10165F

DESCRIPTION

The 10165 is a device designed to provide a 3-bit binary coded output for each of 8 input lines. Priority selection circuitry is included so that the output reflects the highest priority input present and ignores lower order inputs. Each of the outputs is stored in a D type latch which allows synchronous sample and store operation. The operation of the latch may be bypassed by holding the C input low. The Q_3 output is high when any of the inputs are high. This allows extension to another device when more than 8 inputs are to be encoded.

FEATURES

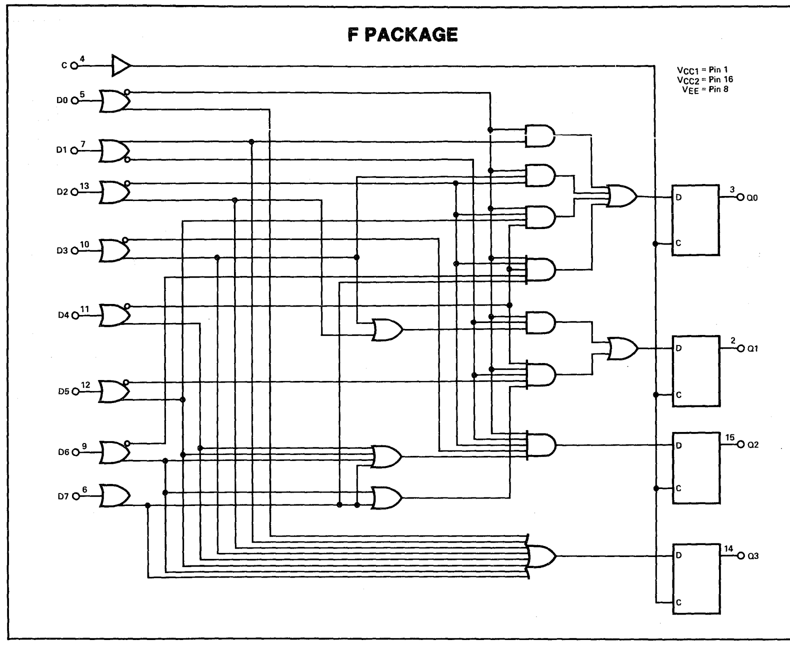
- **High functional density reduces package count**
- **Fast propagation delay = 7.0ns typical**
- **Low power dissipation = 545mW/package typical (no load)**
- **Open emitter logic and bussing capability**
- **High Z inputs — internal 50 kΩ resistors**
- **High fanout capability — can drive 50Ω lines**
- **Controlled output rise and fall times — −2.0ns typical (20% to 80%) (all outputs loaded)**
- **High immunity from power supply variations—V_{EE} = −5.2V±5% recommended**

TRUTH TABLE

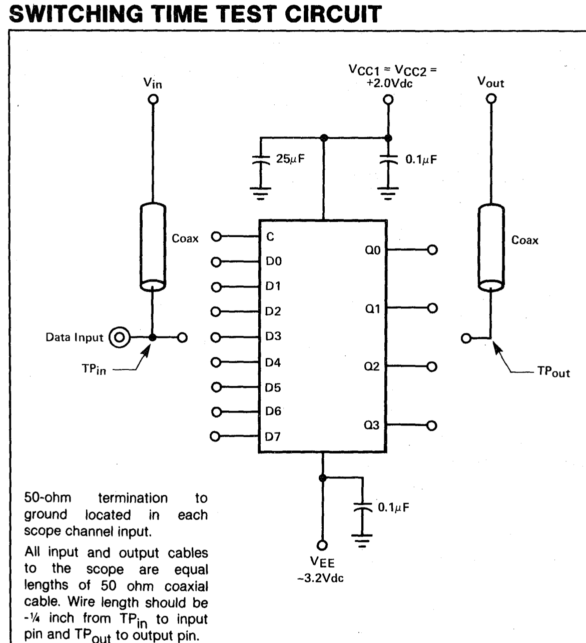
DATA INPUTS								OUTPUTS			
D0	D1	D2	D3	D4	D5	D6	D7	Q3	Q2	Q1	Q0
H	ø	ø	ø	ø	ø	ø	ø	H	L	L	L
L	H	ø	ø	ø	ø	ø	ø	H	L	L	H
L	L	H	ø	ø	ø	ø	ø	H	L	H	L
L	L	L	H	ø	ø	ø	ø	H	L	H	H
L	L	L	L	H	ø	ø	ø	H	H	L	L
L	L	L	L	L	H	ø	ø	H	H	L	H
L	L	L	L	L	L	H	ø	H	H	H	L
L	L	L	L	L	L	L	H	H	H	H	H
L	L	L	L	L	L	L	L	L	L	L	L

ø = don't care
P_D = 545mW typ/pkg (no load)
t_{pd} = 7.0ns typ (data to output)

LOGIC DIAGRAM

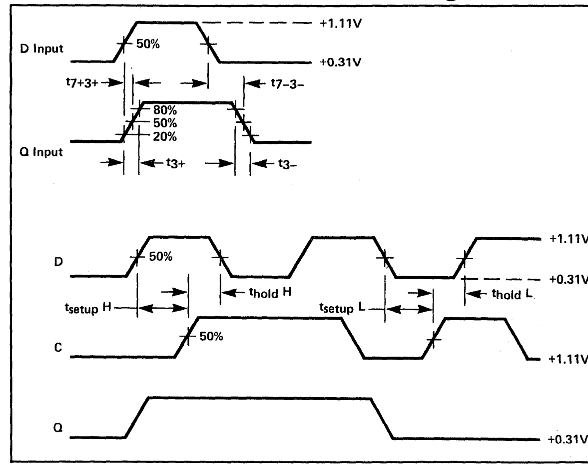


SWITCHING TIME TEST CIRCUIT



10165F

PROPAGATION DELAY WAVEFORMS @ 25°C



9-BIT PARITY CIRCUIT (WITH 2 CARRY INPUTS) 10170

10170-F

FEATURES

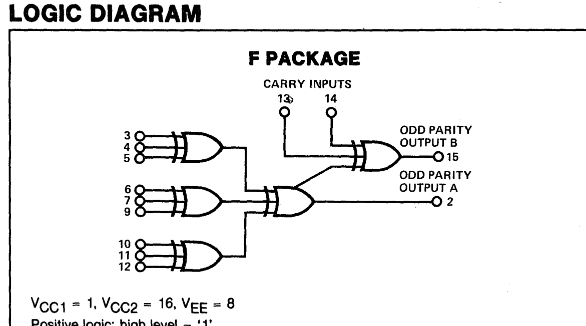
- **Optimized for byte-organized systems**
- **Fast propagation delay**
  - **= 4.0 ns TYP (input to output A)**
  - **= 6.0ns TYP (input to output B)**
  - **= 2.0ns TYP (carry to output B)**
- **Carry inputs for easy expansion or odd/even control**
- **Up to 9 bit check in 4.0ns**
- **Up to 27 bit check in 6.0ns with no additional gates required**
- **Low power dissipation = 280mW/package TYP (no load)**
- **High fanout capability — can drive 50Ω lines**
- **High Z inputs — internal 50kΩ pulldowns**
- **High immunity from power supply variations**
- **Open emitter outputs for logic and bussing capability**

APPLICATIONS

DETECTION OR GENERATION OF PARITY IN:

- **High speed central processors**
- **High speed peripherals**
- **High speed minicomputers**
- **Communication systems**
- **Instrumentation**

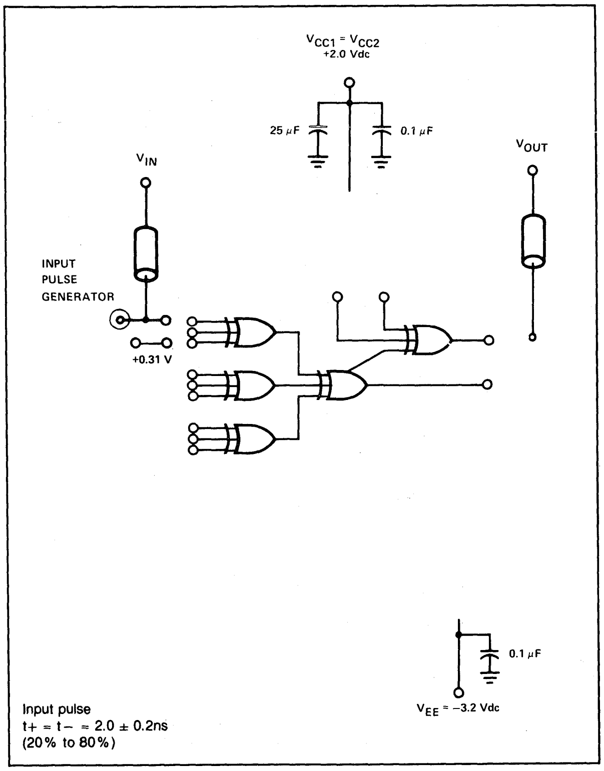
LOGIC DIAGRAM



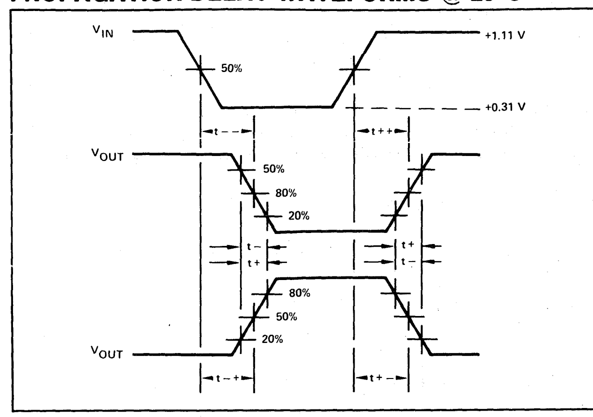
TRUTH TABLE

INPUT	OUTPUT
SUM OF HIGH LEVEL INPUTS PINS 3-12	PIN 2
EVEN	LOW
ODD	HIGH
SUM OF ALL HIGH LEVEL INPUTS (INCLUDING CARRY INPUTS)	PIN 15
EVEN	LOW
ODD	HIGH

SWITCHING TIME TEST CIRCUIT



PROPAGATION DELAY WAVEFORMS @ 25°C



NOTES:

1. Each ECL 10,000 series device has been designed to meet the DC specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 fpm is maintained. Voltage levels will shift approximately 5mV with an air flow of 200 linear fpm. Outputs are terminated through a 50-ohm resistor to −2.0 volts.
2. For AC tests, all input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire lengths should be <¼ inch from TP_{in} to input pin and TP_{out} to output pin. A 50-ohm termination to ground is located in each scope channel input. Unused outputs are connected to a 50-ohm resistor to ground.
3. Test procedures are shown for only one input or set of input conditions. Other inputs are tested in the same manner.
4. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.

10171-F

FEATURES

- **Fast propagation delay**
  = 4.0 ns TYP address to output
  = 4.5 ns TYP enable or data to output
- **Low power dissipation = 310 mW/package TYP (no load)**
- **High fanout capability — can drive eight 50 Ω lines**
- **True parallel decoder — eliminates unequal delay times**
- **High immunity from power supply variations: $V_{EE} = -5.2V \pm 5\%$ recommended**
- **High Z inputs — internal 50 kΩ pulldowns**
- **Open emitter outputs**
- **Meets ECL 10,000 series standard interface specifications**

APPLICATIONS

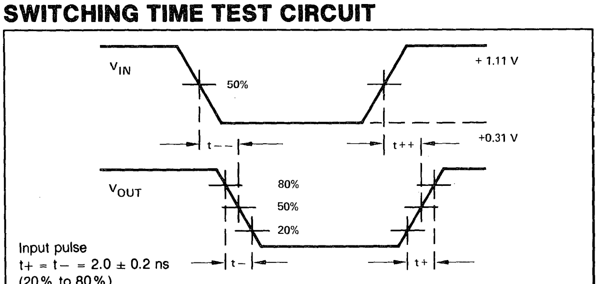
- **Dual 1 line to 4 line demultiplexer**
- **Crossbar switch applications**
- **High fanout 1 of 4 decoder**
- **Memory chip select decoder**

TRUTH TABLE

INPUTS				OUTPUTS			
$\overline{EO}$	A1	A0	DAIN	DA0	DA1	DA2	DA3
L	L	L	L	L	H	H	H
L	L	L	H	H	H	H	H
L	L	H	L	H	L	H	H
L	L	H	H	H	H	H	H
L	H	L	L	H	H	L	H
L	H	L	H	H	H	H	H
L	H	H	L	H	H	H	L
L	H	H	H	H	H	H	H
H	ø	ø	ø	H	H	H	H

DB is similar. ø = don't care

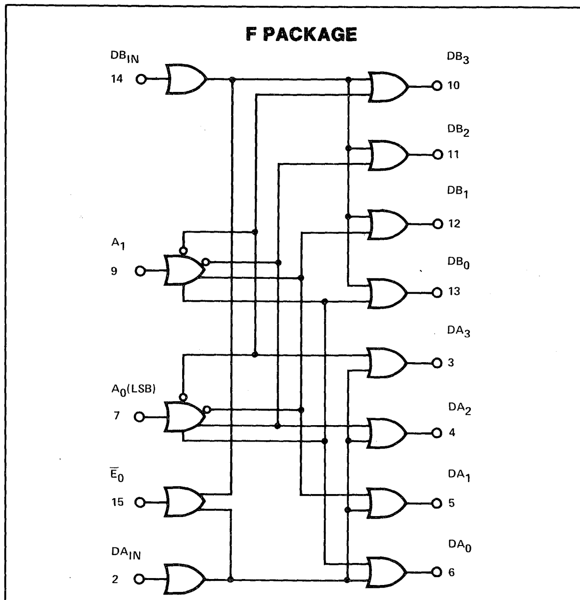
SWITCHING TIME TEST CIRCUIT



NOTES:

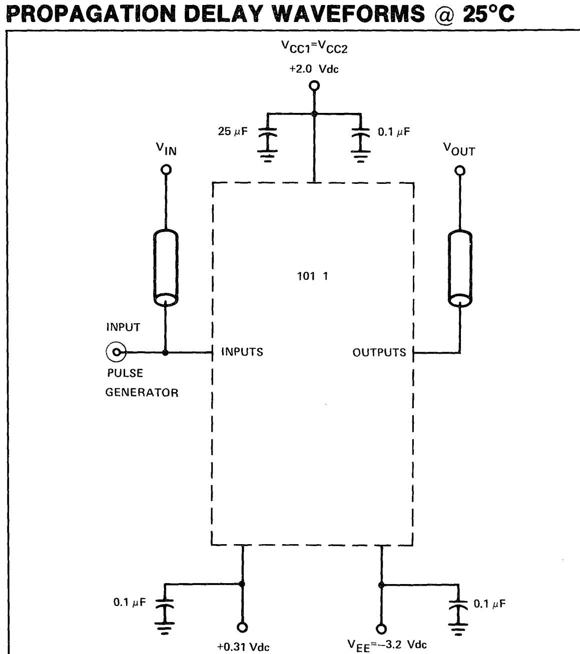
1. Each ECL 10,000 series device has been designed to meet the DC specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Voltage levels will shift approximately 6 mV with an air flow of 200 linear fpm. Outputs are terminated through a 50-ohm resistor to 2.0 volts.
2. For AC tests, all input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be <¼ inch from TP_{in} to input pin and TP_{out} to output pin. A 50-ohm termination to ground is located in each scope input. Unused outputs are connected to a 50-ohm resistor to ground.
3. Test procedures are shown for only one input or set of input conditions. Other inputs are tested in the same manner.
4. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.

LOGIC DIAGRAM



(Internal connections are emitter-dot or)
$V_{CC1} = 1$, $V_{CC2} = 16$, $V_{EE} = 8$
Positive logic: high level = '1'

PROPAGATION DELAY WAVEFORMS @ 25°C



10172-F

FEATURES

- **Fast propagation delay**
  = 4.0ns TYP address to output
  = 4.5ns TYP enable or data to output
- **Low power dissipation = 310 mW/package TYP (no load)**
- **High fanout capability — can drive eight 50 Ω lines**
- **True parallel decoder — eliminates unequal delay times**
- **High immunity from power supply variations: V_{EE} = −5.2 V±5% recommended**
- **High Z inputs — internal 50 kΩ pulldowns**
- **Open emitter outputs**
- **Meets ECL 10,000 series standard interface specifications**

APPLICATIONS

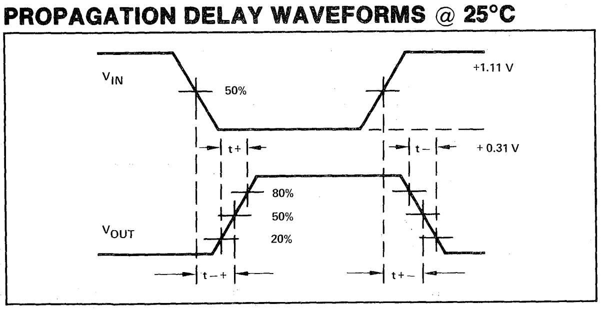
- **Dual 1-line to 4-line Demultiplexer**
- **Crossbar Switch Applications**
- **High Fanout 1 of 4 Decoder**
- **Memory Chip Select Decoding**

TRUTH TABLE

INPUTS				OUTPUTS			
$\overline{EO}$	A1	A0	DA IN	DA0	DA1	DA2	DA3
L	L	L	H	H	L	L	L
L	L	L	L	L	L	L	L
L	L	H	H	L	H	L	L
L	L	H	L	L	L	L	L
L	H	L	H	L	L	H	L
L	H	L	L	L	L	L	L
L	H	H	H	L	L	L	H
L	H	H	L	L	L	L	L
H	ø	ø	ø	L	L	L	L

DB is similar. ø = don't care

PROPAGATION DELAY WAVEFORMS @ 25°C



NOTES:

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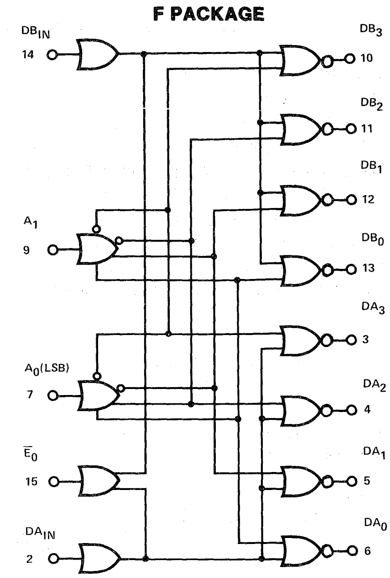
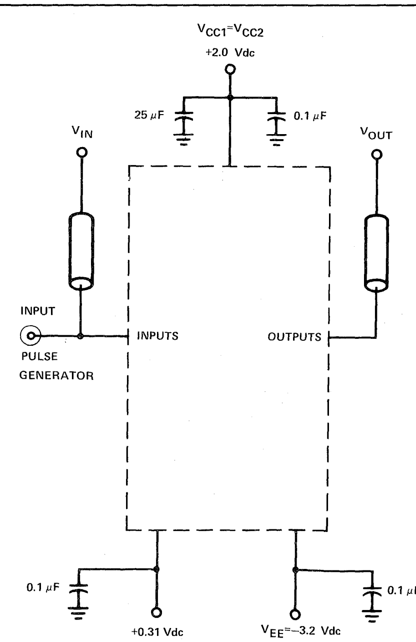
2. For AC tests, all input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be <¼ inch from TP_{in} to input pin and TP_{out} to output pin. A 50-ohm termination to ground is located in each scope input. Unused outputs are connected to a 50-ohm resistor to ground.
3. Test procedures are shown for only one input or set of input conditions. Other inputs are tested in the same manner.
4. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.

LOGIC DIAGRAM



(Internal connections are emitter-dot or)
V_{CC1} = 1, V_{CC2} = 16, V_{EE} = 8
Positive logic: high level = '1'

SWITCHING TIME TEST CIRCUIT



Input pulse
t+ = t− = 2.0 ± 0.2 ns
(20% to 80%)

10173-F

FEATURES

- Simultaneous multiplexing and latching function improves system performance
- Quad latch and multiplexer on one chip increases system density
- Fast propagation delay
  - =2.5ns TYP (data to output)
  - =3.7ns TYP (select to output)
  - =4.3ns TYP (clock to output)
- Low power dissipation = 325 mW/ Package TYP (no load)
- High fanout capability — can drive 50 Ω lines
- High Z inputs — internal 50 kΩ pulldowns
- High immunity from power supply variations: $V_{EE} = \pm 5.2V \pm 5\%$ recommended
- Open emitter outputs — allow wire or and data bussing

APPLICATIONS

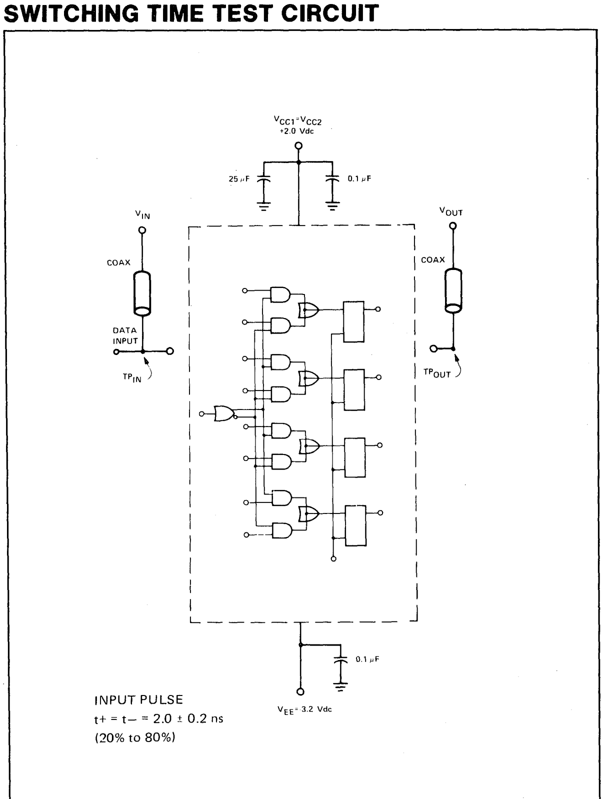
- Combined multiplexer — register for:
  - High speed central processors
  - High speed peripherals
  - High speed minicomputers
  - Communication systems
  - Instrumentation

TRUTH TABLE

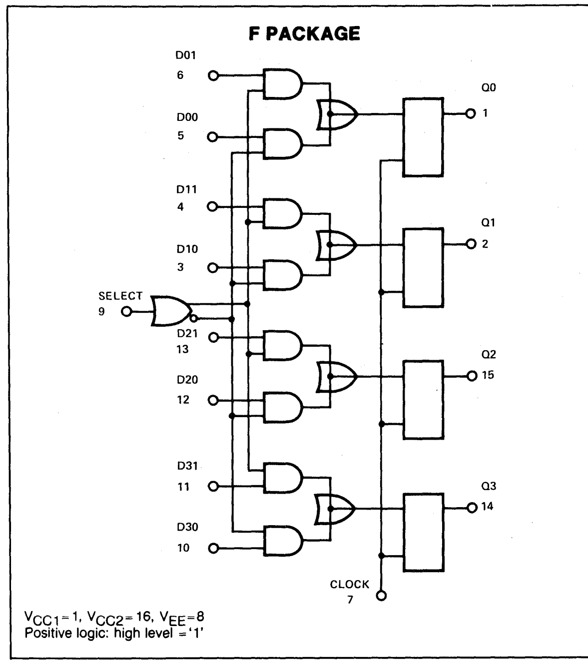
D_n	C	Q_n (N+1)
L	L	L
H	L	H
ø	H	Q_n (N)

$D_n = \bar{S} \cdot D_{n0} + S \cdot D_{n1}$ ø = don't care

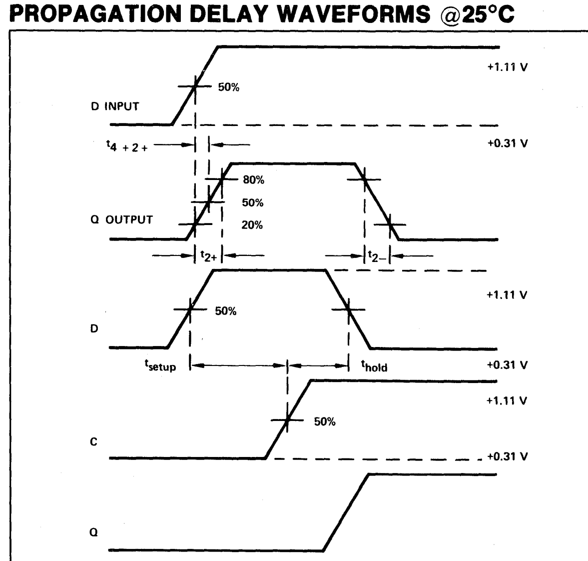
SWITCHING TIME TEST CIRCUIT



LOGIC DIAGRAM



PROPAGATION DELAY WAVEFORMS @25°C



NOTES:

1. Each ECL 10,000 series device has been designed to meet the DC specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 fpm is maintained. VOltage levels will shift approximately 6 mV with an air flow of 200 linear fpm. Outputs are terminated through a 50-ohm resistor to -2.0 volts.
2. For AC tests, all input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be <¼ inch from TP_{in} to input pin and TP_{out} to output pin. A 50-ohm termination to ground is located in each scope input. Unused outputs are connected to a 50-ohm resistor to ground.
3. Test procedures are shown for only one input or set of input conditions. Other inputs are tested in the same manner.
4. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.

10174-F

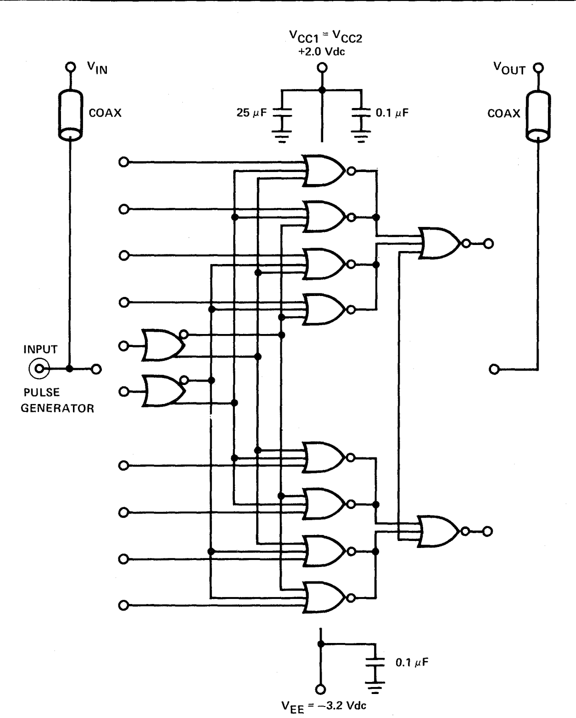
FEATURES

- Fast propagation delay
  - =3.5 ns TYP data to output
  - =5.0ns TYP address to output
  - =2.0 ns TYP enable to output
- Output enable to permit output bussing
- Low power dissipation = 290 mW/package TYP (no load)
- High fanout capability - can drive two 50 Ω lines
- High immunity from power supply variations: $V_{EE} = -5.2V \pm 5\%$ recommended
- Meets ECL 10,000 series standard interface specifications

APPLICATIONS

- Dual 4 to 1 multiplexer
- Dual 4 to 1 data selector
- Cross bar switch applications

SWITCHING TIME TEST CIRCUIT

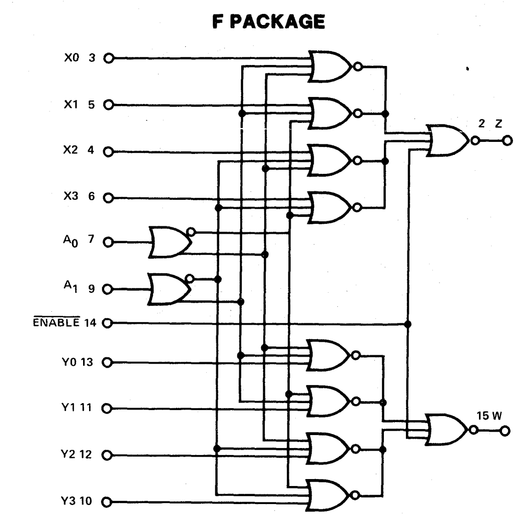


Input pulse
t+ = t- =2.0 ± 0.2 ns
(20% to 80%)

NOTES:

1. Each ECL 10,000 series device has been designed to meet the DC specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 fpm is maintained. Voltage levels will shift approximately 5 mV with an air flow of 200 linear fpm. Outputs are terminated through a 50-ohm resistor to -2.0 volts.
2. For AC tests, all input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be <¼ inch from TP_{in} to input pin and TP_{out} to output pin. A 50-ohm termination to ground is located in each scope channel input. Unused outputs are connected to a 50-ohm resistor to ground.
3. Test procedures are shown for only one input or set of input conditions. Other inputs are tested in the same manner.
4. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.

LOGIC DIAGRAM



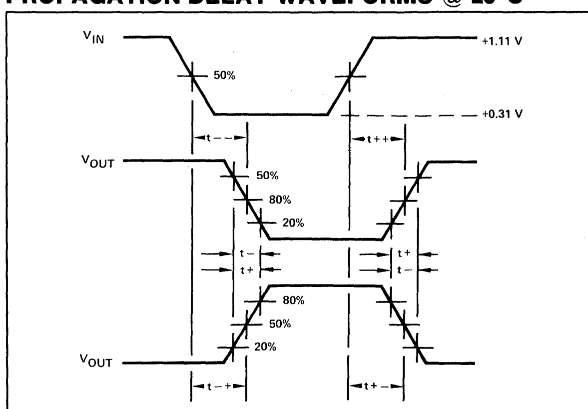
$V_{CC1} = 1$, $V_{CC2} = 16$, $V_{EE} = 8$
Positive logic: high level = '1'

TRUTH TABLE

ENABLE	ADDRESS INPUTS		OUTPUTS	
$\overline{E}$	A1	A0	Z	W
H	ø	ø	L	L
L	L	L	X0	Y0
L	L	H	X1	Y1
L	H	L	X2	Y2
L	H	H	X3	Y3

ø= don't care

PROPAGATION DELAY WAVEFORMS @ 25°C



10175-F

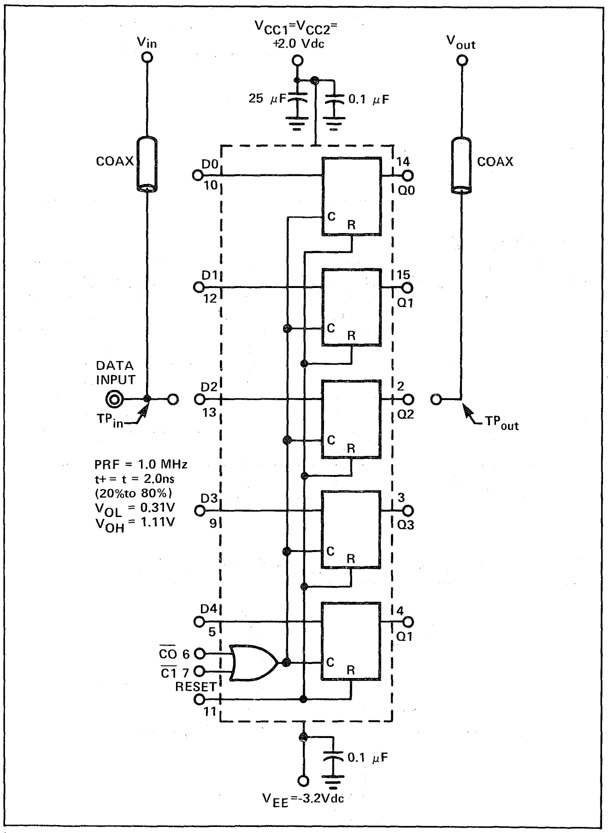
DESCRIPTION

The 10175 is a device which incorporates five D type latches with a common reset and two-input clock. While both of the clock inputs are low the outputs will follow the inputs. The outputs are latched when either of the clocks goes high. The reset is enabled only when the clock is in the high state. Open emitter outputs permit the device to be wire "OR"ed with other open emitter outputs.

FEATURES

- **High speed — 2.5ns data to output delay typical**
- **Common asynchronous reset function**
- **High Z inputs — internal 50kΩ resistors**
- **High fanout capability — drives 50 ohms**
- **Controlled output rise and fall times — 2ns typical**
- **Two separate clock pins — can be used for clock enable function**

SWITCHING TIME TEST CIRCUIT

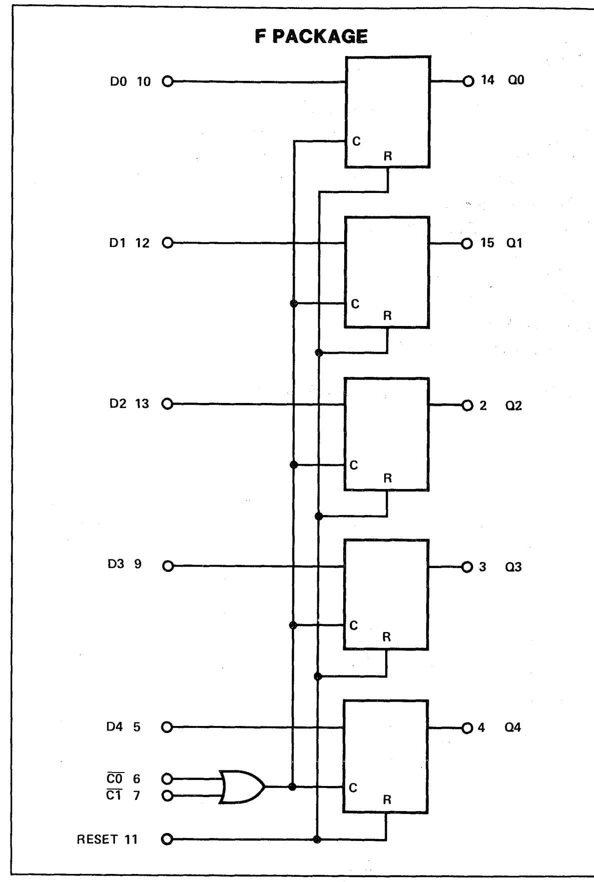


V_{CC1} = pin 1
V_{CC2} = pin 16
V_{EE} = pin 8
P_D = 400mW typ/pkg (no load)
t_{pd} = 2.5nS typ (data to output)

50-ohm termination to ground located in each scope channel input

All input and output cables to the scope are equal lengths of 50 ohm coaxial cable. Wire length should be <¼ inch from TP_{in} to input pin and TP_{out} to output pin.

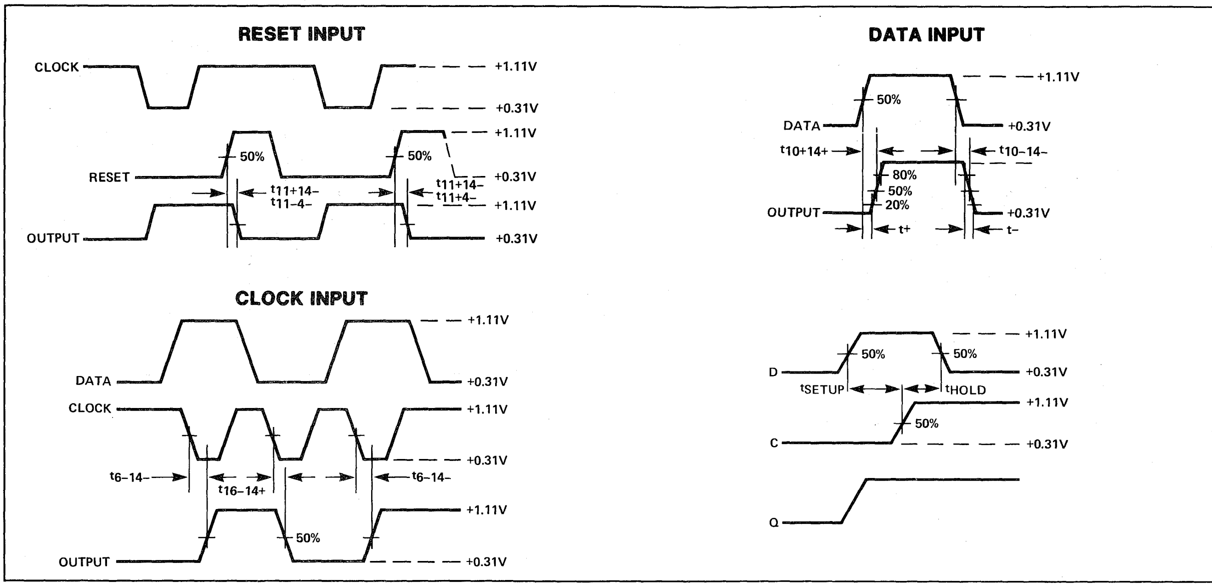
LOGIC DIAGRAM



TRUTH TABLE

D	CO	C1	RESET	Q_{n+1}
L	L	L	L	L
H	L	L	L	H
X	H	X	L	Qn
X	X	H	L	Qn
X	H	X	H	L
X	X	H	H	L

VOLTAGE WAVEFORMS



NOTES:

1. t_{setup} is the minimum time before the positive transition of the clock pulse (c) that information must be present at the data input (D).
2. t_{hold} is the minimum time after the positive transition of the clock pulse (c) that information must remain unchanged at the data input (D).

HEX D-TYPE MASTER-SLAVE FLIP-FLOP 10176

10176-F

DESCRIPTION

The 10176 contains six D-type master-slave flip flops in a single package. Data present on the "D" inputs are entered into all six master bistables when the common clock input is low. This data is subsequently transferred to the slave bistable when the clock goes from low to high. Thus, outputs change only on a positive-going clock input transition. Data present at the inputs, therefore, will not affect the outputs except on the low to high clock transition.

FEATURES

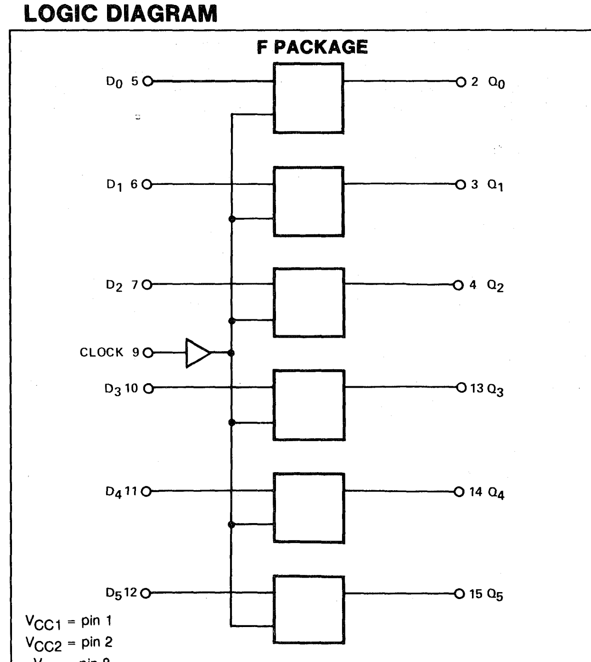
- **High speed**
  Toggle frequency = 150 MHz typical
  Propagation delay = 4.0 ns typical
- **Low power**
  460 mW per package typical
- **High fanout**
  50Ω drive capability
- **High Z inputs with 50KΩ pulldown resistors**
- **Open emitter outputs for bussing applications**

TRUTH TABLE

C	D	On+1
L	ø	Qn
L→H	L	L
L→H	H	H
H→L	ø	Qn

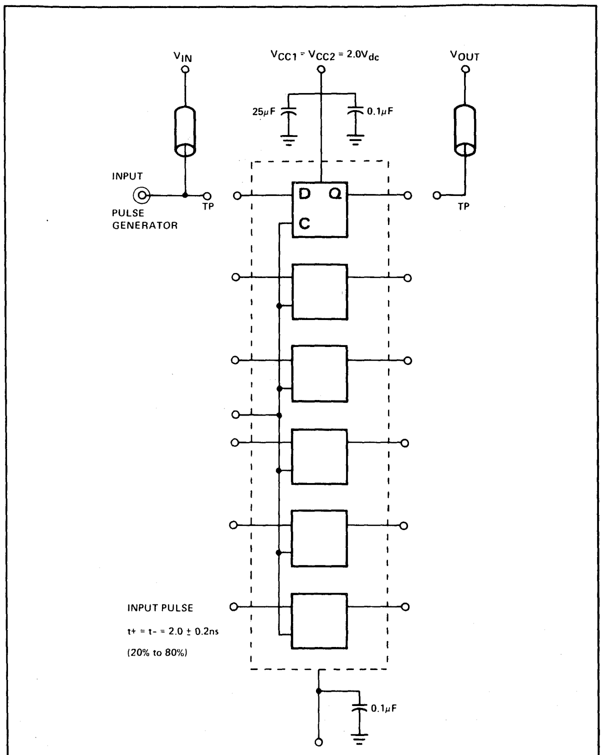
ø= Don't Care

LOGIC DIAGRAM



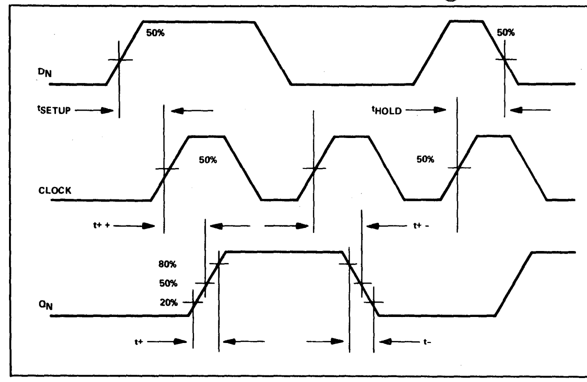
10176-F

SWITCHING TIME TEST CIRCUIT



Input pulse
t+ = t− = 2.0 ± 0.2 ns
(20% to 80%)

PROPAGATION DELAY WAVEFORMS @ 25°



NOTES:

1. Each ECL 10,000 series device has been designed to meet the DC specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Voltage levels will shift approximately 5 mV with an air flow of 200 linear fpm. Outputs are terminated through a 50-ohm resistor to 2.0 volts.
2. For AC tests, all input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be <¼ inch from TP_{in} to input pin and TP_{out} to output pin. A 50-ohm termination to ground is located in each scope input. Unused outputs are connected to a 50-ohm resistor to ground.
3. Test procedures are shown for only one input or set of input conditions. Other inputs are tested in the same manner.
4. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.

LOOK-AHEAD CARRY 10179

10179-F

DESCRIPTION

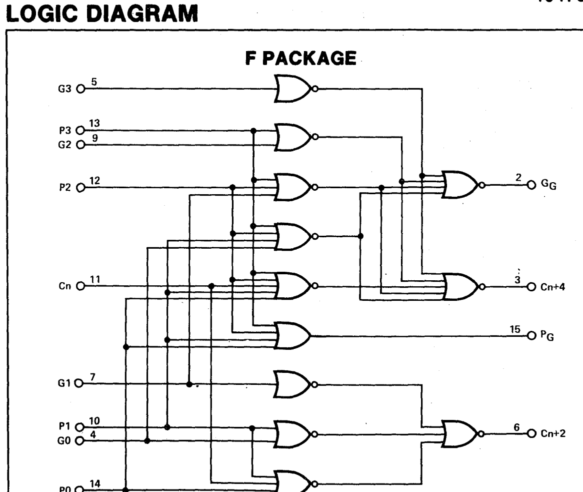
The 10179 is a look-ahead carry device that can be used with the 10180 (dual arithmetic unit) or the 10181 (4 bit ALU) to perform high speed arithmetic on long words. The device is capable of examining carry data from four arithmetic units and generating both 2nd and 4th order look-ahead carries to greatly increase system speed over that which can be obtained using ripple-carry techniques.

Additional features of the 10179 include high Z inputs with pull down resistors to allow unused inputs to be left open and open-emitter outputs with 50Ω drive capability.

FEATURES

- **High speed: propagation delay =**
  3.0ns TYP carry, propagate
  4.0ns TYP generate
- **Low power: 200mW TYP (no load)**
- **High fan out: can drive 50Ω lines**
- **High Z inputs with 50kΩ pull down resistors.**
- **Open emitter outputs**

LOGIC DIAGRAM



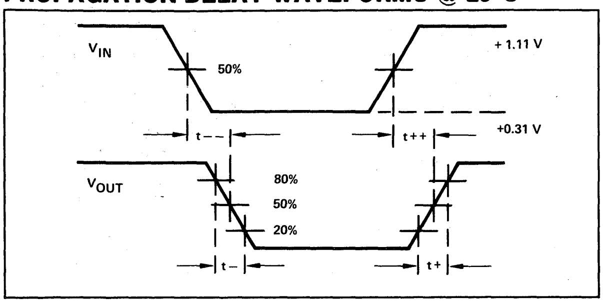
V_{CC1} = 1, V_{CC2} = 16, V_{EE} = 8
Positive logic: high level "1"

10179-F

LOGIC EQUATIONS

PG= P0 + P1 + P2 + P3
GG= (G0 + P1 + P2 + P3)
(G1 + P2 + P3)
(G2 + P3) G3
Cn+2= (Cn + P0 + P1) (G0 + P1) G1
Cn+4= (Cn + P0 + P1 + P2 + P3)
(G0 + P1 + P2 + P3)
(G1 + P2 + P3) (G2 + P3) G3

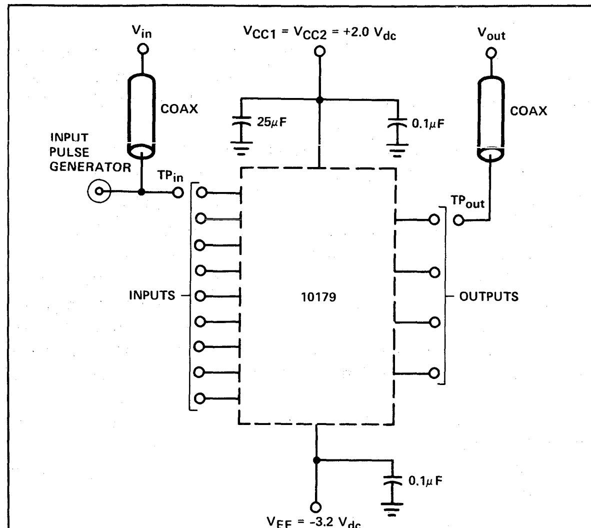
PROPAGATION DELAY WAVEFORMS @ 25°C



NOTES:

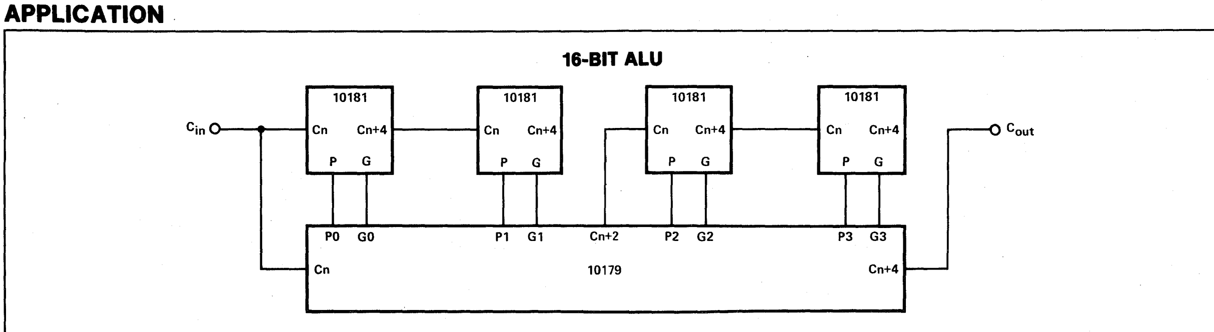
1. Each ECL 10,000 series device has been designed to meet the DC specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Voltage levels will shift approximately 4 mV with an air flow of 200 linear fpm. Outputs are terminated through a 50-ohm resistor to 2.0 volts.
2. For AC tests, all input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be <¼ inch from TP_{in} to input pin and TP_{out} to output pin. A 50-ohm termination to ground is located in each scope input. Unused outputs are connected to a 50-ohm resistor to ground.
3. Test procedures are shown for only one input or set of input conditions. Other inputs are tested in the same manner.
4. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.

SWITCHING TIME TEST CIRCUIT



Input pulse
t+ = t− = 2.0 ± 0.2ns
(20% to 80%)

APPLICATION



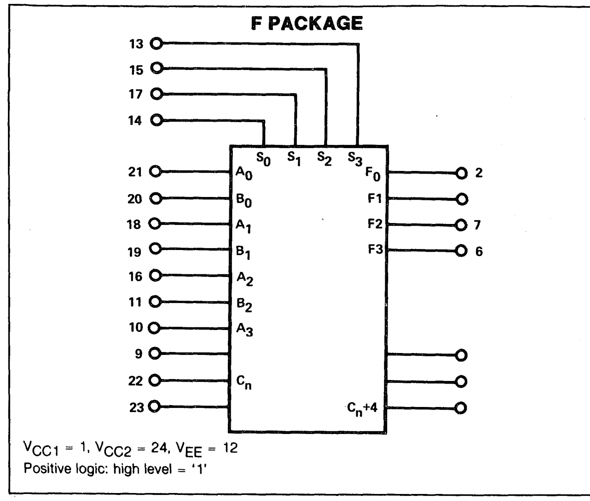
10181F

DESCRIPTION

The 10181 is an extremely versatile high speed arithmetic logic unit capable of performing 16 logic operations and 16 arithmetic functions on two four-bit words. Using advanced circuit design techniques and double layer metalization the 10181 represents the state-of-the-art in standard ECL/LSI functions. As a result, the 10181 has the same power dissipation as the comparable TTL function, while increasing the speed of operation by a factor of 4.

The $\overline{M}$ input selects the arithmetic or logic mode of operation on 2 four-bit words. The desired arithmetic or logic function is selected by applying the appropriate binary word to the select inputs ($\overline{S0}$ thru $\overline{S3}$). Full internal carry is incorporated for ripple-through operation. Group carry propagate (P_G) and carry generate (G_G) are provided to allow fast addition of very long words using a second order look-ahead in conjunction with the 10179 full look-ahead carry block. The internal carry is enabled when the mode control input (M) has a low-level voltage applied (arithmetic operation). Full addition of two 32-bit words, with carry in and carry out can be performed in 18 ns. All inputs have 50kΩ internal pulldown resistors, and outputs are all open emitters for versatility in interconnect techniques.

BLOCK DIAGRAM



FEATURES

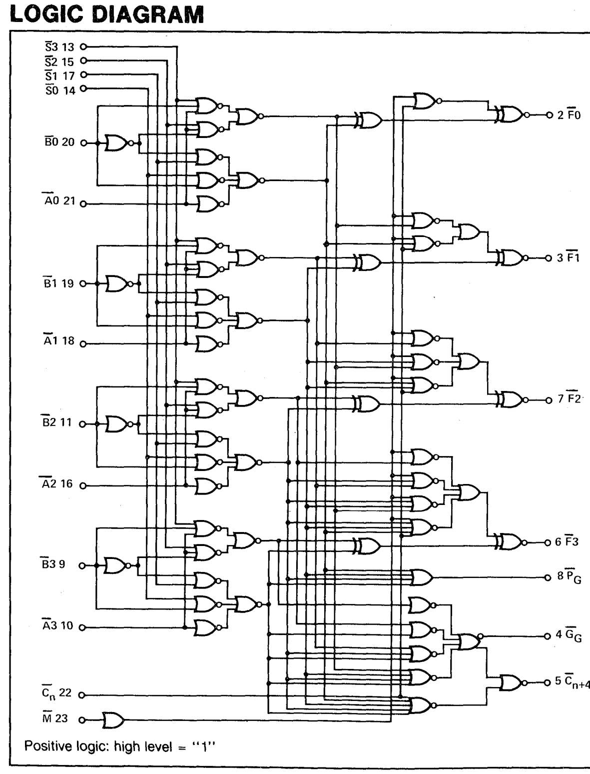
- **Fast propagation delays:**
  - **= 3.1 ns TYP ($\overline{C}_n$ to $\overline{C}_{n+4}$)**
  - **= 5.0 ns TYP ($\overline{C}_n$ to $\overline{F}_1$)**
  - **= 7.0 ns TYP ($\overline{A1}$, $\overline{B1}$ to $\overline{F1}$)**
  - **= 5.0 ns TYP ($\overline{A1}$ to $\overline{C}_{n+4}$)**
- **16 logic operations**
- **16 arithmetic operations**
- **Power dissipation = 600 mW/package TYP (no load)**
- **High Z inputs — internal 50 kΩ pulldowns**
- **High immunity from power supply variations: V_{EE} = −5.2 V ±5% recommended**
- **Open emitters for bussing and logic capability**

FUNCTIONAL TRUTH TABLE

Function Select $\overline{S3}$	$\overline{S2}$	$\overline{S1}$	$\overline{S0}$	Logic Functions $\overline{M}$ is High $\overline{F}$	Arithmetic Operation $\overline{M}$ is Low $\overline{C}_n$ of LSB must be High $\overline{F}$
L	L	L	L	$\overline{F}$ = A	F = A minus 1
L	L	L	H	$\overline{F}$ = A + $\overline{B}$	F = A plus (A + $\overline{B}$)
L	L	H	L	$\overline{F}$ = A + B	F = A plus (A + B)
L	L	H	H	$\overline{F}$ = Logical "1"	F = A times 2
L	H	L	L	$\overline{F}$ = A • B	F = (A • B) minus 1
L	H	L	H	$\overline{F}$ = B	F = (A • B) plus (A + $\overline{B}$)
L	H	H	L	$\overline{F}$ = A ⊙ B	F = A plus B
L	H	H	H	$\overline{F}$ = $\overline{A}$ + B	F = A plus (A • $\overline{B}$)
H	L	L	L	$\overline{F}$ = A • $\overline{B}$	F= (A • $\overline{B}$) minus 1
H	L	L	H	$\overline{F}$ = A ⊕ B	F = A minus B minus 1
H	L	H	L	$\overline{F}$ = $\overline{B}$	F = (A • $\overline{B}$) plus (A + B)
H	L	H	H	$\overline{F}$ = A + $\overline{B}$	F = (A • $\overline{B}$) plus A
H	H	L	L	$\overline{F}$ = Logical "0"	F = minus 1 (two's complement)
H	H	L	H	$\overline{F}$ = $\overline{A}$ • $\overline{B}$	F= (A + $\overline{B}$) plus 0
H	H	H	L	$\overline{F}$ = $\overline{A}$ • B	F = (A + B) plus 0
H	H	H	H	$\overline{F}$ = $\overline{A}$ = $\overline{A}$	F = A plus 0

•$\overline{F}$ outputs of ALU are one's complement of function listed below.

LOGIC DIAGRAM



SWITCHING CHARACTERISTICS

	PARAMETER	INPUT	OUTPUT	TEST CONDITIONS†	+25°C MIN	TYP	MAX	UNIT
t++	Propagation Delay	$\overline{C}_n$	$\overline{C}_{n+4}$	—	—	3.2	—	ns
t−−					—	3.1		
t+	Rise Time				—	2.0		
t−	Fall Time				—	2.0	—	
t++	Propagation Delay	$\overline{C}_n$	$\overline{F}1$	$\overline{M}$ is Low	—	4.9	—	ns
t+−					—	5.0	—	
t−+					—	4.9	—	
t−−					—	5.0	—	
t+	Rise Time				—	2.0	—	
t−	Fall Time				—	2.0	—	
t++	Propagation Delay	$\overline{A}1$	$\overline{F}1$	—	—	7.0	—	ns
t+−					—	7.0	—	
t−+					—	7.0	—	
t−−					—	7.0	—	
t+	Rise Time				—	2.0	—	
t−	Fall Time				—	2.0	—	
t++	Propagation Delay	$\overline{A}1$	$\overline{P}_G$	—	—	3.0	—	ns
t−−					—	3.0	—	
t+	Rise Time				—	2.0	—	
t−	Fall Time				—	2.0	—	
t++	Propagation Delay	$\overline{A}1$	$\overline{G}_G$	—	—	4.0	—	ns
t−−					—	5.0	—	
t+	Rise Time				—	2.0	—	
t−	Fall Time				—	2.0	—	
t+−	Propagation Delay	$\overline{A}1$	$\overline{C}_{n+4}$	—	—	5.4	—	ns
t−+					—	4.4	—	
t+	Rise Time				—	2.0	—	
t−	Fall Time				—	2.0	—	
t++	Propagation Delay	$\overline{B}1$	$\overline{F}1$	$\overline{S}1$ and $\overline{S}2$ High $\overline{S}0$ or $\overline{S}3$ Low	—	7.0	—	ns
t+−					—	7.0	—	
t−+					—	7.0		
t−−					—	7.0	—	
t+	Rise Time				—	2.0	8	
t−	Fall Time				—	2.0	—	
t++	Propagation Delay	$\overline{B}1$	$\overline{P}_G$	$\overline{S}0$ Low, $\overline{S}1$ High	—	3.0	—	ns
t−−					—	3.0	—	
t+	Rise Time				—	2.0	—	
t−	Fall Time				—	2.0	—	
t++	Propagation Delay	$\overline{B}1$	$\overline{B}_G$	$\overline{S}2$ High, $\overline{S}3$ Low	—	4.0	—	ns
t−−					—	5.0	—	
t+	Rise Time				—	2.0	—	
t−	Fall Time				—	2.0	—	
t+−	Propagation Delay	$\overline{B}1$	$\overline{C}_{n+4}$	$\overline{S}1$ and $\overline{S}2$ High, $\overline{S}0$ or $\overline{S}3$ Low	—	5.4	—	ns
t−+					—	4.4	—	
t+	Rise Time				—	2.0	—	
t−	Fall Time				—	2.0	—	
t++	Propagation Delay	$\overline{B}1$	$\overline{F}1$	$\overline{S}1$ or $\overline{S}2$ Low	—	7.5	—	ns
t+−					—	8.0	—	
t−+					—	7.5	—	
t−−					—	8.0	—	
t+	Rise Time				—	2.0	—	
t−	Fall Time				—	2.0	—	

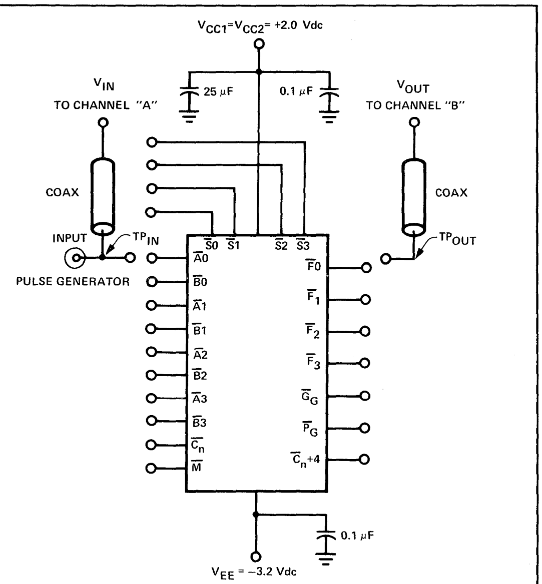
10181F

SWITCHING CHARACTERISTIC

	PARAMETER	INPUT	OUTPUT	TEST CONDITIONS†	+25°C MIN	TYP	MAX	UNIT
t+−	Propagation Delay	$\overline{B}1$	$\overline{P}_G$	$\overline{S}1$ Low	—	4	—	ns
t−+					—	4	—	
t+	Rise Time				—	2.0	—	
t−	Fall Time				—	2.0	—	
t−+	Propagation Delay	$\overline{B}1$	$\overline{G}_G$	$\overline{S}2$ Low	—	5.2	—	ns
t+−					—	5.7	—	
t+	Rise Time				—	2.0	—	
t−	Fall Time				—	2.0	—	
t+−	Propagation Delay	$\overline{B}1$	$\overline{C}_{n+4}$	$\overline{S}0$ or $\overline{S}1$ or $\overline{S}2$ or $\overline{S}3$ Low	—	5.9	—	ns
t−+					—	5.6	—	
t+	Rise Time				—	2.0	—	
t−	Fall Time				—	2.0	—	

+High = +1.11V
Low = +0.31V
$V_{CC1} = V_{CC2}$ = +2.0 Vdc = −3.2 Vdc, V_{EE} = −3.2 Vdc

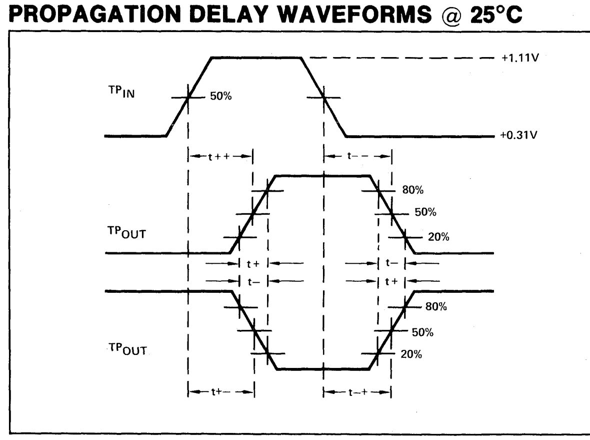
SWITCHING TIME TEST CIRCUIT



Input pulse
t+ = t− = 2.0 ± 0.2 ns
(20% to 80%)

Each ECL 10,000 series has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts.

PROPAGATION DELAY WAVEFORMS @ 25°C



All input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be <¼ inch from TP_{in} to input pin and TP_{out} to output pin.

QUAD DIFFERENTIAL RECEIVER/MST-ECL TRANSLATOR 10190

10190F

DESCRIPTION

The 10190 is both a general purpose ECL 10,000 series line receiver and an MST (IBM 370) to ECL translator. With the V_{CC} Terminal (Pin 9) connected to ground, the device will accept either single-ended or differential ECL 10K signals. With V_{CC} connected to +1.25 Volts, the device will accept MST logic levels (+0.4 and -0.4 nominal). In either case, the output of the 10190 is standard ECL 10K.

When used in the translator mode, one of the differential inputs is tied to ground and the other to the MST source. V_{CC} is non-critical between +0.5 and +2.0 Volts.

In the ECL line receiver mode, a single ended input is accommodated by connecting the other input to an external V_{BB} source.

10190F

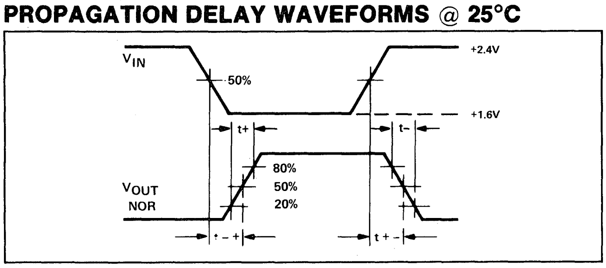
FEATURES

- **High speed; propagation delay = 2.5 ns TYP**
- **High common mode noise rejection**
- **Output drives 50 Ω lines**
- **Dual-purpose**
  - **Quad line receiver (ECL-ECL)**
  - **Transistor (MST-ECL)**
- **High input impedance**
- **Non-critical V_{CC} tolerance in translator mode (0.5 to +2.0 Volts)**
- **Open emitter outputs**
- **Immune to power supply faults**
- **Defined output (low) with both inputs open**

APPLICATIONS

- **Line receiver**
- **MST to ECL translator**

PROPAGATION DELAY WAVEFORMS @ 25°C

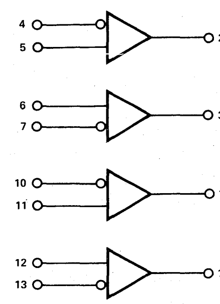


NOTES:

1. Each ECL 10,000 series device has been designed to meet the DC specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Voltage levels will shift approximately 3 mV with an air flow of 200 linear fpm. Outputs are terminated through a 50-ohm resistor to 2.0 volts.
2. For AC tests, all input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be <¼ inch from TP_{in} to input pin and TP_{out} to output pin. A 50-ohm termination to ground is located in each scope input. Unused outputs are connected to a 50-ohm resistor to ground.
3. Test procedures are shown for only one input or set of input conditions. Other inputs are tested in the same manner.
4. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.

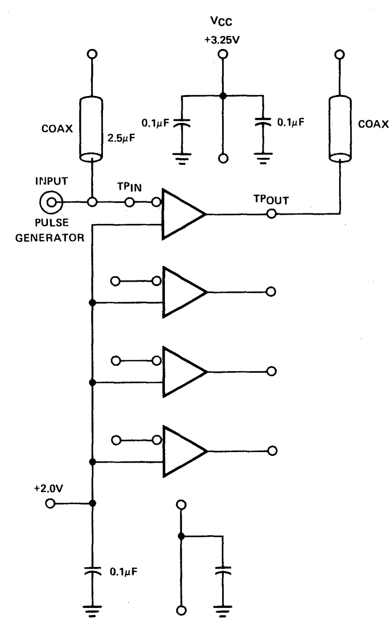
LOGIC DIAGRAM

F PACKAGE



t_{pd} = 2.5 ns TYP
V_{CC} = 9, V_{EE} = 8, GND = 1.16

SWITCHING TIME TEST CIRCUIT



Input pulse
t+ = t− = 2.0 ± 0.2 ns
(20% to 80%)

10191F

DESCRIPTION

The 10191 is a Hex ECL to MST (IBM 370) translator. With a standard 10,000 series logic level on the input, the output responds with an identical MST logic level at the output.

In addition, the translators have a common enable line which drives all six outputs to the low state when an ECL logic "1" level is present on the line.

The 10191 is a companion device to the 10190 which is an MST to ECL translator. With these two devices, a complete, high-speed interface is available to communicate between a standard 10,000 series ECL system and a standard MST system.

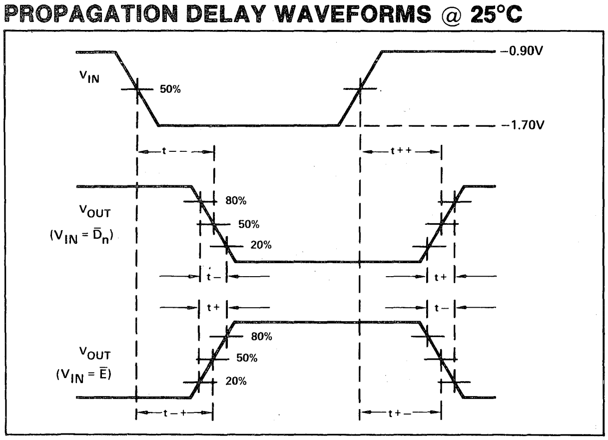
FEATURES

- **High speed; propagation delay = 2.2ns TYP**
- **Six translators per package**
- **90 OHM output drive capability**
- **Common enable input**
- **High impedance inputs with 50K pulldown resistors**
- **Open emitter outputs**

TRUTH TABLE

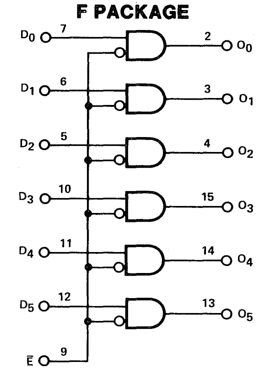
$\bar{E}$	Dn	On
0	0	0
0	1	1
1	X	0

PROPAGATION DELAY WAVEFORMS @ 25°C



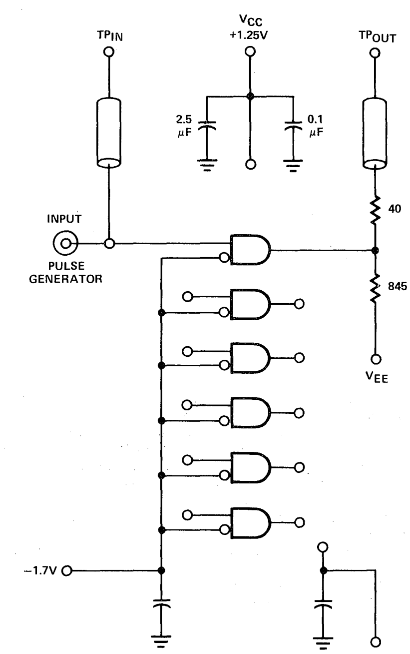
NOTES:
1. Each ECL 10,000 series device has been designed to meet the DC specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Voltage levels will shift approximately 4 mV with an air flow of 200 linear fpm. Outputs are terminated through a 90Ω to gnl and a 845Ω to V_{EE}.
2. For AC tests, all input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire lengths should be <¼ inch from TP_{in} to input pin and TP_{out} to output pin. A 50-ohm termination to ground is located in each scope input. Unused outputs are connected to a 90-ohm resistor to ground and a 845Ω to V_{EE}.
3. Test procedures are shown for only one input or set of input conditions. Other inputs are tested in the same manner.

LOGIC DIAGRAM



t_{pd} (data) = 2.2 ns TYP
t_{pd} ($\bar{E}$) = 2.8 ns TYP.
V_{CC} = 1, V_{EE} = 8, GND = 16

SWITCHING TIME TEST CIRCUIT



Input pulse
t+ = T− 2.0 ± 0.2ns
(20% to 80%)

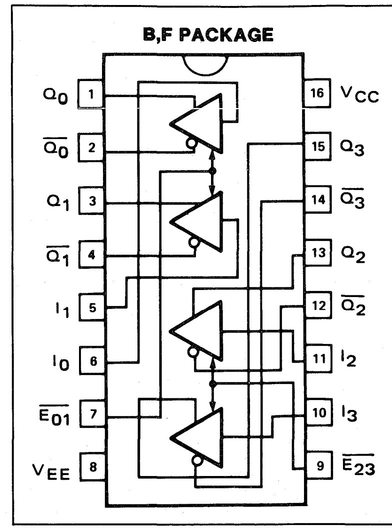
10192B,F

FEATURES

- Capable of party line operation
- Differential or single-ended mode
- 16mA current mode outputs
- 3-logic-state complementary outputs
- Drives long lines
- Excellent noise immunity
- Fast propagation delay — 4.0ns TYP
- Two powerful enable lines
- Power dissipation — 490mW/pkg. TYP
- Four drivers per package
- Outputs accept voltage range ±5.5V to −1.6V

INPUTS		OUTPUT CURRENT		OUTPUT VOLTAGE	
$\overline{E}$	1	$\overline{Q}$	Q	$\overline{Q}$	Q
0	0	I_0	I_1	H	L
0	1	I_1	I_0	L	H
1	X	I_0	I_0	H	H

PIN CONFIGURATION



APPLICATIONS

- Single ended bus driver — saves cost, space, wiring
- Differential mode bus driver — improved noise immunity for long lines
- Party line operation — single ended or differential mode
- ECL to MOS translator — for 5V MOS inputs
- Quad level translator

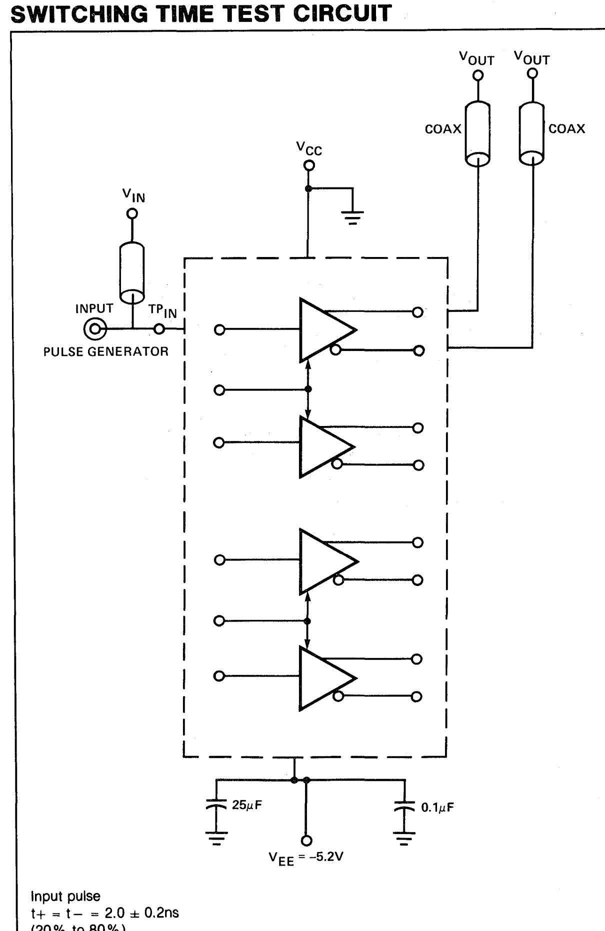
DC ELECTRICAL CHARACTERISTICS

TEST VOLTAGE VALUES — V

TEST TEMPERATURE	V_{IH} MAX	V_{IL} MIN	V_{IHA} MIN	V_{ILA} MAX	V_{EE}
−30°C	−0.890	−1.880	−1.205	−1.500	−5.2
+25°C	−0.810	−1.850	−1.105	−1.475	−5.2
+85°C	−0.700	−1.825	−1.035	−1.440	−5.2

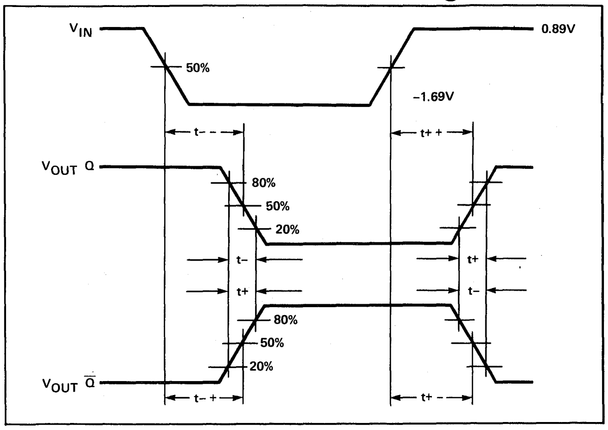
PARAMETER		TEST CONDITIONS	LIMITS +25°C MIN	TYP	MAX	UNIT
I_E	Power Supply Drain Current		76	95	118	mA
I_{IL}	Low Level Input Current	V_{IH} MAX			.5	μA
I_{IH}	High Level Input Current	V_{IL} MIN			320	μA
I_{OL}	Low Level Output Current	V_{IH} MAX	0	0	0.2	mA
I_{OH}	High Level Output Current	V_{IL} MIN	14	16	18	mA
V_{OUT}	Output Voltage		-1.6		5.5	V

SWITCHING TIME TEST CIRCUIT



10192B,F

PROPAGATION DELAY WAVEFORMS @ +25°C



NOTES:

1. Each ECL 10,000 series device has been designed to meet the DC specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Voltage levels will shift approximately 2mW with an air flow of 200 linear fpm. Outputs are terminated through a 50-ohm resistor to ground.
2. For AC tests, all input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be <¼ inch from TP_{IN} to input pin and TP_{OUT} to output pin. A 50-ohm termination to ground is located in each scope input. Unused outputs are connected to a 50-ohm resistor to ground.
3. Test procedures are shown for only one input or set of input conditions. Other inputs are tested in the same manner.
4. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.

BASIC DRIVER OPERATION

OUTPUT VOLTAGES

$V_1 = V_T$

$V_0 = V_T - R_L$ X 16mA TYP

OUTPUT STATES

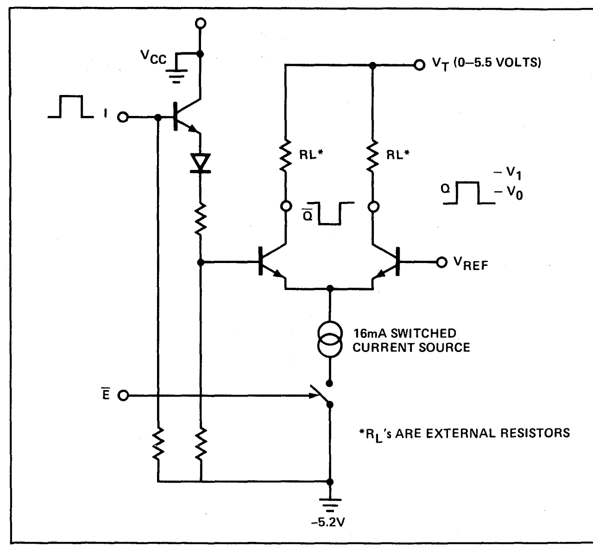
Enabled: $Q_0 = V_{IN}$, $Q_0 = V_{IN}$

Disabled: I_{OUT} = 0mA

RECOMMENDED TERMINATION VOLTAGE

Output collectors will accept voltages from +5.5V to −2.5V. Hence, V_T **should not** exceed +5.5V and RL and V_T should be chosen so that V_0 does not go more negative than −2.5V.

QUAD BUS DRIVER

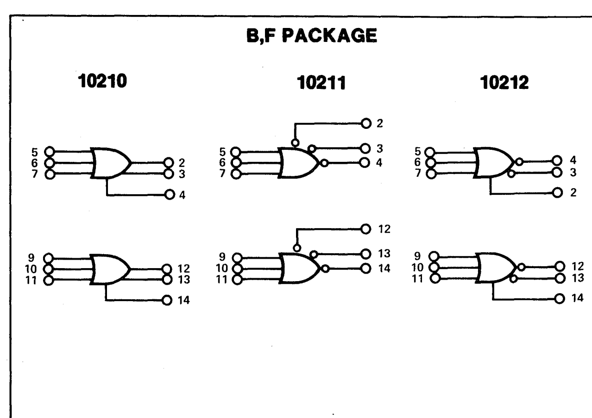


DUAL 3-INPUT 3-OUTPUT HIGH PERFORMANCE GATES 10210/10211/10212

10210-B,F • 10211-B,F • 10212-B,F

FEATURES

- **Fast propagation delay = 1.7ns TYP (all outputs loaded)**
- **Power dissipation = 150m/Wpackage TYP (no load)**
- **Very high fanout capability—can drive six 50Ω lines**
- **Internal 50kΩ pulldown resistors**
- **Open emitters for bussing and logic capability**

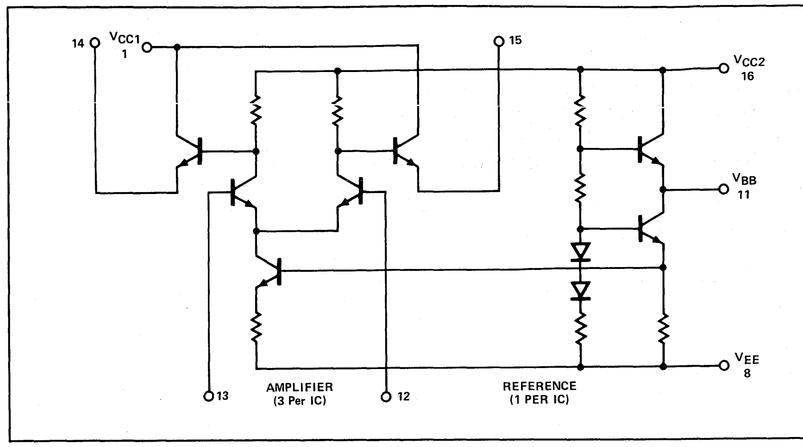


10216B,F

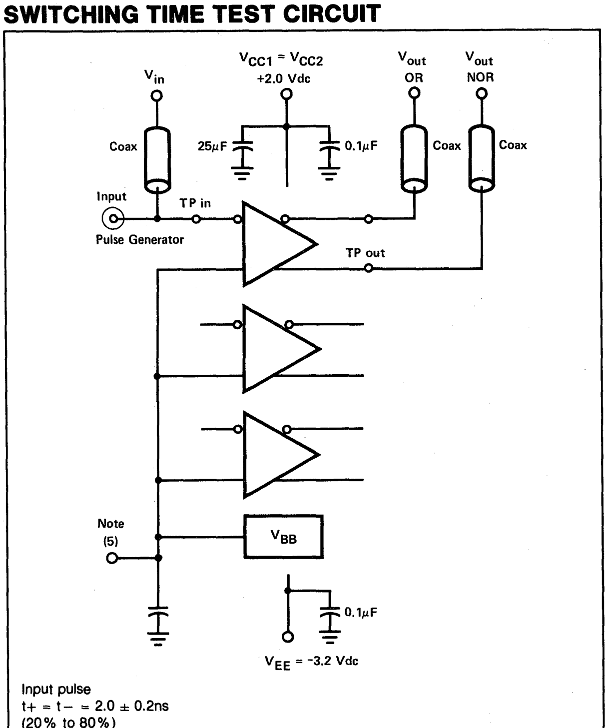
FEATURES:

- Good common mode noise rejection
- Fast propagation delay = 1.8ns TYP (single-ended) 1.5ns TYP (differential)
- Low power dissipation = 100mW/ package TYP (no load)
- High fanout capability—can drive 50Ω lines
- Very high input Z (No 50k pulldowns)
- High immunity from power supply variations (−5.2V ± 5% recommended)
- Complementary outputs
- Open emitter logic and bussing capability
- V_{BB} voltage available on pin 11
- Pin compatible with 10116

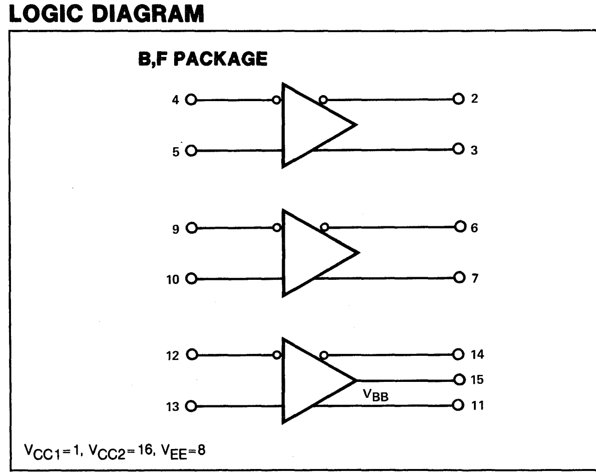
CIRCUIT SCHEMATIC



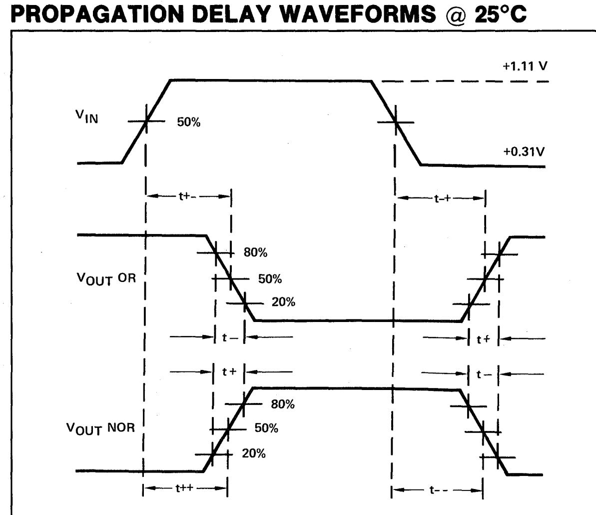
SWITCHING TIME TEST CIRCUIT



LOGIC DIAGRAM



PROPAGATION DELAY WAVEFORMS @ 25°C



NOTES:

1. Each ECL 10,000 series device has been designed to meet the DC specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Voltage levels will shift approximately 3 mV with an air flow of 200 linear fpm. Outputs are terminated through a 50-ohm resistor to 2.0 volts.
2. For AC tests, all input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be <¼ inch from TP_{in} to input pin and TP_{out} to output pin. A 50-ohm termination to ground is located in each scope input. Unused outputs are connected to a 50-ohm resistor to ground.
3. Test procedures are shown for only one input or set of input conditions. Other inputs are tested in the same manner.
4. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
5. One input from each gate must be tied to V_{BB} (Pin 11) during testing.

LOGIC

10231B,F

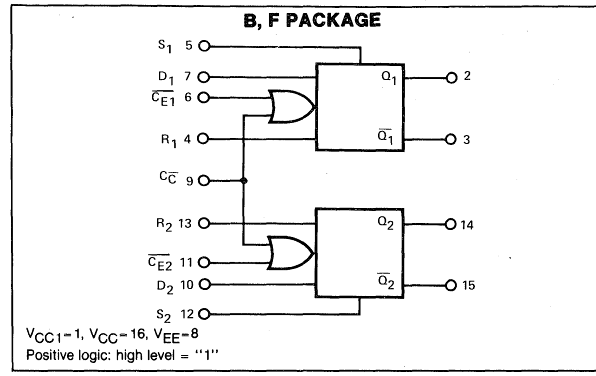
FEATURES

- f_{TOG} = 200 MHz MIN = 225 MHz TYP
- Fast propagation delay
  = 2.0 ns TYP (set, reset)
  = 2.0 ns TYP (clock)
- Low power dissipation = 270 mW/package TYP (no load)
- High fanout capability — can drive 50Ω lines
- High Z inputs — internal 50kΩ pulldowns
- High immunity from power supply variations V_{EE} = −5.2V ± 5% recommended
- Open emitter logic and bussing capability
- Pin compatible with 10130 and 10131

APPLICATIONS

- Control logic
- Status logic
- Counters
- Shift register
- Prescalers

LOGIC DIAGRAM

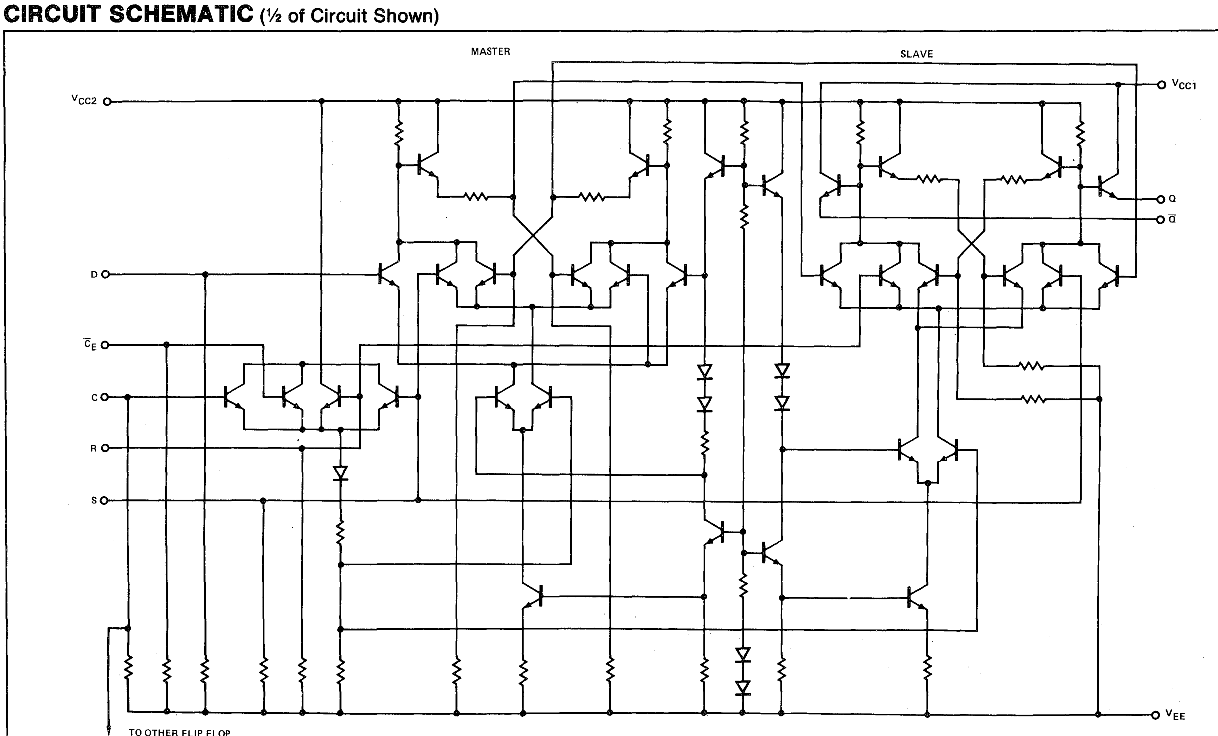


TRUTH TABLE

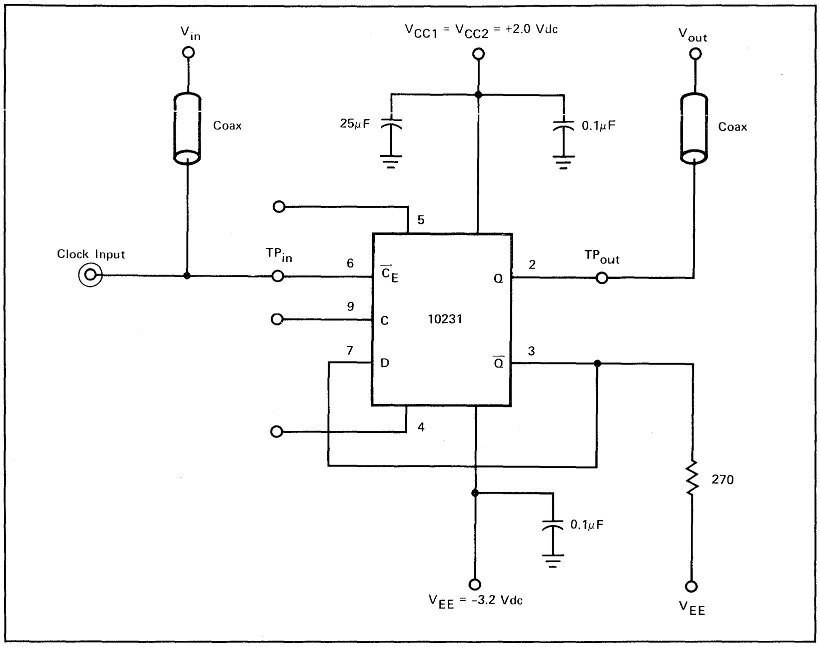
D	C*	S	R	Qn+1
ø	L	L	L	Qn
L	H	L	L	L
H	H	L	L	H
ø	*ø	H	L	H
ø	ø	L	H	L
ø	ø	H	H	N.D.

*An H represents a transition from L to H between t=n and t=n + 1
C = C_C + CE
N.D. = not defined

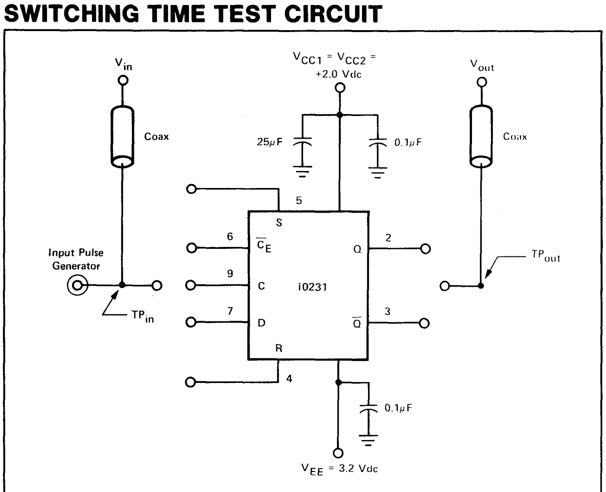
CIRCUIT SCHEMATIC (½ of Circuit Shown)



TOGGLE FREQUENCY TEST CIRCUIT



SWITCHING TIME TEST CIRCUIT

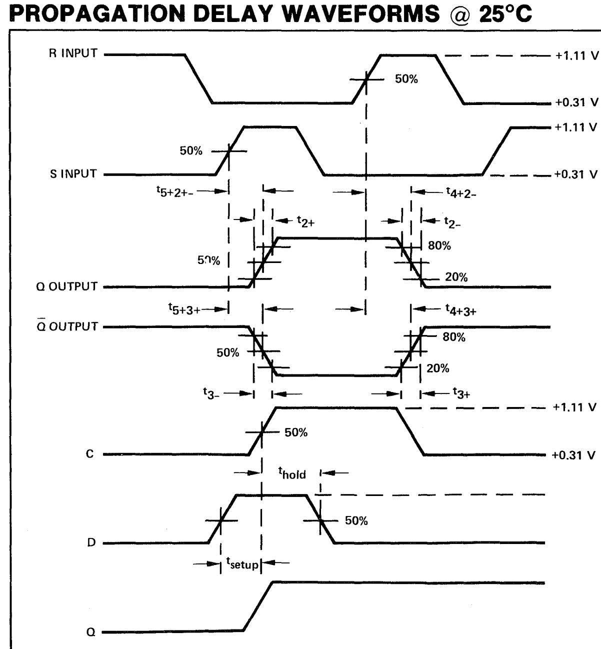


NOTE:

Setup is the minimum time before the positive transition of the clock pulse (C) that information must be present at the data input (D).

Hold is the minimum time after the positive transition of the clock pulse (C) that information must remain unchanged at the data input (D).

PROPAGATION DELAY WAVEFORMS @ 25°C



MEMORIES 2

Bipolar Memories

TABLE OF CONTENTS

RAMs

ROMs

PROMs

MEMORIES

MOS Memories

TABLE OF CONTENTS

ROMS/CHARACTER GENERATORS

MEMORIES

RAMS

Random Access Memories

A complete line of Schottky-clamped TTL, read/write memory arrays is offered. All feature open collector or tri-state output options for optimization of word expansion in bussed organizations. Memory expansion is further enhanced by full on-chip address decoding, chip enable function, and PNP input transistors which reduce input loading requirements.
All devices offer high performance read access and write cycle times making these devices ideally suited in high speed memory applications such as "caches", buffers, scratch pads, writeable control store, main store, etc.

MAXIMUM ALLOWABLE POWER DISSIPATION

MATERIAL	PACKAGE	# OF PINS	θ_{JA}[1] °C/W	P_{MAX} −mW 0+125°C	P_{MAX} −mW 0+75°C
Plastic	B	16	155	—	480
	XA	18	130	384	577
	N	24	100	500	750
	XF	28	100	500	750
Plastic[2]	BA	16	85	588	850
	XAS	18	73	685	>1000
	NA	24	75	666	1000
	XFA	28	75	666	1000
Cerdip	F	16	90	556	835
		18	90	556	835
		24	60	830	>1000
Ceramic	I	16	83	600	900
		24	50	1000	>1000
		28	50	1000	>1000

NOTES:
1. On a mounted surface, in still air.
2. Improved thermal characteristics due to built-in heat spreader.

ABSOLUTE MAXIMUM GUARANTEED RATINGS

	PARAMETER	LIMITS MIN	LIMITS MAX	UNIT
T_A	Operating Ambient Temperature			
	S82S - Military Range	−55	+125	°C
	N82S - Commercial Range	0	+75	°C
T_{STG}	Storage Temperature	−65	+150	°C
V_{IN}	Input Voltage		+5.5	Vdc
V_{OUT}	Output Voltage		+5.5	Vdc
V_{CC}	Power Supply Voltage		+7	Vdc

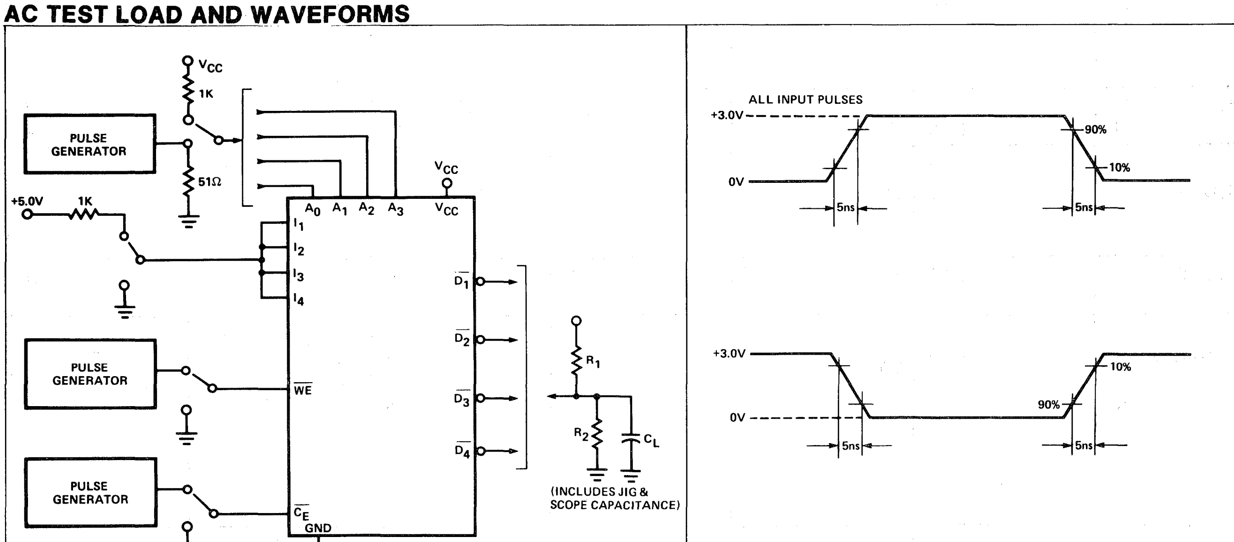
NOTES:
1. Stresses above those listed under "Maximum, Guaranteed Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device of these or any other condition above those indicated in the operation section of the device specifications is not implied.

THERMAL RATINGS

TEMPERATURE	MILITARY	COMMERCIAL
Maximum junction	175°C	150°C
Maximum ambient	125°C	75°C
Allowable thermal rise ambient to junction	50°C	75°C

MEMORIES

AC TEST LOAD AND WAVEFORMS



MEASUREMENTS: ALL CIRCUIT DELAYS ARE MEASURED AT THE +1.5V LEVEL OF INPUTS AND OUTPUT.

BIPOLAR RAMS PRODUCT INFORMATION

ELECTRICAL CHARACTERISTICS

S82S DEVICES — $-55°C \leq T_A \leq +125°C$, $4.5V \leq V_{CC} \leq 5.5$ (SEE NOTES PAGE 4)
N82S DEVICES — $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25$

PARAMETER[8]	INPUT VOLTAGE									OUTPUT VOLTAGE						INPUT CURRENT		
	V_{IL}(V) LOW LEVEL			V_{IH}(V) HIGH LEVEL			V_{IC}[1](V) CLAMP VOLTAGE			V_{OL}[2](V) LOW LEVEL			V_{OH}[6](V) HIGH LEVEL			I_{IL}(μA) LOW LEVEL		
TEST CONDITIONS	V_{CC}=MIN			V_{CC}=MAX			I_{IN}=-12 mA V_{CC}=MIN			I_{OL}=16 mA V_{CC}=MIN			I_{OUT}=-2.0 mA $\overline{CE}_1$=$\overline{CE}_2$="0" "1" STORED			V_{IN}=0.45V		
DEVICE	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
32-BIT																		
82S12 N			0.85	2.0			I_{IN}=-18 mA		-1.2	I_{OL}=9.6 mA		.45		N/A				-250
82S112			0.85	2.0			I_{IN}=-18 mA		-1.2		N/A		I_{OUT}=-3.2 mA 2.6					-250
64-BIT																		
82S21 N			0.85	2.0			I_{IN}=-18 mA		-1.2	I_{OL}=32 mA		0.45		N/A				-1.6 mA
82S25 S			0.80	2.0					-1.5		0.35	0.5		N/A			-10	-150
N			0.85								0.35	0.45					-10	-100
3101A S			0.80	2.0			I_{IN}=-18 mA		-1.2		0.35	0.5		N/A			-10	-150
N			0.85						-1.5		0.35	0.45					-10	-100
74S89 S			0.80	2.0					-1.5		0.35	0.5		N/A			-10	-150
N			0.85						-1.5		0.35	0.45					-10	-100
74S189 S			0.80	2.0			I_{IN}=-18mA		-1.2		0.35	0.5	2.4			V_{IN}=0.5V		-250
N			0.80						-1.2		0.35	0.45	2.4					-250
256-BIT																		
82S16 S			0.80	2.0					-1.5		0.35	0.5	I_{OH}=-3.2 mA 2.4				-10	-250
N			0.85								0.35	0.45	2.6				-10	-100
82S17 S			0.80	2.0					-1.5		0.35	0.5		N/A			-10	-250
N			0.85								0.35	0.45					-10	-100
82S116			0.85	2.0					-1.5		0.35	0.45	I_{OH}=-3.2 mA 2.6				-10	-100
82S117			0.85	2.0					-1.5		0.35	0.45		N/A			-10	-100
54/74S200 S			0.80	2.0			I_{IN}=-18 mA		-1.2		0.35	0.50	I_{OH}=-5.2 mA 2.4				-10	-250
N			0.85								0.35	0.45	I_{OH}=-10.3 mA 2.4				-10	-100
54/74S201 S			0.80	2.0					-1.2		0.35	0.50	I_{OH}=-5.2 mA 2.4				-10	-250
N			0.85								0.35	0.45	I_{OH}=-10.3 mA 2.4				-10	-100

BIPOLAR RAMS PRODUCT INFORMATION

ELECTRICAL CHARACTERISTICS S82S DEVICES — -55° ≤ T_A ≤ +125°C, 4.5V ≤ V_{CC}≤5.5 (SEE NOTES PAGE 4)
N82S DEVICES — 0°C ≤ T_A ≤ +75°C, 4.75V ≤ V_{CC} ≤ 5.25

PARAMETER[8]	INPUT CURRENT			OUTPUT CURRENT									SUPPLY CURRENT			CAPACITANCE					
	$I_{IH}(\mu A)$ HIGH LEVEL			$I_{OLK}^{4}(\mu A)$ LEAKAGE			$I_{O(OFF)}^{4}(\mu A)$ HI-Z STATE			$I_{OS}(mA)^{5}$ SHORT CIRCUIT			$I_{CC}^{3}(mA)$			INPUT (pF)			OUTPUT[4](pF)		
TEST CONDITIONS	V_{IN}=5.5V			V_{CC}=MAX V_{OUT}=5.5V $\overline{CE_1}$ OR $\overline{CE_2}$="1"			V_{CC}=MAX V_{OUT}=5.5V			V_{OUT}=0V V_{CC}=MAX			V_{CC}=MAX			V_{IN}=2.0V V_{CC}=5.0V			V_{CC}=5.0V V_{OUT}=2.0V		
DEVICE	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
32-BIT[7]																					
82S12 N			25			40			40		N/A			110	160		5			8	
82S112			25		N/A			N/A			N/A			N/A			N/A			N/A	
64-BIT																					
82S21			25			40		N/A			N/A				130		N/A			N/A	
					V_{CC}=MIN								NOTE 7								
82S25 S			25		<1	100		N/A			N/A			80	120		5			8	
N			10											80	105						
3101A S			25		<1	100		N/A			N/A			80	105		5			8	
N			10		<1.0	100															
					V_{OUT}=2.4V																
					<1	40								NOTE 8							
74S89 S			25		<1	100		N/A			N/A			80	120		N/A			8	
N			10		<1	100								80	105						
								V_{OUT}=2.4V													
74S189 S			25		N/A				50	-30		-100		75	110		5			8	
								V_{OUT}=.4V													
N			25						-50	-30		-100		75	110		5			8	
256-BIT																					
82S16 S								1	50					80	120						
N		1	25		N/A			1	40					80	115						
								V_{OUT}=0.45V													
								-1	-50												
								-1	-40	-20		-70					5			8	
82S17 S														80	120						
N		1	25		1	40		N/A			N/A			80	115		5			8	
82S116 N		1	25		N/A			1	40												
								V_{OUT}= 0.45V		-20		-70		80	115		5			8	
								-1	-40												
82S117 N		1	25		1	40		N/A			N/A			80	115		5			8	
		V_{IH}=2.7V																			
54/74S200 S		1	25		N/A			1	50	-30		-100		80	130		5			8	
N								1	40					T_A=+125°C	99						
								V_{IH}=2V													
N		1	25		N/A			V_{OUT}=0.4V		-30		-100		80	130		5			8	
S								-1	-50												
N								-1	-40												
		V_{IH}=2.7V																			
54/74S201 S		1	25		N/A			1	50	-30		-100		80	130		5			8	
N								1	40					T_A=+125°C	99						
								V_{IH}=2V													
N		1	25		N/A			V_{OUT}=0.4V		-30		-100		80	130		5			8	
S								-1	-50												
N								-1	-40												

ELECTRICAL CHARACTERISTICS

S82S DEVICES — $-55°C \leq T_A \leq +125°C$, $4.5V \leq V_{CC} \leq 5.5$
N82S DEVICES — $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25$

PARAMETER[8]	INPUT VOLTAGE									OUTPUT VOLTAGE						INPUT CURRENT		
	V_{IL}(V) LOW LEVEL			V_{IH}(V) HIGH LEVEL			V_{IC}[1](V) CLAMP VOLTAGE			V_{OL}[2](V) LOW LEVEL			V_{OH}[6](V) HIGH LEVEL			I_{IL}(μA) LOW LEVEL		
TEST CONDITIONS	V_{CC}=MIN			V_{CC}=MAX			I_{IN}=-12 mA V_{CC}=MIN			I_{OL}=16 mA V_{CC}=MIN			I_{OUT}=-2.0 mA $\overline{CE}_1$=$\overline{CE}_2$="0" "1" STORED			V_{IN}=0.45V		
DEVICE	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
54/74S301 S			0.80	2.0					-1.2		0.35	0.50		N/A			-10	-250
N			0.85								0.35	0.45					-10	-100
576-BIT										I_{OL}=6.4 mA								
82S09 S			0.80	2.2				-1.0	-1.5		0.35	0.50		N/A			-10	-150
N			0.85	2.0							0.35	0.5					-10	-100
1024-BIT[9]																		
82S10 S			0.80	2.1				-1.0	-1.5		0.35	0.50		N/A			-10	-150
N			0.85								0.35	0.45					-10	-100
82S11 S			0.80	2.1				-1.0	-1.5		0.35	0.50	2.4				-10	-150
N			0.85								0.35	0.45					-10	-100
93415A N			0.85	2.1				-1.0	-1.5		0.35	0.45					-10	-100
93425A N			0.85	2.1				-1.0	-1.5		0.35	0.45	2.4				-10	-100

NOTES:

1. Test each input one at the time.
2. Measured with the logic "0" stored. Output sink current is supplied through a resistor to V_{CC}.
3. I_{CC} is measured with the write enable and chip enable inputs grounded; all other inputs at 4.5V, and the outputs open.
4. Measured with V_{IH} applied to $\overline{CE}$.
5. Duration of the short circuit should not exceed one second.
6. Measured with $\overline{CE}_{(s)}$ = OV_1 and output(s) at logic "1".
7. $10°C \leq T_A \leq 75°C$
8. All voltage values are with respect to ground terminal.
9. The Operating Ambient Temperature Ranges are guaranteed with transverse air flow exceeding 400 linear feet per minute and a two minute warm-up. Typical thermal resistance values of the package at maximum temperature are:
   - θ_{JA} Junction to Ambient at 400 fpm air flow — 50°C/Watt
   - θ_{JA} Junction to Ambient — still air — 90°C/Watt
   - θ_{JA} Junction to Case — 20°C/Watt

BIPOPLAR RAMS PRODUCT INFORMATION

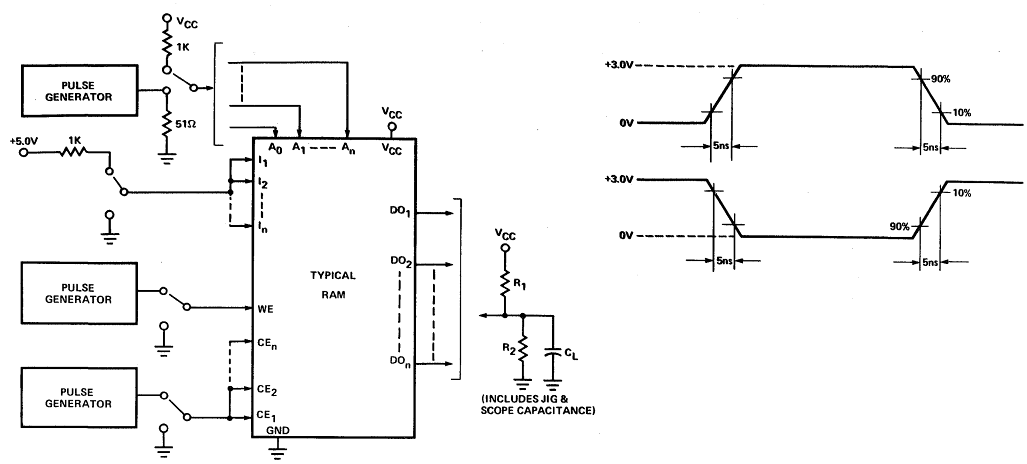
ELECTRICAL CHARACTERISTICS S82S DEVICES — $-55° \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5$
N82S DEVICES — $0°C \le T_A \le +75°C$, $4.75V \le V_{CC} \le 5.25$

PARAMETER[8]		INPUT CURRENT $I_{IH}(\mu A)$ HIGH LEVEL			OUTPUT CURRENT I_{OLK}[4](μA) LEAKAGE			OUTPUT CURRENT $I_{O(OFF)}$[4](μA) HI-Z STATE		
TEST CONDITIONS		$V_{IN}=5.5V$			$V_{CC}=MAX$, $V_{OUT}=5.5V$, $\overline{CE}_1$ OR $\overline{CE}_2$="1"			$V_{CC}=MAX$, $V_{OUT}=5.5V$		
DEVICE		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
		$V_{IH}=2.7V$								
54/74S301	S		1	25		1	50	N/A		
	N					1	40			
	N		1	25	$V_{CC}=MIN$, $V_{OUT}=2.4V$			N/A		
	S					1	50			
	N					1	40			
576-BIT										
82S09	S		1	40		1	60	N/A		
	N		1	25		1	40			
1024-BIT[9]										
82S10	S		1	40		1	60	N/A		
	N		1	25		1	40			
82S11	S		1	40	N/A				1	100
	N		1	25					1	60
								$V_{OUT}=0.45V$		
									-1	-100
									-1	-60
93415A	N		1	25		1	40	N/A		
93425A	N		1	25	N/A				1	60
								$V_{OUT}=0.45V$		
									-1	-60

PARAMETER[8]		OUTPUT CURRENT $I_{OS}(mA)$[5] SHORT CIRCUIT			SUPPLY CURRENT I_{CC}[3](mA)			CAPACITANCE INPUT(pF)			CAPACITANCE OUTPUT[4](pF)		
TEST CONDITIONS		$V_{OUT}=0V$, $V_{CC}=MAX$			$V_{CC}=MAX$			$V_{IN}=2.0V$, $V_{CC}=5.0V$			$V_{CC}=5.0V$, $V_{OUT}=2.0V$		
DEVICE		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
54/74S301	S	N/A				80	130		5			8	
	N												
					$T_A=+125°C$		99						
	N	N/A				80	130		5			8	
	S												
	N												
576-BIT													
82S09	S	N/A				150	200		5			8	
	N					150	190						
1024-BIT[9]													
82S10	S	N/A											
	N												
82S11	S	-20		-100					4			7	
	N												
									4			7	
93415A	N	N/A				120	155		4			7	
					$T_A \ge 25°C$								
						95	130						
					$T_A \le 0°C$								
							170						
93425A	N	-20		-100		120	155		4			7	
					$T_A \ge 25°C$								
						95	130						
					$T_A \le 0°C$								
							170						

MEMORIES

AC TEST FIGURE (UNLESS OTHERWISE SPECIFIED)



MEMORY TIMING DEFINITIONS

- T_{CE} Delay between beginning of CHIP ENABLE low (with ADDRESS valid) and when DATA OUTPUT becomes valid.
- T_{SE} Delay between beginning of OUTPUT SELECT low (with ADDRESS valid) and when DATA OUTPUT becomes valid.
- T_{CD} Delay between when CHIP ENABLE becomes high and DATA OUTPUT is in off state.
- T_{SD} Delay between when OUTPUT SELECT becomes high and DATA OUTPUT is in off state (Hi-Z or "1").
- T_{AA} Delay between beginning of valid ADDRESS (with CHIP ENABLE low) and when DATA OUTPUT becomes valid.
- T_{WSC} Required delay between beginning of valid CHIP ENABLE and beginning of WRITE ENABLE pulse.
- T_{WHC} Required delay between end of WRITE ENABLE pulse and end of CHIP ENABLE.
- T_{WSA} Required delay between beginning of valid ADDRESS and beginning of WRITE ENABLE pulse.
- T_{WHA} Required delay between end of WRITE ENABLE pulse and end of valid ADDRESS.
- T_{WSD} Required delay between beginning of valid DATA INPUT and end of WRITE ENABLE pulse.
- T_{WHD} Required delay between end of WRITE ENABLE pulse and end of valid INPUT DATA.
- T_{WP} Width of WRITE ENABLE pulse.
- T_{WD} TRANSPARENT OUTPUT
  Delay between beginning of WRITE ENABLE pulse and when DATA OUTPUT reflects the contents of the DATA INPUT.
  NON-TRANSPARENT OUTPUT
  Delay between beginning of WRITE ENABLE pulse and when DATA OUTPUT is in off state (Hi-Z or "1").
- T_{WR} Delay between end of WRITE ENABLE pulse and when DATA OUTPUT becomes valid. (Assuming ADDRESS still valid - not as shown.)
- T_{CDS} Minimum delay between leading edge of CHIP ENABLE and trailing edge of STROBE, for latching valid output data.
- T_{CDH} Required delay between trailing edge of STROBE and end of CHIP ENABLE, for latching valid output data.
- T_{SL} Minimum delay between ADDRESS valid time and trailing edge of STROBE, for latching valid output data.
- T_{SW} Minimum width of STROBE pulse required to update contents of output data latches.
- T_{ADH} Required delay between trailing edge of STROBE and end of valid ADDRESS.
- T_{DL} Delay between leading edge of STROBE and when output data latches are released.
- T_{LRW} Minimum delay required between trailing edge of STROBE and leading edges of WRITE ENABLE or WRITE SELECT for latching old output data (being read) while new data is being written (at the same address).
- T_{WSL} Minimum delay between leading edge of WRITE ENABLE or WRITE SELECT and trailing edge of STROBE for latching data being written in output data latches.

82S12 - N · 82S112 - N

DESCRIPTION

The 82S 12/112 is a Schottky TTL 32-bit multiport memory organized as 8 words of 4 bits each.

Data is stored in a single storage matrix which is addressed via two independent sets of address inputs, designated respectively as Port A and Port B.

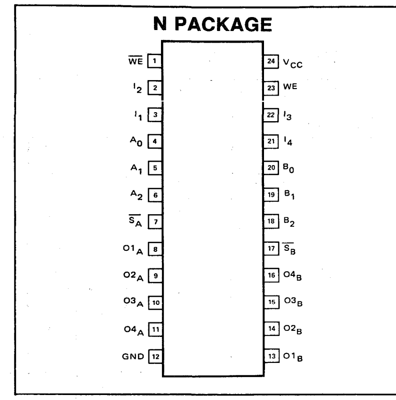
Data can be read from memory via either Port A or B, through their respective output sets. However, input data (latched on the leading edge of write enable in the input data latches) is written only in memory locations specified by the address on Port A, regardless of Port B.

When both Port addresses are equal, data from the same location can be read in either or both Port output sets by means of output select lines S_A and S_B; also, during Write, new data stored in memory is immediately transferred on both Port output sets.

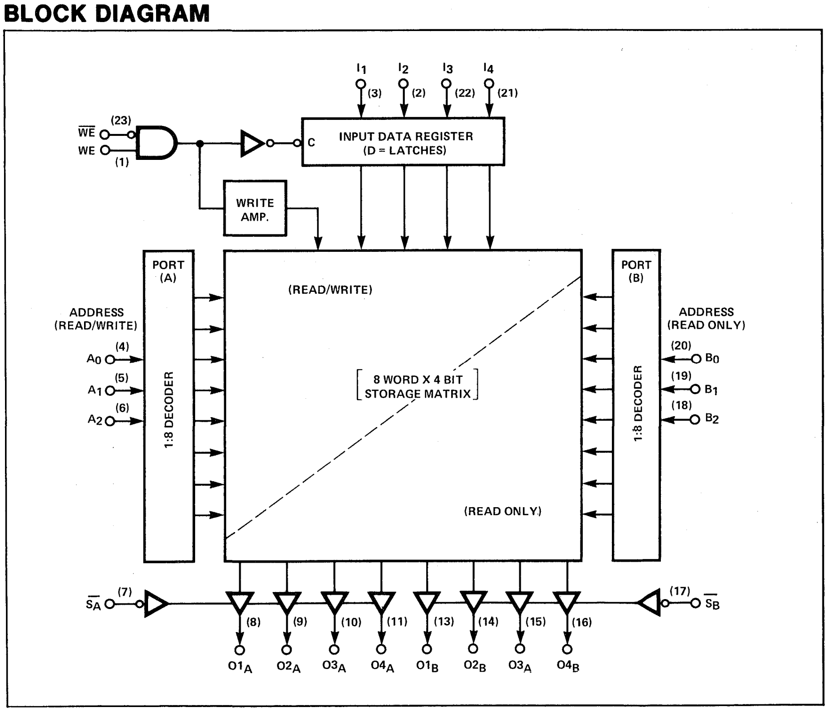
When both Port addresses are different, two different locations can be simultaneously read from memory; also it is possible to simultaneously read through Port B while writing new input data through Port A by utilizing the "A_N" address to specify the location of the word to be written, and the "B_N" address to specify the word to be read.

Both devices are ideally suited for high speed accumulator and buffer memories, and can be readily expanded to form larger arrays by means of their output select and write enable lines.

PIN CONFIGURATION



BLOCK DIAGRAM



TRUTH TABLE

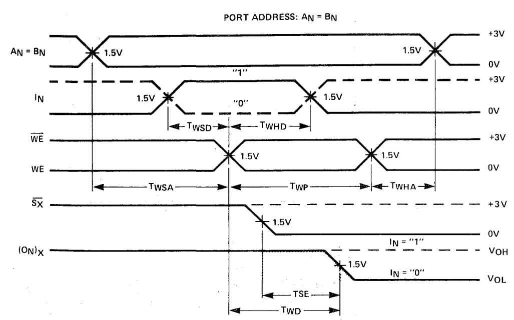
MODE	WE	$\overline{WE}$	I_N	$\overline{S}_A$	$\overline{S}_B$	PORT ADDRESS	82S12 $(O_N)A$	82S12 $(O_N)B$	82S112 $(O_N)A$	82S112 $(O_N)B$
Disabled				1	1	X	1	1	Hi-Z	Hi-Z
Read	0	X	X	0	1	A=B	Stored Data	1	Stored Data	Hi-Z
	or			1	0		1	Stored Data	Hi-Z	Stored Data
				0	0		Stored Data	Stored Data	Stored Data	Stored Data
	X	1		0	1	A≠B	$[A_N]$	1	$[A_N]$	Hi-Z
				1	0		1	$[B_N]$	Hi-Z	$[B_N]$
				0	0		$[A_N]$	$[B_N]$	$[A_N]$	$[B_N]$
Write	1	0	1/0	1	1	A=B	1	1	Hi-Z	Hi-Z
				0	1		I_N	1	I_n	Hi-Z
				1	0		1	I_N	Hi-Z	I_N
				0	0		I_N	I_N	I_N	I_N
				1	1	A≠B	1	1	Hi-Z	Hi-Z
				0	1		I_N	1	I_N	Hi-Z
				1	0		1	$[B_N]$	Hi-Z	$[B_N]$
				0	0		I_N	$[B_N]$	I_N	$[B_N]$

X = Don't care
[ ] = Contents of

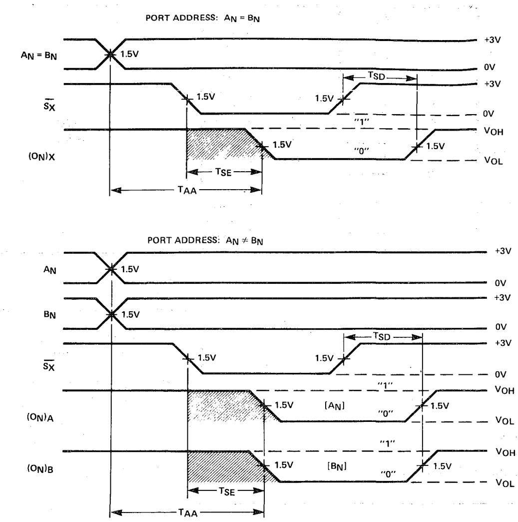
AC ELECTRICAL CHARACTERISTICS 0°C≤TA ≤75°C; −4.75 V ≤VCC ≤5.25 V.

PARAMETER		TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Power Consumption		Outputs Enabled		110/550	160/840	mA/mW
Write Pulse Width	T1	TA = 25°C Only		15	30	ns
	T1	10°C ≤TA ≤75°C	45			ns
Address Set Up Time	T2			10		ns
Address Hold Time	T3			0		ns
Data Input Hold Time	T4			15		ns
Write Access Time	T5			30		ns
Data Input Set Up Time	T6			5		ns
Output Enable Time	T7			10	30	ns
Output Disable Time	T8			10	30	ns
Address Access Time	T9			20	40	ns

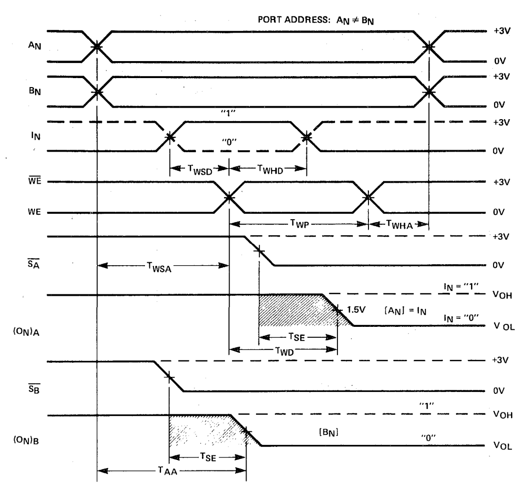
AC WAVEFORMS



WRITE CYCLE (PORT A ONLY)



READ CYCLE

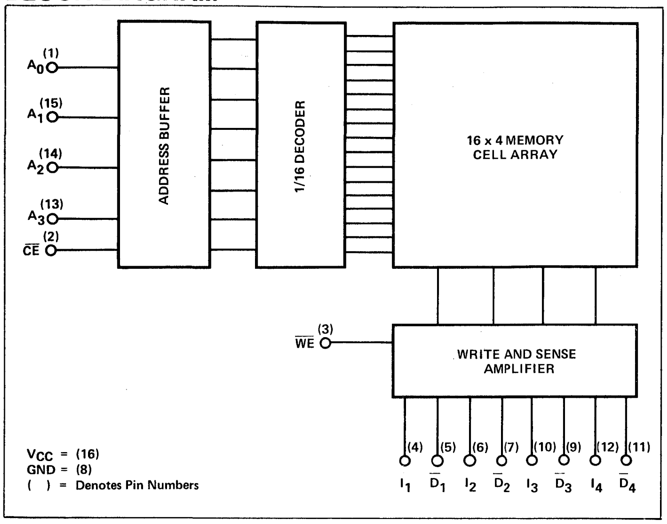


SIMULTANEOUS READ-WRITE CYCLE
(PORT A - WRITE: PORT B - READ)

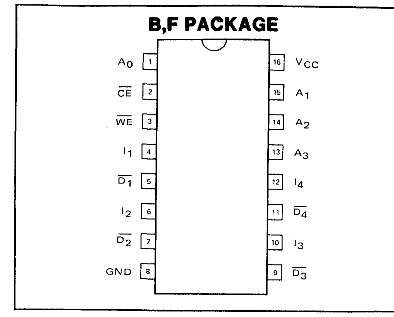
MEMORIES

N82S25-B,F • S82S25-F • N3101A-B,F • S3101A-F

BLOCK DIAGRAM



PIN CONFIGURATION



TRUTH TABLE

MODE	$\overline{CE}$	$\overline{WE}$	In	$\overline{Dn}$
Read	0	1	X	Stored $\overline{DATA}$
Write "0"	0	0	0	1
Write "1"	0	0	1	1
Disabled	1	X	X	1

X = Don't care.

AC ELECTRICAL CHARACTERISTICS

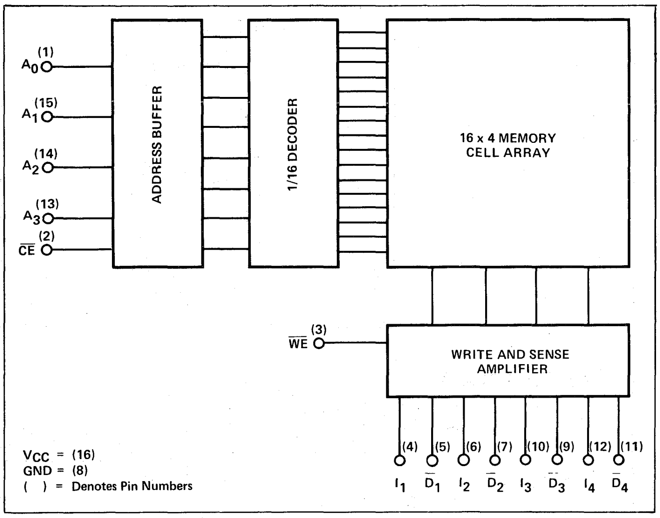
S82S25/S3101A $-55°C \leq T_A \leq +125°C$, $4.5V \leq V_{CC} \leq 5.5V$
N82S25/N3101A $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

PARAMETER		TEST CONDITIONS	S82S25/S3101A MIN	S82S25/S3101A TYP[8]	S82S25/S3101A MAX	N82S25/N3101A MIN	N82S25/N3101A TYP[8]	N82S25/N3101A MAX	UNIT
Propagation Delays									
T_{AA}[1]				25	50		30	35	
T_{AA}[2]	Address Access Time			35	60		35	50	ns
T_{CE}	Chip Enable Access Time			20	35		20	35	ns
T_{CD}	Chip Enable Output Disable Time			20	35		20	35	ns
T_{WD}	Write Enable to Output Disable Time			20	30		20	25	ns
T_{WR}	Write Recovery Time			35	60		35	50	ns
Write Set-up Times		$R_1 = 270\Omega$							
		$R_2 = 600\Omega$							
T_{WSA}	Address to Write Enable	$C_L = 30pF$	10	−8		5	−8		ns
T_{WSD}	Data In to Write Enable		25	5		20	5		ns
T_{WSC}	$\overline{CE}$ to Write Enable		0	−5		0	−5		ns
Write Hold Times									
T_{WHA}	Address to Write Enable		5	0		5	0		ns
T_{WHD}	Data In to Write Enable		5	−3		5	−3		ns
T_{WHC}	$\overline{CE}$ to Write Enable		5	0		5	0		ns
T_{WP}	Write Enable Pulse Width (Note 7)		30	18		30	18		ns

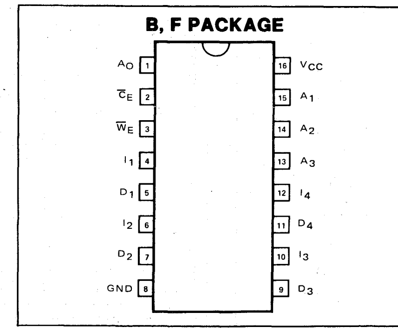
NOTES:
1-3101A Only
2-82S25 Only

64-BIT BIPOLAR SCRATCH PAD MEMORY (16x4 RAM) 74S89

74S89-B,F · 54S89-F



PIN CONFIGURATION



TRUTH TABLE

MODE	$\overline{CE}$	$\overline{WE}$	I_n	$\overline{D_n}$
Read	0	1	X	Stored $\overline{DATA}$
Write "0"	0	0	0	1
Write "1"	0	0	1	0
Disable	1	X	X	1

AC ELECTRICAL CHARACTERISTICS

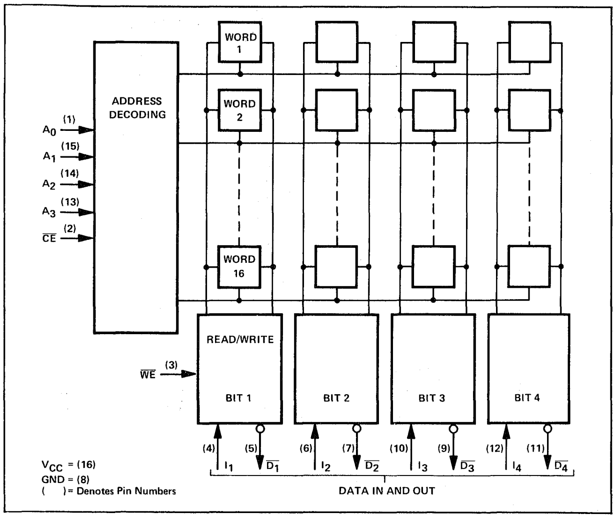
S74S89 $-55°C \leq T_A \leq +125°C$, $4.5V \leq V_{CC} \leq 5.5V$
N74S89 0°C $\leq T_A \leq +75°C$, 4.75°C, $4.75V \leq V_{CC} \leq 5.25V$

PARAMETER		TEST CONDITIONS	S54S189			N74S189			UNIT
			MIN	TYP[8]	MAX	MIN	TYP[8]	MAX	
Propagation Delays									
T_{AA}	Address Access Time			35	60		35	50	ns
T_{CE}	Chip Enable Access Time			20	35		20	35	ns
T_{CD}	Chip Enable Output Disable Time			20	35		20	35	ns
T_{WR}	Write Recovery Time			35	60		35	50	ns
Write Set-up Times		$R_1 = 270\Omega$							
T_{WSA}	Address to Write Enable	$R_2 = 600\Omega$	10	−8		0	−8		ns
T_{WSD}	Data In to Write Enable	$C_L = 30pF$	25	5		25	5		ns
T_{WSC}	$\overline{CE}$ to Write Enable		0	−5		0	−5		ns
Write Hold Times									
T_{WHA}	Address to Write Enable		10	0		5	0		ns
T_{WHD}	Data In to Write Enable		10	−3		5	−3		ns
T_{WHC}	$\overline{CE}$ to Write Enable		5	0		5	0		ns
T_{WP}	Write Enable Pulse Width (Note 7)		30	18		30	18		ns

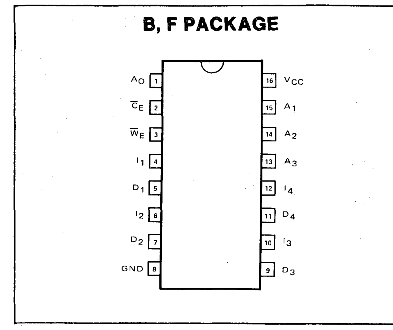
MEMORIES

74S189-B,F · 54S89-F

BLOCK DIAGRAM



PIN CONFIGURATION



TRUTH TABLE

MODE	$\overline{CE}$	$\overline{WE}$	I_n	$\overline{D}n$
Read	0	1	X	Stored $\overline{DATA}$
Write "0"	0	0	0	HI-Z
Write "1"	0	0	1	HI-Z
Disabled	1	X	X	HI-Z

X = Don't care.

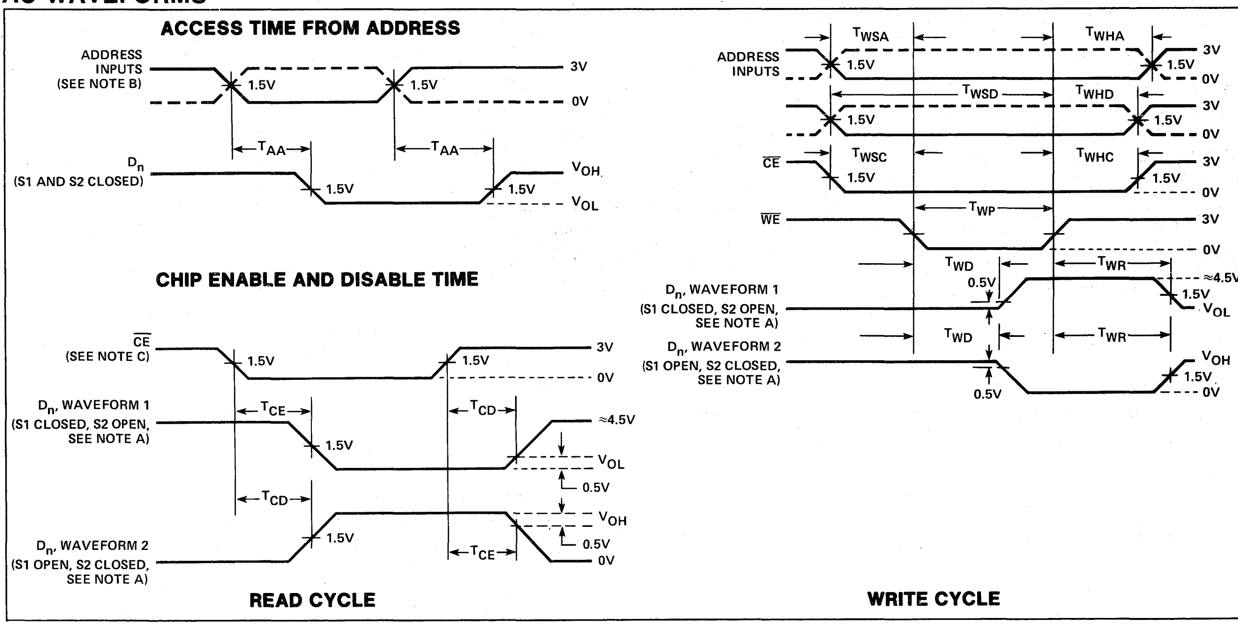
AC ELECTRICAL CHARACTERISTICS

54S189 $-55°C \leq T_A \leq +125°C$, $4.5V \leq V_{CC} \leq 5.5V$
N74S189 $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

PARAMETER		TEST CONDITIONS	S54S189			N74S189			UNIT
			MIN	TYP [1]	MAX	MIN	TYP [1]	MAX	
Propagation Delays									
T_{AA}	Address Access Time	$R_L = 300\Omega$ $C_L = 30pF$		25	50		25	35	ns
T_{CE}	Chip Enable Access Time			12	25		12	17	ns
T_{CD}	Chip Enable Output Disable Time	$R_L = 300\Omega$ $C_L = 5pF$		12	25		12	17	ns
T_{WD}	Write Enable to Output Disable Time			12			12		ns
T_{WR}	Write Recovery Time	$R_L = 300\Omega$ $C_L = 30pF$		22	40		22	35	ns
Write Set-up Times									
T_{WSA}	Address to Write Enable		0			0			ns
T_{WSD}	Data In to Write Enable		25			25			ns
T_{WSC}	$\overline{CE}$ to Write Enable		0			0			ns
Write Hold Times									
T_{WHA}	Address to Write Enable		7			0			ns
T_{WHD}	Data In to Write Enable		5			0			ns
T_{WHC}	$\overline{CE}$ to Write Enable		0			0			ns
T_{WP}	Write Enable Pulse Width (Note 2)		25			25			ns

NOTES:
1. Typical values are at $V_{CC} = +5.0V$, and $T_A = 25°C$.
2. Minimum required to guarantee a WRITE into the slowest bit.

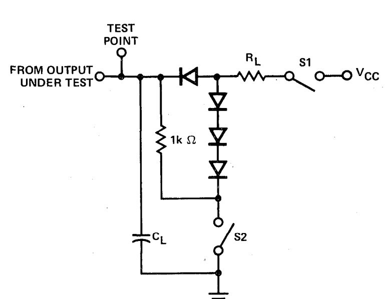
AC WAVEFORMS



NOTES:

A. Waveform 1 is for the output with internal conditions such that the output is low except when disabled. Waveform 2 is for the output with internal conditions such that the output is high except when disabled.
B. When measuring delay times from address inputs, the chip enable inputs are low and the write enable input is high.
C. When measuring delay times from chip enable inputs, the address inputs are steady-state and the write enable input is high.
D. Input waveforms are supplied by pulse generators having the following characteristics: $t_r \leq 2.5ns$, $t_f \leq 2.5ns$, PRR ≤ 1MHz, and $Z_{out} \approx 50\Omega$.
E. t_{PLH} propagation delay time, low-to-high-level output, t_{PHL} propagation delay time, high-to-low-level output.
F. t_{ZH} propagation delay time, hi-Z to high-level output, t_{ZL} propagation delay time, hi-Z to low-level output.
G. t_{HZ} propagation delay time, high-level to hi-Z output, t_{LZ} propagation delay time, low-level to hi-Z output.
H. Minimum required to guarantee a WRITE into the slowest bit.

AC TEST LOAD



C_L INCLUDES PROBE AND JIG CAPACITANCE.
ALL DIODES ARE 1N3064.
ALL RESISTORS VALUES ARE TYPICAL AND IN OHMS.

MEMORIES

N82S21-B,F • S82S21-F

DESCRIPTION

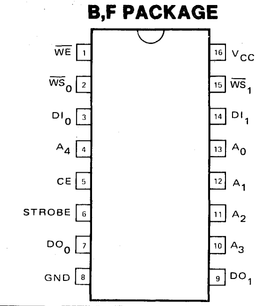
The 82S21 is a TTL 64-bit Write-While-Read Random Access Memory organized as 32 words of 2 bits each. The 82S21 is ideally suited for high speed buffers and as the memory element in high speed accumulators.

Words are selected through a 5-input decoder when the CHIP enable input CE is at logic "1". $\overline{WS_0}$ and $\overline{WS_1}$ are the write select inputs for bit 0 and bit 1 of the word selected. $\overline{TOE}$ is the write enable input. When $\overline{WS_N}$ and $\overline{WE}$ are both at logic "0" data on the DI_0 and DI_1 data lines are written into the addressed word. The read function is enabled when either $\overline{WS_n}$ or $\overline{WE}$ is at logic "1".

An internal latch is on the chip to provide the Write-While-Read capability. When the latch control line, Strobe, is logic "1" and data is being read from the 82S21, the latch is effectively bypassed. The data at the output will be that of the addressed word. When Strobe goes from a logic "1" to logic "0" the outputs are latched and will remain latched regardless of the state of any other address or control line. When Strobe goes from "0" to "1" the outputs unlatch and the outputs will be that of the present address word.

PIN CONFIGURATION

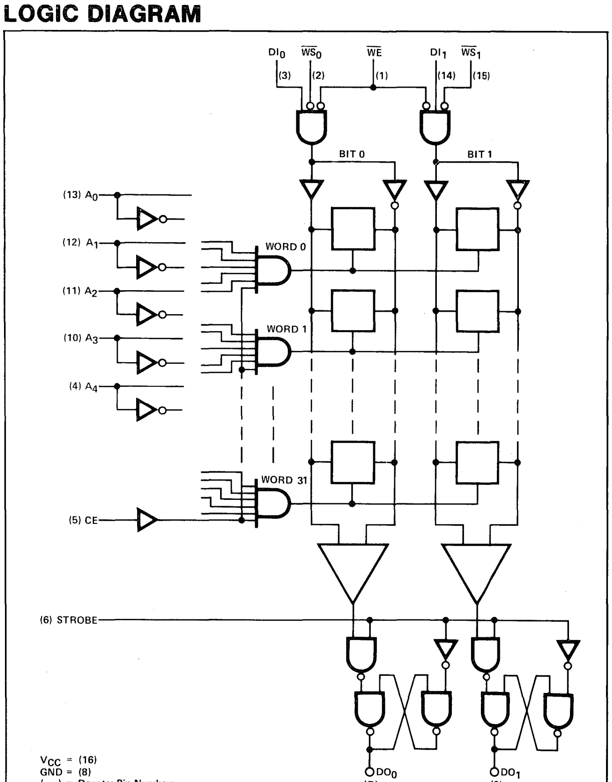
B,F PACKAGE



TRUTH TABLE

CE	$\overline{WE}$	$\overline{WS_0}$	$\overline{WS_1}$	STROBE	MODE	OUTPUTS
X	X	X	X	0	Output Hold	Data from last addressed word when CE = "1"
0	X	X	X	0	Disabled	Logic "1"
1	1	X	X	1 or ↓	Read (transparent/latched)	Data stored in addressed word
1	0	1	1	1 or ↓	Read (transparent/latched)	Data stored in addressed word
1	0	0	0	0	Write Data	Data from last word address when Strobe went from "1" to "0"
1	0	0	0	1	Write Data	Data being written into memory
1	0	0	1	X	Write Data into Bit 0 Only	If Strobe = 0: Data from last word address when Strobe went from "1" to "0"
1	0	1	0	X	Write Data into Bit 1 Only	If Strobe = 1: Data being written into the selected bit, or stored in the addressed location.

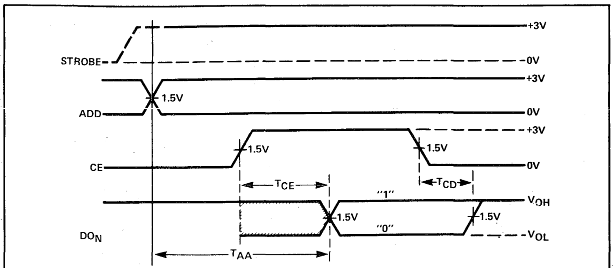
LOGIC DIAGRAM



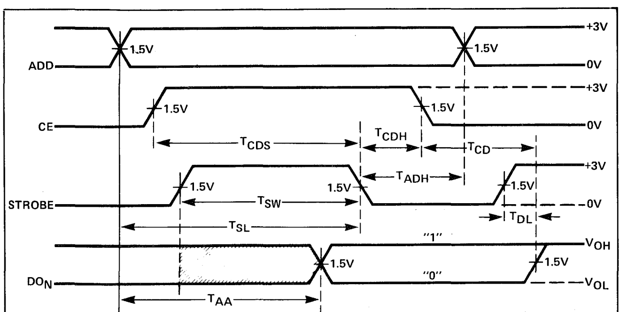
AC ELECTRICAL CHARACTERISTICS $0 \leq T_A \leq 75°C$, $4.75 \leq V_{CC} \leq 5.25V$

PARAMETER		LIMITS MIN	TYP	MAX	UNITS
Read Access Time Address to Output	t_1		25	50	ns
Address Set-Up Time	t_2		8	15	ns
Data Set-Up Time	t_3		15	20	ns
Address Hold Time	t_4			0	ns
Control or Write Pulse Width	t_5		15	20	ns
Write Access Time	t_6		20	25	ns
Address to Latch Set-Up Time	t_7		25	50	ns
Latch Address to Address Hold Time	t_8		7	10	ns
Delatch Access Time	t_9		15	25	ns
Data Hold Time	t_{10}		0	5	ns

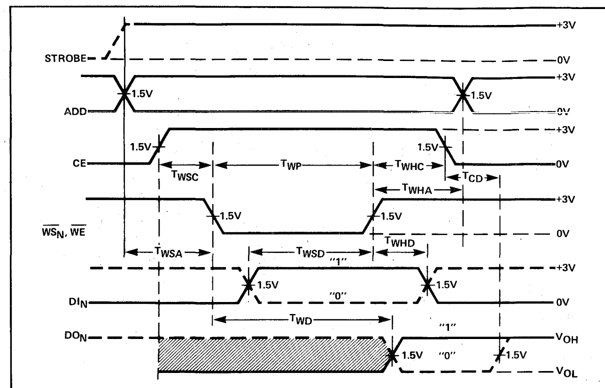
AC WAVEFORMS



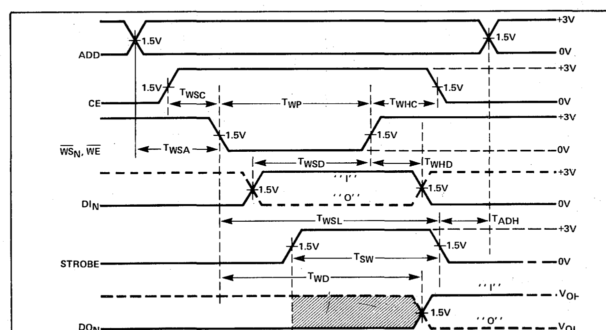
TRANSPARENT READ (OUTPUT LATCHES NOT USED)



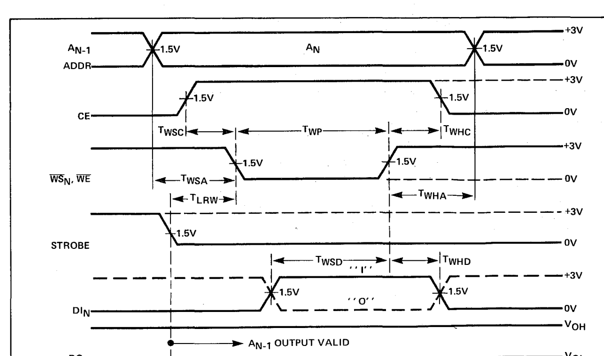
LATCHED READ (OUTPUT LATCHES USED)



TRANSPARENT WRITE (OUTPUT LATCHES NOT USED)



LATCHED WRITE (OUTPUT LATCHES USED)

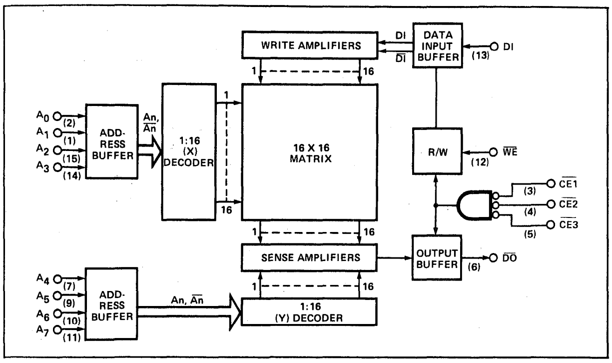


READ WHILE WRITE

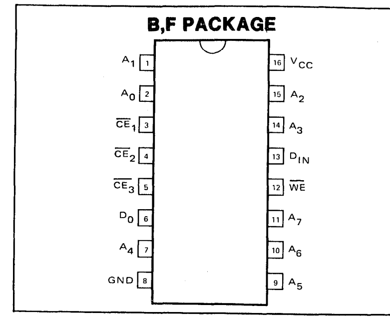
MEMORIES

N82S16 • 117 • 116 • 117-B,F • S82S16 • 17 • 116 • 117-F

BLOCK DIAGRAM



PIN CONFIGURATION



TRUTH TABLE

MODE	$\overline{CE}$*	$\overline{WE}$	D_{IN}	$\overline{D_{OUT}}$ 82S16/116	$\overline{D_{OUT}}$ 82S17/117
READ	0	1	X	STORED $\overline{\text{DATA}}$	STORED $\overline{\text{DATA}}$
WRITE "0"	0	0	0	1	1
WRITE "1'	0	0	1	0	0
DISABLED	1	X	X	High-Z	1

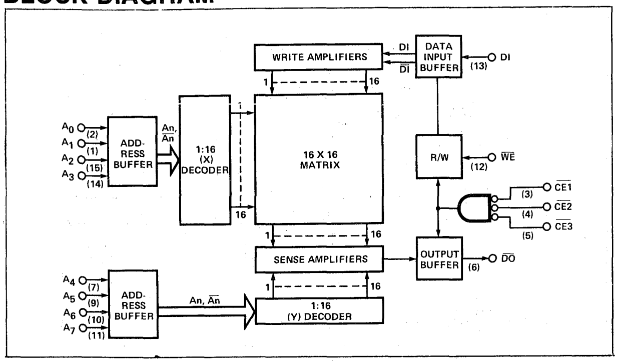
*"0" = All $\overline{CE}$ inputs low; "1" = one or more $\overline{CE}$ inputs high.
X = Don't care.

AC ELECTRICAL CHARACTERISTICS $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

PARAMETER		TEST CONDITIONS	LIMITS MIN	TYP[1]	MAX	UNIT
Propagation Delays						
T_{AA}	Address Access Time	$R_1 = 270\Omega$		30	40	ns
T_{CE}	Chip Enable Access Time	$R_2 = 600\Omega$		15	25	ns
T_{CD}	Chip Enable Output Disable Time	$C_L = 30pF$		15	25	ns
T_{WD}	Write Enable to Output Disable Time			30	40	ns
Write Set-up Times						
T_{WSA}	Address to Write Enable		0	−5		ns
T_{WSD}	Data In to Write Enable		25	15		ns
T_{WSC}	$\overline{CE}$ to Write Enable		0	−5		ns
Write Hold Times						
T_{WHA}	Address to Write Enable		0	−5		ns
T_{WHD}	Data In to Write Enable		0	−5		ns
T_{WHC}	$\overline{CE}$ to Write Enable		0	−5		ns
T_{WP}	Write Enable Pulse Width		25	15		ns

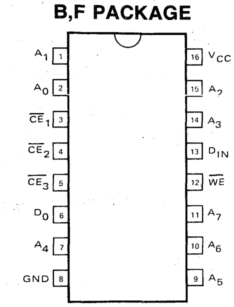
54S200 • 201 • 301-F • 74S200 • 201 • 301-B,F

BLOCK DIAGRAM



PIN CONFIGURATION

B,F PACKAGE



TRUTH TABLE

MODE	$\overline{CE}$*	$\overline{WE}$	DIN	$\overline{D}_{OUT}$ 54/74S301	$\overline{D}_{OUT}$ 54/74S200/201
READ	0	1	X	STORED DATA	STORED DATA
WRITE "0"	0	0	0	1	High-Z
WRITE "1"	0	0	1	1	High-Z
DISABLED	1	X	X	1	High-Z

*"0" = All $\overline{CE}$ inputs low; "1;; = One or more $\overline{CE}$ inputs high.
X = Don't care.

NOTES:
1. All typical values are V_{CC} = 5V, T_A = 25°C.
2. When measuring delay times from address inputs, the chip enable inputs are low and the write enable input is high.
3. When measuring delay times from chip enable inputs, the address inputs are steady-state and the write enable input is high.
4. Input waveforms are supplied by pulse generators having the following characteristics: $t_r \leq$ 2.5ns, $t_f \leq$ 2.5ns, PRR $\leq$ 1MHz, and $Z_{out} \approx 50\Omega$.
5. t_{PLH} propagation delay time, low-to-high-to-low-level output.
6. t_{ZH} propagation delay time, Hi-Z to high-level output, t_{ZL} propagation delay time, Hi-Z to low-level output.
7. t_{HZ} propagation delay time, high-level to Hi-Z output, t_{LZ} propagation delay time, low-level to Hi-Z output.
8. Minimum required to guarantee a WRITE into the slowest bit.

AC ELECTRICAL CHARACTERISTICS

S54S200/201/301 −55°C ≤ T_A ≤ +125°C, 4.5V ≤V_{CC} ≤5.5V
N74S200/201/301 0°C ≤T_A ≤ +70°C, 4.75V ≤V_{CC} ≤5.25V

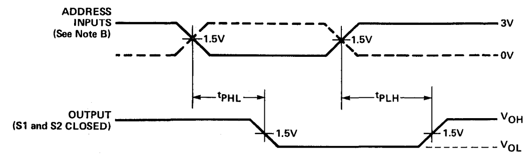
PARAMETER		TEST CONDITIONS		S54S200/201			N74S200/201			S54S301			N74S301			UNIT
				MIN	TYP[1]	MAX	MIN	TYP[1]	MAX	MIN	TYP[1]	MAX	MIN	TYP[1]	MAX	
t_{PLH}	Access Time From Address [2, 4, 5]	R_L = 270Ω C_L = 15pF	R_L = 270Ω C_L = 15pF		40	70		40	50		40	70		40	50	ns
t_{PHL}					40	70		40	50		40	70		40	50	ns
t_{ZH}	Enable Time From Chip Enable [3, 4, 5]					45[6]			35[6]			45			35	ns
t_{ZL}						45			35							
t_{HZ}	Disable Time From Chip Enable [3, 4, 5]	R_L = 270Ω C_L = 5pF	R_L = 270Ω C_L = 5pF			30[6]			20[6]			30			20	ns
t_{LZ}						30			20							
t_{HZ}	Disable Time From Write Enable					40			30			40			30	ns
t_{LZ}						40			30							
t_{ZH}	Sense-Recovery Time 4					50[6]			40[6]			50			40	ns
t_{ZL}						50			40							
t_w	Width of Write Enable Pulse [8]			50			40			50			40			ns
t_{setup}	**Setup Time: 4** Address-to-Write Enable	R_L = 270Ω C_L = 15pF	R_L = 270Ω C_L = 15pF	0			0			0			0			ns
	Data-to-Write Enable			50			40			50			40			ns
	Chip Enable-to-Write Enable			0			0			0			0			ns
	Hold Time: Address-From-Write Enable			10			10			10			10			ns
t_{hold}	Data-From-Write Enable			10			10			10			10			ns
	Chip Enable-From-Write Enable			0			0			0			0			ns

MEMORIES

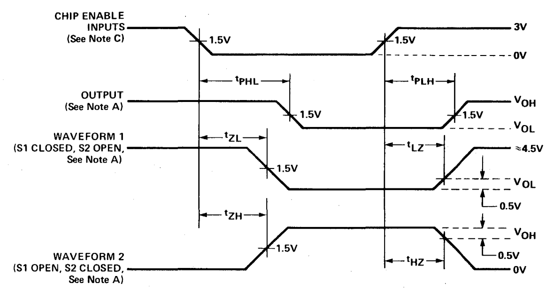
54S200/201/301-F • 74S200/201/301-B,F

SWITCHING PARAMETER MEASUREMENT INFORMATION

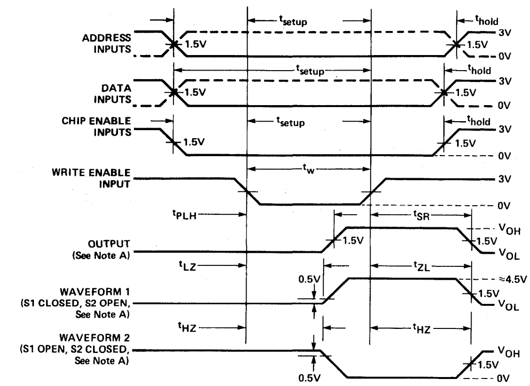
ACCESS TIME FROM ADDRESS



CHIP ENABLE AND DISABLE TIME

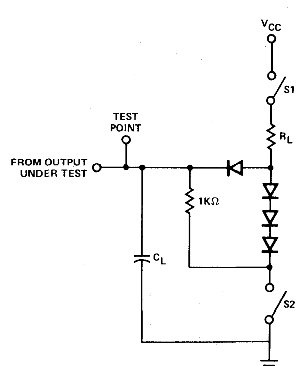


READ CYCLE



WRITE CYCLE

AC TEST LOAD



C_L INCLUDES PROBE AND JIG CAPACITANCE.
ALL DIODES ARE 1N3064.
ALL RESISTOR VALVES ARE TYPICAL.

NOTES:

A. Waveform 1 is for the output with internal conditions such that the output is low except when disabled. Waveform 2 is for the output with internal conditions such that the output is high except when disabled.
B. When measuring delay times from address inputs, the chip enable inputs are low and the write enable input is high.
C. When measuring delay times from chip enable inputs, the address inputs are steady-state and the write enable input is high.
D. Input waveforms are supplied by pulse generators having the following characteristics: $t_r \leq$ 2.5ns, $t_f \leq$ 2.5ns, PRR ≤ MHz, and $Z_{out} \approx 50\Omega$.
E. t_{PLH} propagation delay time, low-to-high-level output, t_{PHL} propagation delay time, high-to-low-level output.
F. t_{ZH} propagation delay time, hi-Z to high-level output, t_{ZL} propagation delay time, hi-Z to low-level output.
G. t_{HZ} propagation delay time, high-level to hi-Z output, t_{LZ} propagation delay time, low-level to hi-Z output.
H. Minimum required to guarantee a WRITE into the slowest bit.

N82S09-I

DESCRIPTION

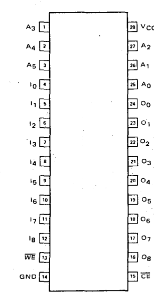
The 82S09 is a 576-Bit, Schottky clamped TTL, random access memory, organized as 64X9. This organization allows byte manipulation of data, including parity. Where parity is not monitored, the ninth bit can be used as a flag or status indicator for each word stored. With a typical access time of 30ns, it is ideal for scratch-pad, push-down stacks, buffer memories, and other internal memory applications in which cost and performance requirements dictate a wide data path in favor of word depth.

The 82S09 is fully TTL compatible, and features open collector outputs, chip enable input, and a very low current PNP input structure to enhance memory expansion.

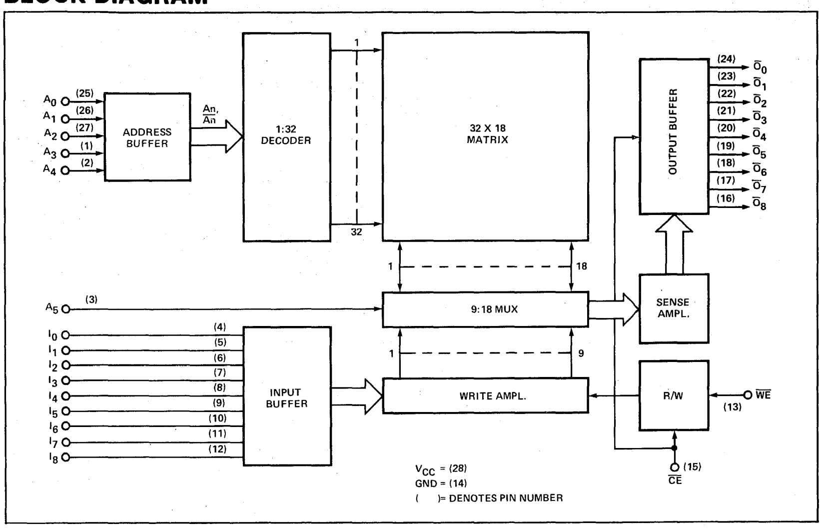
During WRITE operation, the logic state of the device output follows the complement of the data input being written. This feature allows faster execution of WRITE-READ cycles, enhancing the performance of systems utilizing indirect addressing modes, and/or requiring immediate verification following a WRITE cycle.

PIN CONFIGURATION

I PACKAGE



BLOCK DIAGRAM



TRUTH TABLE

MODE	$\overline{CE}$	$\overline{WE}$	I_N	O_N
READ	0	1	X	Complement of Data Stored
WRITE "0"	0	0	0	1
WRITE "1"	0	0	1	0
DISABLED	1	X	X	1

X = Don't care.

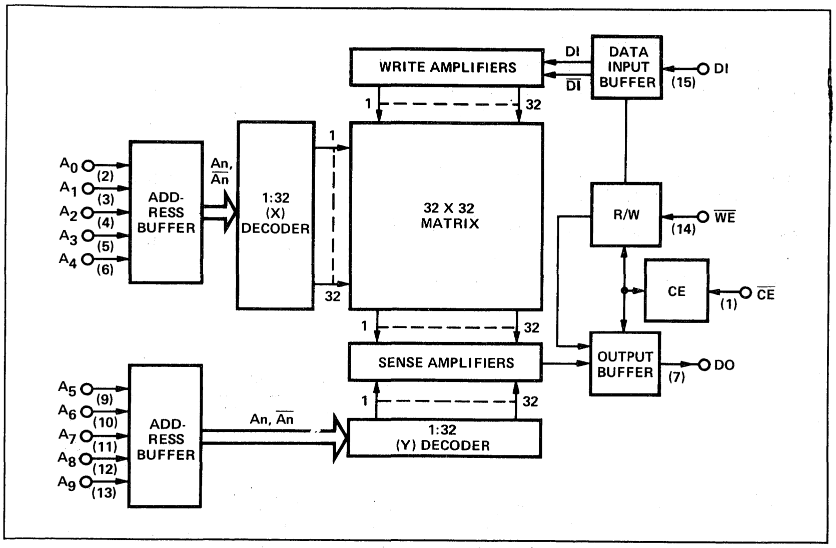
AC ELECTRICAL CHARACTERISTICS[3]

S82S09 $-55°C \leq T_A \leq +125°C$, $4.5V \leq V_{CC} \leq 5.5$
N82S09 $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25$

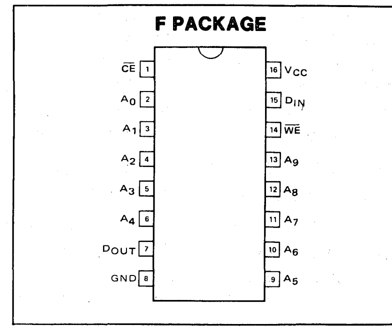
PARAMETER		TEST CONDITIONS	S82S09			N82S09			UNIT
			MIN	TYP1	MAX	MIN	TYP1	MAX	
Propagation Delays									
T_{AA}	Address Access Time	C_L = 30pF, R_1 = 600Ω, R_2 = 900Ω		30	80		30	45	ns
T_{CE}	Chip Enable Access Time			15	50		15	30	ns
T_{CD}	Chip Enable Output Disable Time			15	50		15	30	ns
T_{WD}	Write Enable to Output Valid Time			25	80		25	50	
Write Set-up Times									
T_{WSA}	Address to Write Enable		10	0		5	0		ns
T_{WSD}	Data In to Write Enable		50	25		35	25		ns
T_{WSC}	$\overline{CE}$ to Write Enable		10	0		5	0		ns
Write Hold Times									
T_{WHA}	Address to Write Enable		10	0		5	0		ns
T_{WHD}	Data In to Write Enable		5	0		5	0		ns
T_{WHC}	$\overline{CE}$ to Write Enable		10	0		5	0		ns
T_{WP}	Write Enable Pulse Width (Note 2)		50	25		35	25		ns

NOTES:
1. All voltage values are with respect to network ground terminal.
2. All typical values are at VCC = 5V, TA = 25°C.
3. ICC is measured with the write enable and memory enable input grounded, all other inputs at 4.5V, and the outputs open.

BLOCK DIAGRAM



PIN CONFIGURATION



TRUTH TABLE

MODE	CE	WE	D_{IN}	D_{OUT} 82S10 93415A	D_{OUT} 82S11 93425A
READ	0	1	X	STORED DATA	STORED DATA
WRITE "0"	0	0	0	1	High-Z
WRITE "1"	0	0	1	1	High-Z
DISABLED	1	X	X	1	High-Z

X = Don't care.

AC ELECTRICAL CHARACTERISTICS[3]

S82S10/11 $-55°C \leq T_A \leq +125°C$, $4.5V \leq V_{CC} \leq 5.5$
N82S10/11 $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25$

PARAMETER		TEST CONDITIONS	S82S10/11 MIN	S82S10/11 TYP[1]	S82S10/11 MAX	N82S10/11 MIN	N82S10/11 TYP[1]	N82S10/11 MAX	UNIT
Propagation Delays									
T_{AA}	Address Access Time			30	70		30	45	ns
T_{CE}	Chip Enable Access Time			15	45		15	30	ns
T_{CD}	Chip Enable Output Disable Time			15	45		15	30	ns
T_{WD}	Write Enable to Output Disable Time			20	45		20	30	ns
T_{WR}	Write Recovery Time			20	45		20	30	ns
Write Set-up Times		$C_L = 30pF$							
T_{WSA}	Address to Write Enable	$R_1 = 270\Omega$	15	0		5	0		ns
T_{WSD}	Data In to Write Enable	$R_2 = 600\Omega$	55	35		40	35		ns
T_{WSC}	CE to Write Enable		5	0		5	0		ns
Write Hold Times									
T_{WHA}	Address to Write Enable		10	0		5	0		ns
T_{WHD}	Data In to Write Enable		5	0		5	0		ns
T_{WHC}	CE to Write Enable		5	0		5	0		ns
T_{WP}	Write Enable Pulse Width (Note 2)		50	25		35	25		ns

NOTES:
1. Typical values are at $V_{CC} = +5.0V$, and $T_A = +25°C$.
2. Minimum required to guarantee a WRITE into the slowest bit.
3. The Operating Ambient Temperature Ranges are guaranteed with transverse air flow exceeding 400 linear feet per minute *and a two minute warm-up*. Typical thermal resistance values of the package at maximum temperature are:

Θ_{JA} Junction to Ambient at 400 fpm air flow — 50°C/Watt
Θ_{JA} Junction to Ambient — still air — 90°C/Watt
Θ_{JA} Junction to Case — 20°C/Watt

ROMS

Mask Programmable Read Only Memories

Signetics offers the industry's broadest line of High Performance Bipolar ROMs. Most ROMs have pin and performance compatible PROMs offering the user the ultimate in flexibility and long term cost reduction.

All ROMs are fully TTL compatible and include on-chip decoding and chip enable function for ease of memory expansion. Tri-state and open collector functions are available, and low input current requirements reduce the need for input buffering.

THERMAL RATINGS

TEMPERATURE	MILITARY	COMMERCIAL
Maximum junction	175°C	150°C
Maximum ambient	125°C	75°C
Allowable thermal rise ambient to junction	50°C	75°C

PARAMETER		LIMITS MIN	LIMITS MAX	UNITS
T_A	Operating Ambient Temperature			
	S82S - Military Range	−55	+125	°C
	N82S - Commercial Range	0	+75	°C
T_{STG}	Storage Temperature	−65	+150	°C
V_{IN}	Input Voltage		+5.5	Vdc
V_{OUT}	Output Voltage		+5.5	Vdc
V_{CC}	Power Supply Voltage		+7	Vdc

NOTES:
1. Stresses above those listed under "Maximum, Guaranteed Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device of these or any other condition above those indicated in the operation section of the device specifications is not implied.

MAXIMUM ALLOWABLE POWER DISSIPATION

MATERIAL	PACKAGE	# OF PINS	θ_{JA}[1] °C/W	P_{MAX} − mW 0+125°C	P_{MAX} − mW 0+75°C
Plastic	B	16	155	——	480
	XA	18	130	384	577
	N	24	100	500	750
	XF	28	100	500	750
Plastic[2]	BA	16	85	588	850
	XAS	18	73	685	>1000
	NA	24	75	666	1000
	XFA	28	75	666	1000
Cerdip	F	16	90	556	835
		18	90	556	835
		24	60	830	>1000
Ceramic	I	16	83	600	900
		24	50	1000	>1000
		28	50	1000	>1000

NOTES:
1. On a mounted surface, in still air.
2. Improved thermal characteristics due to built-in heat spreader.

BIPOLAR ROMS PRODUCT INFORMATION

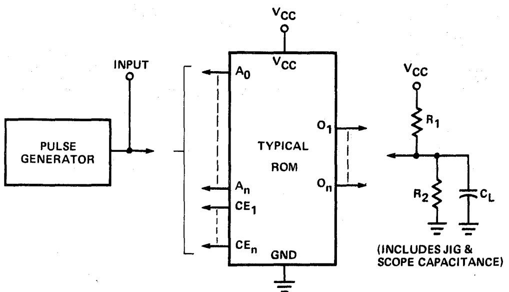
ELECTRICAL CHARACTERISTICS S82S DEVICES — $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5$
N82S DEVICES — $0°C \le T_A \le +75°C$, $4.75V \le 5.25$

PARAMETER	INPUT VOLTAGE									OUTPUT VOLTAGE						INPUT CURRENT		
	V_{IL}(V) LOW LEVEL			V_{IH}(V) HIGH LEVEL			V_{IC}[1](V) CLAMP VOLTAGE			V_{OL}[2](V) LOW LEVEL			V_{OH}[6] (V) HIGH LEVEL			i_{IL} (μA) LOW LEVEL		
TEST CONDITIONS	V_{CC} = MIN			V_{CC} = MAX			I_{IN} = -18 mA V_{CC} = MIN			I_{OL} = 16 mA V_{CC} = MIN			I_{OUT} = -2.0 mA CE_1 = CE = "0" "1" STORED			V_{IN} = 0.45V		
DEVICE	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
1024-BIT																		
825226 S N			.80 .85	2.0				-0.8	-1.2			0.5	2.4					-150 -100
825229 S N			.80 .85	2.0				-0.8	-1.2			0.5	2.4					-150 -100
2048-BITS																		
82S214 S N			.80 .85	2.0				-0.8	-1.2		I_{OUT} = 9.6 mA	0.5	2.4 2.7	3.3 3.3				-150 -100
82S215 S N			.80 .85	2.0				-0.8	-1.2		I_{OUT} = 9.6 mA	0.5	2.4 2.7	3.3 3.3				-150 -100
82S230 S N			.80 .85	2.0				-0.8	-1.2			0.5 0.45		N/A				-150 -100
82S231 S N			.80 .85	2.0				-0.8	-1.2			0.5 0.45	I_{OUT} = -2.4 mA 2.4					-150 -100
4096-BIT																		
8228 N			.85	2.0					-1.2		I_{OUT} = 11.2 mA	0.5	I_{OUT} = -1.0 mA 2.7					
8192-BITS																		
82S280 S N			.80 .85	2.0				-0.8	-1.2		I_{OUT} = 9.6 mA	0.5 0.45	CE_2 = "1" 2.7	3.3				-150 -100
82S281 S N			.80 .85	2.0				-0.8	-1.2		I_{OUT} = 9.6 mA	0.5 0.45	CE_2 = "1" 2.7	3.3				-150 -100

NOTES:
1. Test each input one at the time
2. Measured with the logic "0" stored Output sink current is supplied through a resistor to V_{CC}
3. I_{CC} is measured with the write enable and chip enable inputs grounded; all other inputs at 4.5V, and the outputs open
4. Measured with V_{IH} applied to CE
5. Duration of the short circuit should not exceed one second
6. Measured with $CE_{(S)}$ = OV, and outputs (s) at logic "1".
7. All voltage values are with respect to network ground terminal.

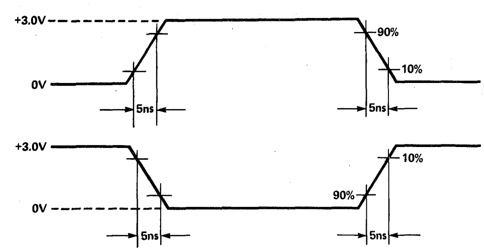
PARAMETER		INPUT CURRENT			OUTPUT CURRENT									SUPPLY CURRENT			CAPACITANCE					
		I_{IH} (µA) HIGH LEVEL			I_{OLK} (µA) LEAKAGE			I_O (OFF) HI-Z STATE			I_{OS} (mA)^6 SHORT CIRCUIT			I_{CC} (mA)^6			C_{IN} (pF) INPUT			C_{OUT}^4 (pF) OUTPUT		
TEST CONDITIONS		V_{IN} = 5.5V			V_{CC} = MAX, V_{OUT} = 5.5V, CE_1 OR CE_2 = "1"			V_{CC} = MAX, V_{OUT} = 5.5V			V_{OUT} = 0V, V_{CC} = MAX			V_{CC} = MAX			V_{IN} = 2.0V, V_{CC} = 5.0V			V_{CC} = 5.0V, V_{OUT} = 2.0V		
DEVICE		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
1024-BIT																						
82S226	S			50			60				-15		-85		105	125		5			8	
	N			40			40				-20		-70		105	120						
										V_{OUT} = 0.5V												
82S229	S			50						-60	-15		-85		105	125		5			8	
	N			40						-40	-20		-70		105	120						
2048-BIT																						
82S214	S			50		N/A				100	-15		-85		130	185		5			8	
	N			25						40	-20		-70		130	175						
										V_{OUT} = 0.5V												
82S215	S			50		N/A				-100	-15		-85		130	185		5			8	
	N			25						-40	-20		-70		130	175						
82S230	S			50			60			60	-15		-85		120	140		5			8	
	N			40			40			40	-20		-70		120	135						
										V_{OUT} = 0.5V												
										-60												
										-40												
82S231	S			50						60	-15		-85		120	140		5			8	
	N			40						40	-20		-70		120	135						
										V_{OUT} = 0.54												
										-60												
										-40												
4096-BIT																						
8228											-20		-70									
8192-BITS										CE_2 = "0"												
82S280	S			50		N/A				100	-15		-85		135	150		5			8	
	N			25						40	-20		-70		130	140						
										V_{OUT} = 0.5V												
										-100												
										-40												
										CE_2 = "0"												
82S281	S			50		N/A				100	-15		-85		135	150		5			8	
	N			25						40	-20		-70		130	140						
										V_{OUT} = 0.5V												
										-100												
										-40												

AC TEST FIGURE (UNLESS OTHERWISE SPECIFIED)



INPUT WAVEFORMS

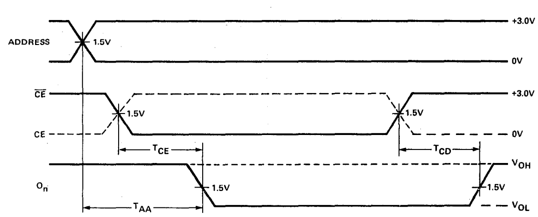
INPUT PULSES



Measurements: All Circuit Delays are measured at the +1.5V level of inputs and outputs.

TYPICAL AC WAVEFORMS (UNLESS OTHERWISE SPECIFIED)

READ CYCLE



All Inputs: tr = tf = 5ns (10% to 90%)

MEMORY TIMING DEFINITIONS

MEMORY TIMING DEFINITIONS

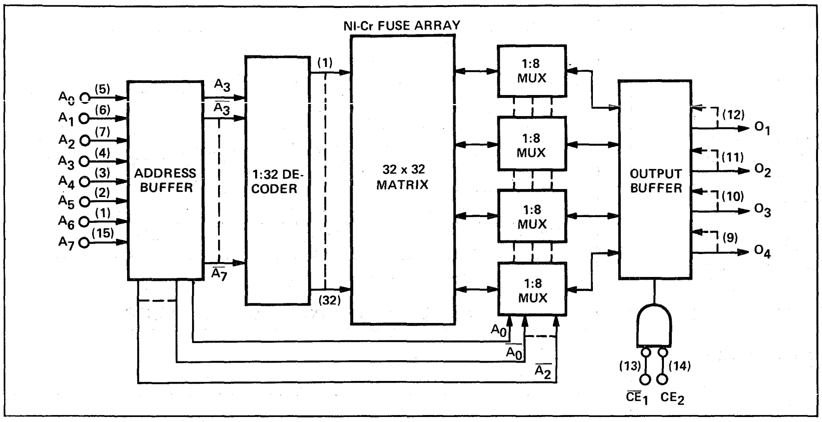
T_{CE}	Delay between beginning of CHIP ENABLE low (with ADDRESS valid) and when DATA OUTPUT becomes valid.
T_{CD}	Delay between when CHIP ENABLE becomes high and DATA OUTPUT is in off state.
T_{AA}	Delay between beginning of valid ADDRESS (with CHIP ENABLE low) and when DATA OUTPUT becomes valid.
T_{CDS}	Minimum delay between leading edge of CHIP ENABLE and trailing edge of STROBE, for latching valid output data.
T_{CDH}	Required delay between trailing edge of STROBE and end of CHIP ENABLE, for latching valid output data.
T_{SL}	Minimum delay between ADDRESS valid time and trailing edge of STROBE, for latching valid output data.
T_{SW}	Minimum width of STROBE pulse required to update contents of output data latches.
T_{ADH}	Required delay between trailing edge of STROBE and end of valid ADDRESS.
T_{DL}	Delay between leading edge of STROBE and when output data latches are released.

1024 BIT BIPOLAR ROM (256x4) — 82S226/229

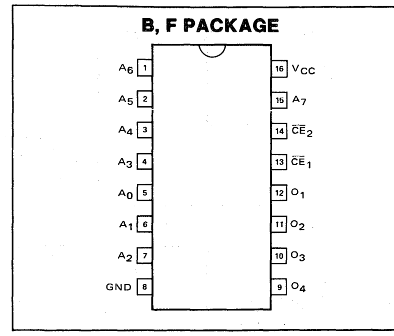
FULLY COMPATIBLE W/82S126/129

N82S226-B,F • S82S226-F
N82S229-B,F • S82S229-F

BLOCK DIAGRAM



PIN CONFIGURATION



AC ELECTRICAL CHARACTERISTICS

S82S226/229 −55°C ≤T_A ≤+125°C, 4.5V ≤V_{CC} ≤5.5V
N82S226/229 0°C ≤T_A ≤+75°C, 4.75V ≤V_{CC} ≤5.25V

PARAMETER		TEST CONDITIONS	S82S226/229			N82S226/229			UNIT
			MIN	TYP[2]	MAX	MIN	TYP[2]	MAX	
Propagation Delay									
T_{AA}	Address to Output	C_L = 30pF		35	70		35	50	ns
T_{CD}	Chip Disable to Output	R_1 = 270Ω		15	35		15	20	ns
T_{CE}	Chip Enable to Output	R_2 = 600Ω		15	35		15	20	ns

NOTES:
1. Positive current is defined as into the terminal referenced.
2. Typical values are at V_{CC} = 5.0V, T_A = +25°C.

2048-BIT BIPOLAR ROM (256x8) — 82S214
4096-BIT BIPOLAR ROM (512x8) — 82S215

FULLY COMPATIBLE W/82S114/115

N82S214-I • S82S114-I
N82S215-I • S82S115-I

DESCRIPTION

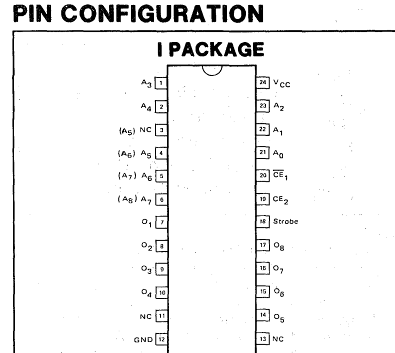
The 82S214 and 82S215 are Schottky-clamped Read Only Memories, incorporating on-chip data output registers.

The 82S214 and 82S215 are fully TTL compatible, and include on-chip decoding and two chip enable inputs for ease of memory expansion. They feature Tri-State outputs for optimization of word expansion in bussed organizations. A D-type latch is used to enable the Tri-State output drivers. In the TRANSPARENT READ mode, stored data is addressed by applying a binary code to the address inputs while holding STROBE high. In this mode the bit drivers will be controlled solely by $\overline{CE1}$ and CE2 lines.

In the LATCHED READ mode, outputs are held in their previous state (1,0, or High-Z) as long as STROBE is low, regardless of the state of address or chip enable. A positive STROBE transition causes data from the applied address to reach the outputs if the chip is enabled, and causes outputs to go to the High-Z state if the chip is disabled.

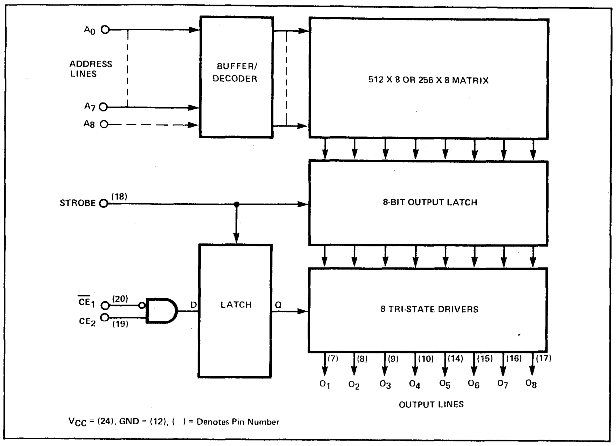
A negative STROBE transition causes outputs to be locked into their last Read Data condition if the chip was enabled, or causes outputs to be locked into the High-Z condition if the chip was disabled.

PIN CONFIGURATION

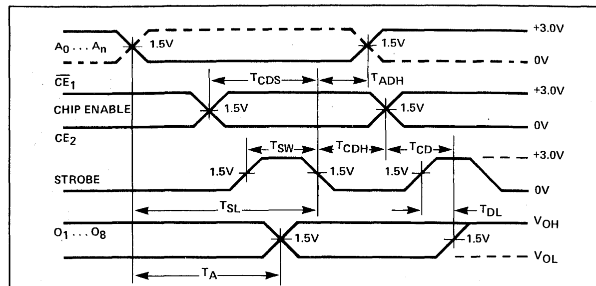


( ) 82S215 PIN CONNECTION

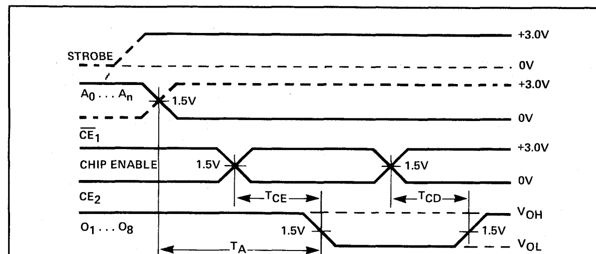
BLOCK DIAGRAM



AC WAVEFORMS



LATCHED READ (INPUT LATCHES USED)



TRANSPARENT READ (INPUT LATCHES NOT USED)

AC ELECTRICAL CHARACTERISTICS

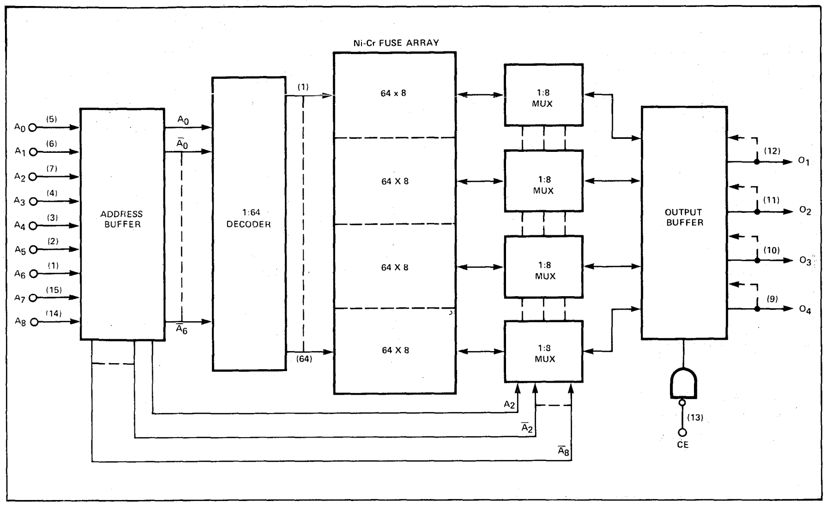
N82S214/215 $-55°C \leq T_A \leq +125°C$, $4.5V \leq V_{CC} \leq 5.5V$
S82S214/215 $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

PARAMETER		TEST CONDITIONS	N82S214/215			S82S214/215			UNIT
			MIN	TYP[2]	MAX	MIN	TYP[2]	MAX	
T_{AA}	Address Access Time	LATCHED or TRANSPARENT READ		35	60		35	90	ns
T_{CE}	Chip Enable Access Time	$R_1 = 470\Omega$, $R_2 = 1k\Omega$, $C_L = 30pF$ (Note 4)		20	40		20	50	ns
T_{CD}	Chip Disable Time			20	40		20	50	ns
T_{ADH}	Address Time		0	−10		5	−10		ns
T_{CDH}	Chip Enable Hold Time		10	0		10	0		ns
T_{SW}	Strobe Pulse Width	LATCHED READ ONLY	30	20		40	20		ns
T_{SL}	Strobe Latch Time	$R_1 = 470\Omega$, $R_2 = 1k\Omega$, $C_L = 30pF$	60	35		90	35		ns
T_{DL}	Strobe Delatch Time	(Note 5)			30			35	ns
T_{CDS}	Chip Enable Set-up Time		40			50			ns

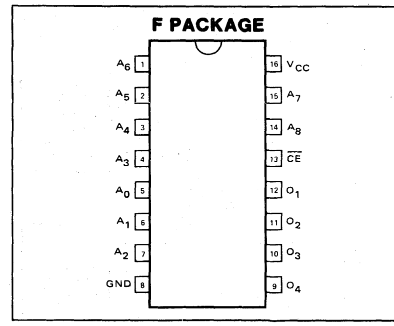
NOTES:
1. Positive current is defined as into the terminal referenced.
2. Typical values are at $V_{CC} = +5.0V$ and $T_A = +25°C$.
3. No more than one output should be grounded at the same time and strobe should be disabled. Strobe is in "1" state.
4. If the strobe is high, the device functions in a manner identical to conventional bipolar ROMS. The timing diagram shows valid data will appear T_A nanoseconds after the address has changed and T_{CE} nanoseconds after the output circuit is enabled. T_{CD} is the time required to disable the output and switch it to an "off" or high impedance state after it has been enabled.
5. In Latched Read Mode data from any selected address will be held on the output when strobe is lowered. Only when strobe is raised will new location data be transferred and chip enable conditions be stored. The new data will appear on the outputs if the chip enable conditions enable the outputs.

FULLY COMPATIBLE W/82S130/131 N82S231-F• S82S231-F

BLOCK DIAGRAM



PIN CONFIGURATION



AC ELECTRICAL CHARACTERISTICS

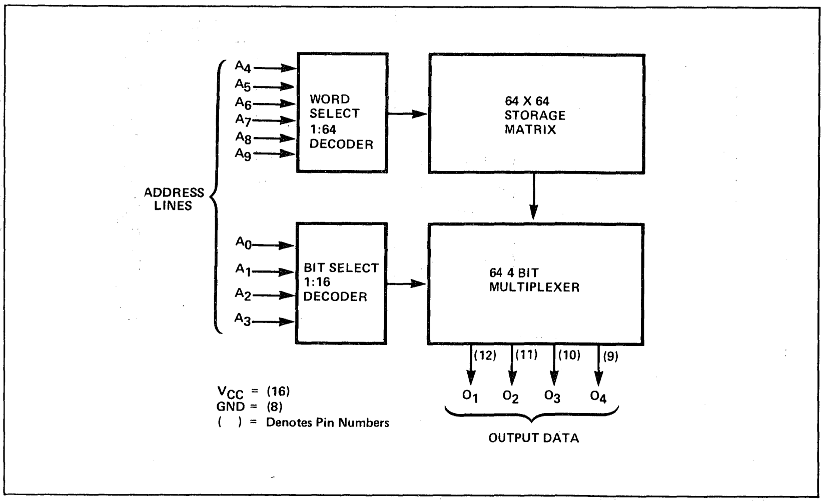
S82S230/231 −55°C ≤T_A ≤+125°C, 4.5V ≤V_{CC} ≤5.5V
N82S230/231 0°C ≤T_A ≤+75°C, 4.75V ≤V_{CC} ≤5.25V

PARAMETER		TEST CONDITIONS	S82S230/231			N82S230/231			UNIT
			MIN	TYP[2]	MAX	MIN	TYP[2]	MAX	
Propagation Delay									
T_{AA}	Address to Output	C_L = 30pF		40	70		40	50	ns
T_{CD}	Chip Disable to Output	R_1 = 270Ω		20	30		20	30	ns
T_{CE}	Chip Enable to Output	R_2 = 600Ω		20	30		20	30	ns

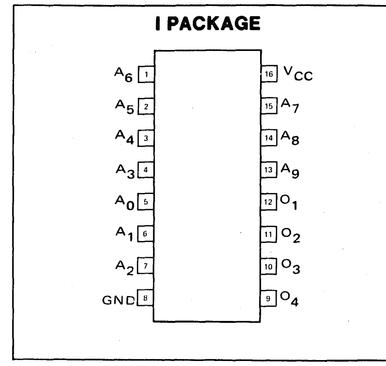
NOTES:
1. Positive current is defined as into the terminal referenced.
2. Typical values are at V_{CC} = 5.0V, T_A = +25°C.

N8228-I

BLOCK DIAGRAM



PIN CONFIGURATION



ELECTRICAL CHARACTERISTICS $0 \leq T_A \leq 75°C$, $4.75 \leq V_{CC} \leq 5.25V$

PARAMETERS	LIMITS			UNITS
	MIN	TYP	MAX	
Access Time—Address to Output		50	70	ns

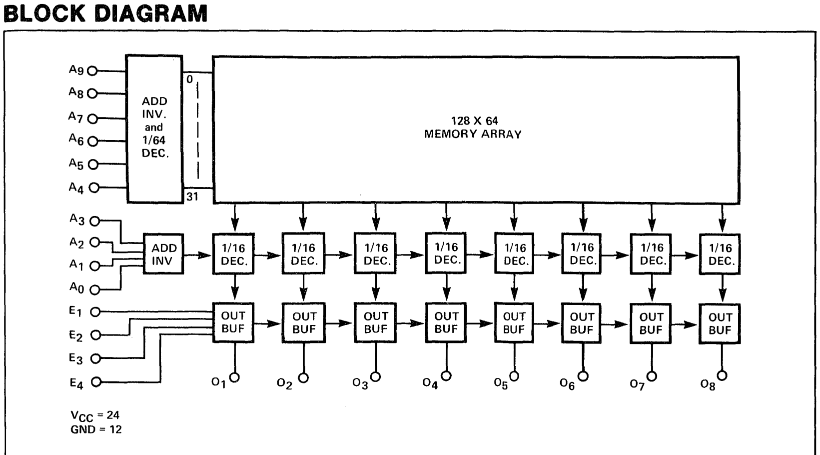
NOTES:
1. Positive current is defined as into the terminal referenced.
2. No more than one output should be grounded at the same time.
3. Manufacturer reserves the right to make design and process changes and improvements.
4. Applied voltages must not exceed 6.0V. Input currents must not exceed ±30mA. Output currents must not exceed ±100mA. Storage temperature must be between −60°C to +150°C.
5. Rise and fall time for this test must be less than 5ns. Input amplitudes are 2.8V and all measurements are made at 1.5V.

8192-BIT BIPOLAR ROM (1024x8) 82S280/281

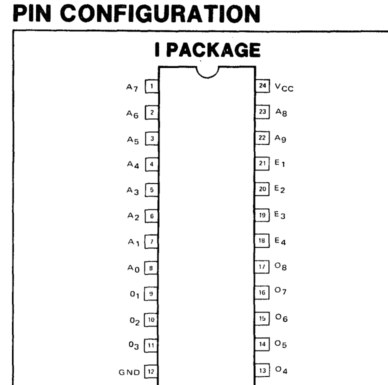
OBJECTIVE SPECIFICATION

N82S280/281-I • S82S280/281-I

BLOCK DIAGRAM



PIN CONFIGURATION



PROMS

Field Programmable Read Only Memories

Signetics offers the industry's broadest line of Bipolar High Performance PROMs. These PROMs are field programmable, which means that custom patterns are immediately available by following the provided fusing procedures. Signetics PROMs are supplied with all outputs at logical "0". Outputs are programmed to a logic "1" at any specified address by fusing a Ni-Cr link matrix.

All PROMs are fully TTL compatible, and include on-chip decoding and chip enable functions for ease of memory expansion. Tri-state and open collector output functions are available, and low input currents reduce input buffer requirements.

Most Signetics PROMs also have pin and performance compatible ROMs, offering the user the ultimate in flexibility and cost reduction.

THERMAL RATINGS

TEMPERATURE	MILITARY	COMMERCIAL
Maximum junction	175°C	150°C
Maximum ambient	125°C	75°C
Allowable thermal rise ambient to junction	50°C	75°C

ABSOLUTE MAXIMUM GUARANTEED RATINGS

PARAMETER	LIMITS		UNIT
	MIN	MAX	
T_A Operating Ambient Temperature			
S82S - Military Range	−55	+125	°C
N82S - Commercial Range	0	+75	°C
T_{STG} Storage Temperature	−65	+150	°C
V_{IN} Input Voltage		+5.5	Vdc
V_{OUT} Output Voltage		+5.5	Vdc
V_{CC} Power Supply Voltage		+7	Vdc

NOTES:
1. Stresses above those listed "Maximum, Guaranteed Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device of these or any other condition above those indicated in the operation section of the device specifications is not implied.
2. For operating at elevated temperatures, the device must be derated based on a + 150°C maximum junction temperature and a thermal resistance of 160°C/W junction to ambient.
3. For operating at elevated temperatures, the devices must be derated based on a + 160°C maximum junction temperature and a thermal resistance of 110°C/W junction to ambient.

MAXIMUM ALLOWABLE POWER DISSIPATION

MATERIAL	PACKAGE	# OF PINS	θ_{JA}[1] °C/W	P_{MAX} − mW	
				0+125°C	0+75°C
Plastic	B	16	155	——	480
	XA	18	130	384	577
	N	24	100	500	750
	XF	28	100	500	750
Plastic[2]	BA	16	85	588	850
	XAS	18	73	685	>1000
	NA	24	75	666	1000
	XFA	28	75	666	1000
Cerdip	F	16	90	556	
		18	90	556	835
		24	60	830	>1000
Ceramic	I	16	83	600	900
		24	50	1000	>1000
		28	50	1000	>1000

NOTES:
1. On a mounted surface, in still air.
2. Improved thermal characteristics due to built-in heat spreader.

BIPOLAR PROMS PRODUCT INFORMATION

ELECTRICAL CHARACTERISTICS S82S DEVICES — $-55°C \leq T_A \leq +125°C$, $4.5V \leq V_{CC} \leq 5.5$
N82S DEVICES — $0°C \leq T_A \leq +75°C$, $4.75V + V_{CC} \leq 5.25$

PARAMETER[8]	INPUT VOLTAGE									OUTPUT VOLTAGE						INPUT CURRENT		
	V_{IL}(V) LOW LEVEL			V_{IH}(V) HIGH LEVEL			V_{IC}[1](V) CLAMP VOLTAGE			V_{OL}[2](V) LOW LEVEL			V_{OH}[6](V) HIGH LEVEL			I_{IL}(μA) LOW LEVEL		
TEST CONDITIONS	V_{CC} = MIN			V_{CC} = MAX			I_{IN} = -18 mA V_{CC} = MIN			I_{OL} = 16 mA V_{CC} = MIN			I_{OUT} = -2.0 mA $CE_1 = CE_2$ = "0" "1" STORED			V_{IN} = 0.45V		
DEVICE	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYPE	MAX
256-BIT																		
82S23 S N			0.80 0.85	2.0					-1.2			0.5 0.45		N/A				-150 -100
82S123 S N			0.80 0.85	2.0					-1.2			0.5 0.45	2.4					-150 -100
10139	FOR ELECTRICAL SPECIFICATIONS SEE DATA SHEET																	
1024-BIT										I_{OUT} = 32mA							V_{IN} = 5V	
82S27 N			.80	2.0				I_{IN} = -12 mA	-1.5		0.45	0.50		N/A				-1.6mA
82S126 S N			.80 85	2.0					-1.2			0.5		N/A				-150 -100
82S129 S N			.80 .85	2.0					-1.2			0.5	2.4					-150 -100
82S130 S N			.80 .85	2.0					-1.2			0.5 0.45		N/A				-150 -100
82S131 S N			.80 .85	2.0					-1.2			0.5 0.45	2.4					-150 -100
2048-BIT										I_{OL} = 9.6 mA								
82S114 N			.85	2.0					-1.2			0.5	2.7	3.3				-100
82S115 N			.85	2.0					-1.2	I_{OL} = 9.6 mA		0.5	2.7	3.3				-100
4096-BIT																		
82S136 S N			.80 .85	2.0					-1.2			0.5 0.45		N/A				-150 -100
82S137 S N			.80 .85	2.0					-1.2			0.5 0.45	I_{OUT} = 2.4 mA 2.4					-150 -100
8192-BIT																		
825184 S N			.80 .85	2.0				-0.8	-1.2			0.5 0.45		N/A				-150 -100
82S185 S N			.80 .85	2.0				-0.8	-1.2			0.5 0.45	I_{OUT} = -2.4 mA 2.4					-150 -100

NOTES:
1. Test each input one at a time.
2. Measured with the logic "0" stored. Output sink current is supplied through a resistor to V_{CC}.
3. I_{CC} is measured with the write enable and chip enable inputs grounded; all other inputs at 4.5V, and the outputs open.
4. Measured with V_{IH} applied to $\overline{CE}$.
5. Duration of the short circuit should not exceed one second.
6. Measured with $\overline{CE}_{(S)}$ = OV, and output(s) at logic "1".
7. All voltage values are with respect to network ground terminal.

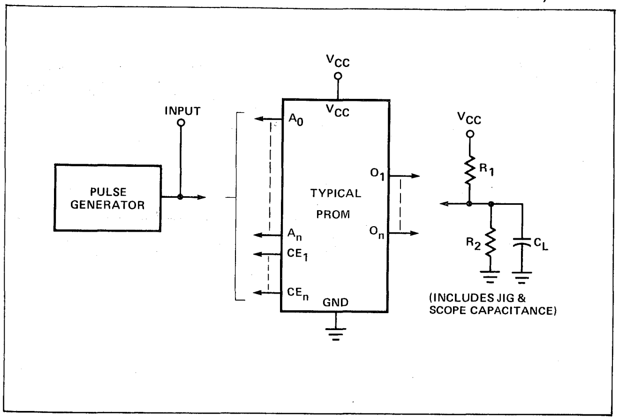
BIPOLAR PROMS PRODUCT INFORMATION

ELECTRICAL CHARACTERISTICS

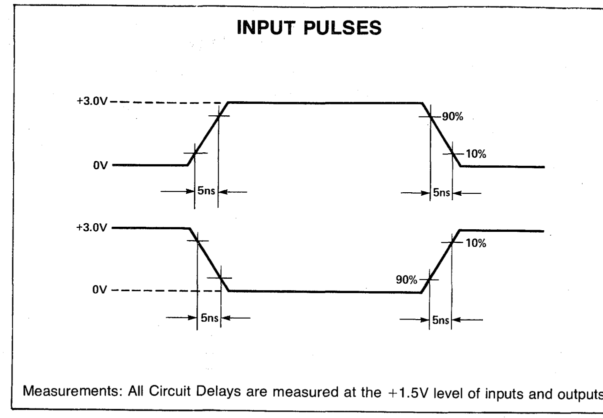
PARAMETER[8]	INPUT CURRENT			OUTPUT CURRENT									SUPPLY CURRENT			CAPACITANCE					
	I_{IH} (μA) HIGH LEVEL			I_{OLK}[4] (μA) LEAKAGE			I_O[4](OFF)(μA) HI-Z STATE			I_{OS}[5] (mA) SHORT CIRCUIT			I_{CC} (mA)[3]			C_{IN} (pF) INPUT			C_{OUT}[4] (pF) OUTPUT		
TEST CONDITIONS	V_{IN} = 5.5V			V_{CC} = MAX, V_{OUT} = 5.5V, CE_1 or CE_2 = "1"			V_{CC} = MAX, V_{OUT} = 5.5V			V_{OUT} = 0V, V_{CC} = MAX			V_{CC} = MAX			V_{IN} = 2.0V, V_{CC} = 5.0V			V_{CC} = 5.0V, V_{OUT} = 2.0V		
DEVICE	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
256-BIT																					
82S23 S			50			50		N/A			N/A			65	85		5			8	
N						40								65	77						
82S123 S			50		N/A				50	-20		-100		65	85		5			8	
N									40	-20		-90		65	77						
								V_{OUT} = 0.5V													
									-50												
									-40												
10139	FOR ELECTRICAL SPECIFICATIONS SEE DATA SHEET																				
1024-BIT																					
82S27 N			1000			100		N/A			N/A			120	140		5			8	
82S126 S			50			60		N/A			N/A			105	125		5			8	
N			40			40								105	120						
82S129 S			50		N/A				60	-15		-85		105	125		5			8	
N			40						40	-20		-70		105	120						
								V_{OUT} = 0.5V													
									-60												
									-40												
82S130 S			50			60		N/A			N/A			120	140		5			8	
N			40			40															
82S131 S			50		N/A				60	-15		-85		120	140		5			8	
N			40						40	-20		-70									
								V_{OUT} = 0.5V													
									-60												
									-40												
2048-BIT								V_{OUT} = 0.5V													
82S114 N			25		N/A				-40	-20		-70		135	185		5			8	
82S115 N			25		N/A																
4096-BIT																					
82S136 S			50		N/A			N/A			N/A			120	140		5			8	
N			40																		
82S137 S			50		N/A				60	-15		-85		120	140		5			8	
N			40						40	-20		-70									
								V_{OUT} = 0.5V													
									-60												
									-40												
8192-BIT																					
82S184 S			50			60					N/A			80	130		5			8	
N			40			40								80	120						
82S185 S			50		N/A				60	-15		-85		80	130		5			8	
N			40						40	-20		-70		80	120						
								V_{OUT} = 0.5V													
									-60												
									-40												

MEMORIES

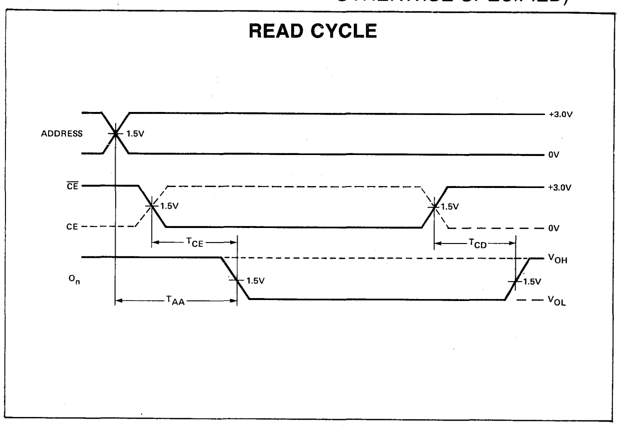
AC TEST FIGURE (UNLESS OTHERWISE SPECIFIED)



INPUT WAVEFORMS



TYPICAL AC WAVEFORMS (UNLESS OTHERWISE SPECIFIED)

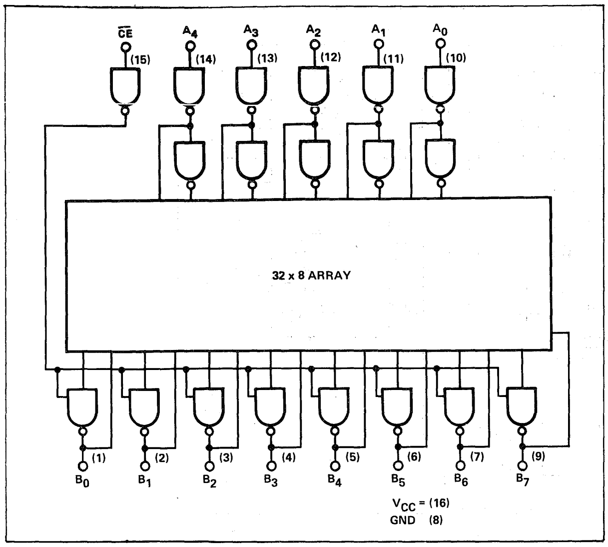


MEMORY TIMING DEFINITIONS

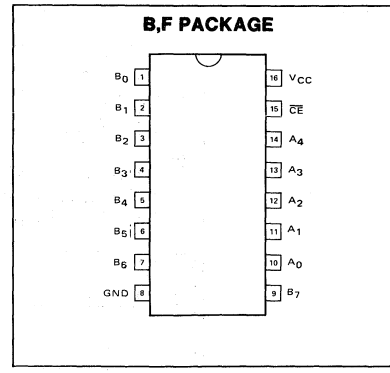
- T_{CE} Delay between beginning of CHIP ENABLE low (with ADDRESS valid) and when DATA OUTPUT becomes valid.
- T_{CD} Delay between when CHIP ENABLE becomes high and DATA OUTPUT is in off state.
- T_{AA} Delay between beginning of valid ADDRESS (with CHIP ENABLE low) and when DATA OUTPUT becomes valid.
- T_{CDS} Minimum delay between leading edge of CHIP ENABLE and trailing edge of STROBE, for latching valid output data.
- T_{CDH} Required delay between trailing edge of STROBE and end of CHIP ENABLE, for latching valid output data.
- T_{SL} Minimum delay between ADDRESS valid time and trailing edge of STROBE, for latching valid output data.
- T_{SW} Minimum width of STROBE pulse required to update contents of output data latches.
- T_{ADH} Required delay between trailing edge of STROBE and end of valid ADDRESS.
- T_{DL} Delay between leading edge of STROBE and when output data latches are released.

N82S23/123-B,F • S82S23/123-F

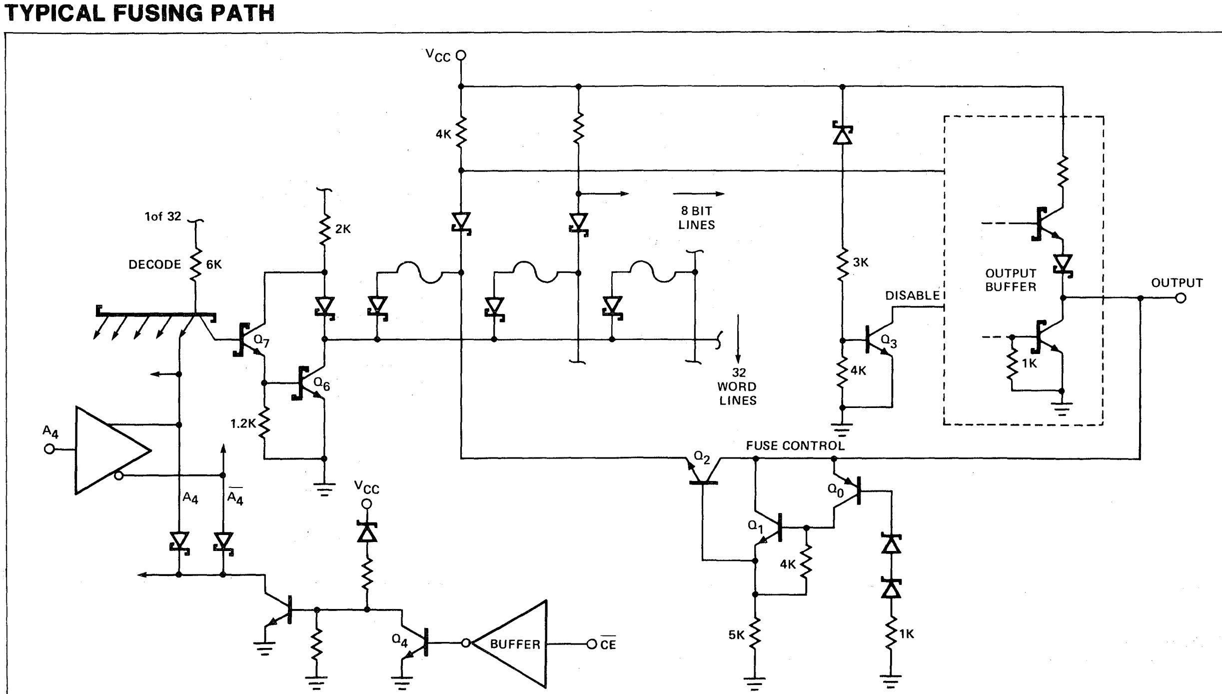
LOGIC DIAGRAM



PIN CONFIGURATION



TYPICAL FUSING PATH



AC ELECTRICAL CHARACTERISTICS

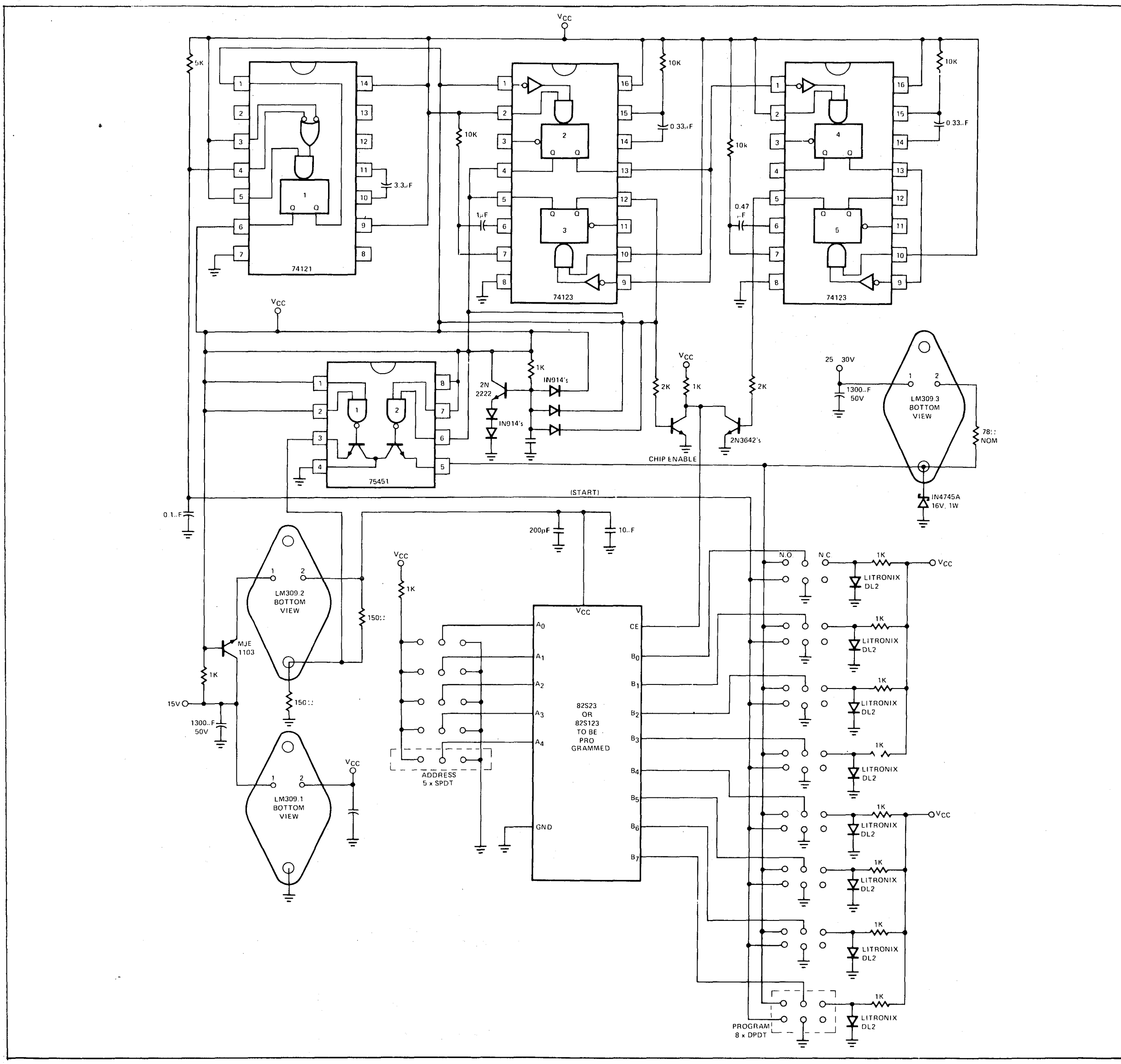
S82S23/S82S123 $-55°C \leq T_A \leq +125°C$, $4.5 \leq V_{CC} \leq 5.5V$
N82S23/N82S123 $0°C \leq T_A \leq +75°C$, $4.75 \leq V_{CC} \leq 5.25V$

PARAMETER	TEST CONDITIONS1	S83S23/S82S123			N82S23/N82S123			UNIT
		MIN	TYP2	MAX	MIN	TYP2	MAX	
Propagation Delay								
T_{AA} Address to Output	$C_L = 30pF$		35	65		35	50	ns
T_{CD} Chip Disable to Output	$R_1 = 270\Omega$		25	40		25	35	ns
T_{CE} Chip Enable to Output	$R_2 = 600\Omega$		25	40		25	35	ns

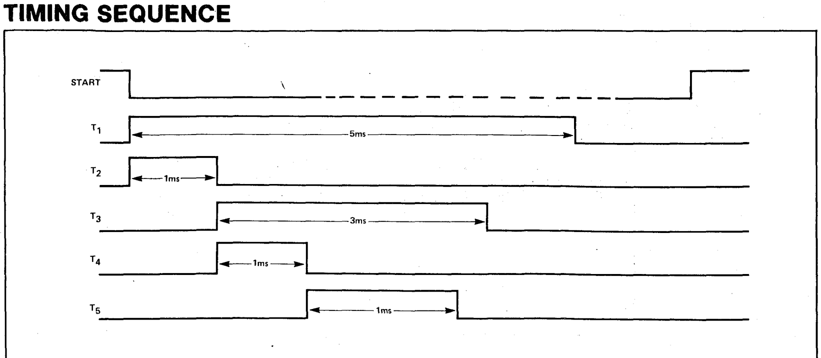
NOTES:
1. Positive current is defined as into the terminal referenced.
2. Typical values are at $V_{CC} = 5.0V$, $T_A = +25°C$.

MEMORIES

MANUAL PROGRAMMER



TIMING SEQUENCE



PROGRAMMING SPECIFICATIONS (Testing of these limits may cause programming of device.) $T_A = +25°C$

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
Power Supply Voltage						
V_{CCP}[1]	To Program	$I_{CCP} = 250 \pm 50mA$ (Transient or steady state)	9.5	10.0	10.5	V
V_{CCH}	Upper Verify Limit		5.3	5.5	5.7	V
V_{CCL}	Lower Verify Limit		4.3	4.5	4.7	V
V_S[3]	Verify Threshold		0.9	1.0	1.1	V
I_{CCP}	Programming Supply Current	$V_{CCP} = +10.0 \pm 0.5V$	200	250	300	mA
Input Voltage						
V_{IH}	Logical "1"		2.4		5.5	V
V_{IL}	Logical "0"		0	0.4	0.6	V
Input Current						
I_{IH}	Logical "1"	$V_{IH} = +5.5V$			50	μA
I_{IL}	Logical "0"	$V_{IL} = +0.4V$			-500	μA
V_{OUT}[2]	Output Programming Voltage	$I_{OUT} = 65 \pm 3mA$ (Transient or steady state)	15.0	15.5	16.0	V
I_{OUT}	Output Programming Current	$V_{OUT} = +15.5 \pm 0.5V$	62	65	68	mA
T_R	Output Pulse Rise Time		10		50	μs
t_P	$\overline{CE}$ Programming Pulse Width		1		2	ms
t_V	Verify Delay		50			μs
t_D	Pulse Sequence Delay		10			μs
T_{PR}	Programming Time	$V_{CC} = V_{CCP}$			2.5	sec
T_{PS}	Programming Pause	$V_{CC} = 0V$	5			sec
$\frac{T_{PR}}{T_{PR}+T_{PS}}$[4]	Programming Duty Cycle				33	%

PROGRAMMING PROCEDURE

1. Terminate all device outputs with a 10kΩ resistor to V_{CC}.
2. Select the Address to be programmed, and raise V_{CC} to $V_{CCP} = +10 \pm 0.5V$.
3. After 10μs delay, apply $I_{OUT} = 65 \pm 3mA$ to the output to be programmed. Program one output at a time.
4. After 10μs delay, pulse the $\overline{CE}$ input to logic "0" for 1 to 2 ms.
5. After 10μs delay, remove I_{OUT} from the programmed output.
6. After 10μs delay, return V_{CC} to 0V.
7. To verify programming, after 50μs delay, raise V_{CC} to $V_{CCH} = +5.5 \pm .2V$, and apply a logic "0" level to the $\overline{CE}$ input. The programmed output should remain in the "1" state. Again, lower V_{CC} to $V_{CCL} = +4.5 \pm .2V$, and verify that the programmed output remains in the "1" state.
8. Raise V_{CC} to $V_{CCP} = +10 \pm 0.5V$ and repeat steps 3 through 7 to program other bits at the same address.
9. After 10μs delay, repeat steps 2 through 8 to program all other address locations.

NOTES:
1. Bypass V_{CC} to GND with a 0.01μF capacitor to reduce voltage spikes.
2. Care should be taken to insure that $+15.5 \pm 0.5V$ output voltage is maintained during the entire fusing cycle. The recommended supply is a constant current source clamped at the specified voltage limit.
3. V_S is the sensing threshold of the PROM output voltage for a programmed bit. It normally constitutes the reference voltage applied to a comparator circuit to verify a successful fusing attempt.
4. Continuous fusing for an unlimited time is also allowed, provided that a 33% duty cycle is maintained. This may be accomplished by following each Program Verify cycle with a Rest period (V_{CC} = 0V) of 4ms.

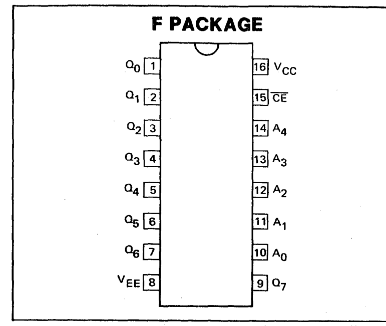
MEMORIES

10139-F

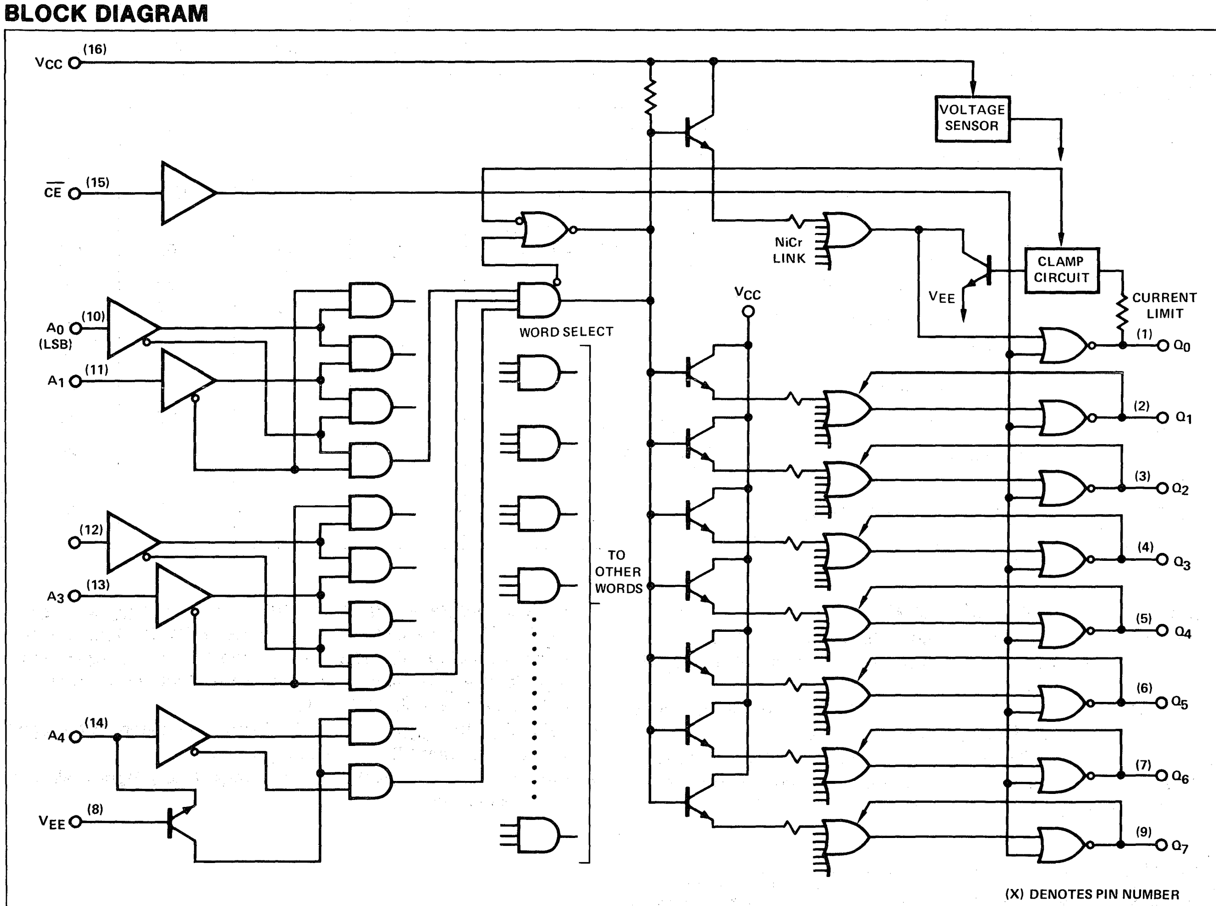
DESCRIPTION

The 10139 is an ECL 256-Bit Read Only Memory organized as 32 words with 8 bits per word. The words are selected by five binary address lines; full word decoding is incorporated on the chip. A chip enable input is provided for additional decoding flexibility, which causes all eight outputs to go to low state when the chip enable input is high. This device is fully compatible with all of Signetics series 10,000 products. Address to output access time is 15ns typical. Power dissipation is 580 milliwatts typical with separate internal bond wires and metal systems for VCC1 and VCC2. The 10139 may be programmed to any desired pattern by the user. The 10139 is suitable for use in high performance ECL systems. The 10139 features open emitter outputs, a 50kΩ pulldown input termination and a temperature range of −30°C to +85°C.

PIN CONFIGURATION



BLOCK DIAGRAM



DC ELECTRICAL CHARACTERISTICS (T_A = +25°C, V_{CC} = 0V, R_L = 50Ω, V_{EE} = −5.2V)

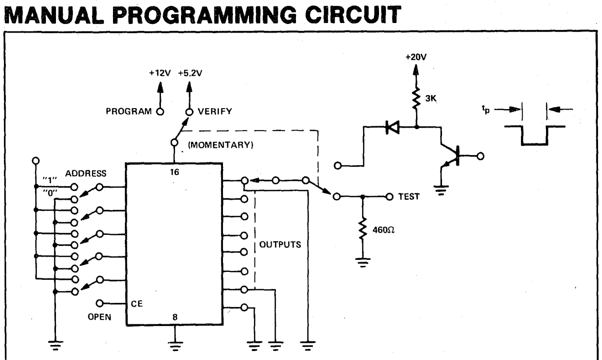
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{EO}	Power Supply Drain Current			110	145	mA
I_{IL} I_{IH}	Low Level Input Current High Level Input Current	V_{IL} = −1.850V V_{IH} = −0.810V	30		 265	μA μA
V_{OH}	High Level Output Voltage	V_{IH} = −0.810V V_{IL} = −1.850V	−0.960		−0.810	V
V_{OL}	Low Level Output Voltage	V_{IH} = −0.810V V_{ILA} = 1.850V	−1.990		−1.650	V
V_{OHA}		V_{IHA} = −1.105V V_{ILA} = −1.475V	−0.980			V
V_{OLA}		V_{IHA} = −1.105V V_{ILA} = −1.475V			−1.630	V

SWITCHING CHARACTERISTICS

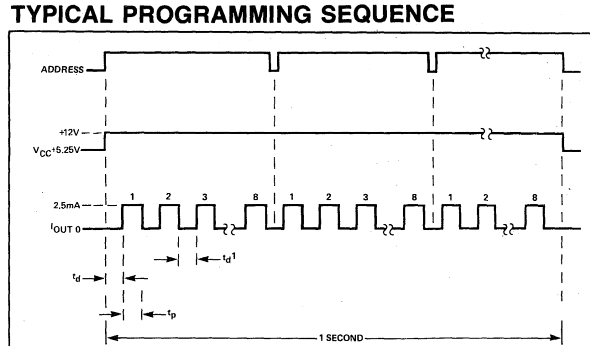
(T_A = +25°C, V_{CC} = 0V, V_{EE} = -5.2V, R_L = 50Ω)

PARAMETER	MIN	TYP	MAX	UNIT
Chip Enable Prop Delay		10	15	ns
Output Rise Time (20 to 80%) Output Fall Time (20 to 80%)		4.2 4.2		ns ns
T_{AD} Access Time Address to Output	T_{AD}	15	20	ns

MANUAL PROGRAMMING CIRCUIT



TYPICAL PROGRAMMING SEQUENCE



MEMORIES

PROGRAMMING SPECIFICATIONS

		TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
	Power Supply Voltage					
V_{CCP}	To Program		11.5	12.0	12.5	V
V_{CCV}	To Verify		5.0	5.2	5.4	V
I_{CCP}	Programming Supply Current	$V_{CC}=12.0V$			250	mA
	Address Voltage					
V_{IH}	logical "1"		4.0		4.6	V
V_{IL}	logical "0"		0.0		1.0	V
	Max. Time at $V_{CC}=V_{CCP}$				1.0	Sec.
I_{OP}	Output Programming Current		2.0	2.5	3.0	mA
t_p	Output Program Pulse Width		0.5		1.0	ms
	Output Pulse Rise Time				10.0	μs
	Programming Pulse Delay (1)					
t_d	following V_{CC} change		0.1		1.0	ms
t_d1	between output pulses		0.01		1.0	ms

NOTE:
(1) Maximum is specified to minimize the amount of time V_{CC} is at 12 volts.

RECOMMENDED PROGRAMMING PROCEDURE

The 10139 is shipped with all bits at logical "0" (low). To write logical "1's", proceed as follows:

STEP 1

Connect V_{EE} (Pin 8) to ground and V_{CC} (Pin 16) to +5.2 volts. Address the word to be programmed by applying 4.0 to 4.6 volts for a logic "1" and 0.0 to 1.0 volts for a logic "0" to the appropriate address inputs.

STEP 2

Raise V_{CC} (Pin 16) to 12 volts.

STEP 3

After a minimum delay of 100 μs apply a 2.5 mA current pulse to the first bit to be programmed (0.5 ≤PW≤1 ms).

STEP 4

Return V_{CC} to 5.2 volts.

CAUTION: To prevent excessive chip temperature rise, V_{CC} should not be allowed to remain at 12 volts for more than 1 second.

STEP 5

Verify that the selected bit has programmed by connecting a 460Ω resistor to ground and measuring the voltage at the output pin. If a logic "1" is not detected at the output, the procedure should be repeated once.

STEP 6

Repeat Step 3 for each bit of the selected word specified as a logic "1". (Program only one bit at a time; the delay between output programming pulses should be equal to or less than 1.0 ms.)

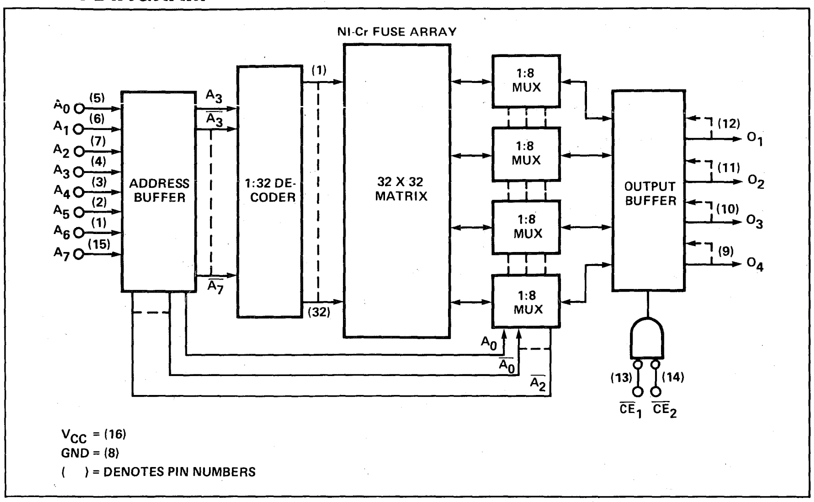
STEP 7

After all the desired bits of the selected word have been programmed, change address data and repeat Steps 2 and 3.

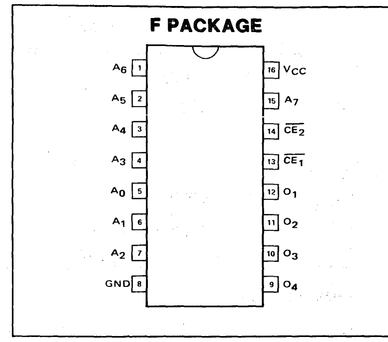
NOTE: If all the maximum times listed above are maintained, the entire memory will program in less than 1 second. Therefore, it would be permissible for V_{CC} to remain at 12 volts during the entire programming time.

N82S27-F

BLOCK DIAGRAM



PIN CONFIGURATION



AC ELECTRICAL CHARACTERISTICS $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP2	MAX	
Propagation Delay						
T_{AA}	Address to Output	$C_L = 30pF$		30	40	ns
T_{CD}	Chip Disable to Output	$R_1 = 270\Omega$		15	20	ns
T_{CE}	Chip Enable to Output	$R_2 = 600\Omega$		15	20	ns

NOTES:
1. Positive current is defined as into the terminal referenced.
2. Typical values are at V_{CC} = 5.0V, T_A = +25°C.

MEMORIES

N82S27-F

PROGRAMMING SPECIFICATIONS (Testing of these limits may cause programming of device.) $T_A = +25°C$

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
Power Supply Voltage						
V_{CCP}[1]	To Program	$I_{CCP} = 300 \pm 50mA$ (Transient or steady state)	5.0		5.25	V
V_{CCH}	Upper Verify Limit		5.0	5.25	5.5	V
V_{CCL}	Lower Verify Limit		4.5	4.75	5.0	V
V_S[3]	Verify Threshold		0.9	1.0	1.1	V
I_{CCP}	Programming Supply Current	$V_{CCP} = +5.0 \pm 0.25V$	250	300	350	mA
Input Voltage						
V_{IH}	Logical "1" (Except $\overline{CE}_1$)		3.0		5.0	V
V_{IN}	Program Level ($\overline{CE}_1$ Only)		14.0	14.5	15.0	V
V_{IL}	Logical "0"		0	0.4	0.5	V
Input Current						
I_{IH}	Logical "1"	$V_{IH} = +3.0V$			100	μA
I_{IL}	Logical "0"	$V_{IL} = +0.5V$			-1.6	mA
I_{IN}	Program Level ($\overline{CE}_1$ Only)	$V_{IN} = +15.0V$			15	mA
V_{OUT}[2]	Output Programming Voltage	$I_{OUT} = 115 \pm 10mA$ (Transient or steady state)	16.5	17.0	17.5	V
I_{OUT}	Output Programming Current	$V_{OUT} = +17.0 \pm 0.5V$	105	115	125	mA
T_R[5]	Output Pulse Rise Time		0.2		0.5	μs
t_P	Programming Pulse Width		1		2	ms
t_D	Pulse Sequence Delay		10			μs
T_{PR}	Programming Time	$V_{CC} = V_{CCP}$			2.5	sec
T_{PS}	Programming Pause	$V_{CC} = 0V$	5			sec
$\frac{T_{PR}}{T_{PR}+T_{PS}}$[4]	Programming Duty Cycle				33	%

PROGRAMMING PROCEDURE

The 82S27 is shipped with all bits at logical "0" (low). To write logical "1", proceed as follows:

SET-UP

a. Apply GND to pin 12.
b. Terminate all device outputs with a 10kΩ resistor to V_{CC}.
c. Set $\overline{CE}_2$ to logic "0".

PROGRAM-VERIFY SEQUENCE

Step 1 Raise V_{CC} to V_{CCP}, and address the word to be programmed by applying TTL "1" and "0" logic levels to the device address inputs.

Step 2 After 10μs delay, apply to $\overline{CE}_1$ (pin 13) a voltage source of 14.5 ± 0.5V, with 15mA sourcing current capability.

Step 3 After 10μs delay, apply a voltage source of + 17.0 ± 0.5v to the output to be programmed. The source must have a current limit of 115mA. Program one output at the time.

Step 4 After 10μs delay, remove + 17.0V supply from programmed output.

Step 5 To verify programming, after 10μs delay, return $\overline{CE}_1$ to 0V. Raise V_{CC} to $V_{CCH} = \pm 5.25 \pm .25V$. The programmed output should remain in the "1" state. Again, lower V_{CC} to $V_{CCL} = +4.75 \pm .25V$, and verify that the programmed output remains in the "1" state.

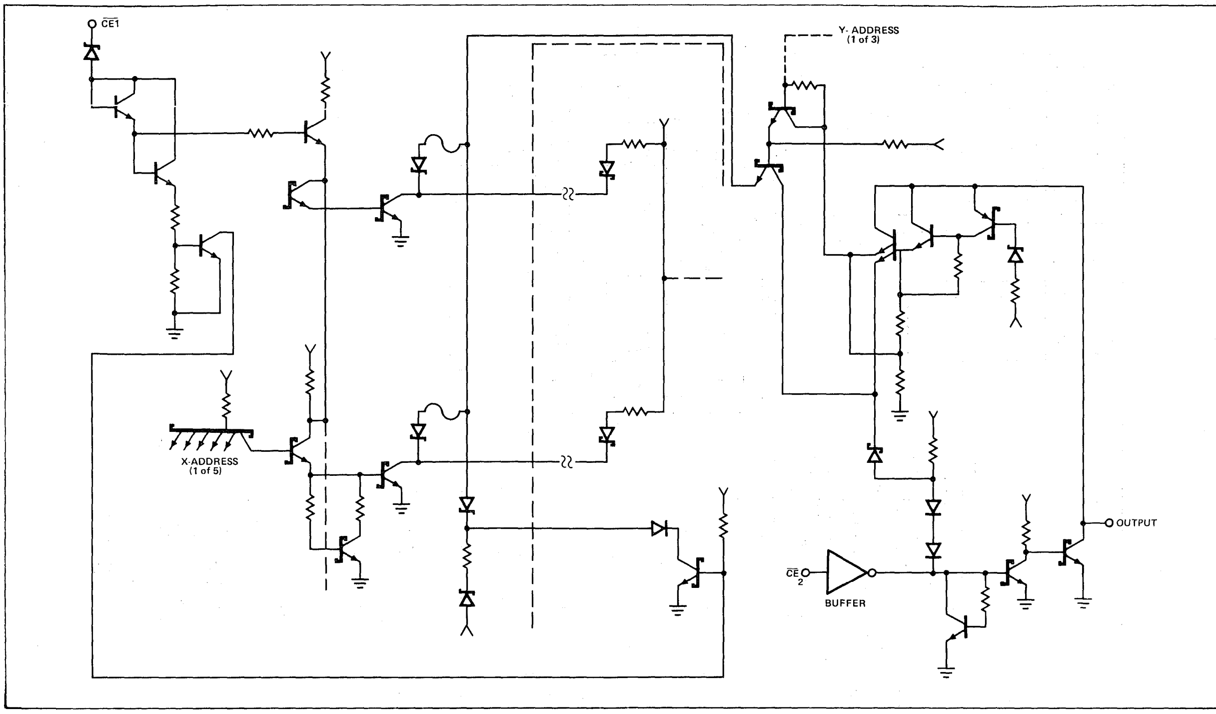
Step 6 Raise V_{CC} to V_{CCP}, and repeat steps 2 through 5 to program other bits at the same address.

Step 7 Repeat steps 1 through 6 to program all other address locations.

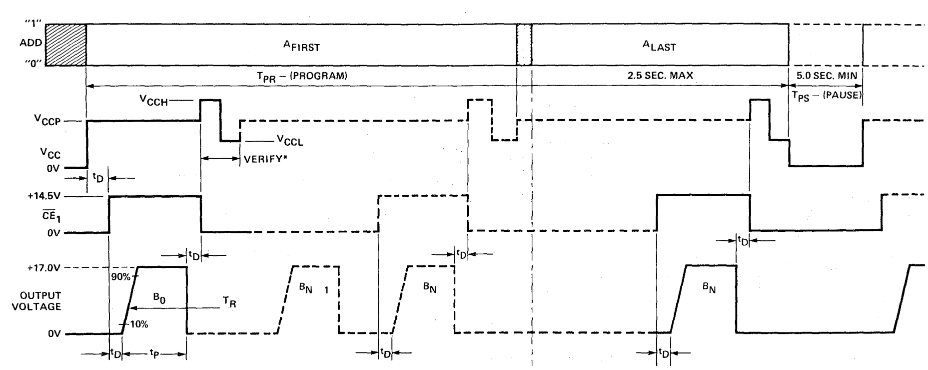
NOTES:
1. Bypass V_{CC} to GND with a 0.01μF capacitor to reduce voltage spikes.
2. Care should be taken to insure the 17 ± 0.5V output voltage is maintained during the entire fusing cycle. The recommended supply is a constant current source clamped at the specified voltage limit.
3. V_S is the sensing threshold of the PROM output voltage for a programmed bit. It normally constitutes the reference voltage applied to a comparator circuit to verify a successful fusing attempt.
4. Continuous fusing for an unlimited time is also allowed, provided that a 33% duty cycle is maintained. This may be accomplished by following each Program Verify cycle with a Rest period (V_{CC} = 0V) of 4ms.
5. Measured with a 1k dummy load connected across the fusing source.

N82S27-F

TYPICAL FUSING PATH



TYPICAL PROGRAMMING SEQUENCE

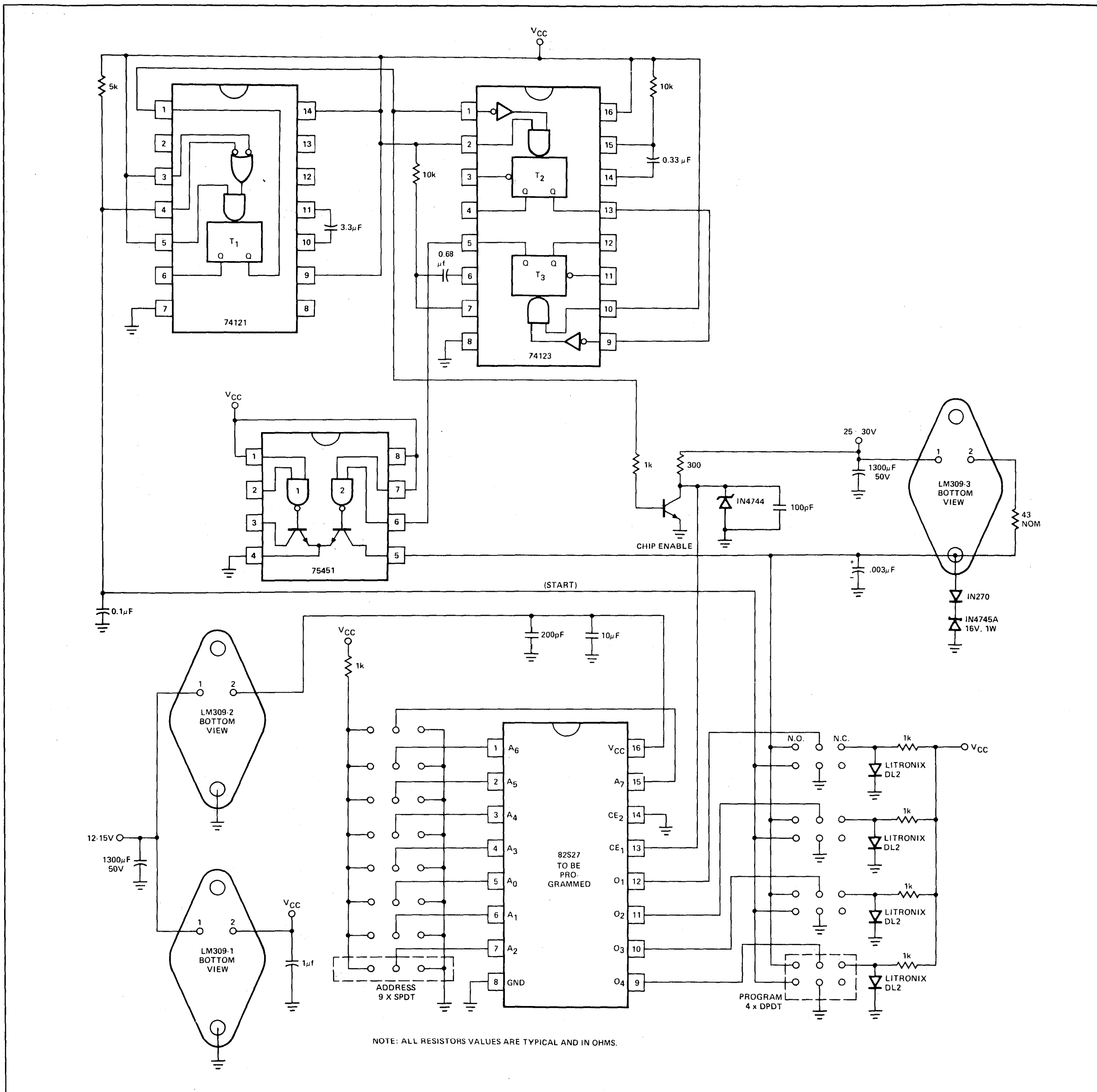


*PROGRAMMING VERIFICATION AT BOTH HIGH AND LOW V_{CC} MARGINS IS OPTIONAL. FOR CONVENIENCE, VERIFICATION CAN ALSO BE EXECUTED AT THE OPERATING V_{CC} LIMITS SPECIFIED IN THE DC CHARACTERISTICS.

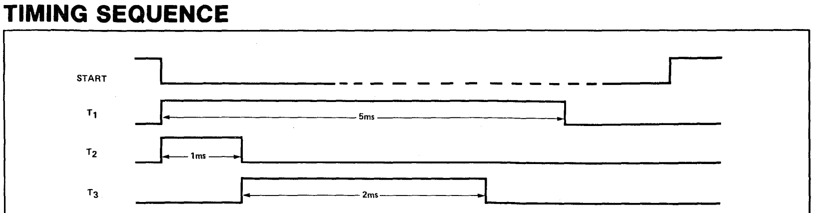
MEMORIES

N82S27-F

MANUAL PROGRAMMER

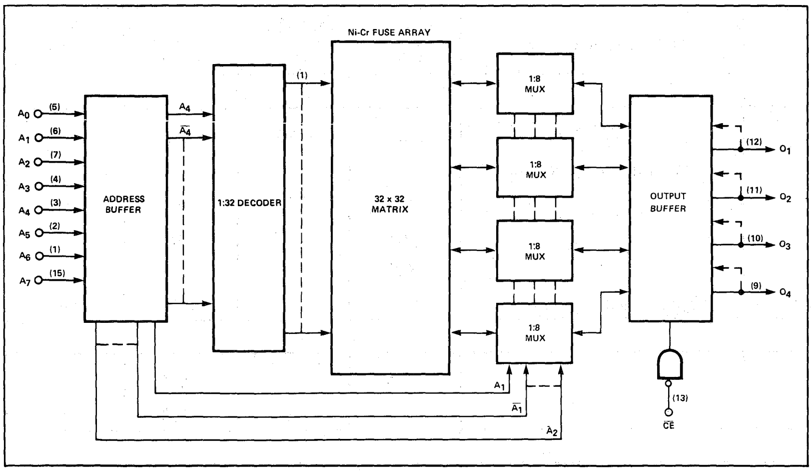


TIMING SEQUENCE

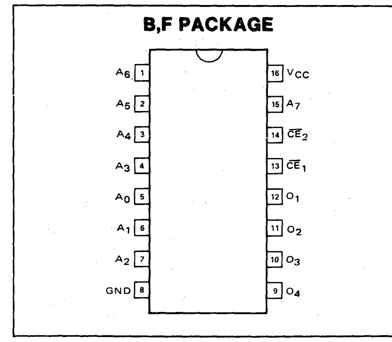


N82S126/129-B,F. • S82S126/129F

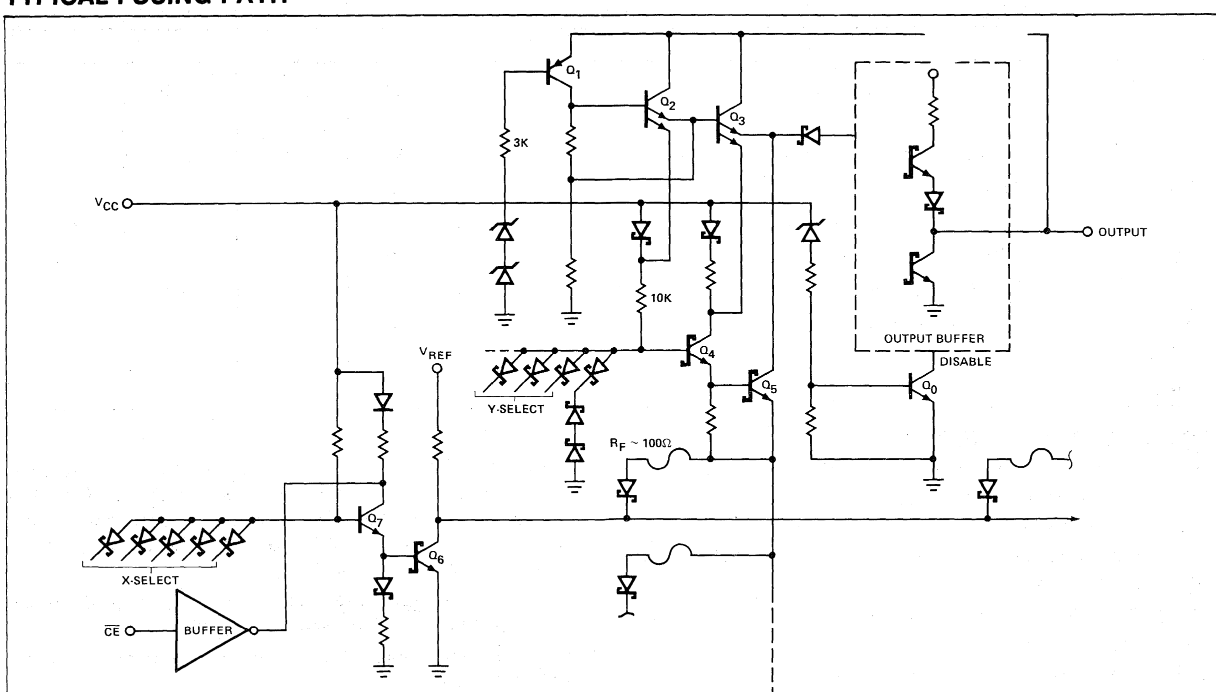
BLOCK DIAGRAM



PIN CONFIGURATION



TYPICAL FUSING PATH



AC ELECTRICAL CHARACTERISTICS

S82S126/129 $-55°C \leq T_A \leq +125°C$, $4.5V \leq V_{CC} \leq 5.5V$
N82S126/129 $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

PARAMETER		TEST CONDITIONS	S82S126/129			N82S126/129			UNIT
			MIN	TYP2	MAX	MIN	TYP2	MAX	
Propagation Delay									
T_{AA}	Address to Output	$C_L = 30pF$		35	70		35	50	ns
T_{CD}	Chip Disable to Output	$R_1 = 270\Omega$		15	35		15	20	ns
T_{CE}	Chip Enable to Output	$R_2 = 600\Omega$		15	35		15	20	ns

NOTES:
1. Positive current is defined as into the terminal referenced.
2. Typical values are at $V_{CC} = 5.0V$, $T_A = +25°C$.

PROGRAMMING SPECIFICATIONS (Testing of these limits may cause programming of device.) $T_A = +25°C$

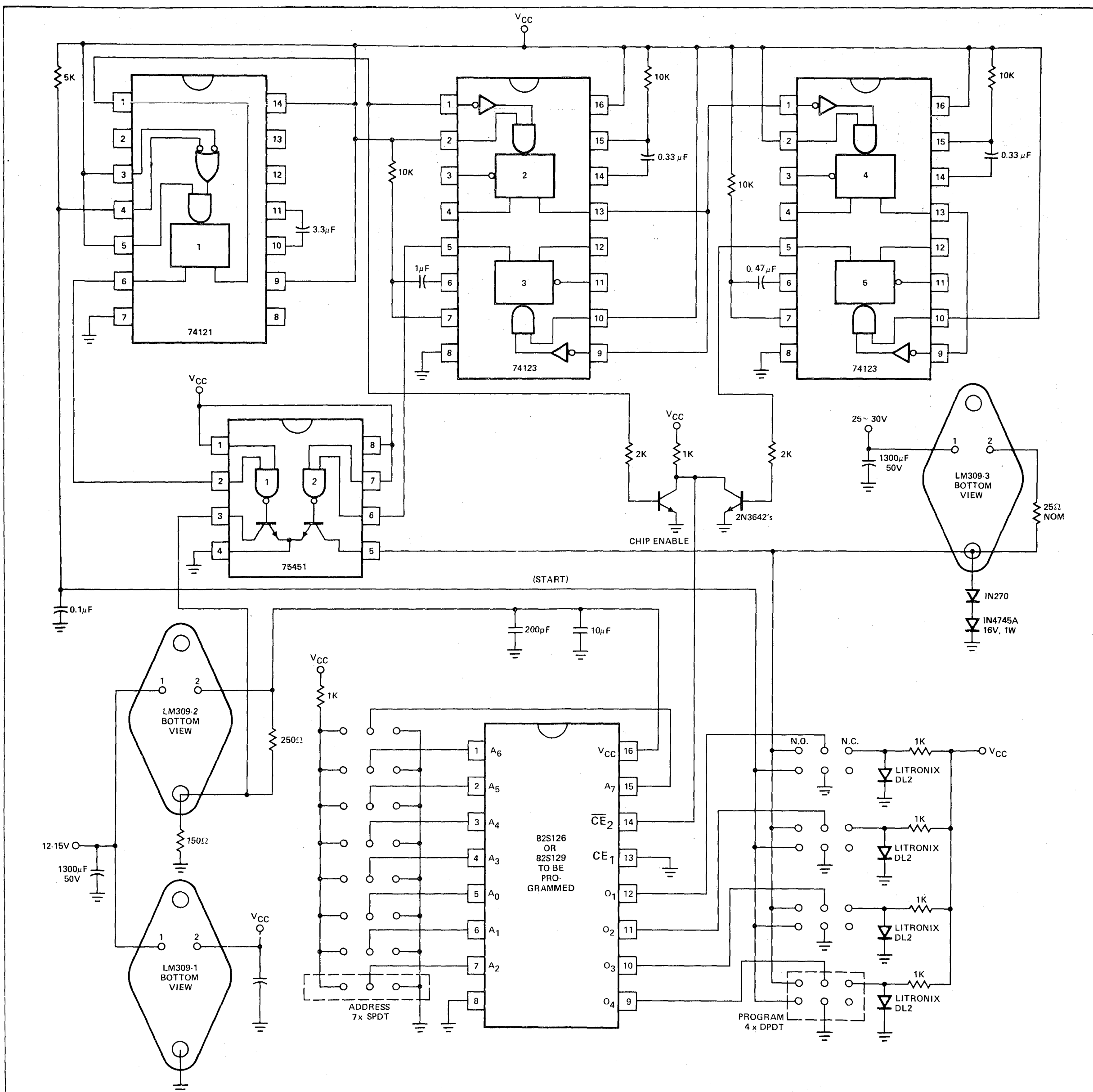
PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
Power Supply Voltage						
V_{CCP} [1]	To Program	$I_{CCP} = 350 \pm 50mA$ (Transient or steady state)	8.5	8.75	9.0	V
V_{CCH}	Upper Verify Limit		5.3	5.5	5.7	V
V_{CCL}	Lower Verify Limit		4.3	4.5	4.7	V
V_S [3]	Verify Threshold		0.9	1.0	1.1	V
I_{CCP}	Programming Supply Current	$V_{CCP} = +8.75 \pm .25V$	300	350	400	mA
Input Voltage						
V_{IH}	Logical "1"		2.4		5.5	V
V_{IL}	Logical "O"		0	0.4	0.8	V
Input Current						
I_{IH}	Logical "1"	$V_{IH} = +5.5V$			50	μA
I_{IL}	Logical "O"	$V_{IL} = +0.4V$			-500	μA
V_{OUT} [2]	Output Programming Voltage	$I_{OUT} = 200 \pm 20mA$ (Transient or steady state)	16.0	17.0	18.0	V
I_{OUT}	Output Programming Current	$V_{OUT} = +17 \pm 1V$	180	200	220	mA
T_R	Output Pulse Rise Time		10		50	μs
t_p	$\overline{CE}$ Programming Pulse Width		1		2	ms
t_D	Pulse Sequence Delay		10			μs
T_{PR}	Programming Time	$V_{CC} = V_{CCP}$			2.5	sec
T_{PS}	Programming Pause	$V_{CC} = 0V$	5			sec
$\frac{T_{PR}}{T_{PR} + T_{PS}}$ [4]	Programming Duty Cycle				33	%

PROGRAMMING PROCEDURE

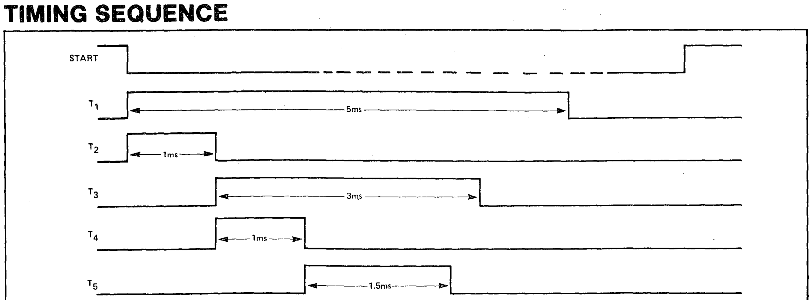
1. Terminate all device outputs with a 10KΩ resistor to V_{CC}.
2. Select the Address to be programmed, and raise V_{CC} to $V_{CCP} = 8.75 \pm .25V$.
3. After 10μs delay, apply $V_{OUT} = +17 \pm 1V$ to the output to be programmed. Program one output at the time.
4. After 10μs delay, pulse both $\overline{CE}$ inputs to logic "O" for 1 to 2 ms.
5. After 10μs delay, remove +17V from the programmed output.
6. To verify programming, after 10μs delay, lower V_{CC} to $V_{CCH} = +5.5 \pm .2V$, and apply a logic "0" level to both $\overline{CE}$ inputs. The programmed output should remain in the "1" state. Again, lower V_{CC} to $V_{CCL} = +4.5 \pm .2V$, and verify that the programmed output remains in the "1" state.
7. Raise V_{CC} to $V_{CCP} = 8.75 \pm .25V$, and repeat steps 3 through 6 to program other bits at the same address.
8. After 10μs delay, repeat steps 2 through 7 to program all other address locations.

NOTES:
1. Bypass V_{CC} to GND with a 0.01μF capacitor to reduce voltage spikes.
2. Care should be taken to insure the 17 ± 1V output voltage is maintained during the entire fusing cycle. The recommended supply is a constant current source clamped at the specified voltage limit.
3. V_S is the sensing threshold of the PROM output voltage for a programmed bit. It normally constitutes the reference voltage applied to a comparator circuit to verify a successful fusing attempt.
4. Continuous fusing for an unlimited time is also allowed, provided that a 33% duty cycle is maintained. This may be accomplished by following each Program Verify cycle with a Rest period (VCC = 0V) of 4ms.

MANUAL PROGRAMMER



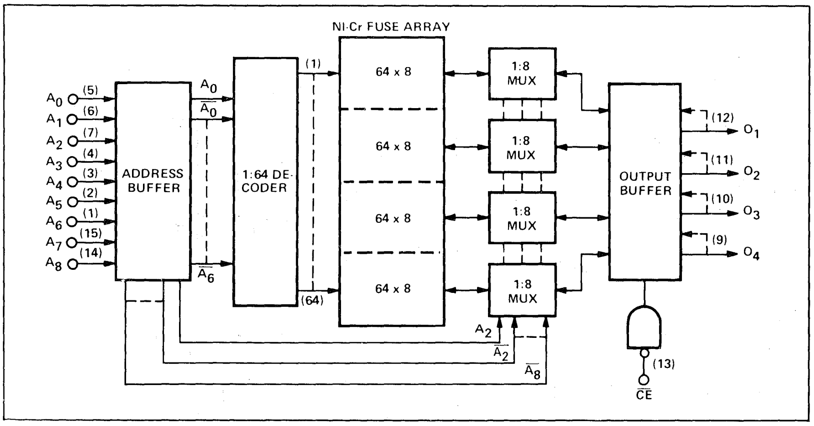
TIMING SEQUENCE



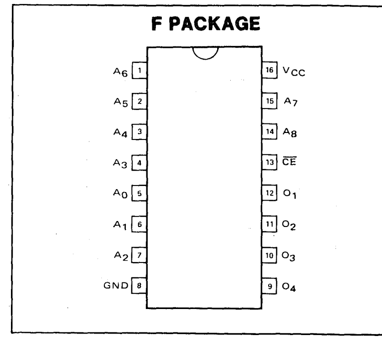
MEMORIES

N82S130-F • S82S130-F

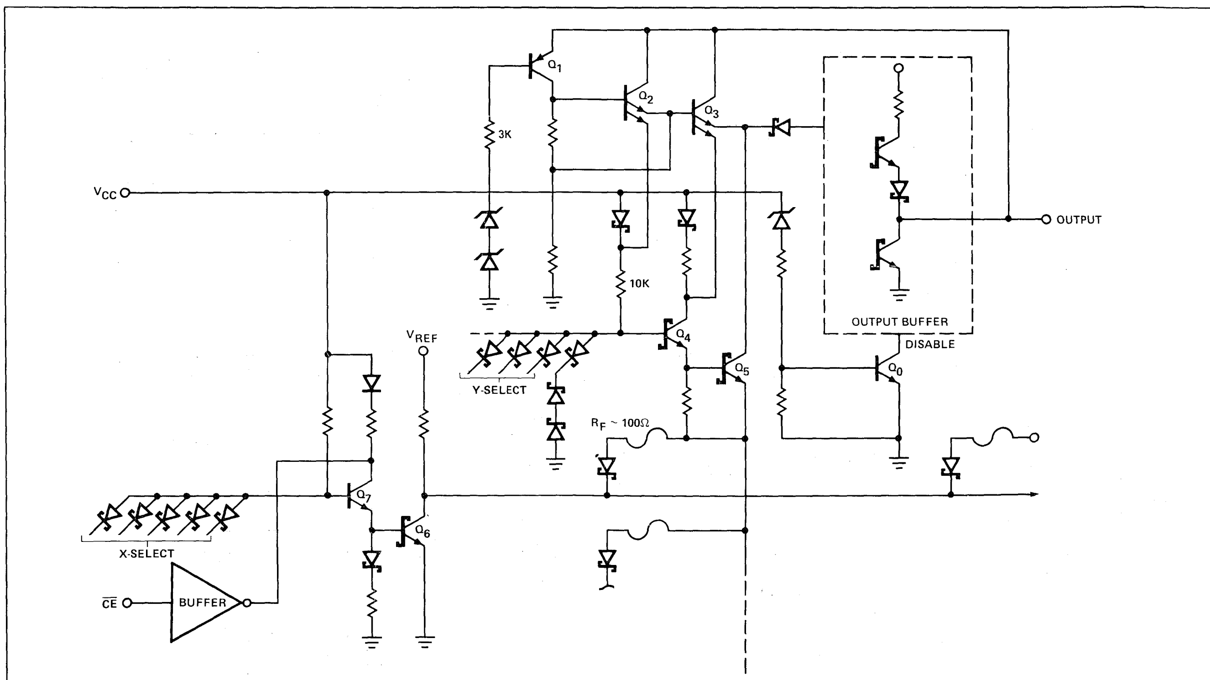
BLOCK DIAGRAM



PIN CONFIGURATION



TYPICAL FUSING PATH



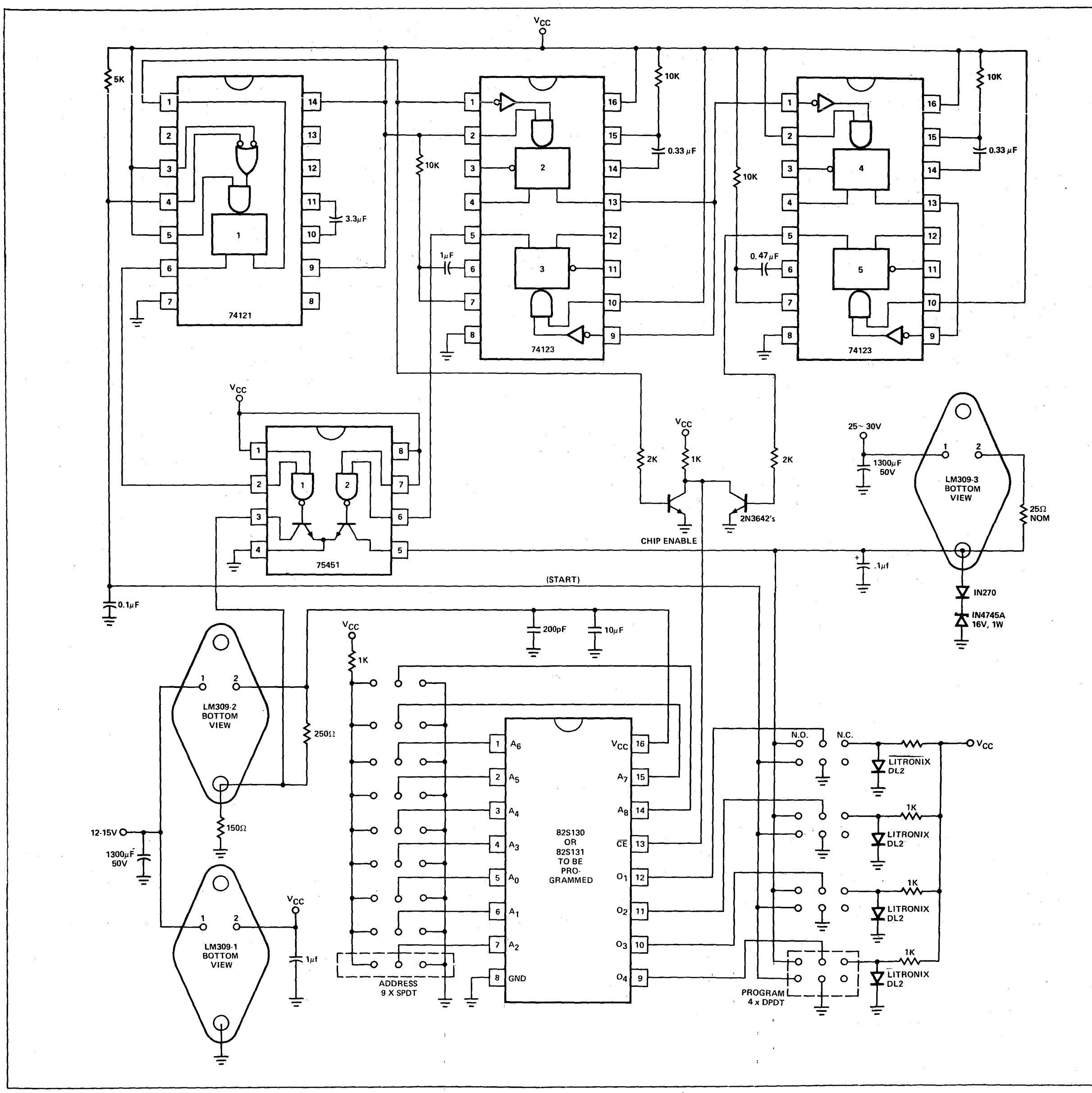
AC ELECTRICAL CHARACTERISTICS

S82S130/131 $-55°C \leq T_A \leq +125°C$, $4.5 \leq V_{CC} \leq 5.5V$
N82S130/131 $0°C \leq T_A \leq +75°C$, $4.75 \leq V_{CC} \leq 5.25V$

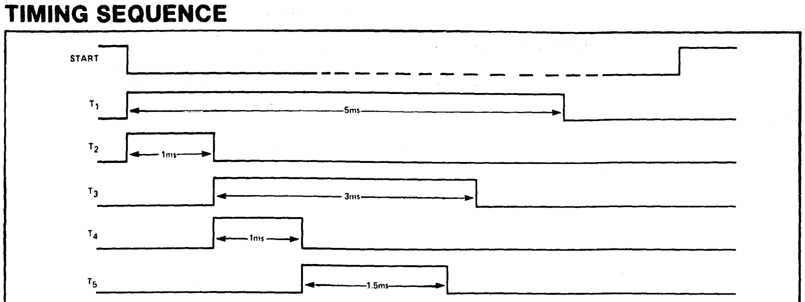
PARAMETER		TEST CONDITIONS1	S82S130/131			N82S130/131			UNIT
			MIN	TYP2	MAX	MIN	TYP2	MAX	
Propagation Delay									
T_{AA}	Address to Output	$C_L = 30pF$		40	70		40	50	ns
T_{CD}	Chip Disable to Output	$R_1 = 270\Omega$		20	30		20	30	ns
T_{CE}	Chip Enable to Output	$R_2 = 600\Omega$		20	30		20	30	ns

NOTES:
1. Positive current is defined as into the terminal referenced.
2. Typical values are at $V_{CC} = 5.0V$, $T_A = +25°C$.

MANUAL PROGRAMMER



TIMING SEQUENCE



MEMORIES

N82S130-F • S82S130-F

PROGRAMMING SPECIFICATIONS (Testing of these limits may cause programming of device.) $T_A = +25°C$

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
Power Supply Voltage						
V_{CCP}[1]	To Program	$I_{CCP} = 350 \pm 50mA$ (Transient or steady state)	8.5	8.75	9.0	V
V_{CCH}	Upper Verify Limit		5.3	5.5	5.7	V
V_{CCL}	Lower Verify Limit		4.3	4.5	4.7	V
V_S[3]	Verify Threshold		0.9	1.0	1.1	V
I_{CCP}	Programming Supply Current	$V_{CCP} = +8.75 \pm .25V$	300	350	400	mA
Input Voltage						
V_{IH}	Logical "1"		2.4		5.5	V
V_{IL}	Logical "0"		0	0.4	0.8	V
Input Current						
I_{IH}	Logical "1"	$V_{IH} = +5.5V$			50	µA
I_{IL}	Logical "0"	$V_{IL} = +0.4V$			-500	µA
V_{OUT}[2]	Output Programming Voltage	$I_{OUT} = 200 \pm 20mA$ (Transient or steady state)	16.0	17.0	18.0	V
I_{OUT}	Output Programming Current	$V_{OUT} = +17 \pm 1V$	180	200	220	mA
T_R	Output Pulse Rise Time		10		50	µs
t_P	$\overline{CE}$ Programming Pulse Width		1		2	ms
t_D	Pulse Sequence Delay		10			µs
T_{PR}[5]	Programming Time	$V_{CC} = V_{CCP}$			2.5	sec
T_{PS}	Programming Pause	$V_{CC} = 0V$	5			sec
$\frac{T_{PR}}{T_{PR}+T_{PS}}$[4]	Programming Duty Cycle				33	%

PROGRAMMING PROCEDURE

1. Terminate all device outputs with a 10kΩ resistor to V_{CC}.
2. Select the Address to be programmed, and raise V_{CC} to $V_{CCP} = 8.75 \pm .25V$.
3. After 10µs delay, apply $V_{OUT} = + 17 \pm 1V$ to the output to be programmed. Program one output at the time.
4. After 10µs delay, pulse the $\overline{CE}$ input to logic "0" for 1 to 2 ms.
5. After 10µs delay, remove +17V from the programmed output.
6. To verify programming, after 10µs delay, lower V_{CC} to $V_{CCH} = +5.5 \pm .2V$, and apply a logic "0" level to the $\overline{CE}$ input. The programmed output should remain in the "1" state. Again, lower V_{CC} to $V_{CCL} = +4.5 \pm .2V$, and verify that the programmed output remains in the "1" state.
7. Raise V_{CC} to $V_{CCP} = 8.75 \pm .25V$, and repeat steps 3 through 6 to program other bits at the same address.
8. After 10µs delay, repeat steps 2 through 7 to program all other address locations.

NOTES:
1. Bypass V_{CC} to GND with a 0.01µF capacitor to reduce voltage spikes.
2. Care should be taken to insure the +17 ± 1V output voltage is maintained during the entire fusing cycle. The recommended supply is a constant current source clamped at the specified voltage limit.
3. V_S is the sensing threshold of the PROM output voltage for a programmed bit. It normally constitutes the reference voltage applied to a comparator circuit to verify a successful fusing attempt.
4. Continuous fusing for an unlimited time is also allowed, provided that a 33% duty cycle is maintained. This may be accomplished by following each Program-Verify cycle with a Rest period (V_{CC} = OV) of 4ms.
5. On the first programming attempt (from cold start) a maximum limit of 5 sec. is allowed. In most cases, depending on the truth table, this will decrease total programming time.

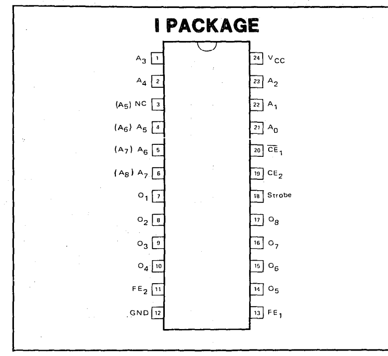
DESCRIPTION

The 82S114 and 82S115 are fully TTL compatible, and include on-chip decoding and two chip enable inputs for ease of memory expansion. They feature Tri-State outputs for optimization of word expansion in bussed organizations. A D-type latch is used to enable the Tri-State output drivers. In the TRANSPARENT READ mode, stored data is addressed by applying a binary code to the address inputs while holding STROBE high. In this mode the bit drivers will be controlled solely by $\overline{CE}1$ and CE2 lines.

In the LATCHED READ mode, outputs are held in their previous state (1, 0, or High-Z) as long as STROBE is low, regardless of the state of address or chip enable. A positive STROBE transition causes data from the applied address to reach the outputs if the chip is enabled, and causes outputs to go to the High-Z state if the chip is disabled.

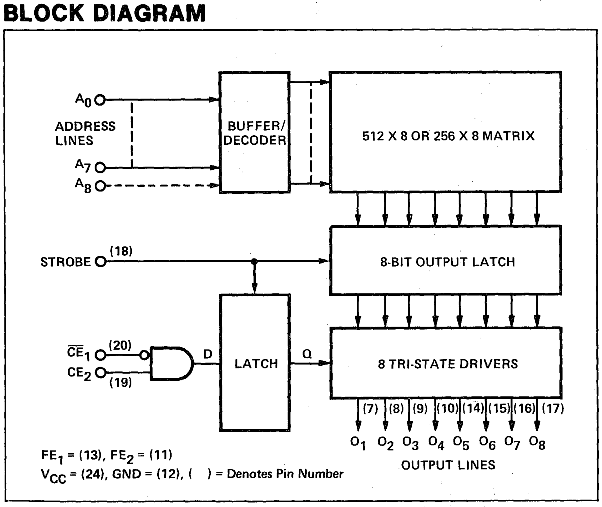
A negative STROBE transition causes outputs to be locked into their last Read Data condition if the chip was enabled, or causes outputs to be locked into the High-Z condition if the chip was disabled.

PIN CONFIGURATION



( ) 82S115 PIN CONNECTION

BLOCK DIAGRAM

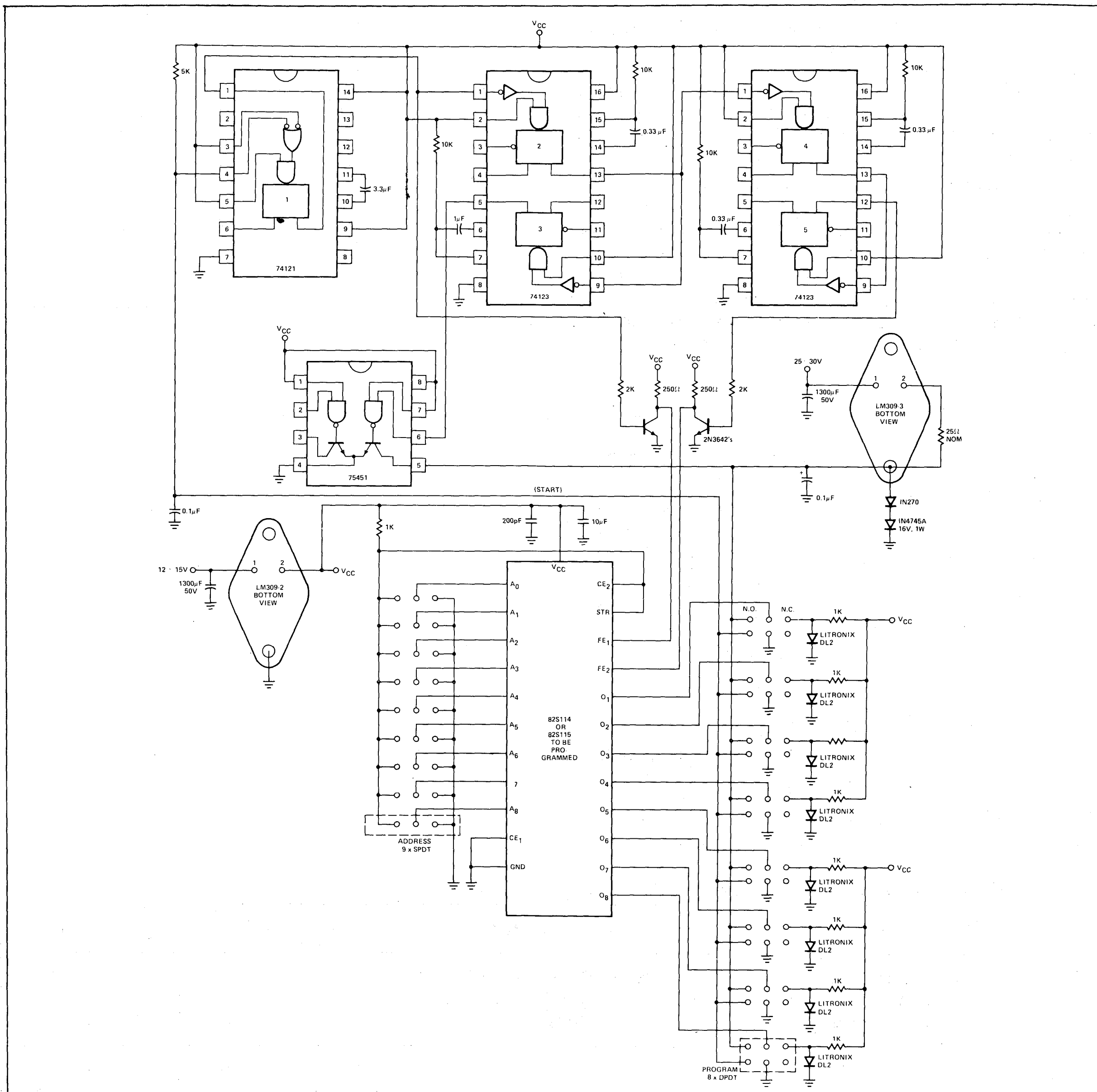


AC ELECTRICAL CHARACTERISTICS $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

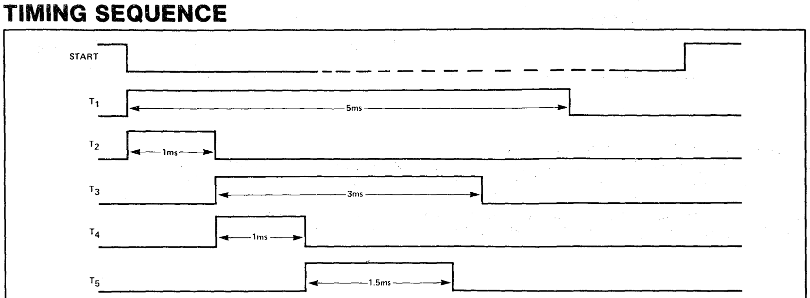
PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP[2]	MAX	
T_{AA}	Address Access Time	LATCHED or TRANSPARENT READ		35	60	ns
T_{CE}	Chip Enable Access Time	$R_1 = 270\Omega$, $R_2 = 600\Omega$, $C_L = 30pF$		20	40	ns
T_{CD}	Chip Disable Time	(Note 4)		20	40	ns
T_{ADH}	Address Hold Time		0	−10		ns
T_{CDH}	Chip Enable Hold Time		10	0		ns
T_{SW}	Strobe Pulse Width	LATCHED READ ONLY	30	20		ns
T_{SL}	Strobe Latch Time	$R_1 = 270\Omega$, $R_2 = 600\Omega$, $C_L = 30pF$	60	35		ns
T_{DL}	Strobe Delatch Time	(Note 5)			30	ns
T_{CDS}	Chip Enable Set-up Time		40			ns

NOTES:
1. Positive current is defined as into the terminal referenced.
2. Typical values are at $V_{CC} = +5.0V$ and $T_A = +25°C$.
3. No more than one output should be grounded at the same time and strobe should be disabled. Strobe is in "1" state.
4. If the strobe is high, the device functions in a manner identical to conventional bipolar ROMs. The timing diagram shows valid data will appear TA nanoseconds after the address has changed and T_{CE} nanoseconds after the output circuit is enabled. T_{CD} is the time required to disable the output and switch it to an "off" or high impedance state after it has been enabled.
5. In Latched Read Mode data from any selected address will be held on the output when strobe is lowered. Only when strobe is raised will new location data be transferred and chip enable conditions be stored. The new data will appear on the outputs if the chip enable conditions enable the outputs.

82S114/115 MANUAL PROGRAMMER



TIMING SEQUENCE



PROGRAMMING SPECIFICATIONS (Testing of these limits may cause programming of device.) $T_A = +25°C$

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
Power Supply Voltage						
V_{CCP}[1]	To Program	$I_{CCP} = 200 \pm 25$ mA (Transient or steady state)	4.75	5.0	5.25	V
V_{CCH}	Upper Verify Limit		5.3	5.5	5.7	V
V_{CCL}	Lower Verify Limit		4.3	4.5	4.7	V
V_S[3]	Verify Threshold		0.9	1.0	1.1	V
I_{CCP}	Programming Supply Current	$V_{CCP} = +5.0 \pm .25V$	175	200	225	mA
Input Voltage						
V_{IL}	Low Level Input Voltage		0	0.4	0.8	V
V_{IH}	High Level Input Voltage		2.4		5.5	V
Input Current (FE_1 & FE_2 Only)						
I_{IL}	Low Level Input Current	$V_{IL} = +0.45V$			-100	μA
I_{IH}	High Level Input Current	$V_{IH} = +5.5V$			10	mA
Input Current (Except FE_1 & FE_2)						
I_{IL}	Low Level Input Current	$V_{IL} = +0.45V$			-100	μA
I_{IH}	High Level Input Current	$V_{IH} = +5.5V$			25	μA
V_{OUT}[2]	Output Programming Voltage	$I_{OUT} = 200 \pm 20$ mA (Transient or steady state)	16.0	17.0	18.0	V
I_{OUT}	Output Programming Current	$V_{OUT} = +17 \pm 1V$	180	200	220	mA
T_R	Output Pulse Rise Time		10		50	μs
t_P	FE_2 Programming Pulse Width		1		1.5	ms
t_D	Pulse Sequence Delay		10			μs
T_{PR}	Programming Time	$V_{CC} = V_{CCP}$			10	sec
T_{PS}	Programming Pause	$V_{CC} = 0V$	7			sec
$\frac{T_{PR}}{T_{PR} + T_{PS}}$[4]	Programming Duty Cycle				60	%

RECOMMENDED PROGRAMMING PROCEDURE

The 82S114/115 are shipped with all bits at logical "0" (low). To write logical "1", proceed as follows:

SET-UP

a. Apply GND to pin 12.

b. Terminate all device outputs with a 10KΩ resistor to V_{CC}.

c. Set $\overline{CE}1$ to logic "0", and CE2 to logic "1" (TTL levels).

d. Set Strobe to logic "1" level.

PROGRAM-VERIFY SEQUENCE

Step 1 Raise V_{CC} to V_{CCP}, and address the word to be programmed by applying TTL "1" and "0" logic levels to the device address inputs.

Step 2 After 10 μs delay, apply to FE1 (pin 13) a voltage source of $+5.0 \pm 0.5V$, with 10 mA sourcing current capability.

Step 3 After 10μs delay, apply a voltage source of $+17.0 \pm 1.0V$ to the output to be programmed. The source must have a current limit of 200 mA. Program one output at the time.

Step 4 After 10μs delay, raise FE2 (pin 11) from 0V to $+5.0 \pm 0.5V$ for a period of 1ms, and then return to 0V. Pulse source must have a 10 mA sourcing current capability.

Step 5 After 10μs delay, remove +17.0V supply from programmed output.

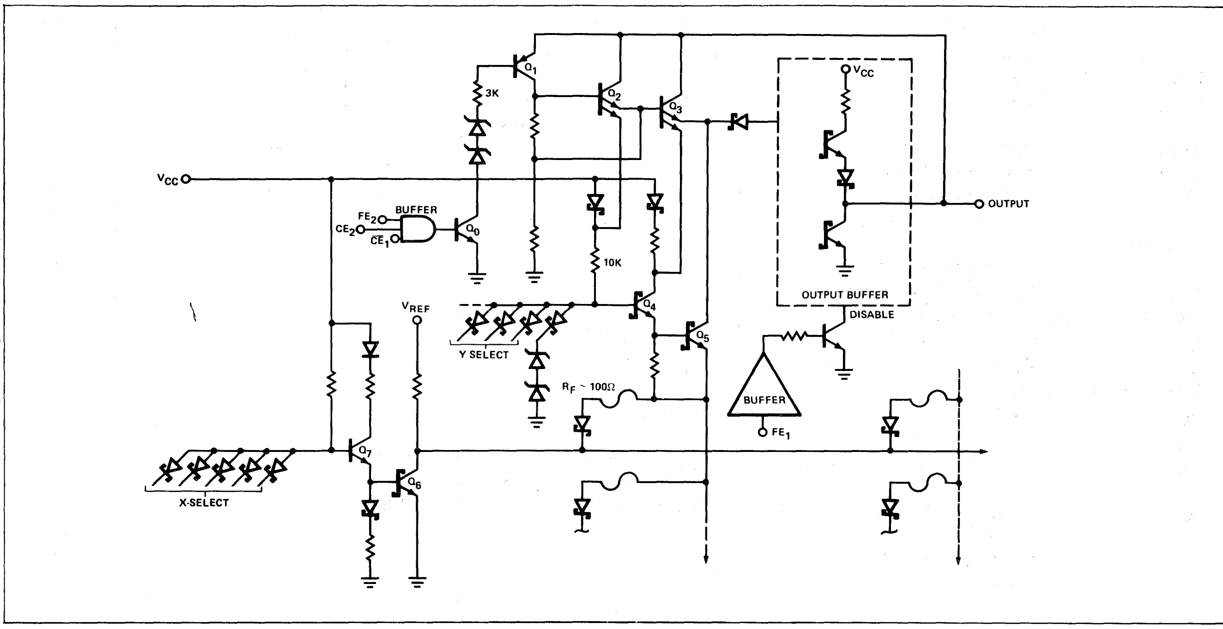
Step 6 To verify programming, after 10μs delay, return FE1 to 0V. Raise V_{CC} to $V_{CCH} = +5.5 \pm .2V$. The programmed output should remain in the "1" state. Again, lower V_{CC} to $V_{CCL} = +4.5 \pm .2V$, and verify that the programmed output remains in the "1" state.

Step 7 Raise V_{CC} to V_{CCP}, and repeat steps 2 through 6 to program other bits at the same address.

Step 8 Repeat steps 1 through 7 to program all other address locations.

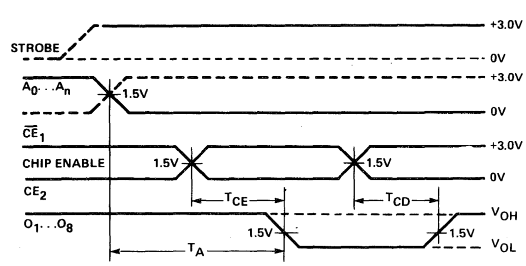
NOTES:
1. Bypass V_{CC} to GND with a 0.01 μF capacitor to reduce voltage spikes.
2. Care should be taken to insure the $17 \pm 1V$ output voltage is maintained during the entire fusing cycle. The recommended supply is a constant current source clamped at the specified voltage limit.
3. V_S is the sensing threshold of the PROM output voltage for a programmed bit. It normally constitutes the reference voltage applied to a comparator circuit to verify a successful fusing attempt.
4. Continuous fusing for an unlimited time is also allowed, provided that a 60% duty cycle is maintained. This may be accomplished by following each Program Verify cycle with a Rest period (V_{CC} = 0V) of 3 mS.

TYPICAL FUSING PATH

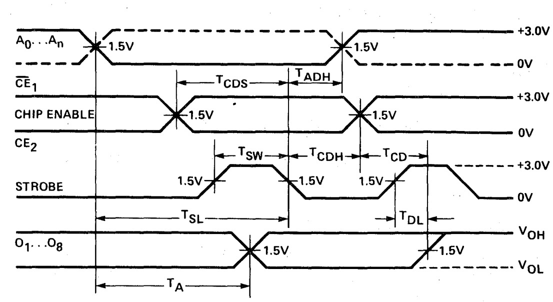


AC WAVEFORMS

TRANSPARENT READ[1]
(Output Latches Not Used)

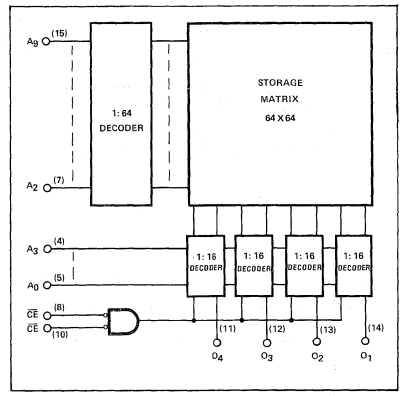


LATCHED READ[2]
(Output Latches Used)

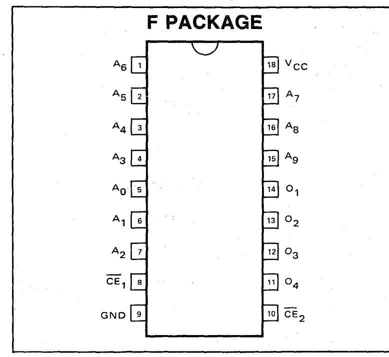


N82S136-F • N82S137-F
S82S136-F • S82S137-F

BLOCK DIAGRAM



PIN CONFIGURATION



AC ELECTRICAL CHARACTERISTICS

S82S136/137 $-55°C \leq T_A \leq +125°C$, $4.5 \leq V_{CC} \leq 5.5V$
N82S136/137 $0°C \leq T_A \leq +75°C$, $4.75 \leq V_{CC} \leq 5.25V$

PARAMETER		TEST CONDITIONS[1]	S82S136/137			N82S136/137			UNIT
			MIN	TYP[2]	MAX	MIN	TYP[2]	MAX	
Propagation Delay									
T_{AA}	Address to Output	$C_L = 30pF$		40	80		40	60	ns
T_{CD}	Chip Disable to Output	$R_1 = 270\Omega$		20	40		20	30	ns
T_{CE}	Chip Enable to Output	$R_2 = 600\Omega$		20	40		20	30	ns

S82S136/N82S136-F
S82S137/N82S137-F

PROGRAMMING SPECIFICATIONS (Testing of these limits may cause programming of device.) $T_A = +25°C$

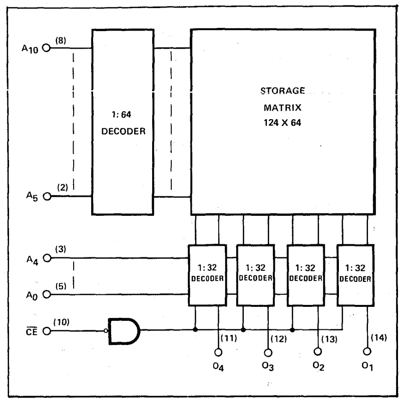
PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
Power Supply Voltage						
V_{CCP}[1]	To Program	$I_{CCP} = 350 \pm 50mA$ (Transient or steady state)	8.5	8.75	9.0	V
V_{CCH}	Upper Verify Limit		5.3	5.5	5.7	V
V_{CCL}	Lower Verify Limit		4.3	4.5	4.7	V
V_S[3]	Verify Threshold		0.9	1.0	1.1	V
I_{CCP}	Programming Supply Current	$V_{CCP} = +8.75 \pm .25V$	300	350	400	mA
Input Voltage						
V_{IH}	Logical "1"		2.4		5.5	V
V_{IL}	Logical "0"		0	0.4	0.8	V
Input Current						
I_{IH}	Logical "1"	$V_{IH} = +5.5V$			50	μA
I_{IL}	Logical "0"	$V_{IL} = +0.4V$			-500	μA
V_{OUT}[2]	Output Programming Voltage	$I_{OUT} = 200 \pm 20mA$ (Transient or steady state)	16.0	17.0	18.0	V
I_{OUT}	Output Programming Current	$V_{OUT} = +17 \pm 1V$	180	200	220	mA
T_R	Output Pulse Rise Time		10		50	μs
t_P	$\overline{CE}$ Programming Pulse Width		1		2	ms
t_D	Pulse Sequence Delay		10			μs
T_{PR}[5]	Programming Time	$V_{CC} = V_{CCP}$			2.5	sec
T_{PS}	Programming Pause	$V_{CC} = 0V$	5			sec
$\frac{T_{PR}}{T_{PR}+T_{PS}}$[4]	Programming Duty Cycle				33	%

PROGRAMMING PROCEDURE

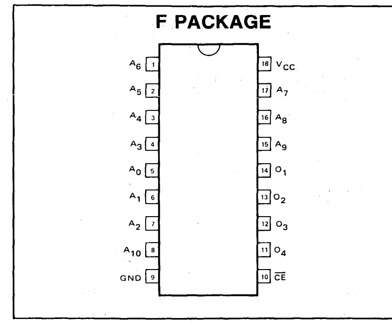
1. Terminate all device outputs with a 10kΩ resistor to V_{CC}.
2. Select the Address to be programmed, and raise V_{CC} to $V_{CCP} = 8.75 \pm .25V$.
3. After 10μs delay, apply $V_{OUT} = +17 \pm 1V$ to the output to be programmed. Program one output at the time.
4. After 10μs delay, pulse the $\overline{CE}$ input to logic "0" for 1 to 2 ms.
5. After 10μs delay, remove +17V from the programmed output.
6. To verify programming, after 10μs delay, lower V_{CC} to $V_{CCH} = +5.5 \pm .2V$, and apply a logic "0" level to the $\overline{CE}$ input. The programmed output should remain in the "1" state. Again, lower V_{CC} to $V_{CCL} = +4.5 \pm .2V$, and verify that the programmed output remains in the "1" state.
7. Raise V_{CC} to $V_{CCP} = 8.75 \pm .25V$ and repeat steps 3 through 6 to program other bits at the same address.
8. After 10μs delay, repeat steps 2 through 7 to program all other address locations.

NOTES:
1. Bypass V_{CC} to GND with a 0.01μF capacitor to reduce voltage spikes.
2. Care should be taken to insure the +17 ± 1V output voltage is maintained during the entire fusing cycle. The recommended supply is a constant current source clamped at the specified voltage limit.
3. V_S is the sensing threshold of the PROM output voltage for a programmed bit. It normally constitutes the reference voltage applied to a comparator circuit to verify a successful fusing attempt.
4. Continuous fusing for an unlimited time is also allowed, provided that a 33% duty cycle is maintained. This may be accomplished by following each Program-Verify cycle with a Rest period (V_{CC} = OV) of 4ms.
5. On the first programming attempt (from cold start) a maximum limit of 5 sec. is allowed. In most cases, depending on the truth table, this will decrease total programming time.

S82S184/N82S184-F
S82S185/N82S185-F



PIN CONFIGURATION



AC ELECTRICAL CHARACTERISTICS

S82S184/185 $-55°C \leq T_A \leq +125°C$, $4.5 \leq V_{CC} \leq 5.5V$
N82S184/185 $0°C \leq T_A \leq +75°C$, $4.75 \leq V_{CC} \leq 5.25V$

PARAMETER		TEST CONDITIONS[1]	S82S184/185			N82S184/185			UNIT
			MIN	TYP[2]	MAX	MIN	TYP[2]	MAX	
Propagation Delay									
T_{AA}	Address to Output	$C_L = 30pF$		70	150		70	100	ns
T_{CD}	Chip Disable to Output	$R_1 = 270\Omega$		30	60		30	40	ns
T_{CE}	Chip Enable to Output	$R_2 = 600\Omega$		30	60		30	40	ns

S82S184/N82S184-F
S82S185/N82S185-F

PROGRAMMING SPECIFICATIONS (Testing of these limits may cause programming of device.) $T_A = +25°C$

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
Power Supply Voltage						
V_{CCP}[1]	To Program	$I_{CCP} = 350 \pm 50mA$ (Transient or steady state)	8.5	8.75	9.0	V
V_{CCH}	Upper Verify Limit		5.3	5.5	5.7	V
V_{CCL}	Lower Verify Limit		4.3	4.5	4.7	V
V_S[3]	Verify Threshold		0.9	1.0	1.1	V
I_{CCP}	Programming Supply Current	$V_{CCP} = +8.75 \pm .25V$	300	350	400	mA
Input Voltage						
V_{IH}	Logical "1"		2.4		5.5	V
V_{IL}	Logical "0"		0	0.4	0.8	V
Input Current						
I_{IH}	Logical "1"	$V_{IH} = +5.5V$			50	μA
I_{IL}	Logical "0"	$V_{IL} = +0.4V$			-500	μA
V_{OUT}[2]	Output Programming Voltage	$I_{OUT} = 200 \pm 20mA$ (Transient or steady state)	16.0	17.0	18.0	V
I_{OUT}	Output Programming Current	$V_{OUT} = +17 \pm 1V$	180	200	220	mA
T_R	Output Pulse Rise Time		10		50	μs
tp	$\overline{CE}$ Programming Pulse Width		1		2	ms
t_D	Pulse Sequence Delay		10			μs
T_{PR}[5]	Programming Time	$V_{CC} = V_{CCP}$			2.5	sec
T_{PS}	Programming Pause	$V_{CC} = 0V$	5			sec
$\frac{T_{PR}}{T_{PR}+T_{PS}}$[4]	Programming Duty Cycle				33	%

PROGRAMMING PROCEDURE

1. Terminate all device outputs with a 10kΩ resistor to V_{CC}.
2. Select the Address to be programmed, and raise V_{CC} to $V_{CCP} = 8.75 \pm .25V$.
3. After 10μs delay, apply $I_{OUT} = +17 \pm 1V$ to the output to be programmed. Program one output at the time.
4. After 10μs delay, pulse both $\overline{CE}$ inputs to logic "0" for 1 to 2 ms.
5. After 10μs delay, remove +17V from the programmed output.
6. To verify programming, after 10μs delay, lower V_{CC} to $V_{CCH} = +5.5 \pm .2V$, and apply a logic "0" level to the $\overline{CE}$ input. The programmed output should remain in the "1" state. Again, lower V_{CC} to $V_{CCL} = +4.5 \pm .2V$, and verify that the programmed output remains in the "1" state.
7. Raise V_{CC} to $V_{CCP} = 8.75 \pm .25V$ and repeat steps 3 through 6 to program other bits at the same address.
8. After 10μs delay, repeat steps 2 through 7 to program all other address locations.

NOTES:
1. Bypass V_{CC} to GND with a 0.01μF capacitor to reduce voltage spikes.
2. Care should be taken to insure the +17 ± 1V output voltage is maintained during the entire fusing cycle. The recommended supply is a constant current source clamped at the specified voltage limit.
3. V_S is the sensing threshold of the PROM output voltage for a programmed bit. It normally constitutes the reference voltage applied to a comparator circuit to verify a successful fusing attempt.
4. Continuous fusing for an unlimited time is also allowed, provided that a 33% duty cycle is maintained. This may be accomplished by following each Program-Verify cycle with a Rest period (V_{CC} = OV) of 4ms.
5. On the first programming attempt (from cold start) a maximum limit of 5 sec. is allowed. In most cases, depending on the truth table, this will decrease total programming time.

FPLA: Field Programmable Logic Arrays

GENERAL

Although strictly a logic element, an FPLA can also be viewed as a Conditionally Addressable Memory. In this respect, the FPLA is analogous to a small PROM of 46 words X 8 bits working storage. In contrast with PROMS however, FPLAs contain a programmable input decoder which allows "linear" selection of each device output word only when the FPLA input address matches any of the programmed combinations in the input matrix.

The potential hardware savings possible with FPLAs when applied to implement any kind of combinatorial logic function are readily apparent because storage for unused minterms is no longer required. Also, the proper logic output for all inactive minterms occurs by input "default", and Don't Care states of the input variables can be directly programmed in the input matrix. The advantage comes about because with FPLAs we have a choice to select any 48-input words (or more, as determined by Don't Care input variables) from a total available pool of 65,536 (2^{16}). This can be done at any time, in the field, by the user.

THE 82S100/82S101

The 82S100 (Tri-State Outputs) and the 82S101 (Open Collector Outputs) are Bipolar Programmable Logic Arrays, containing 48 Product terms (AND terms), and 8 Sum terms (OR terms). Each OR term controls an output function which can be programmed either true active-High (Fp), or true active-Low (Fp). The true state of each output function is activated by any logical combination of 16-input variables, or their complements, up to 48 terms. Both devices are field-programmable, which means that custom patterns are immediately available by following the fusing procedure outlined in this data sheet.

The 82S100 and 82S101 are fully TTL compatible, and include chip-enable control for expansion of input variables, and output inhibit. They feature either Open Collector or Tri-State outputs for ease of expansion of product terms and application in bus-organized systems.

APPLICATIONS

Large read only memory
Random logic
Code conversion
Peripheral controllers
Look-up and decision tables
Microprogramming
Address mapping
Character generators
Sequential controllers

ABSOLUTE MAXIMUM GUARANTEED RATNGS

PARAMETER		LIMITS MIN	MAX	UNIT
T_A	Operating Ambient Temperature			
	S82S - Military Range	−55	+125	°C
	N82S - Commercial Range	0	+75	°C
T_{STG}	Storage Temperature	−65	+150	°C
V_{IN}	Input Voltage		+5.5	Vdc
V_{OUT}	Output Voltage		+5.5	Vdc
V_{CC}	Power Supply Voltage		+7	Vdc

NOTES:
1. Stresses above thos listed under "Maximum Guaranteed Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device of these or any other condition above those indicated in the operation section of the device specifications is not implied.

THERMAL RATINGS

TEMPERATURE	MILITARY	COMMERCIAL
Maximum junction	175°C	150°C
Maximum ambient	125°C	75°C
Allowable thermal rise ambient to junction	50°C	75°C

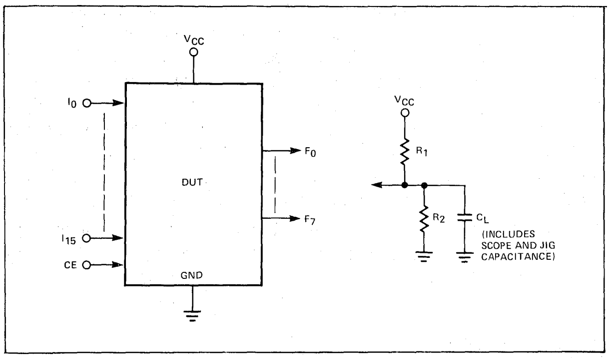
MAXIMUM ALLOWABLE POWER DISSIPATION

MATERIAL	PACKAGE	# OF PINS	θ_{JA}[1] °C/W	P_{MAX} – mW 0+125°C	0+75°C
Plastic	B	16	155	——	480
	XA	18	130	384	577
	N	24	100	500	750
	XF	28	100	500	750
Plastic[2]	BA	16	85	588	850
	XAS	18	73	685	>1000
	NA	24	75	666	1000
	XFA	28	75	666	1000
Cerdip	F	16	90	556	835
		18	90	556	835
		24	60	830	>1000
Ceramic	I	16	83	600	900
		24	50	1000	>1000
		28	50	1000	>1000

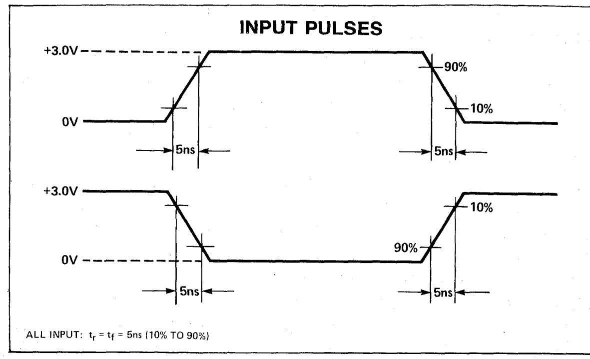
NOTES:
1. On a mounted surface, in still air.
2. Improved thermal characteristics due to built-in heat spreader.

MEMORIES

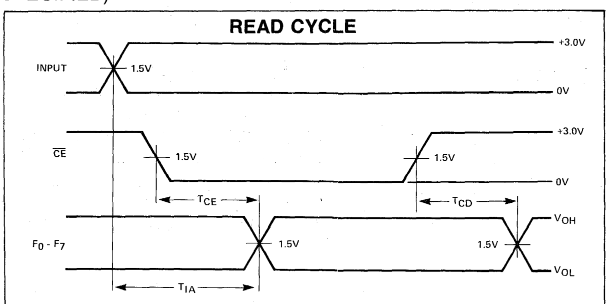
AC TEST FIGURE (UNLESS OTHERWISE SPECIFIED)



INPUT WAVEFORMS



TYPICAL AC WAVEFORMS (UNLESS OTHERWISE SPECIFIED)



Measurements: All Circuit Delays are measured at the +1.5V level of inputs and outputs.

ARRAY TIMING DEFINITIONS

T_{CE} Delay between beginning of CHIP ENABLE low (with ADDRESS valid) and when DATA OUTPUT becomes valid.

T_{CD} Delay between when CHIP ENABLE becomes high and DATA OUTPUT is in off state (Hi-Z or "1").

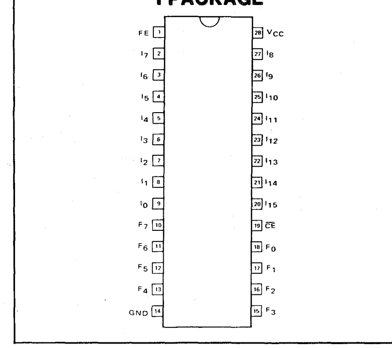
T_{IA} Delay between beginning of valid INPUT (with CHIP ENABLE low) and when DATA OUTPUT becomes valid.

SWITCHING CHARACTERISTICS

0°C ≤ T_A ≤ + 75°C, 4.75V ≤ V_{CC} ≤ 5.25V

PARAMETER	TEST CONDITIONS	LIMITS MIN	TYP2	MAX	UNIT
Propagation Delay					
T_{IA} Input to Output	C_L=30pF		35	50	ns
T_{CD} Chip Disable to Output	R_1=270		15	30	ns
T_{CE} Chip Enable to Output	R_2=600		15	30	ns

PIN CONFIGURATION



TRUTH TABLE

MODE	P_n	$\overline{CE}$	$S_r \stackrel{?}{=} f(P_n)$	F_p	F_p^*
Disabled (82S101)	X	1	X	1	1
Disabled (82S100)				Hi-Z	Hi-Z
Read	1	0	YES	1	0
	0	0		0	1
	X	0	NO	0	1

LET:

$P_n = \Pi_0^{15} (k_m I_m + j_m \overline{I_m})$; k = 0, 1, X (Don't Care)

n = 0, 1, 2,.....,47

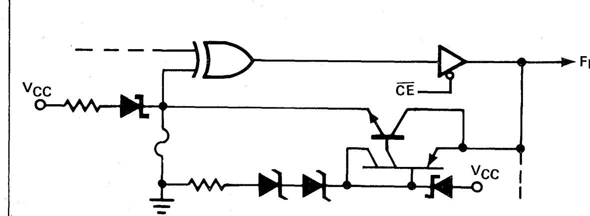
$S_r = f(\Sigma_0^{47} t_n P_n)$; r ≡ p = 0, 1, 2,....,7

where:

Unprogrammed state : $j_m = k_m = 0$; $t_n = 1$

Programmed state : $j_m = \overline{k_m}$; $t_n = 0$

OUTPUT POLARITY

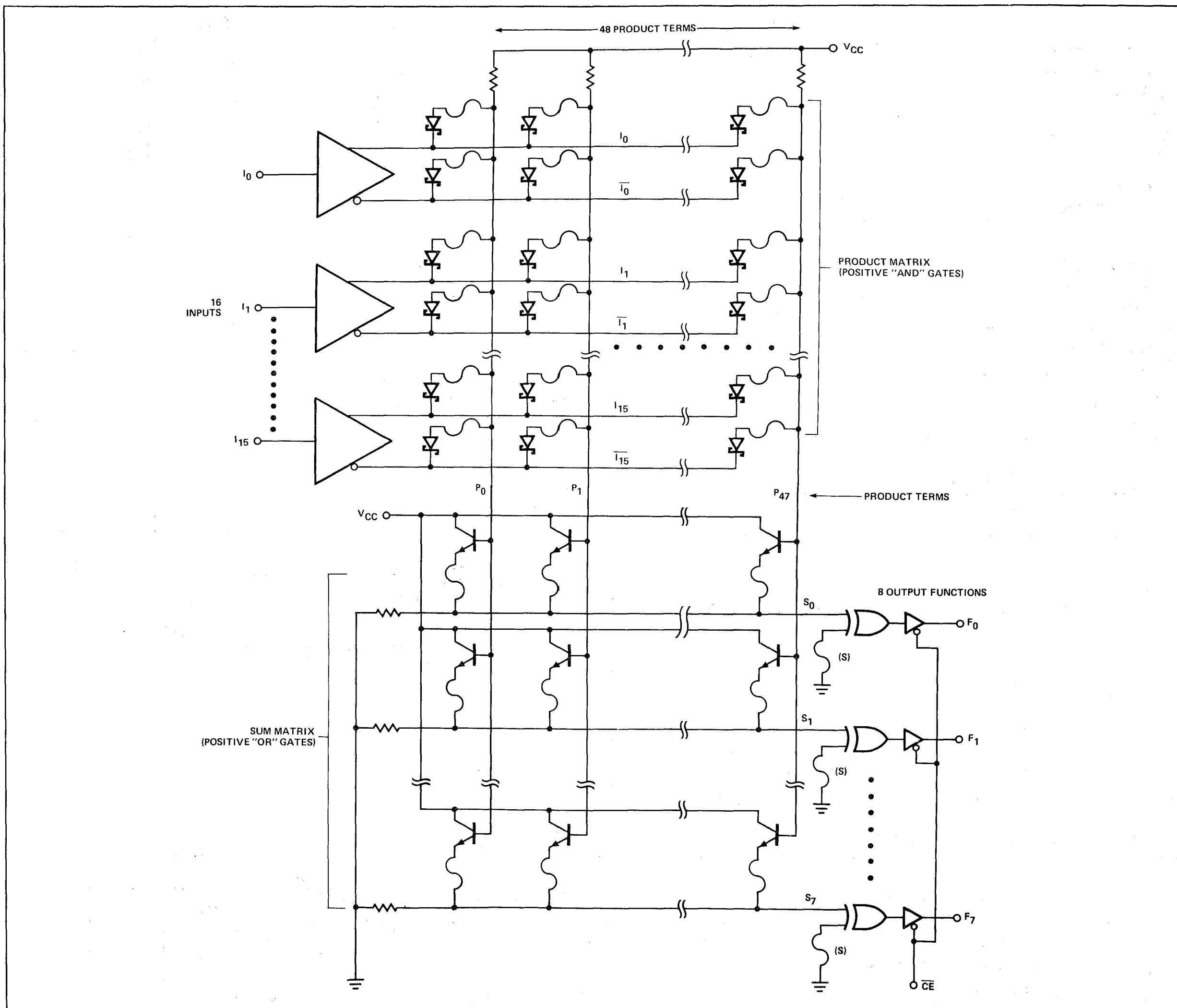


DC ELECTRICAL CHARACTERISTICS 0°C≤ T_A ≤ 75°C; 4.75 V ≤ V_{CC} ≤ 5.25V

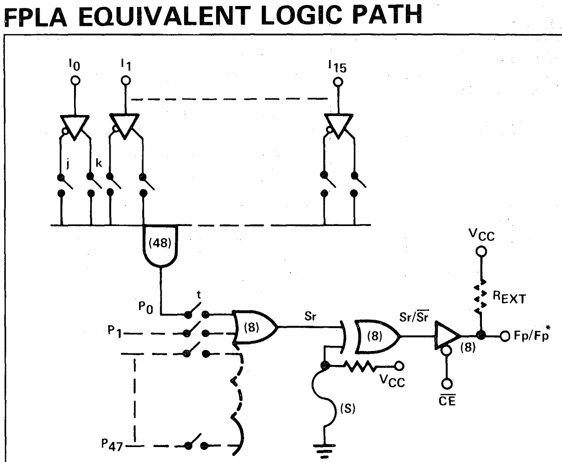
	PARAMETER[1]	TEST CONDITIONS		LIMITS MIN	TYP2	MAX	UNIT	NOTES
V_{IH}	High-Level Input Voltage	V_{CC}= 5.25V			2		V	1
V_{IL}	Low-Level Input Voltage	V_{CC}=4.75V				0.8	V	1
V_{IC}	Input Clamp Voltage	V_{CC}=4.75V, I_{IN}= − 18mA			0.8	1.2	V	1,7
V_{OH}	High-Level Output Voltage (82S100)	V_{CC}=4.75V, I_{OH}= − 2mA		2.4			V	1,5
V_{OL}	Low-Level Output Voltage	V_{CC}=4.75V, I_{OL}=9.6mA			0.35	0.45	V	1,8
I_{OLK}	Output Leakage Current (82S101)		V_{OUT}=5.25V		1	40	μA	6
$I_{O(OFF)}$	Hi-Z State Output Current (82S100)	V_{CC}=5.25V	V_{OUT}=5.25V		1	40	μA	
			V_{OUT}=0.45V		−1	−40	μA	6
I_{IH}	High-Level Input Current	V_{IN}=5.5V			<1	25	μA	
I_{IL}	Low-Level Input Current	V_{IN}=0.45V V			−10	−100	μA	
I_{OS}	Short-Circuit Output Current (82S100)	V_{CC}=5.25V, V_{OUT} = 0V		−20		−70	mA	3,7
I_{CC}	VCC Supply Current (82S100, 82S101)	V_{CC}=5.25V			120	170	mA	4
C_{IN}	Input Capacitance	V_{CC}=5.0V	V_{IN}=2.0V		5		pF	
C_O	Output Capacitance		V_{OUT}=2.0V		8		pF	6

NOTES:
1. All voltage values are with respect to network ground terminal.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Duration of short circuit should not exceed one second.
4. I_{CC} is measured with the chip enable input grounded, all other inputs at 4.5V and the outputs open.
5. Measured with V_{IL} applied to $\overline{CE}$ and a logic "1" stored.
6. Measured with V_{IH} applied to $\overline{CE}$.
7. Test each output one at the time.
8. Measured with a programmed logic condition for which the output under test is at a "0" logic level. Output sink current is supplied thru a resistor to V_{CC}.

BLOCK DIAGRAM

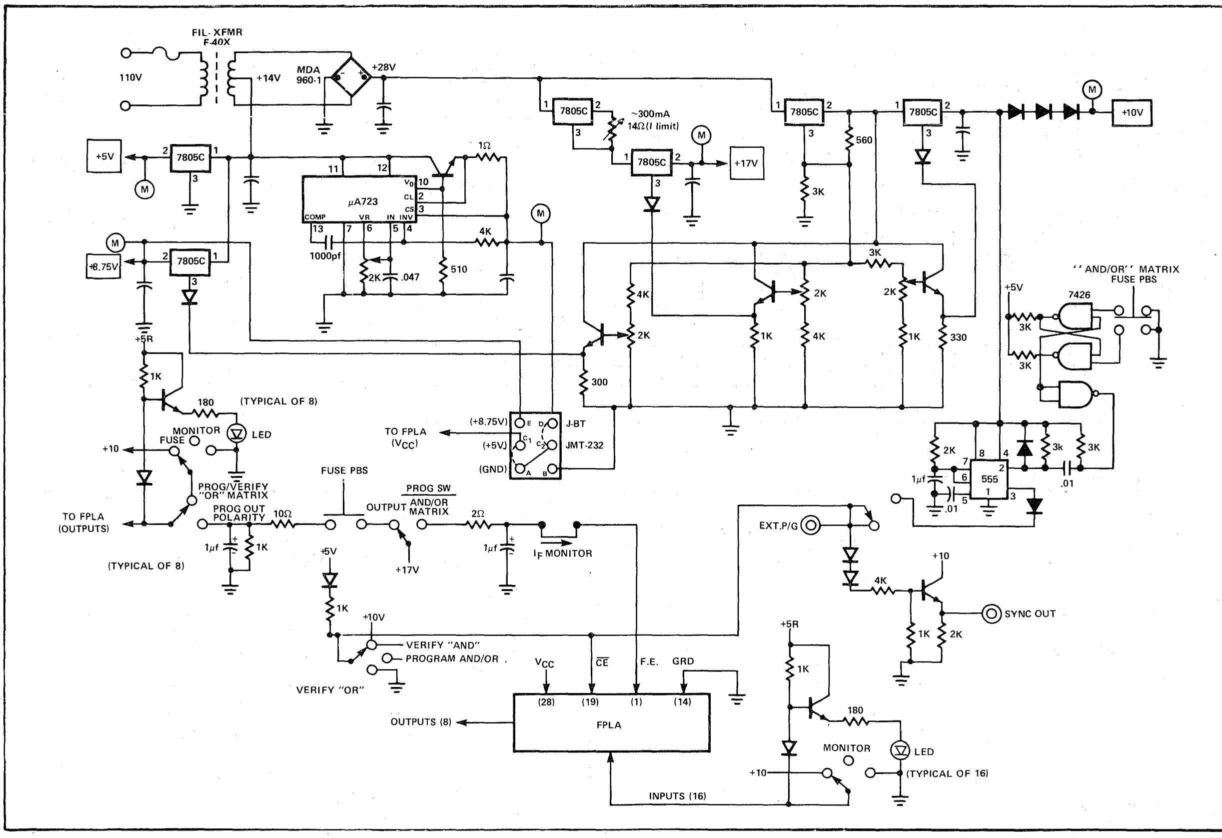


FPLA EQUIVALENT LOGIC PATH

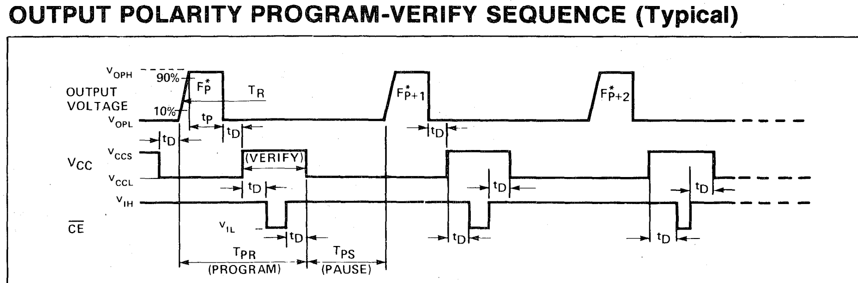


NOTE:
FOR EACH OF THE 8 OUTPUTS, EITHER THE FUNCTION Fp (ACTIVE HIGH) OR Fp* (ACTIVE LOW) IS AVAILABLE, BUT NOT BOTH. THE REQUIRED FUNCTION POLARITY IS USER PROGRAMMABLE VIA FUSE (S).

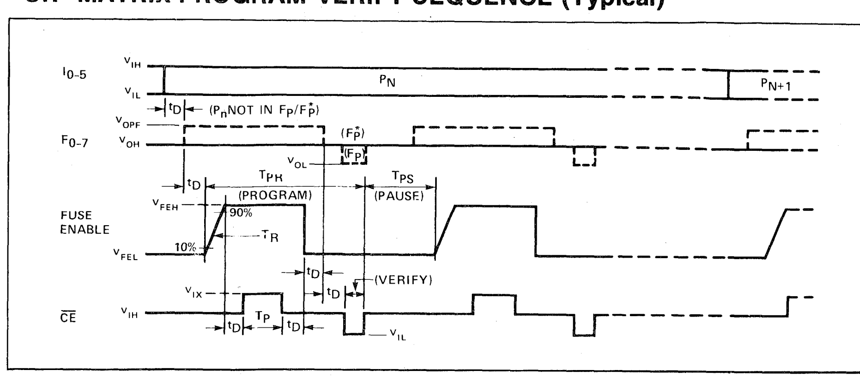
FPLA MANUAL FUSER



OUTPUT POLARITY PROGRAM-VERIFY SEQUENCE (Typical)

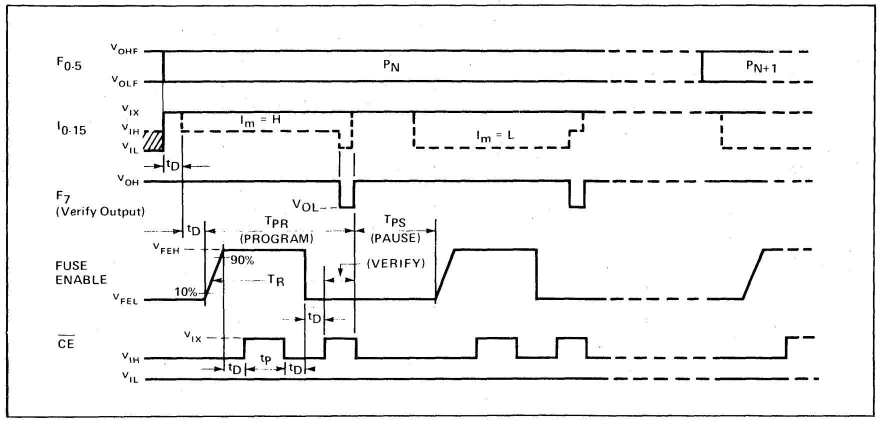


"OR" MATRIX PROGRAM-VERIFY SEQUENCE (Typical)

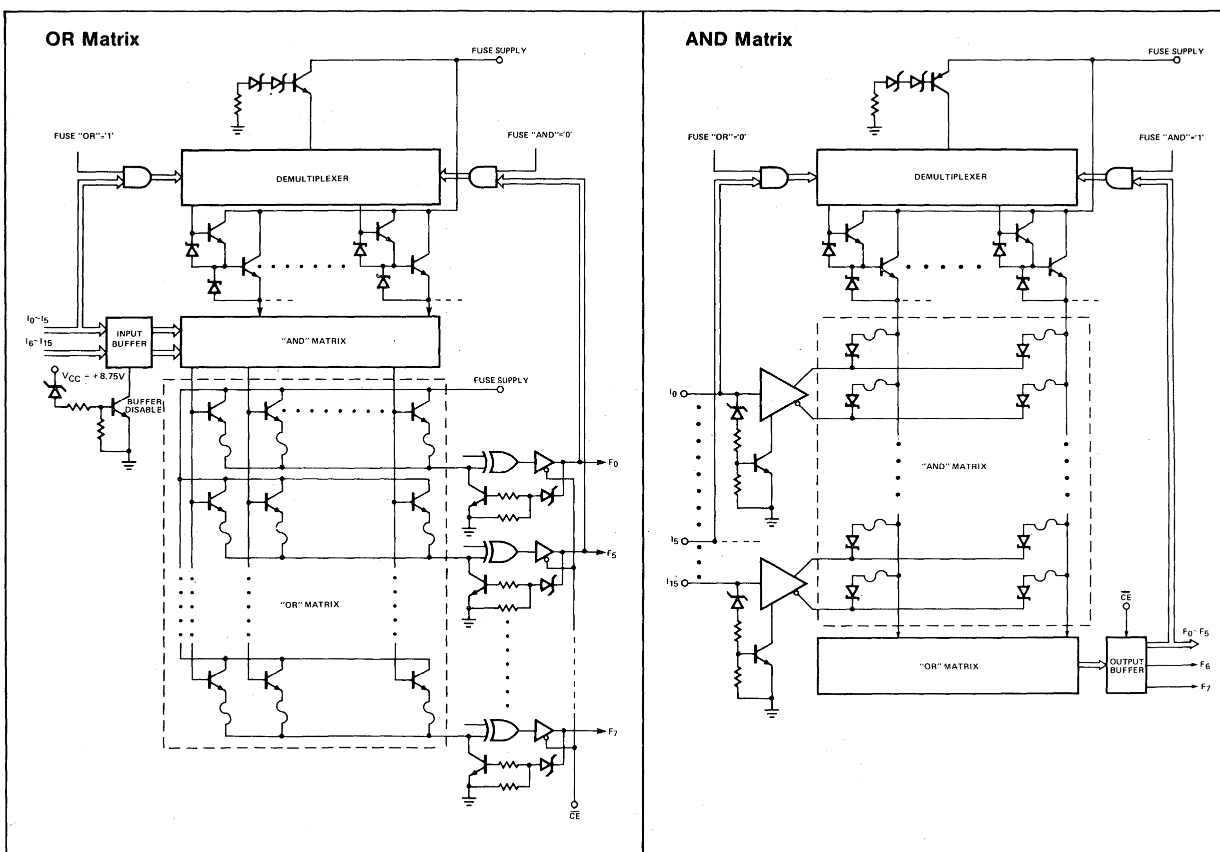


MEMORIES

"AND" MATRIX PROGRAM-VERIFY SEQUENCE (Typical)



TYPICAL FUSING PATHS



MOS SHIFT REGISTERS
AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{DD} = -5V +5%, VILC 11V (4, 5, 6, 7, 8)

	Frequency						Clock Pulse									Data											
TEST CONDITION	Clock Rep Rate (MHz) W=R=V_{CC} R_L=3K			Data Rep Rate (MHz) W=R=V_{CC}			$t_{\phi PW}$ (μs) Width F=3MHz			$t_{\phi D}$ (μs) Delay F=3MHz			t_R, t_F (ns) Transition			t_{DW} (ns) Data Write Time (setup)			t_{DH} (ns) Data to Clock Hold Time			t_{A+} (ns) Clock to Data Out Delay V_0 = V_{CC} -16V Data Out = 2.5V			t_{A-} (ns)		
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max
2506[1,2]			3		N/A		150 ns		01																		
							100 ns		02	10			10		1000	75 .								150			
2507[1,2]			3		N/A		150 ns		01	10			10		1000	75								150			
							100 ns		02																		
2517[1,2]			3		N/A		150 ns		01	10			10		1000	75								150			
							100 ns		02																		
1405	V_{ILC}=V_{CC}-14.5 To V_{CC} = 17			V_{ILC}=V_{CC}-14.5 To V_{CC} = 17			0.200		10	30					1 μs	120			20					250			250
			2			2										V_{DD}=9V±5% V_{ILC}=V_{CC}-12.6 To V_{CC}-14.7, R_L=5.6K											
			1.5			1.5	0.240		10	30					1 μs	120			20					250			250
2505			2.5			2.5	180 ns			10					1 μs	120			10					100			100
2524			3			3	135 ns			25			10		1000	70			20					100		N/A	
1402A			2.5			5.0	0.130		10	10					1000	30			20					90			90
																V_{DD}=-9V±5%											
			1.5			3.0	0.170		10	10					1000	60			20					110			110
2502[1,2]			4			8	85[9]			10			10		1000	50				N/A				90		N/A	
1403A			2.5			5.0	0.130		10	10					1000	30			20					90			90
																V_{DD}=-9V±5%											
			1.5			3.0	0.170		10	10					1000	60			20					110			110
2503[1,2]			4			8	85[9]			10			10		1000	50				N/A				90		N/A	
1404A			2.5			5.0	0.130		10	10					1000	30			20					90			90
																V_{DD}=-9V±5%											
			1.5			3.0	0.170		10	10					1000	60			20					110			110
2504A			4			8	85[9]			10			10		1000	50				N/A				90		N/A	
2512			2.5			2.5	180 ns			10					1 μs	120			10					100			100
2525			3			3	135 ns			25			10		1000	70			20					100		N/A	
2518[1,2]			2		N/A			Clock			N/A				5 μs	100			50					350			350
							0.200		DC																		
2538[1,2]			2		N/A			Clock			N/A				5 μs	100			50					350			350
							0.200		DC																		
2519[1,2]			2		N/A			Clock			N/A				5 μs	100			50					350			350
							0.200		DC																		
2539[1,2]			2		N/A			Clock			N/A				5 μs	100			50					350			350
							0.200		DC																		
2509	DC		1.5		N/A			Clock			N/A				1 μs	50			50					350			350
							0.290		100																		
							0.210		DC																		
2532[1,2]	DC		1.5		N/A		0.33		100		N/A				5 μs		N/A		75			I_{OL}=1.6mA			I_{OL}=1.6mA		
								Clock																			
							0.33		DC															400			400
2532-1[1,2]	DC		2.5		N/A		0.020		100		N/A				5 μs		N/A		75			I_{OL}=1.6mA			I_{OL}=1.6mA		
								Clock																			
							0.020		DC															225			225
2510	DC		1.5		N/A		0.290		100		N/A				1 μs	50			50					350			350
								Clock																			
							0.210		DC																		
2521	DC		1.5		N/A		0.350		DC		N/A				1 μs	75			50					350			350
2522	DC		1.5		N/A		0.350		DC		N/A				1 μs	75			50					350			350
2511	DC		1.5		N/A		0.290		100		N/A				1 μs	50			50					350			350
								Clock																			
							0.210		DC																		
2529	DC		1.5		N/A		0.2		100		N/A				1 μs		N/A		65			I_{OL}=1.6mA			I_{OL}=1.6mA		
								Clock																			
							0.2		DC															450			450
2528	DC		1.5		N/A		0.2		100		N/A				1 μs		N/A		65			I_{OL}=1.6mA			I_{OL}=1.6mA		
								Clock																			
							0.2		DC															450			450
2527	DC		1.5		N/A		0.2		100		N/A				1 μs		N/A		65			I_{OL}=1.6mA			I_{OL}=1.6mA		
								Clock																			
							0.2		DC															450			450
2533			1.5			1.5	0.350		100		N/A				1 μs	50			75					300			300
								Clock																			
							250																				

MOS SHIFT REGISTERS
AC ELECTRICAL CHARACTERISTICS TA ‡ 25°C, VDD = −5V +5%, VILC 11V (4, 5, 6, 7, 8)

	Frequency						Clock Pulse									Data											
TEST CONDITION	Clock Rep Rate (MHz) $W=R=V_{CC}$ $R_L=3K$			Data Rep Rate (MHz) $W=R=V_{CC}$			t0PW (μs) Width F=3MHz			t0D (μs) Delay F=3MHz			t_R, t_F (ns) Transition			t_{DW} Data Write Time (setup)			t_{DH} Data to Clock Hold Time			t_{A+} (ns) Clock to Data Out Delay $V_0 = V_{CC}$ −16V Data Out = 2.5V			t_{A-} (ns)		
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max
2560	DC		2.0	DC		2.0	0.2		100		N/A				1 μs		N/A		50			I_{OL}=1.6mA			I_{OL}=1.6mA		
								Clock																			
							0.2		DC															250			250
2561	DC		2.0	DC		2.0	0.2		100		N/A				1 μs		N/A		50			I_{OL}=1.6mA			I_{OL}=1.6mA		
								Clock																			
							0.2		DC															250			250
2562	DC		2.0	DC		2.0	0.2		100		N/A				1 μs		N/A		50			I_{OL}=1.6mA			I_{OL}=1.6mA		
								Clock																			
							0.2		DC															250			250
2563	DC		2.0	DC		2.0	0.2		100		N/A				1 μs		N/A		50			I_{OL}=1.6mA			I_{OL}=1.6mA		
								Clock																			
							0.2		DC															250			250
5060	$0t_R=0t_F$=10ns				N/A		$0t_R=0t_F$=10ns				N/A				1 μs	t_R, t_F=10ns			t_R, t_F=10ns				N/A			N/A	
	DC		1.5				0.300		100							Data, Load			Data, Load								
								Clock								70			50								
							0.200		DC																		

MEMORIES

MOS-RAMS

ELECTRICAL CHARACTERISTICS TABLE (Cont'd)

TA = 0°C to 70°C, VCC = +5V[8], VDD = VD= −12V +5% [4,5,6,7]

TEST CONDITIONS		INPUT VOLTAGE						OUTPUT VOLTAGE						INPUT CURRENT		
		V_{IL}(V)* LOW LEVEL			V_{IH}(V)* HIGH LEVEL			V_{OL}(V)* LOW LEVEL			V_{OH}(V)* HIGH LEVEL			I_{LI}(μA) LOAD		
								T_A=25 C I_{OL}=2.0mA			T_A=25 C I_{OH}=−150μA			T_A=25°C V_{IN}=0V to 5.25V		
NUMBER OF BITS		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
256	25L01	−12		V_{CC}−4.5	V_{CC}−2.0		V_{CC}+0.3	I_{OL} = 3.0 mA		0.45	I_{OH}=−100μA 3.5			V_{IN}=0V		500nA
1024	2101	−0.5		0.65	2.2		V_{CC}			0.45	2.2					10
1024	2101-1	−0.5		0.65	2.2		V_{CC}			0.45	2.2					10
1024	2101-2	−0.5		0.65	2.2		V_{CC}			0.45	2.2					10
1024	2601	−0.5		0.65	2.2		V_{CC}			0.45	2.2					10
1024	2102	−0.5		0.65	2.2	V_{CC}		I_{OL}=1.9mA		0.4	I_{OH}= 100μA 2.2					10
1024	21L02-1	−0.5		0.65	2.2	V_{CC}		I_{OL}=1.9mA		0.4	I_{OH}= 100μA 2.2					10
1024	21L02-3	−0.5		0.65	2.2	V_{CC}		I_{OL}=1.9mA		0.4	I_{OH}= 100μA 2.2					10
1024	21F02	−0.5		0.65	2.2	V_{CC}		I_{OL}=1.9mA		0.4	I_{OH}= 100μA 2.2					10
1024	2111	−0.5		0.65	2.2		V_{CC}			0.45	2.2					10
1024	2111-1	−0.5		0.65	2.2		V_{CC}			0.45	2.2					10
1024	2111-2	−0.5		0.65	2.2		V_{CC}			0.45	2.2					10
1024	2611	−0.5		0.65	2.2		V_{CC}			0.45	2.2					10
1024	2112	−0.5		0.65	2.2		V_{CC}			0.45	2.2					10
1024	2112-1	−0.5		0.65	2.2		V_{CC}			0.45	2.2					10
1024	2112-2	−0.5		0.65	2.2		V_{CC}			0.45	2.2					10
1024	2612	−0.5		0.65	2.2		V_{CC}			0.45	2.2					10
1024	2606	−0.5		0.65	2.2	V_{CC}		I_{OL}=1.9mA		0.45	I_{OH}=−100μA 2.4					10
1024	2606-1	−0.5		0.65	2.2	V_{CC}		I_{OL}=1.9mA		0.45	I_{OH}=−100μA 2.4					10
DYNAMIC 1024	1103[12]	Address/Data in[13] T_A=0°C V_{SS}−17 V_{SS}−14.2 T_A=70°C V_{SS}−17 V_{SS}−14.5 Recharge Enable Read/Write 13, 14 T_A=0°C V_{SS}−17 V_{SS}−14.7 T_A=70°C V_{SS}−17 V_{SS}−15.0			T_A=0°C[13] V_{SS}−1 V_{SS}+1 T_A=70°C[13] V_{SS}−0.7 V_{SS}+1			I_{OL} = 3.2mA See Note 15			60mV	R_L=100[16] T_A=70°C	400mV	R_L=100Ω[16]		1

MOS-RAMS
ELECTRICAL CHARACTERISTICS TABLE (Cont'd)
T_A = 0°C to 70°C, VCC = +5V[8], VDD = VD= −12V +5% [4,5,6,7]

TEST CONDITIONS		INPUT CURRENT						OUTPUT CURRENT						SUPPLY CURRENT		
		I_{LOL} (µA) LOW LEVEL LEAKAGE			I_{LOH} (µA) HIGH LEVEL LEAKAGE			I_{OL} (mA)			I_{OH} (mA)			I_{BB} (µA)		
		T_A=25°C V_{OUT}=0.45V $\overline{CE}$=2.2V			T_A=25°C V_{OUT}= 4.0V $\overline{CE}$=2.2V			SINK T_A=25°C V_{OUT}= −0.7V			SOURCE T_A=25°C V_{OUT}=0V					
NUMBER OF BITS		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
256	2501	V_{OUT}=0V, C_S=3.3V		1000nA	V_{OUT} = 0.45V N/A					13	3.0 2.0	T_A=70°C			N/A	
1024	2101			10			15		N/A			N/A			N/A	
1024	2101-1			10			15		N/A			N/A			N/A	
1024	2101-2			10			15		N/A			N/A			N/A	
1024	2601			10			15		N/A			N/A			N/A	
1024	2102			100			10		N/A			N/A			N/A	
1024	21L02-1			100			10		N/A			N/A			N/A	
1024	21L02-3			100			10		N/A			N/A			N/A	
1024	21F02	$\overline{CE}$=2.0V V_{OUT}=0.4V		10	V_{OUT}=2.4 to V_{CC}		5		N/A			N/A			N/A	
1024	2111			-50			15		N/A			N/A			N/A	
1024	2111-1			-50			15		N/A			N/A			N/A	
1024	2111-2			-50			15		N/A			N/A			N/A	
1024	2611			-50			15		N/A			N/A			N/A	
1024	2112			-50			15		N/A			N/A			N/A	
1024	2112-1			-50			15		N/A			N/A			N/A	
1024	2112-2			-50			15		N/A			N/A			N/A	
1024	2612			-50			15		N/A			N/A			N/A	
1024	2606			-100			10		N/A			N/A			N/A	
1024	2606-1			-100			10		N/A			N/A			N/A	
DYNAMIC 1024	1103[12]	V_{OUT}=0V		1		N/A		See Note 15			600µA / T_A=70°C 500µA	R_L=100[16]	4000µA / 4000µA			100

(See Notes-Page 9)

MOS-RAMS
ELECTRICAL CHARACTERISTICS TABLE (Cont'd)
T_A = 0°C to 70°C, VCC = +5V[8], VDD = VD= −12V +5% [4,5,6,7]

	SUPPLY CURRENT									CAPACITANCE					
	I_{CC1}(mA)			I_{CC2}(mA)			I_{DD}(mA)			C_{IN}(pF)			C_{OUT}(pF)		
TEST CONDITIONS	T_A=25 C V_{IN}=5.25V I_{OUT}=0mA			T_A=0 C V_{IN}=5.25V I_{OUT}=0mA			T_A=25 C I_{OL}=0mA			V_{IN}=5V F=1MHz			V_{IN}=5V F=1MHz		
NUMBER OF BITS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
256 2501		N/A			N/A				9			10			10
1024 2101		30	60			70		N/A			N/A			N/A	
1024 2101-1		30	60			70		N/A			N/A			N/A	
1024 2101-2		30	60			70		N/A			N/A			N/A	
1024 2601		30	60			70		N/A			N/A			N/A	
1024 2102			60			70		N/A			N/A			N/A	
1024 21L02-1			40			40		N/A			N/A			N/A	
1024 21L02-3			40			40		N/A			N/A			N/A	
1024 21F02			60			70		N/A			N/A			N/A	
1024 2111		30	60			70		N/A			N/A			N/A	
1024 2111-1		30	60			70		N/A			N/A			N/A	
1024 2111-2		30	60			70		N/A			N/A			N/A	
1024 2611		30	60			70		N/A			N/A			N/A	
1024 2112		30	60			70		N/A			N/A			N/A	
1024 2112-1		30	60			70		N/A			N/A			N/A	
1024 2112-2		30	60			70		N/A			N/A			N/A	
1024 2612		30	60			70		N/A			N/A			N/A	
1024 2606	40		70			80		N/A		V_{IN}=0V 4		7	V_{OUT}=0V 7		10
1024 2606-1	40		70			80		N/A		V_{IN}=0V 4		7	V_{OUT}=0V 7		10
DYNAMIC 1024 1103[12]		N/A			N/A			All Addresses, Precharge = 0V Cenable = V_{SS} During t_{pc} During t_{ov} Precharge = V_{SS} Cenable = 0V During t_{pov} Precharge, Cenable = V_{SS}	 56 59 11 4	← See Data Sheet →					

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MOS-RAMS
ELECTRICAL CHARACTERISTICS TABLE (Cont'd)

TA = 0°C to 70°C, VCC = +5V[8], VDD = VD= –12V +5% [4,5,6,7]

	INPUT VOLTAGE						OUTPUT VOLTAGE						INPUT CURRENT		
TEST CONDITIONS	$V_{IL}(V)$[8] LOW LEVEL			$V_{IH}(V)$[8] HIGH LEVEL			$V_{OL}(V)$[8] LOW LEVEL			$V_{OH}(V)$[8] HIGH LEVEL			$I_{LI}(\mu A)$ LOAD		
							T_A=25°C I_{OL}=3.2mA			T_A=25°C I_{OH}=–200μA			T_A=25°C V_{IN}=0V to 5.25V		
NUMBER OF BITS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
1024 1103-1[12]	Address/Data in[13] T_A=0°C V_{SS}-20		V_{SS}-18	V_{SS}-1	T_A=0°C	V_{SS}+1		I_{OL} = 3.2mA See Note 15		115 mV 90 mV	R_L=100[16] T_A=70°C	700mV 700mV	R_L=100Ω[16]		1
4096 2680	See Data Sheet for Electrical Specifications														
4096 2680-1	See Data Sheet for Electrical Specifications														
4096 2680-2	See Data Sheet for Electrical Specifications														

MOS-RAMS
ELECTRICAL CHARACTERISTICS TABLE (Cont'd)

$T_A = 0°C$ to $70°C$, $V_{CC} = +5V$[8], $V_{DD} = V_D = -12V +5\%$ [4,5,6,7]

	INPUT CURRENT						OUTPUT CURRENT								
TEST CONDITIONS	I_{LOL}(µA) LOW LEVEL LEAKAGE			I_{LOH}(µA) HIGH LEVEL LEAKAGE			I_{OL}(mA)			I_{OH}(mA)			I_{BB}		
	T_A=25°C V_{OUT}=0.45V $\overline{CE}$=2.2V			T_A=25°C V_{OUT}=0.45V $\overline{CE}$=2.2V			SINK T_A=25°C V_{OUT}=4.5V			SOURCE T_A=25°C V_{OUT}=0V					
NUMBER OF BITS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
1024 1103-1[12]		V_{OUT}=0V	10		N/A			See Note 15		1.15µA	R_L=100Ω[16]	7.0µA			100
											T_A=55°C				
										0.9µA		7.0µA			
4096 2680	See Data Sheet for Electrical Specifications														
4096 2680-1	See Data Sheet for Electrical Specifications														
4096 2680-2	See Data Sheet for Electrical Specifications														

MOS-RAMS
ELECTRICAL CHARACTERISTICS TABLE (Cont'd)

TA = O°C to 70°C, VCC = +5V[8], VDD = VD= –12V +5% [4,5,6,7]

	SUPPLY CURRENT									CAPACITANCE					
TEST CONDITIONS	I_{CC1}(mA)			I_{CC2}(mA)			I_{DD}(mA)			C_{IN}(pF)			C_{OUT}(pF)		
	T_A=25 C V_{IN}=5.25V I_{OUT}=0mA			T_A=0 C V_{IN}=5.25V I_{OUT}=0mA			T_A=25 C I_{OL}=0mA			V_{IN}=5V F=1MHz			V_{IN}=5V F=1MHz		
NUMBER OF BITS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
1024 1103-1[1,2]		N/A			N/A		Average Cycle Time = 580ns Precharge Width = 190ns		25	← See Data Sheet →					
							All Addresses, Precharge = 0V Cenable = V_{SS} During t_{pc}		60						
							During t_{ov}		68.5						
							Precharge = V_{SS} Cenable = 0V During t_{pov}		11						
							Precharge, Cenable = V_{SS}		4						
							Average Cycle Time = 500ns Precharge Width = 190ns		23						
4096 2680	See Data Sheet for Electrical Specifications														
4096 2680-1	See Data Sheet for Electrical Specifications														
4096 2680-2	See Data Sheet for Electrical Specifications														

MOS-CHARACTER GENERATORS
ELECTRICAL CHARACTERISTICS TABLE

	Input Voltage –						Output Voltage						Input Current			Output Current		
TEST CONDITIONS	V_{IL} (V)[8] Low Level			V_{IH} (V)[8] High Level			V_{OL} (V)[8] Low Level I_{OL}=1.6mA			V_{OH} (V)[8] High Level I_{OH}=100μA			I_{LI} (μA) Load T_A=25°C V_{IN}=5.5V			I_{LOL} (μA) Low Level Leakage T_A=25°C V_{OUT}=5.5V V_{CE}=V_{CC}		
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max
# of Bits																		
2560 2513	–5		0.6	3.4		5.3	–5		0.4	3.0					500nA			1000nA
3072 2516	–5		0.6	3.4		5.3	–5		0.5	3.8					500nA			1000nA
4096 2530	–5		0.6	3.4		5.3			0.5	3.8					500nA			1000nA
5184 2526	–5		0.6	3.4		5.3			0.5	3.8					500nA			1000nA
8192 2580	–5		0.6	3.4		5.3			0.5	3.8					500nA			1000nA
8192 2608	–5		0.65	2.2					0.45	2.4			$0 \leq V_{IN} \leq 5.25V$		10	V_{OUT}=0.4V		10
8192 2608-1	–5		0.65	2.2					0.45	2.4			$0 \leq V_{IN} \leq 5.25V$		10	V_{OUT}=0.4V		10

NOTES:

1. Stresses above those listed under "Maximum Guaranteed Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these are at any other condition above those indicated in the operation specifications is not implied.
2. For operating at elevated temperatures, the devices must be derated based on a +150°C maximum junction temperature and a thermal resistance of 150°C/W (T_A and V package) or a 125°C/W (B package).
3. All inputs are protected against static charge.
4. Parameters are valid over operating temperature range unless specified.
5. All voltage measurements are referenced to ground.
6. Manufacturer reserves the right to make design and process changes and improvements.
7. Typical values at +25°C and typical supply voltages.
8. Guaranteed input levels are stated for worst case conditions including a ±5% variation in V_{CC} and a temperature variation of 0°C to +70°C. Actual input requirements with respect to V_{CC} are V_{IH} = V_{CC} = 1.85V and V_{IL} = V_{CC} = 4.15V.
9. When cascading, use 140ns maximum pulse width to allow data set-up time for driver register.
10. V_{OL} is a function of the input characteristics of the driver TTL/DTL gate I_{OI} and V_{CLAMP} and the value of the pull-down resistor (R_L).
11. Typically I_{GG} will reduce by 40μA/bit reduction in total register length.
12. T_A = 0°C to +70°C, V_{SS} (Note 17) = 16V ±5%, (V_{BB} – V_{SS}) Note 18 = 3V to 4V, V_{DD} = 0V unless otherwise specified.
13. The maximum values for V_{IL} and the minimum values for V_{IH} are linearly related to temperature between 0°C and 70°C can be calculated using a straight-line relationship.
14. The maximum values for V_{IL} (for precharge, cenable and read/write) may be increased to V_{SS} – 14.2 @ 0°C and V_{SS} – 14.5 @ 70°C (same values as those specified for the address and data-in lines) with a 40ns degradation (worst case) in t_{AC}, t_{PC}, t_{RC}, t_{WC}, t_{RWC}, t_{ACC1} and t_{ACC2}.
15. The output current when reading a low output is the leakage current of the 1103 plus external noise coupled into the output line from the clocks. V_{OL} equals I_{OL} across the load resistor.
16. This value of load resistance is used for measurement purposes. In applications the resistance may range from 100Ω to 1kΩ.
17. The V_{SS} current drain is equal to (I_{DD} + I_{OH}) or (I_{DD} + I_{OL}).
18. (V_{BB} – V_{SS}) supply should be applied at or before V_{SS}.

MOS-CHARACTER GENERATORS
ELECTRICAL CHARACTERISTICS TABLE

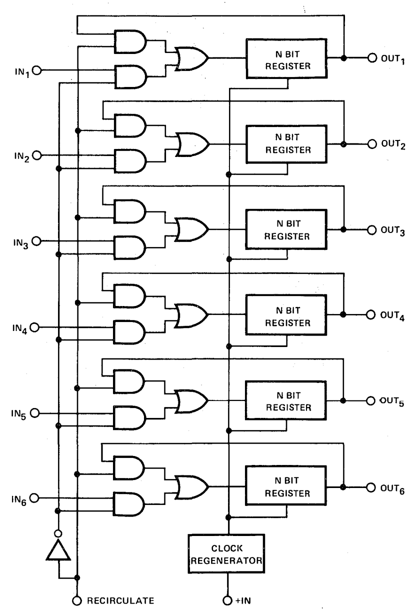
	Output Current			Supply Voltage									Capacitance					
TEST CONDITIONS	I_{LOH} (µA) High Level Leakage			I_{GG} (mA) V_{OUT}=0V V_{CE}=V_{CC}			I_{CC} (mA) V_{CC}=5.25V			I_{DD} (mA) T_A=25°C V_{OUT}=0V			C_{IN} (pF) F=1 MHz V_{IH}=V_{CC} V_{AC}=25MVP-P			C_{OUT} (pF)		
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max
# of Bits																		
2560 2513		N/A				15		N/A				15			10			
3072 2516		N/A				12		N/A				21			10			
4096 2530		N/A				45			45		N/A				10			
5184 2526		N/A				45			45		N/A				10			
8192 2580		N/A				35			35		N/A				10			
8192 2608	V_{OUT}=2.4V				N/A		T_A=0°C		80		N/A		V_{IN}=0V		7.5	V_{OUT}=0V		15
8192 2608-1	V_{OUT}=2.4V				N/A		T_A=0°C		80				V_{IN}=0V		7.5	V_{OUT}=0V		15

2518-B,I,F

DESCRIPTION

The 2518 and 32-bit recirculating static shift registers consist of enhancement mode P-channel silicon gate MOS devices integrated on a single monolithic chip. Internal recirculation logic plus TTL/DTL level clock signals are provided for maximum interfacing ease.

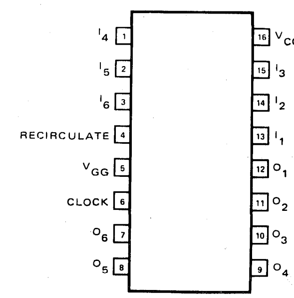
BLOCK DIAGRAM



SWITCHING CHARACTERISTICS

PARAMETER	LIMITS MIN	LIMITS MAX	UNIT
t_{RS} Recirculate set-up time	150		ns
t_{RH} Recirculate hold time	50		ns
t_{DOE} Output enable time		100	ns
t_{DOD} Output disable time		100	ns

PIN CONFIGURATION

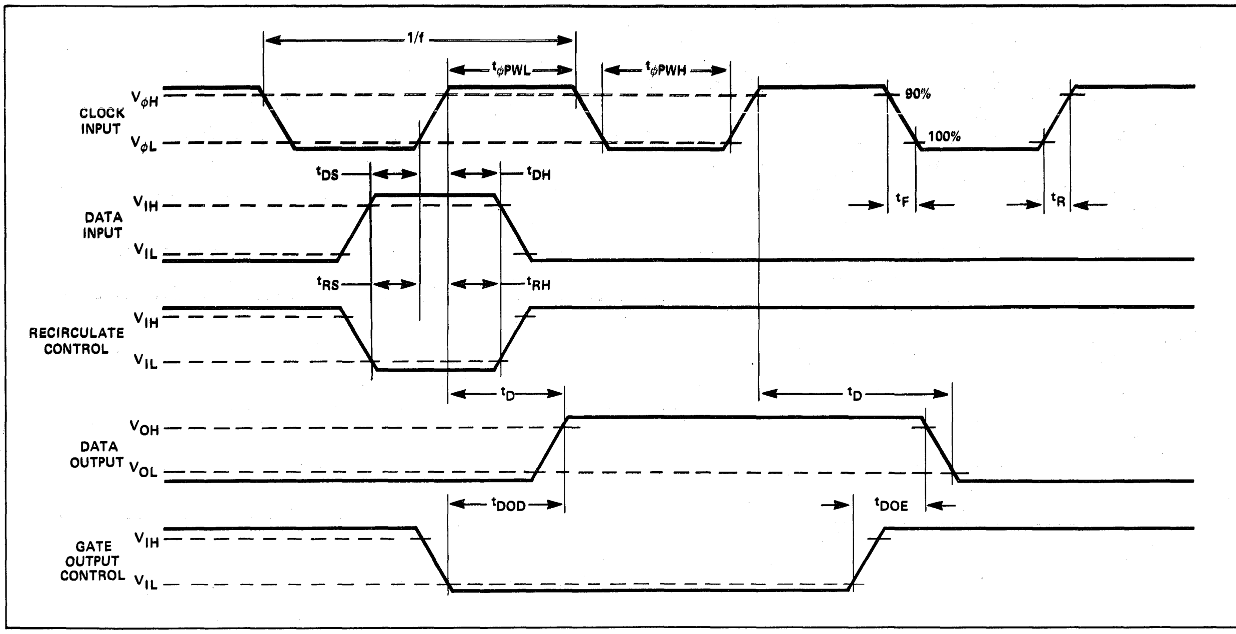


TRUTH TABLE

RECIRCULATE	INPUT	FUNCTION
1	0	Recirculate
1	1	Recirculate
0	0	"0" is Written
0	1	"1" is Written

Data is Read Out when output enable is "low." Output is tri-stated when output enable is "high."

TIMING DIAGRAM



HEX 40-BIT STATIC SHIFT REGISTER 2519

2519-B,I,F

DESCRIPTION

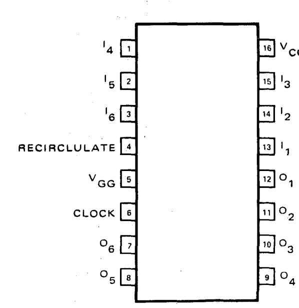
The 2519 40-bit recirculating static shift registers consist of enhancement mode P-channel silicon gate MOS devices integrated on a single monolithic chip. Internal recirculation logic plus TTL/DTL level clock signals are provided for maximum interfacing ease.

SWITCHING CHARACTERISTICS

PARAMETER	LIMITS		UNIT
	MIN	MAX	
t_{RS} Recirculate set-up time	150		ns
P_{RH} Recirculate hold time	50		ns
t_{DOE} Output enable time		100	ns
t_{DOD} Output disable time		100	ns

PIN CONFIGURATION

B, I, F PACKAGE

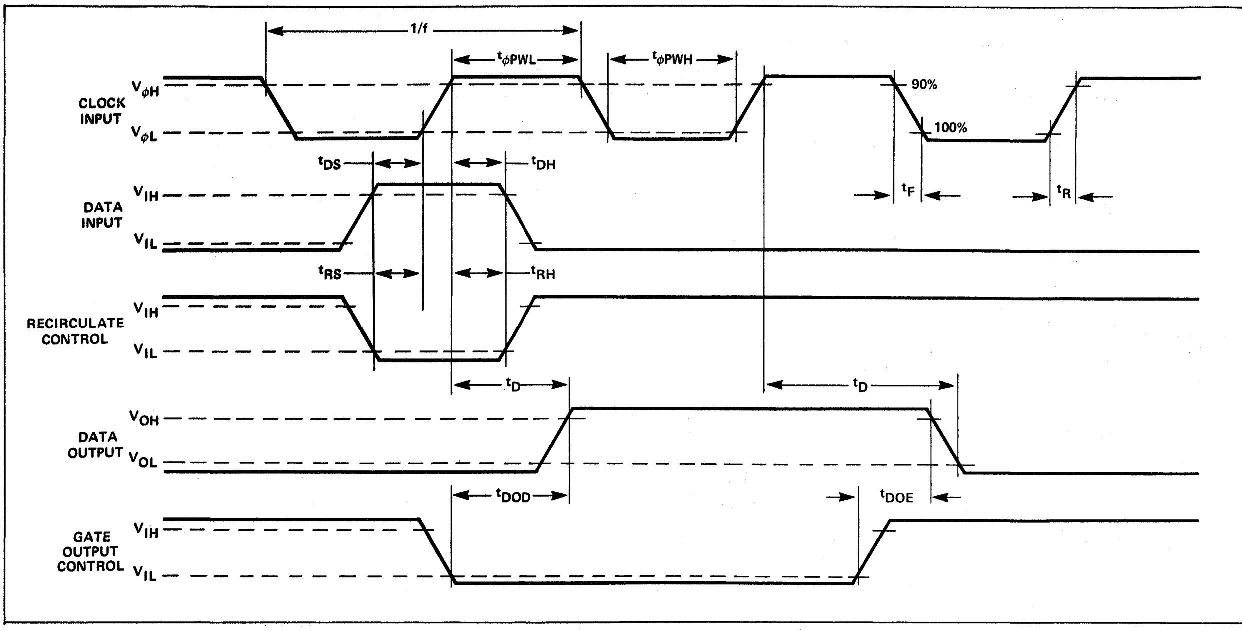


TRUTH TABLE

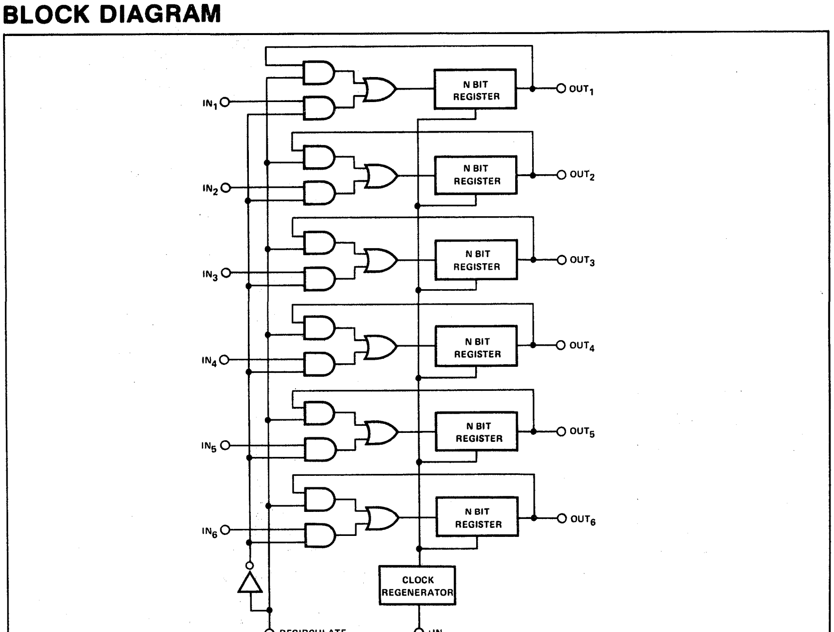
RECIRCULATE	INPUT	FUNCTION
1	0	Recirculate
1	1	Recirculate
0	0	"0" is Written
0	1	"1" is Written

Data is Read out when output enable is "low." Output is tri-stated when output enable is "high."

TIMING DIAGRAM



BLOCK DIAGRAM

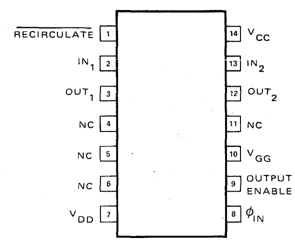


DESCRIPTION

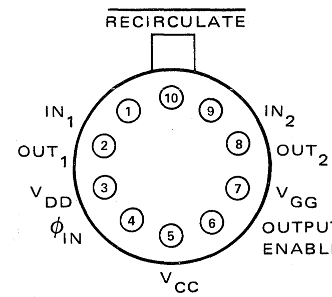
The 2509 50-bit recirculating static shift register consists of enhancement mode P-channel silicon gate MOS devices integrated on a single monolithic chip. Internal recirculation logic plus TTL/DTL level clock signals plus tri-state outputs are provided for maximum interfacing ease.

PIN CONFIGURATION

A PACKAGE



K PACKAGE



SWITCHING CHARACTERISTICS

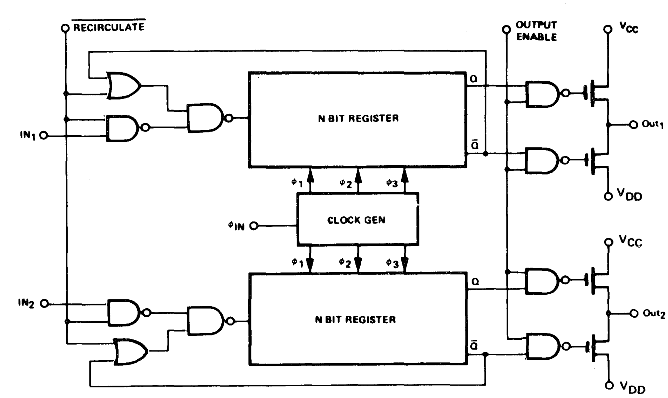
PARAMETER	LIMITS MIN	LIMITS MAX	UNIT
t_{DE} Disconnect		300	

TRUTH TABLE

RECIRCULATE	INPUT	FUNCTION
0	0	Recirculate
0	1	Recirculate
1	0	"0" is Written
1	1	"1" is Written

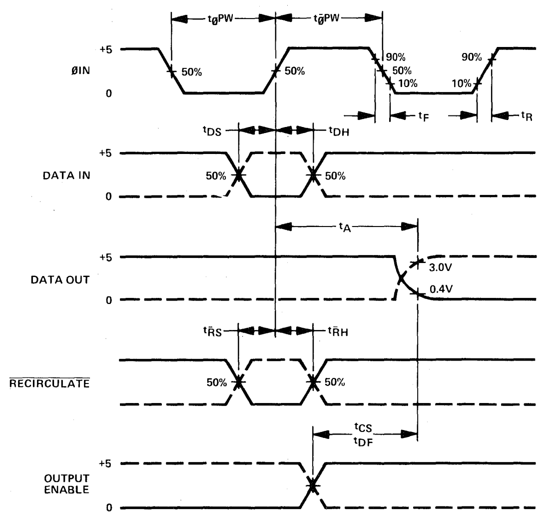
NOTE: "0" = OV; "1" = +5V.

BLOCK DIAGRAM



NOTES:
1: If output enable = "0", output is "off".
2: If output enable = "1", see Truth Table.

TIMING DIAGRAM



$t_R = t_F$ <10 NSEC FOR ALL INPUTS

2532-B • 2532-1-B

DESCRIPTION

The 2532 Static Shift Register consists of enhancement mode P-Channel silicon gate MOS devices integrated on a single monolithic chip. Each of the four 80-bit registers is provided with an independent input, push-pull output and recirculation control. The single phase clock is common to all four registers. All inputs and outputs including the clock interface directly with TTL or DTL circuits without external components.

Data is entered when the clock is at a logic "1". Data is shifted when the clock goes low. When the Recirculate control is at a logic "1", data recirculates and is continuously available at the output, data input is inhibited. With the Recirculate control is at a logic "0", data is entered.

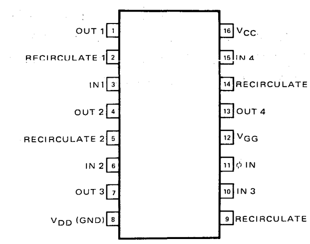
TRUTH TABLE

RECIRCULATE	FUNCTION	INPUT
0	"0" is Written	0
0	"1" is Written	1
1	Recirculate	0
1	Recirculate	1

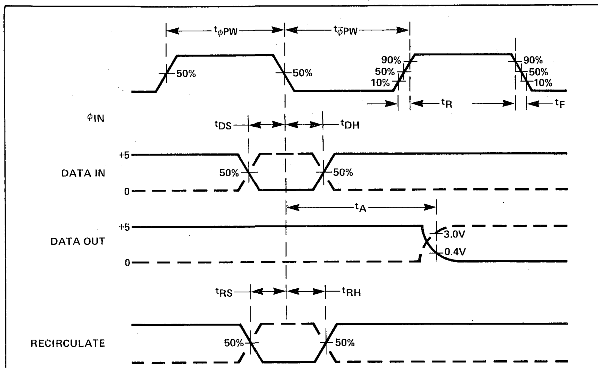
NOTE: "0" = OV, "1" = +5V

PIN CONFIGURATION

B PACKAGE

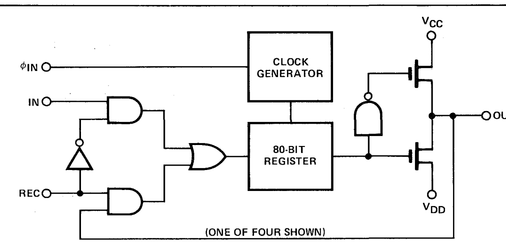


TIMING DIAGRAM



$t_R = t_F$ 10 NSEC FOR ALL INPUTS
NOTE: CLOCK MUST BE STOPPED IN THE TTL "0" STATE TO RETAIN DATA DURING STATIC OPERATION.

BLOCK DIAGRAM



SWITCHING CHARACTERISTICS

PARAMETER	2532		2532-1		UNIT
	MIN	MAX	MIN	MAX	
t_{RS} Recirculate set-up time	150		80		ns
t_{RH} Recirculate hour time	50		30		ns

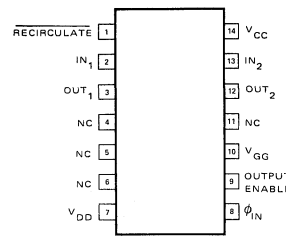
2510-A.K

DESCRIPTION

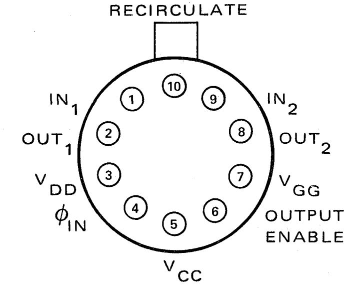
The 2510 100-bit recirculating static shift register consists of enhancement mode P-channel silicon gate MOS devices integrated on a single monolithic chip. Internal recirculation logic plus TTL/DTL level clock signals plus tri-state outputs are provided for maximum interfacing ease.

PIN CONFIGURATION

A PACKAGE



K PACKAGE



SWITCHING CHARACTERISTICS

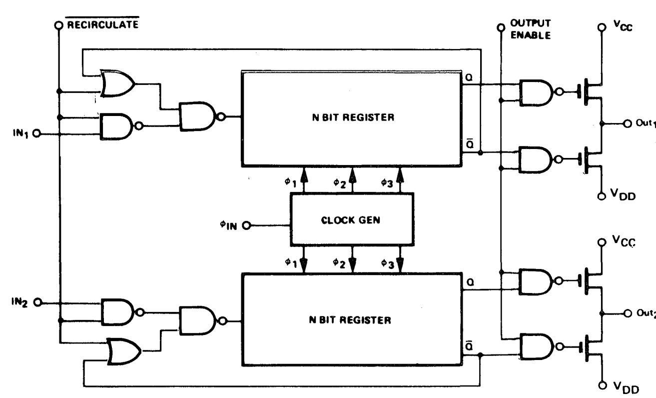
PARAMETER	LIMITS		UNIT
	MIN	MAX	
t_{DE} Disconnect		300	

TRUTH TABLE

RECIRCULATE	INPUT	FUNCTION
0	0	Recirculate
0	1	Recirculate
1	0	"0" is Written
1	1	"1" is Written

NOTE: "0" = OV; "1" = +5V.

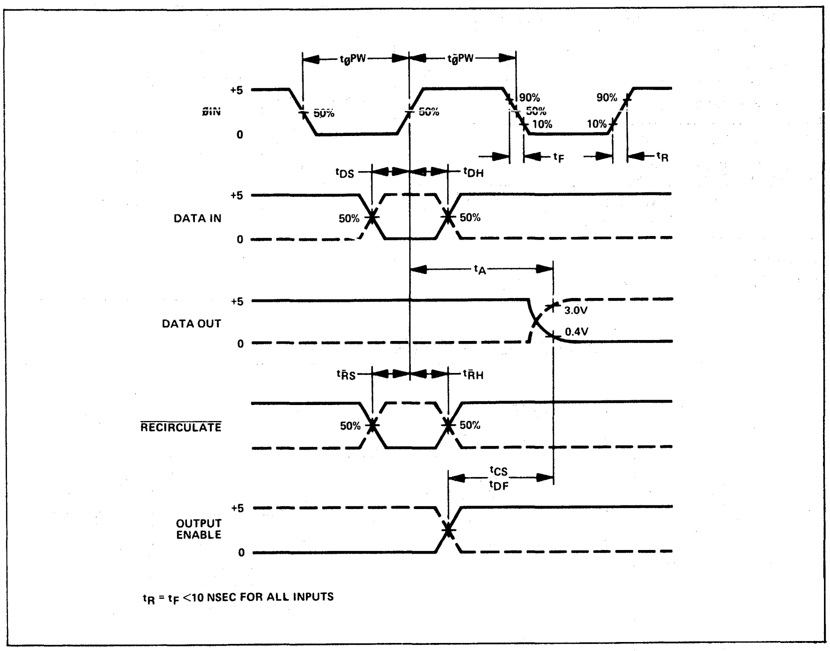
BLOCK DIAGRAM



NOTES:
1: If output enable = "0", output is "off".
2: If output enable = "1", see Truth Table.

2510-A.K

TIMING DIAGRAM



MEMORIES

2521-V

DESCRIPTION

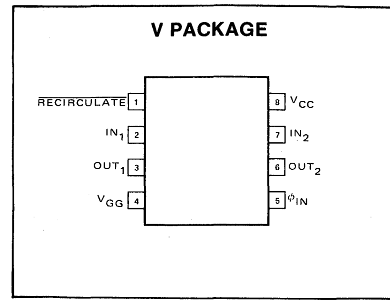
The 2521 128-bit recirculating static shift register consists of enhancement mode P-channel silicon gate MOS devices integrated on a single monolithic chip.

TRUTH TABLE

FUNCTION	INPUT	RECIRCULATE
Recirculate	0	0
Recirculate	1	0
"0" is Written	0	1
"1" is Written	1	1

NOTE: "0" = 0V; "1" = +5V.

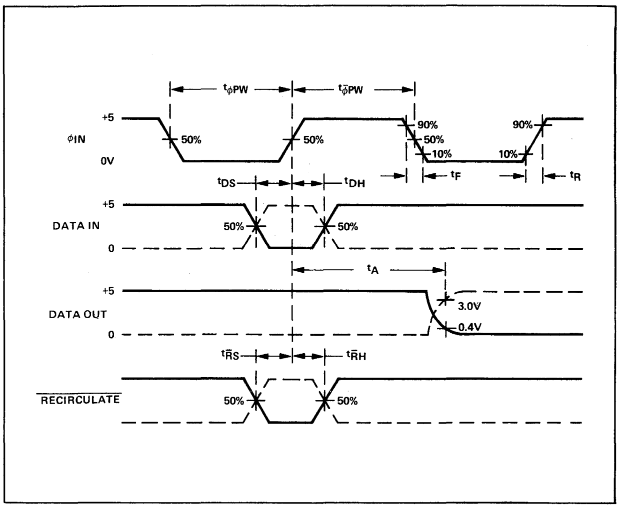
PIN CONFIGURATION



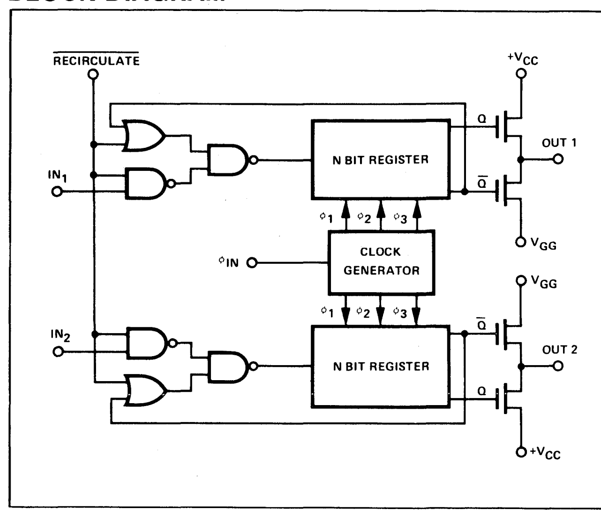
SWITCHING CHARACTERISTICS

PARAMETER	LIMITS MIN	LIMITS MAX	UNIT
t_{RS} Recirculate setup time	50		ns
t_{RH} Recirculate hold time	50		ns

TIMING DIAGRAM



BLOCK DIAGRAM



DESCRIPTION

The 2522 132-bit recirculating static shift register consists of enhancement mode P-channel silicon gate MOS devices integrated on a single monolithic chip.

TRUTH TABLE

RECIRCULATE	INPUT	FUNCTION
0	0	Recirculate
0	1	Recirculate
1	0	"0" is Written
1	1	"1" is Written

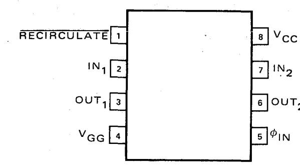
NOTE: "0" = 0V; "1" = **+5V.**

SWITCHING CHARACTERISTICS

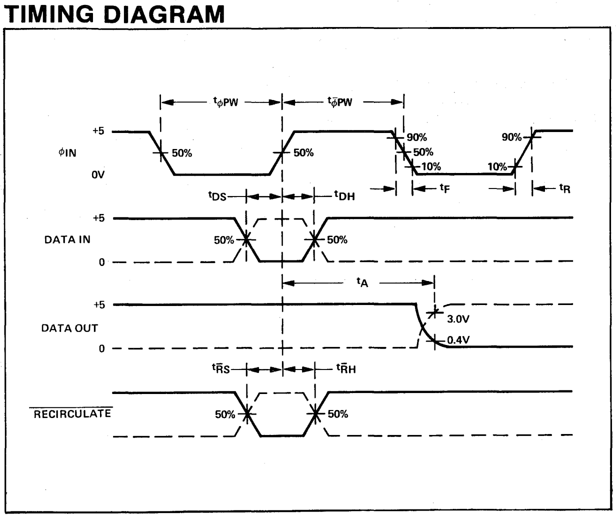
PARAMETER	LIMITS MIN	LIMITS MAX	UNIT
t_{RS} Recirculate set-up time	50		ns
t_{RH} Recirculate hold time	50		ns

PIN CONFIGURATION

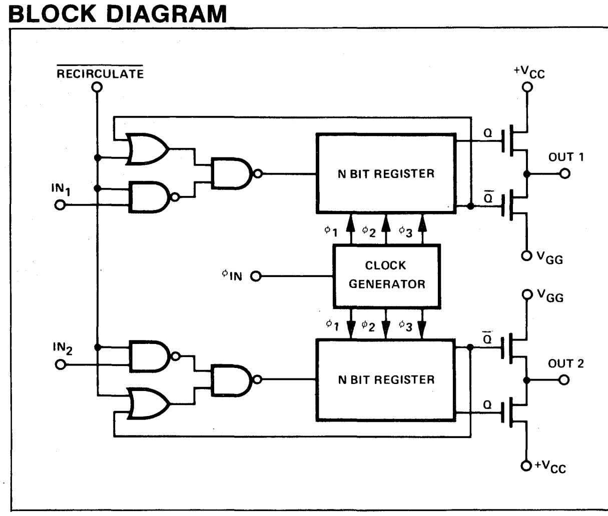
V PACKAGE



TIMING DIAGRAM



BLOCK DIAGRAM



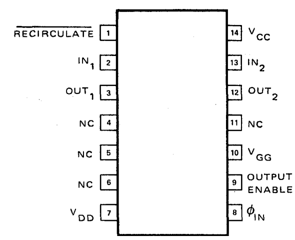
2511-A,K

DESCRIPTION

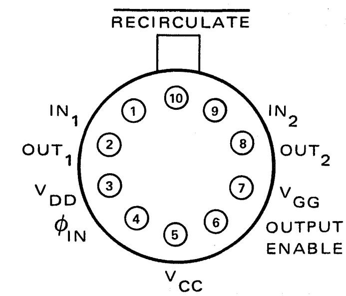
The 2511 200-bit recirculating static shift register consists of enhancement mode P-channel silicon gate MOS devices integrated on a single monolithic chip. Internal recirculation logic plus TTL/DTL level clock signals and tri-state outputs are provided for maximum interfacing ease.

PIN CONFIGURATION

A PACKAGE



K PACKAGE



SWITCHING CHARACTERISTICS

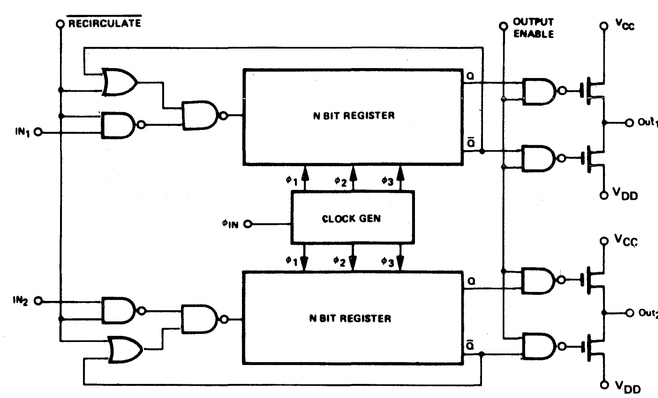
PARAMETER	LIMITS MIN	LIMITS MAX	UNIT
t_{DE} Disconnect		300	

TRUTH TABLE

RECIRCULATE	INPUT	FUNCTION
0	0	Recirculate
0	1	Recirculate
1	0	"0" is Written
1	1	"1" is Written

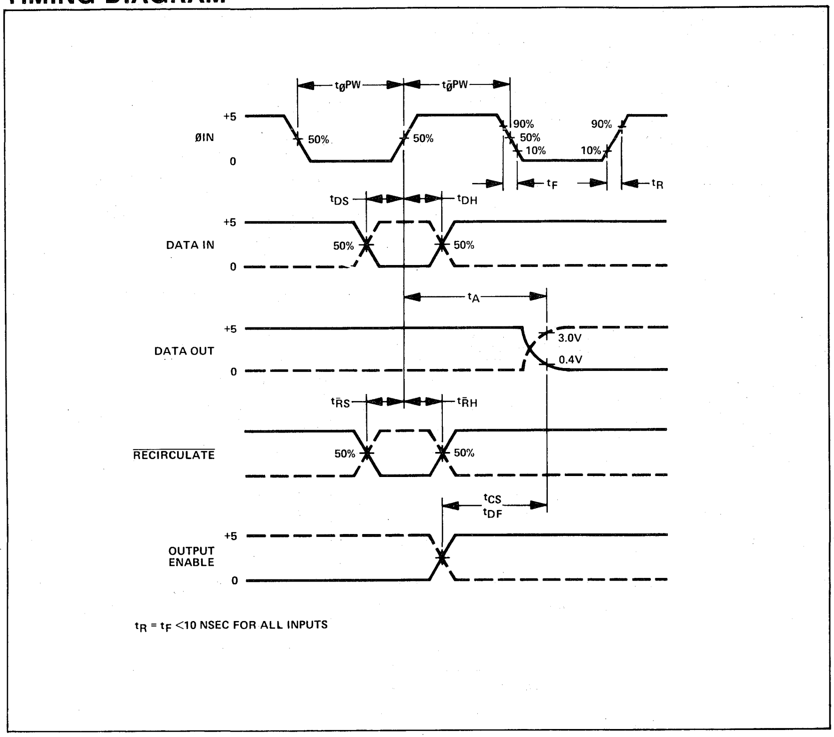
NOTE: "0" = OV; "1" = +5V.

BLOCK DIAGRAM



NOTES:
1: If output enable = "0", output is "off".
2: If output enable = "1", see Truth Table.

TIMING DIAGRAM



MEMORIES

2529-V

DESCRIPTION

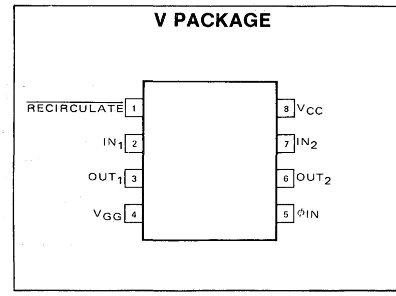
The 2529 240-bit recirculating static shift register consists of enhancement mode P-channel silicon gate MOS devices integrated on a single monolithic chip.

TRUTH TABLE

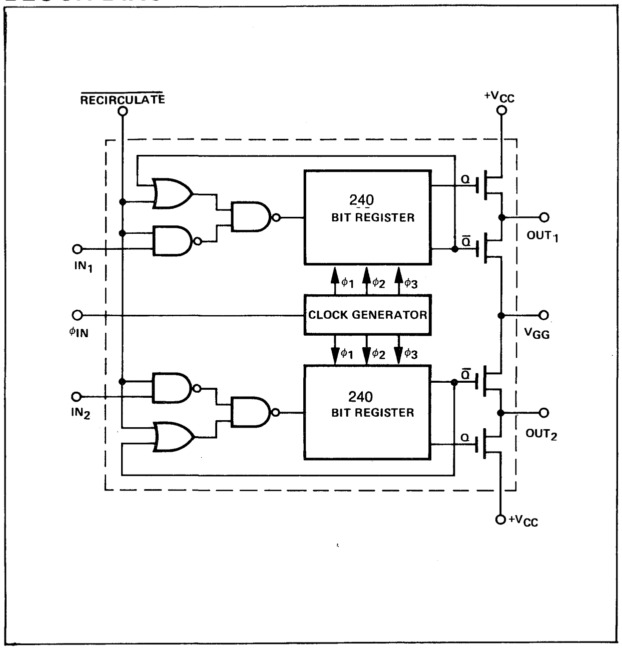
RECIRCULATE	INPUT	FUNCTION
0	0	Recirculate
0	1	Recirculate
1	0	"0" is Written
1	1	"1" is Written

NOTE: "0" = 0V; "1" = +5V

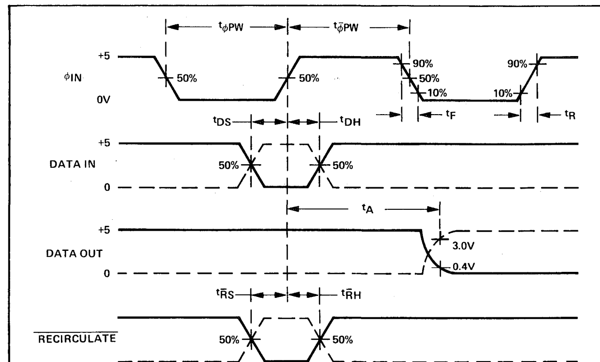
PIN CONFIGURATION



BLOCK DIAGRAM



TIMING DIAGRAM



$t_R = t_F < 10$ NSEC FOR ALL INPUTS

NOTE: FOR STATIC OPERATION, THE INPUT CLOCK MUST BE STOPPED IN THE TTL "1" STATE IN ORDER TO RETAIN DATA (SEE CLOCK PULSE WIDTH SPECIFICATION).

DESCRIPTION

The 2528 250-bit recirculating static shift register consists of enhancement mode P-channel silicon gate MOS devices integrated on a single monolithic chip.

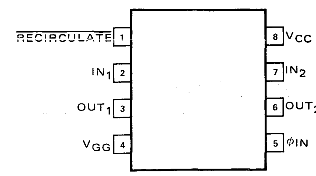
TRUTH TABLE

RECIRCULATE	INPUT	FUNCTION
0	0	Recirculate
0	1	Recirculate
1	0	"0" is Written
1	1	"1" is Written

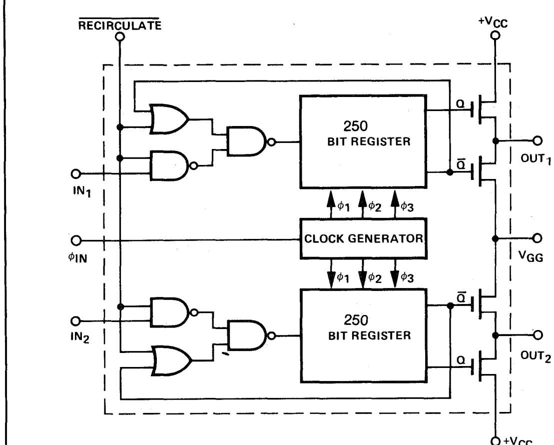
NOTE: "0" = 0V; "1" = +5V

PIN CONFIGURATION

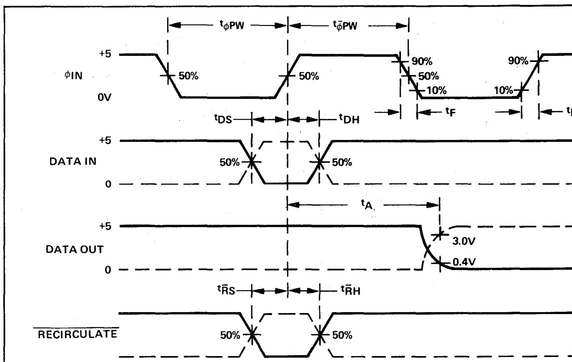
V PACKAGE



BLOCK DIAGRAM



TIMING DIAGRAM



$t_R = t_F < 10$ NSEC FOR ALL INPUTS

NOTE: FOR STATIC OPERATION, THE INPUT CLOCK MUST BE STOPPED IN THE TTL "1" STATE IN ORDER TO RETAIN DATA (SEE CLOCK PULSE WIDTH SPECIFICATION).

2527-V

DESCRIPTION

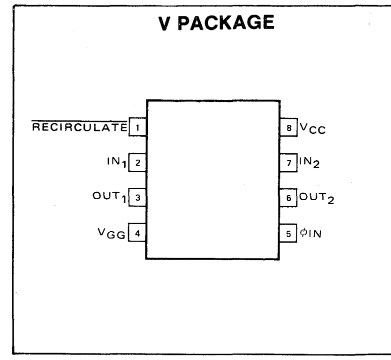
The 2527 256-bit recirculating static shift register consists of enhancement mode P-channel silicon gate MOS devices integrated on a single monolithic chip.

TRUTH TABLE

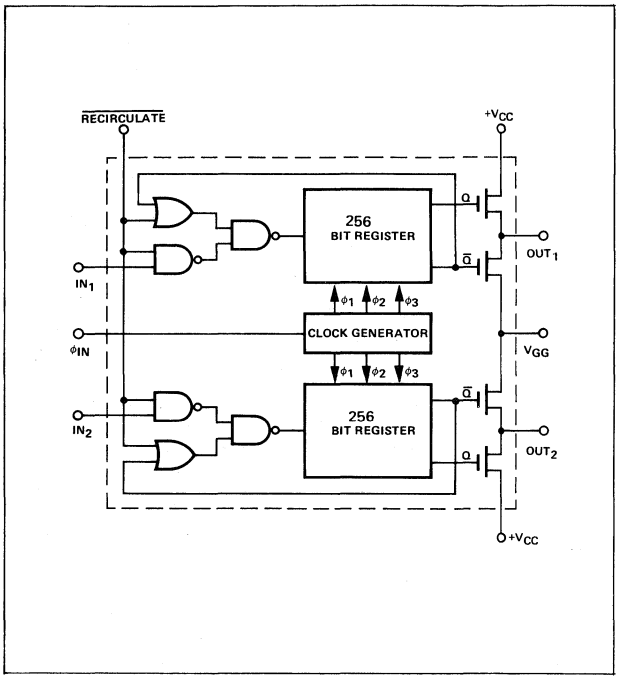
RECIRCULATE	INPUT	FUNCTION
0	0	Recirculate
0	1	Recirculate
1	0	"0" is Written
1	1	"1" is Written

NOTE: "0" = 0V; "1" = +5V

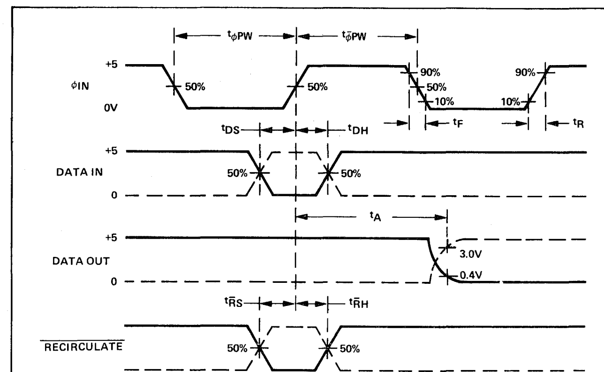
PIN CONFIGURATION



BLOCK DIAGRAM



TIMING DIAGRAM



$t_R = t_F$ 10 NSEC FOR ALL INPUTS

NOTE: FOR STATIC OPERATION, THE INPUT CLOCK MUST BE STOPPED IN THE TTL "1" STATE IN ORDER TO RETAIN DATA (SEE CLOCK PULSE WIDTH SPECIFICATION).

DESCRIPTION

The 2533 Static Shift Register consists of enhancement mode P-channel silicon gate MOS devices integrated on a single monolithic chip.

The 1024-bit register is equipped with two data inputs together with a "Stream Select" control to facilitate external recirculation.

The single phase clock input, data input, data output, and stream select control will interface directly with TTL/DTL circuits without external components.

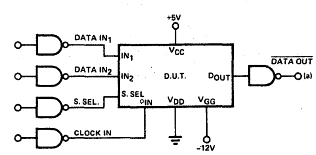
Data is entered when the clock is at a logic "1". Data is shifted when the clock goes low.

TRUTH TABLE

STREAM SELECT	FUNCTION
0	IN 1 SELECTED
1	IN 2 SELECTED

NOTE: "0" = 0V, "1" = +5V

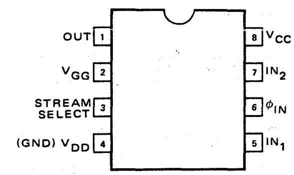
AC TEST SETUP



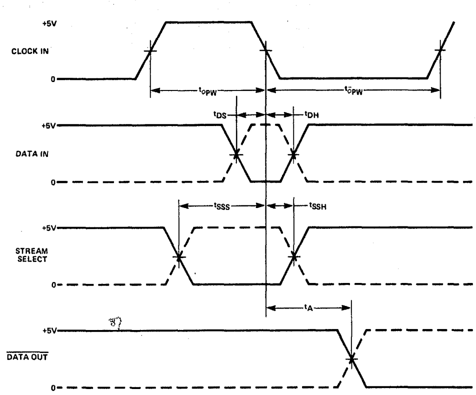
NOTES:
Measure t_A between device input and point (a). Gates are standard 7400.

PIN CONFIGURATION

V PACKAGE



TIMING DIAGRAM



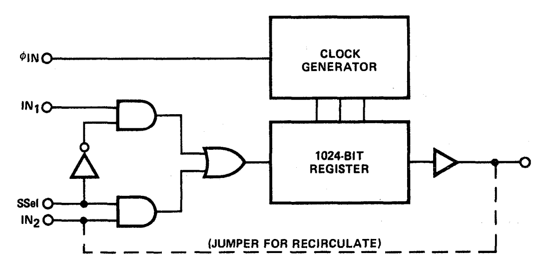
NOTE: A TIMES MEASURED AT 50% POINTS WITH INPUT tr, tf ⩽ 10ns.

B CLOCK MUST BE STOPPED IN TTL "0" STATE TO RETAIN DATA DURING STATIC MODE OPERATION.

SWITCHING CHARACTERISTICS

PARAMETER	LIMITS		UNIT
	MIN	MAX	
t_{SSH} Stream select hold time	50		ns
t_{SSS} Stream select set-up time	80		ns

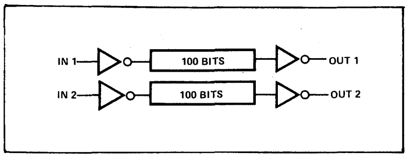
BLOCK DIAGRAM



DESCRIPTION

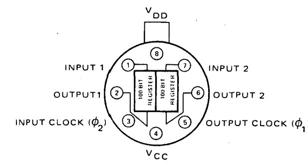
These Signetics 2500 Series dual 100-Bit dynamic shift registers consist of enhancement mode P-channel MOS devices integrated on a single monolithic chip. They use two clock phases.

BLOCK DIAGRAM

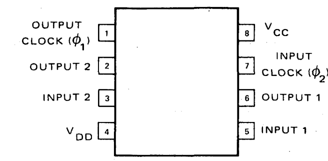


PIN CONFIGURATION

T PACKAGE



V PACKAGE

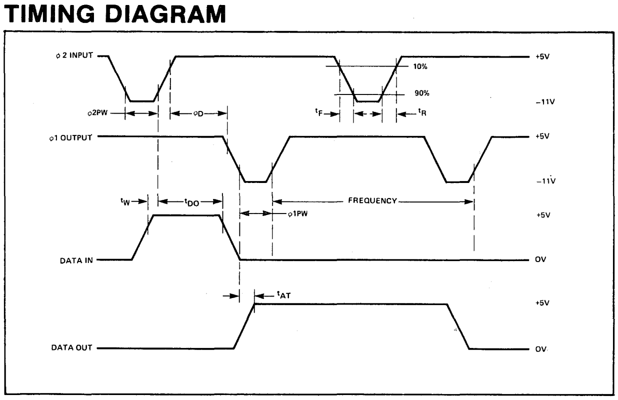


SWITCHING CHARACTERISTICS

PARAMETER	TEST CONDITIONS	LIMITS		UNIT
		MIN	MAX	
t_{DO} Data in overlap	$t_{r2} = t_{r1}$ = 10ns	10		

PART NO.	OUTPUT	PACKAGE
2506T	Bare Drain	8 Pin TO-5
2506 V	Bare Drain	8 Pin DIP
2507 T	7.5k Pull Down	8 Pin TO-5
2507 V	7.5k Pull Down	8 Pin DIP
2517 T	20k Pull Down	8 Pin TO-5
2517 V	20k Pull Down	8 Pin DIP

TIMING DIAGRAM

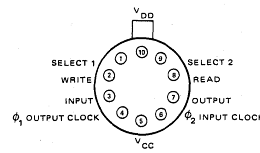


2505/1405-K

DESCRIPTION

The 2505/1405 512-bit recirculating dynamic shift registers consist of enhancement mode P-channel MOS devices integrated on a single monolithic chip. Internal recirculation logic plus write and read controls, together with two chip select controls are included on the chip.

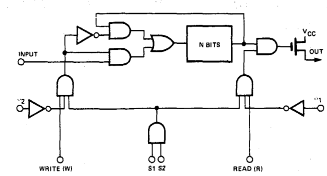
BLOCK DIAGRAM



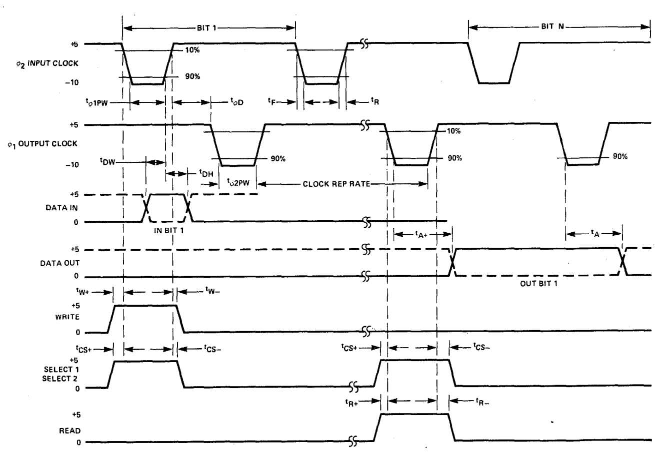
NOTES:
N = 512 '0' = OV, '1' = +5V.
When S1 or S2 is '0' Data Recirculates
When S1 and S2 are '1' see truth table

PIN CONFIGURATION

K PACKAGE



TIMING DIAGRAM



NOTE:
1. N=512
2. Note that the Read Input is AND'ed with $\overline{\Phi}_1$; therefore this function is not valid until $\underline{\Phi}_1$ occurs.

TRUTH TABLE

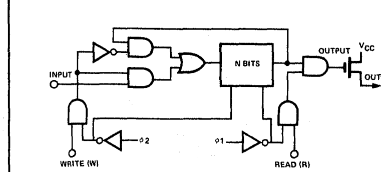
WRITE	READ	FUNCTION
0	0	Recirculate, Output is '0'
0	1	Recirculate, Output is Data
1	0	Write Mode, Output is '0'
1	1	Read/Write, Output is Data

MEMORIES

DESCRIPTION

The 2524 512-bit recirculating dynamic shift register consists of enhancement mode P-channel MOS devices integrated on a single monolithic chip. Internal recirculation logic plus write and read controls are included on the chip.

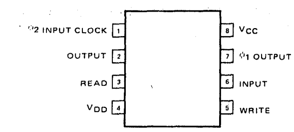
BLOCK DIAGRAM



NOTE
N = 512 '0' = 0V, '1' = +5V.

PIN CONFIGURATION

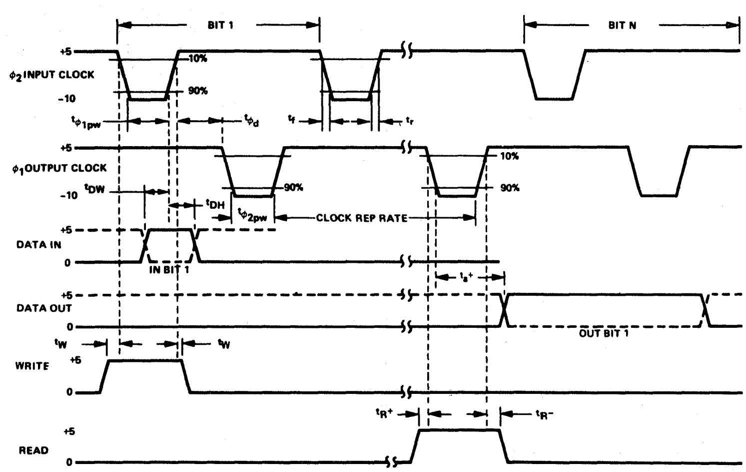
V PACKAGE



CONDITIONS OF TEST

Input rise and fall times: 10 ns Output load is 1 TTL gate

TIMING DIAGRAM



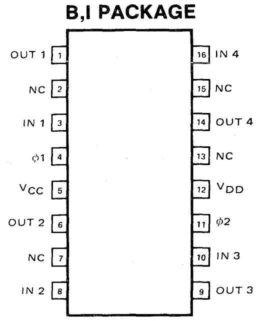
NOTE:
1. N = 512
2. Note that the Read Input is AND'ed with $\overline{\phi}_1$; therefore this function is not valid until ϕ_1 occurs.

TRUTH TABLE

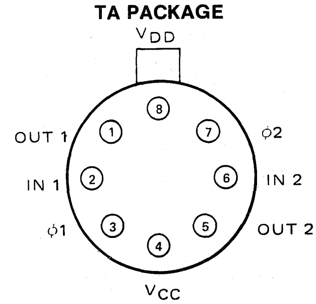
WRITE	READ	FUNCTION
0	0	Recirculate, Output is '0'
0	1	Recirculate, Output is Data
1	0	Write Mode, Output is '0'
1	1	Read Mode Output is Data

PIN CONFIGURATION

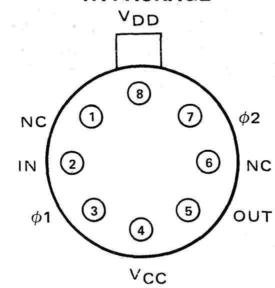
2502
B,I PACKAGE



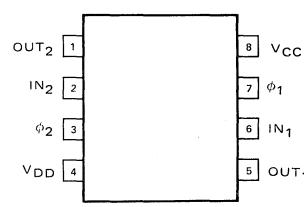
2503
TA PACKAGE



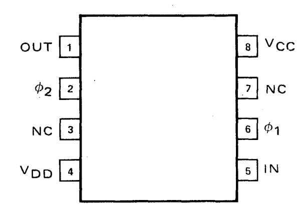
2504
TA PACKAGE



2503
V PACKAGE



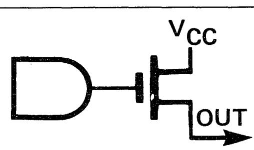
2504
V PACKAGE



DESCRIPTION

These Signetics 2500 Series 1024-bit multiplexed dynamic shift registers consist of enhancement mode P-channel MOS devices integrated on a single monolithic chip. Due to on-chip multiplexing, the data rate is twice the clock rate.

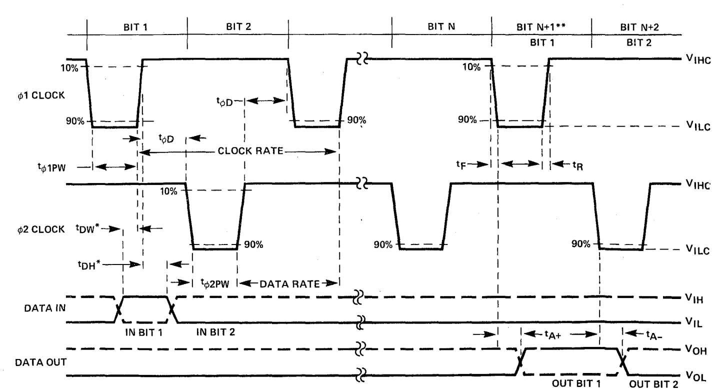
OUTPUT BUFFER



SWITCHING CHARACTERISTICS

	LIMITS		UNIT
	MIN	MAX	
t_{DO} DATA IN OVERLAP	10		NS

TIMING DIAGRAM

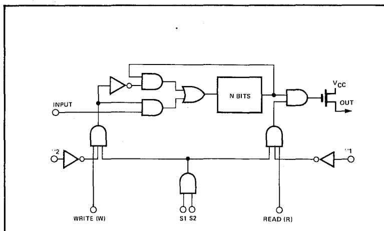


*t_{DW} and t_{DH} same for $t\phi 2$ **N = 256 for 1402A, N = 512 for 1403A, N = 1024 for 1404A

DESCRIPTION

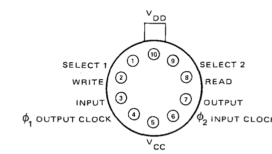
The 2512 1024-bit recirculating dynamic shift register consists of enhancement mode P-channel MOS devices integrated on a single monolithic chip. Internal recirculation logic plus write and read controls, together with two chip select controls are included on the chip.

BLOCK DIAGRAM

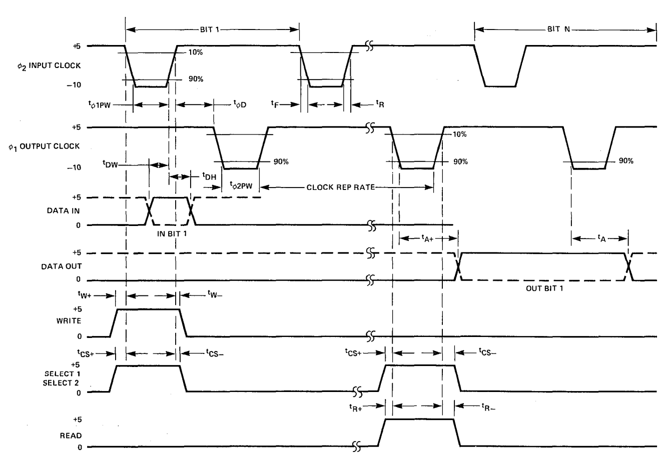


NOTES:
N = 1024 '0' = 0V, '1' = +5V.
When S1 or S2 is '0' Data Recirculates
When S1 and S2 are '1' see truth table

PIN CONFIGURATION



TIMING DIAGRAM



NOTE:
1. N=1024
2. Note that the Read Input is AND'ed with $\overline{\phi}_1$; therefore this function is not valid until ϕ_1 occurs.

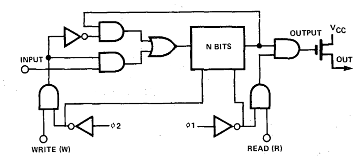
TRUTH TABLE

WRITE	READ	FUNCTION
0	0	Recirculate, Output is '0'
0	1	Recirculate, Output is Data
1	0	Write Mode, Output is '0'
1	1	Read/Write, Output is Data

DESCRIPTION

The 2525 1024-bit recirculating dynamic shift register consists of enhancement mode P-channel MOS devices integrated on a single monolithic chip. Internal recirculation logic plus write and read controls are included on the chip.

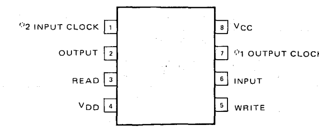
BLOCK DIAGRAM



NOTE
N = 1024 '0' = 0V, '1' = +5V.

PIN CONFIGURATION

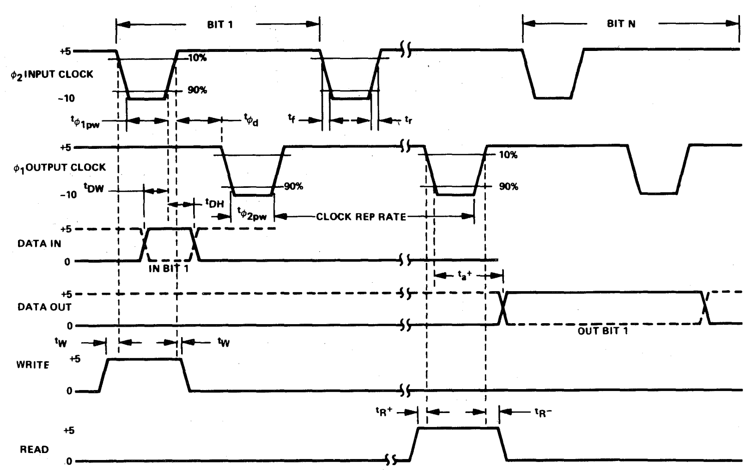
V PACKAGE



CONDITIONS OF TEST

Input rise and fall times: 10 ns Output load is 1 TTL gate

TIMING DIAGRAM



NOTE:
1. N = 1024
2. Note that the Read Input is AND'ed with $\overline{\phi_1}$; therefore this function is not valid until ϕ_1 occurs.

TRUTH TABLE

WRITE	READ	FUNCTION
0	0	Recirculate, Output is '0'
0	1	Recirculate, Output is Data
1	0	Write Mode, Output is '0'
1	1	Read Mode Output is Data

DESCRIPTION

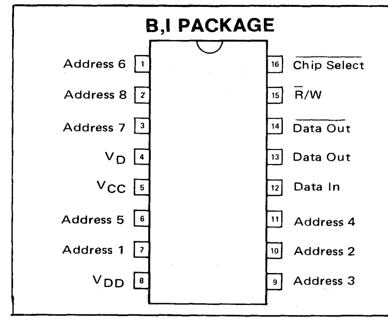
The Signetics 2500 Series 256-bit Random Access Memory employs enhancement mode P-channel MOS devices integrated on a single monolithic chip. It is fully decoded, permitting the use of a 16-pin dual in-line package. Complete static operation requires no clocking.

SWITCHING CHARACTERISTICS

Guaranteed Limits T_A = 0 to +70°C, V_{CC}=+5V ±5%, V_{DD} = V_D = -12V ±5%

READ CYCLE			WRITE CYCLE		
SYMBOL	TEST	LIMITS (μsec) MAX	SYMBOL	TEST	LIMITS (μsec) MIN.
t_a	Access Time	1μsec	t_{WD}	Address to Write Pulse Delay	0.3
			t_{WP}	Write Pulse Width	0.4
			t_W	Write Time	0.3
			t_{DO}	Data-Write Pulse Overlap	0.1

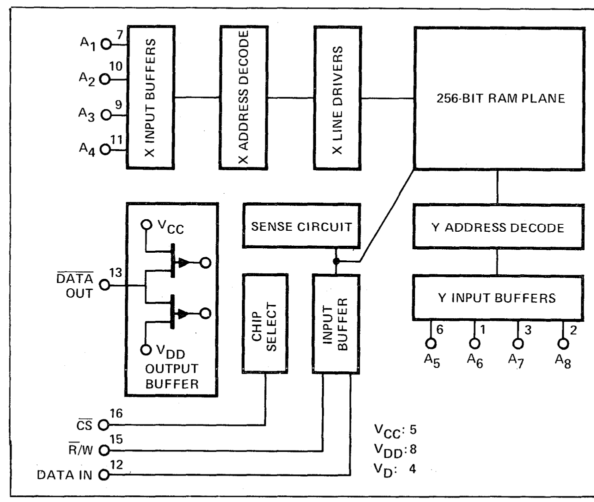
PIN CONFIGURATION



AC CONDITIONS OF TEST

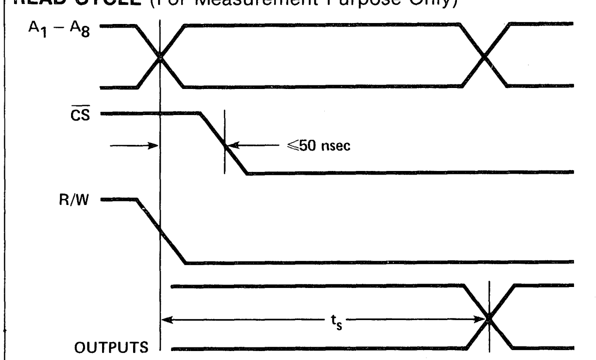
Input pulse amplitudes: 0 to +5V, Input pulse rise and fall times: < 10 nsec. Speed measurements referenced to 1.5V levels. Output load is 1 TTL gate; measurements made at output of TTL gate (t_{pd} ⩽ 10 nsec)

BLOCK DIAGRAM

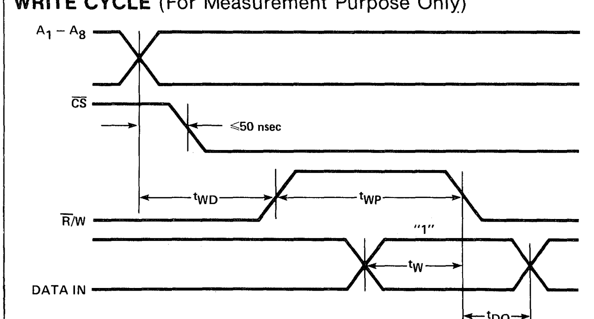


NOTE:
The 25L01 is available which will reduce the I_{DD} to 9mA at 25°C. I_D reduces to 16mA at 25°C and I_{OL} = 0mA at 25°C.

READ CYCLE (For Measurement Purpose Only)



WRITE CYCLE (For Measurement Purpose Only)



POWER DISSIPATION

The maximum power dissipation of 1.7 mW/bit is required only during Read or Write. For standby operation 100 μW/bit is obtained by removing V_D and reducing V_{DD} to -8.0V.

2101-F • 2101-1-F • 2101-2-F • 2601-F

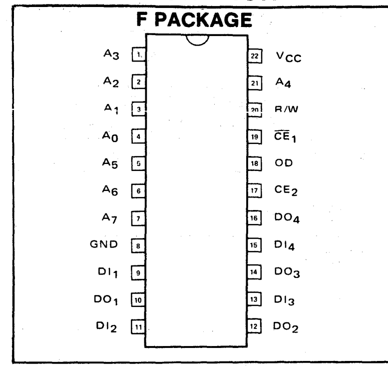
DESCRIPTION

The 2101 series and the 2601 are 1024-bit high performance, low power static read/write RAMs organized as 256 words by 4 bits.

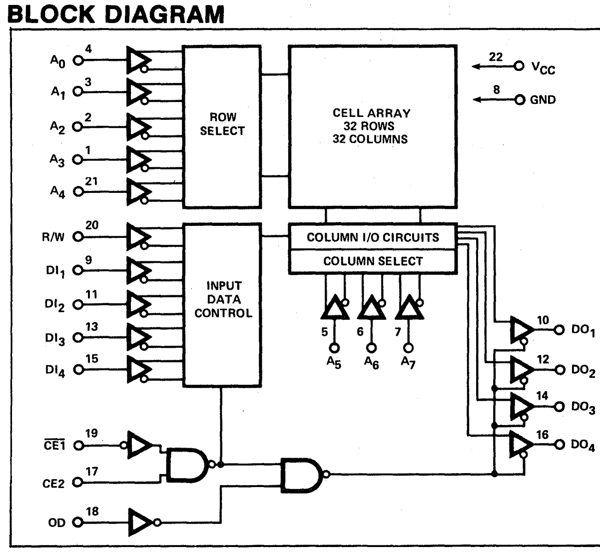
The 2101 series and the 2601 are fully static and no refresh operations, sense amplifiers, or clocks are required. All inputs and outputs are directly TTL-compatible and only one +5V power supply is required.

The 2101 series and the 2601 are fabricated with N-channel silicon gate technology which allows the design of high performance easy to use MOS circuits and provides a high functional density on a given monolithic chip.

PIN CONFIGURATION



BLOCK DIAGRAM



SWITCHING CHARACTERISTICS for 2101,2101-1,2101-2,2601

T_A = 0°C to 70°C, V_{CC} = 5V ±5%, unless otherwise specified.

READ CYCLE

	Parameter	Test Conditions	2101 Min.	2101 Max.	2101-1 Min.	2101-1 Max.	2101-2 Min.	2101-2 Max.	2601 Min.	2601 Max.	Unit
t_{RC}	Read Cycle		1,000		500		650		400		ns
t_A	Access Time	t_r, t_f = 20ns		1,000		500		650		400	ns
t_{CO}	Chip Enable To Output	V_{IN} = +0.65V to +2.2V		800		350		400		175	ns
t_{OD}	Output Disable To Output	Timing Reference = 1.5V		700		300		350		150	ns
t_{DF} (3)	Data Output to High Z State	Load = 1 TTL Gate	0	200	0	150	0	150		125	ns
t_{OH}	Previous Read Data Valid after change of Address	and C_L = 100pF.	40		40		40		40		ns

WRITE CYCLE

	Parameter	Test Conditions	2101 Min.	2101 Max.	2101-1 Min.	2101-1 Max.	2101-2 Min.	2101-2 Max.	2601 Min.	2601 Max.	Unit
t_{WC}	Write Cycle		1,000		500		650		400		ns
t_{AW}	Write Delay	t_r, t_f = 20ns	150		100		150			400	ns
t_{CW}	Chip Enable To Write	V_{IN} = +0.65V to +2.2V	900		400		550		150		ns
t_{DW}	Data Setup	Timing Reference = 1.5V	700		280		400		125		ns
t_{DH}	Data Hold	Load = 1 TTL Gate	100		100		100		50		ns
t_{WP}	Write Pulse	and C_L = 100pF.	750		300		400		150		ns
t_{WR}	Write Recovery		50		50		50		0		ns
t_{DS}	Output Disable Setup		200		150		150		150		ns

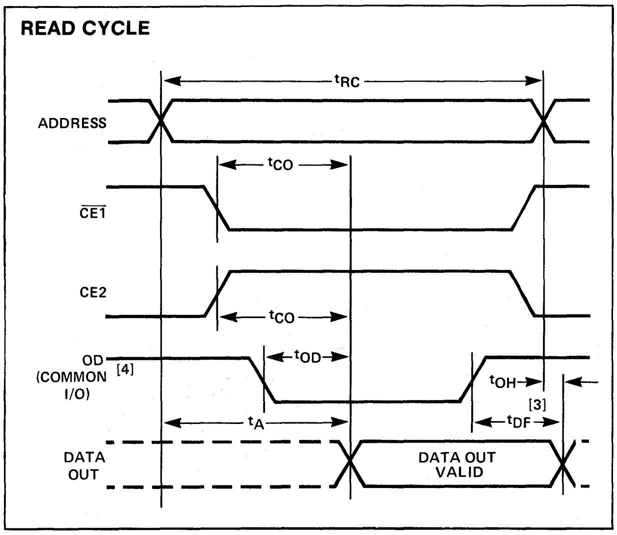
CAPACITANCE (2) $T_A = 25°C$, f = 1 MHz

Parameter		Limits (pF)	
		Typ. (1)	Max.
C_{IN}	Input Capacitance (All Input Pins) $V_{IN} = 0V$	4	8
C_{OUT}	Output Capacitance $V_{OUT} = 0V$	8	12

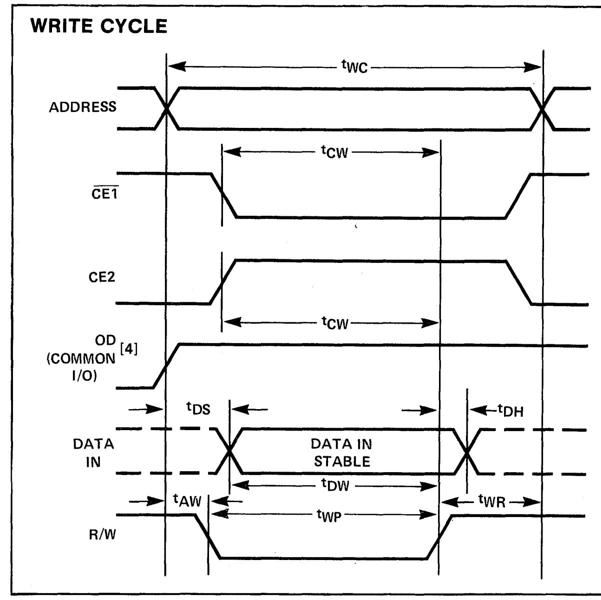
AC CONDITIONS OF TEST

Input Pulse Levels:	+0.65 Volt to 2.2 Volt
Input Pulse Rise and Fall Times:	20ns
Timing Measurement Reference Level:	1.5 Volt
Output Load:	1 TTL Gate and C_L = 100pF

WAVEFORMS



NOTES:
1. Typical values are for T_A = 25°C and nominal supply voltage.
2. This parameter is periodically sampled and is not 100% tested.
3. t_{DF} is with respect to the trailing edge of $\overline{CE}_1$, CE_2, or OD, whichever occurs first.
4. CD should be tied low for separate I/O operation.



2111 • 2111-1 • 2111-2 • 2611-XA, IK

DESCRIPTION

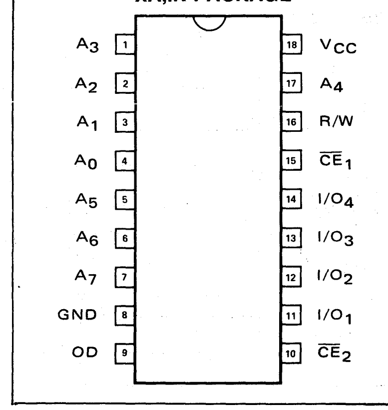
The 2111 series are 1024-bit high performance, low power static read/write RAMS organized as 256 words by 4 bits.

The 2111 series are fully static and no refresh operations, sense amplifiers, or clocks are required. All inputs and outputs are directly TTL-compatible and only one +5V power supply is required.

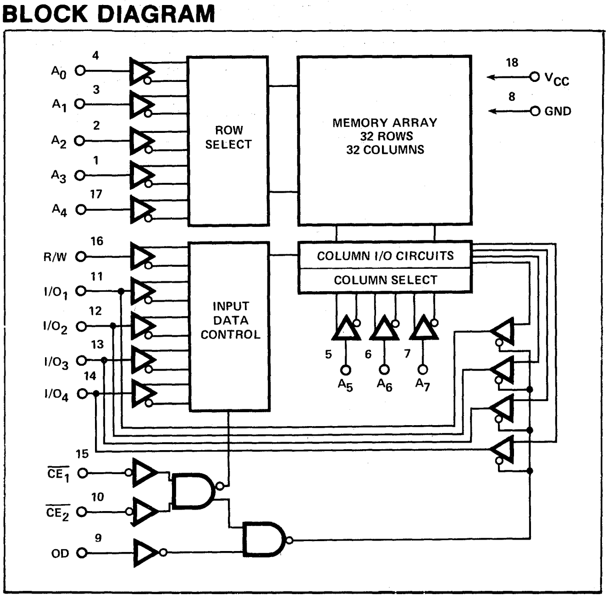
The 2111 series is fabricated with N-channel silicon gate technology which allows the design of high performance easy to use MOS circuits and provides a high functional density on a given monolithic chip.

PIN CONFIGURATION

XA,IK PACKAGE



BLOCK DIAGRAM

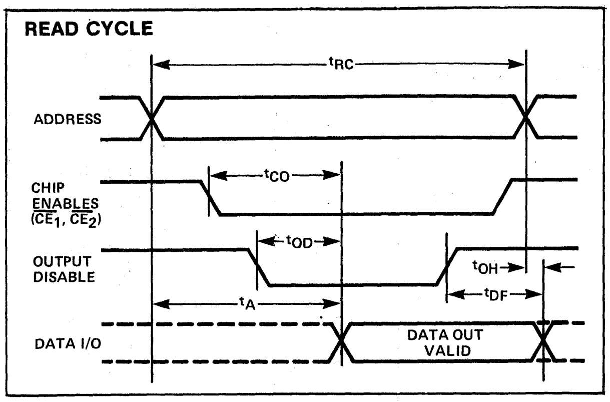


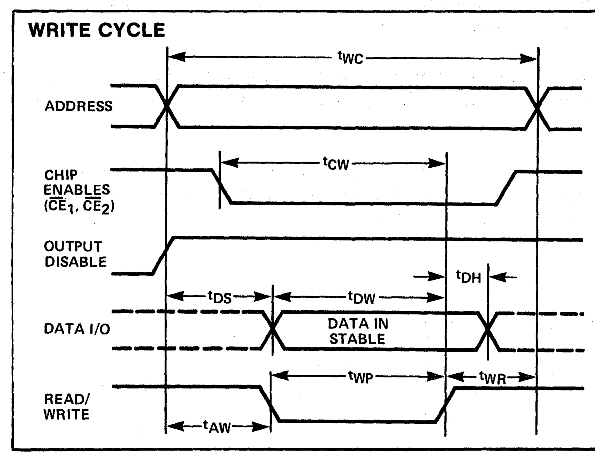
MEMORIES

SWITCHING CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = 5V ±5%, unless otherwise specified.

	Parameter	Test Conditions	2111 Min.	2111 Max.	2111-1 Min.	2111-1 Max.	2111-2 Min.	2111-2 Max.	2611 Min.	2611 Max.	Unit
READ CYCLE											
t_{RC}	Read Cycle		1,000		500		650		400		ns
t_A	Access Time	t_r, t_f = 20ns		1,000		500		650		400	ns
t_{CC}	Chip Enable To Output	V_{IN} = +0.65V to +2.2V		800		350		400		175	ns
t_{OD}	Output Disable To Output	Timing Reference = 1.5V		700		300		350		150	ns
t_{DF} (3)	Data Output to High Z State	Load = 1 TTL Gate	0	200	0	150	0	150		125	ns
t_{OH}	Previous Read Data Valid after change of Address	and C_L = 100pF.	40		40		40		40		ns
WRITE CYCLE											
t_{WC}	Write Cycle		1,000		500		650		400		ns
t_{AW}	Write Delay	t_r, t_f = 20ns	150		100		150			400	ns
t_{CW}	Chip Enable To Write	V_{IN} = +0.65V to +2.2V	900		400		550		150		ns
t_{DW}	Data Setup	Timing Reference = 1.5V	700		280		400		125		ns
t_{DH}	Data Hold	Load = 1 TTL Gate	100		100		100		50		ns
t_{WP}	Write Pulse	and C_L = 100pF.	750		300		400		150		ns
t_{WR}	Write Recovery		50		50		50		0		ns
t_{DS}	Output Disable Setup		200		150		150		150		ns


READ CYCLE
tRC
ADDRESS
CHIP ENABLES (CE1, CE2)
tCO
OUTPUT DISABLE
tOD
tOH
tDF
tA
DATA I/O
DATA OUT VALID


WRITE CYCLE
tWC
ADDRESS
CHIP ENABLES (CE1, CE2)
tCW
OUTPUT DISABLE
tDH
tDS
tDW
DATA I/O
DATA IN STABLE
tWP
tWR
READ/ WRITE
tAW

2112-F,B•2112-1-F,B•2112-2-F,B•2612-F,B

DESCRIPTION

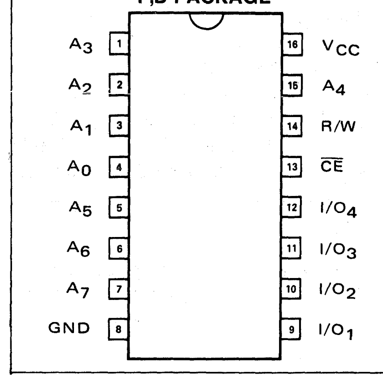
The 2112 series and the 2612 are 1024-bit high performance, low power static read/write RAMs organized as 256 words by 4 bits.

The 2112 series and the 2612 are fully static and no refresh operations, sense amplifiers, or clocks are required. All inputs and outputs are directly TTL-compatible and only one +5V power supply is required.

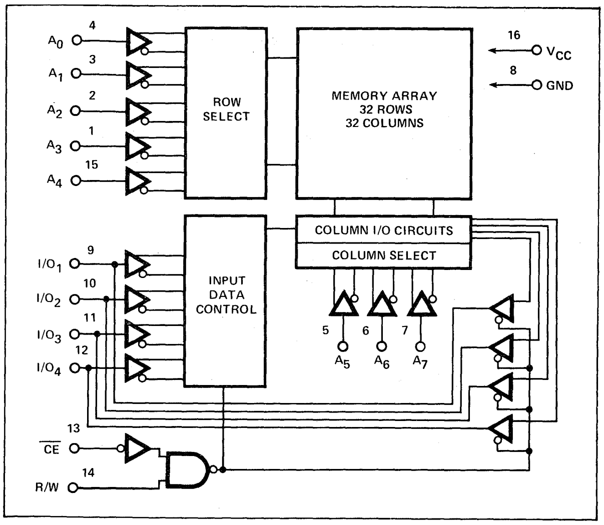
The 2112 series and the 2612 are fabricated with N-channel silicon gate technology which allows the design of high performance easy to use MOS circuits and provides a high functional density on a given monolithic chip.

PIN CONFIGURATION

F,B PACKAGE



BLOCK DIAGRAM



CAPACITANCE[2] T_A = 25°C, f = 1 MHz

Symbol	Test	Limits (pF)	
		Typ.[1]	Max.
C_{IN}	Input Capacitance (All Input Pins) V_{IN} = 0V	4	8
$C_{I/O}$	I/O Capacitance $V_{I/O}$ = 0V	10	15

NOTES:
1. Typical values are for T_A = 25°C and nominal supply voltage.
2. This parameter is periodically sampled and is not 100% tested.

SWITCHING CHARACTERISTICS for 2112,2112-2,2612

WRITE CYCLE #1 T_A = 0°C to 70°C, VCC = 5V ±5%

Parameter		Test Conditions	2112		2112-2		2612		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
t_{WC1}	Write Cycle	t_r, t_f = 20ns	850		500		400		ns
t_{AW1}	Address to Write Setup Time	V_{IN} = +0.65V to +2.2V	150		100		100		ns
t_{DW1}	Write Setup Time	Timing Reference = 1.5V	650		280		150		ns
t_{WP1}	Write Pulse Width	Load = 1 TTL Gate	650		350		150		ns
t_{CS1}	Chip Enable Setup Time	and C_L = 100pF.	0		0		0		ns
t_{CH1}	Chip Enable Hold Time		0		0		0		ns
t_{WR1}	Write Recovery Time		50		50		50		ns
t_{DH1}	Data Hold Time		100		50		50		ns
t_{CW1}	Chip Enable To Write Setup Time		650		350		150		ns

WRITE CYCLE #2 T_A = 0°C to 70°C, VCC = 5V ±5%

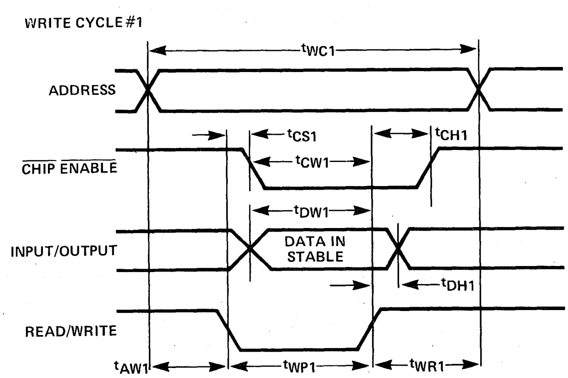
Parameter		Test Conditions	Min.	Max.	Min.	Max.	Min.	Max.	Unit
t_{WC2}	Write Cycle	t_r, t_f = 20ns	1050		650		550		ns
t_{AW2}	Address To Write Setup Time	V_{IN} = +0.65V to +2.2V	150		100		100		ns
t_{DW2}	Write Setup Time	Timing Reference = 1.5V	650		280		150		ns
t_{WD2}	Write To Output Disable Time	Load = 1 TTL Gate	200		200		200		ns
t_{CS2}	Chip Enable Setup Time	and C_L = 100pF.	0		0		0		ns
t_{CH2}	Chip Enable Hold Time		0		0		0		ns
t_{WR2}	Write Recovery Time		50		50		50		ns
t_{DH2}	Data Hold Time		100		50		50		ns

SWITCHING CHARACTERISTICS T_A = 0° to 70°C, VCC = 5V ±5% unless otherwise specified.

Read Cycle	Parameter	Test Conditions	2112		2112-2		2612		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
t_{RC}	Read Cycle	t_r, t_f = 20ns	1,000		650		400		ns
t_A	Access Time	VIN = +0.65V to +2.2V		1,000		650		400	ns
t_{CO}	Chip Enable To Output Time	Timing Reference = 1.5V		800		500		150	ns
t_{CD}	Chip Enable To Output Disable Time	Load = 1 TTL Gate	0	200	0	150		100	ns
t_{OH}	Previous Read Data Valid After	and C_L = 100pF.	40		40		40		ns

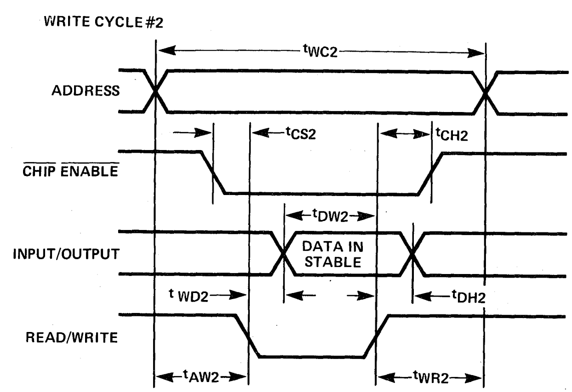
SWITCHING WAVEFORMS

WRITE CYCLE #1

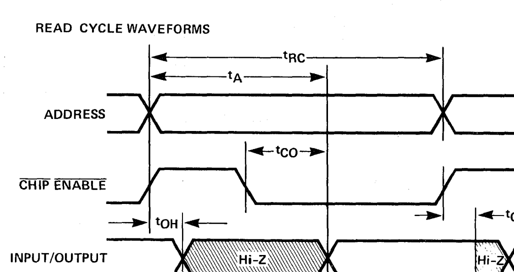


NOTE: Typical values are for T_A = 25°C and nominal supply voltage.

WRITE CYCLE #2



READ CYCLE WAVEFORMS



Notes:

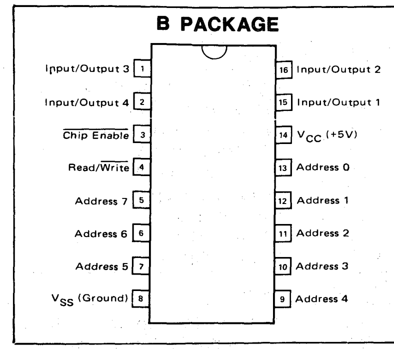
1. Output is enabled and t_{CO} commences only with both $\overline{CE}$ LOW and $\overline{WE}$ HIGH.
2. Output is disabled and t_{DF} combined from either the rising edge of $\overline{CE}$ or the falling edge of $\overline{WE}$.
3. Minimum t_{WP} is valid when $\overline{CE}$ has been HIGH at least t_{DF} before $\overline{WE}$ goes LOW. Otherwise t_{WP}(min.) = t_{DW}(min.) + t_{DF}(max.)
4. When $\overline{WE}$ goes HIGH at the end of the write cycle, it will be possible to turn on the output buffers if $\overline{CE}$ is still LOW. The data out will be the same as the data just written and so will not conflict with input data that may still be on the I/O bus.

2606-B • 2606-1-B

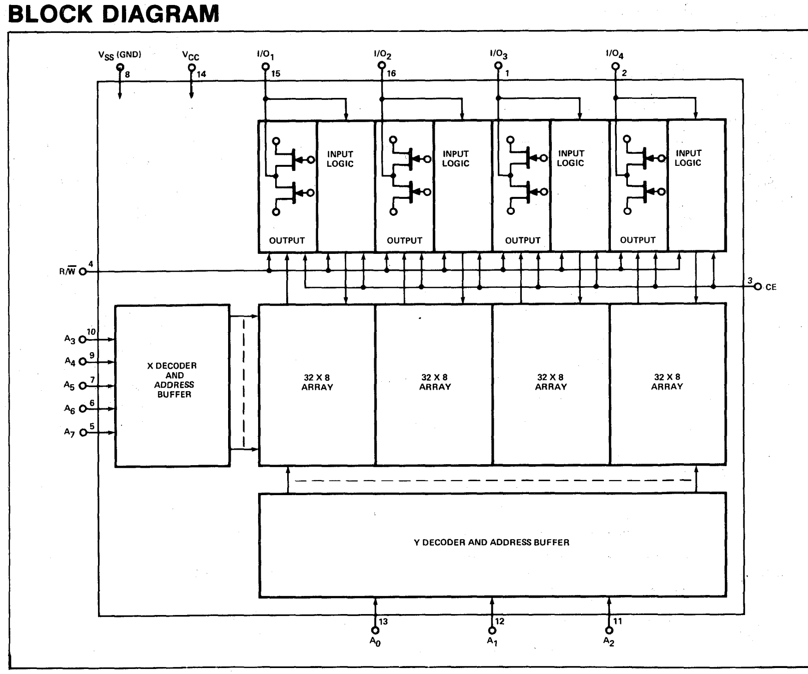
DESCRIPTION

The 2606 is a fully decoded, static, read/write, random access memory. It has a capacity of 1024-bits and is organized as 256 x 4. The 2606 is fabricated with N-Channel silicon gate MOS technology and achieves an access time of less than 750 nanoseconds. No clocks are required and all interface signals are directly TTL compatible including the power supply.

PIN CONFIGURATION



BLOCK DIAGRAM



2606-B • 2606-1-B

AC OPERATING CHARACTERISTICS

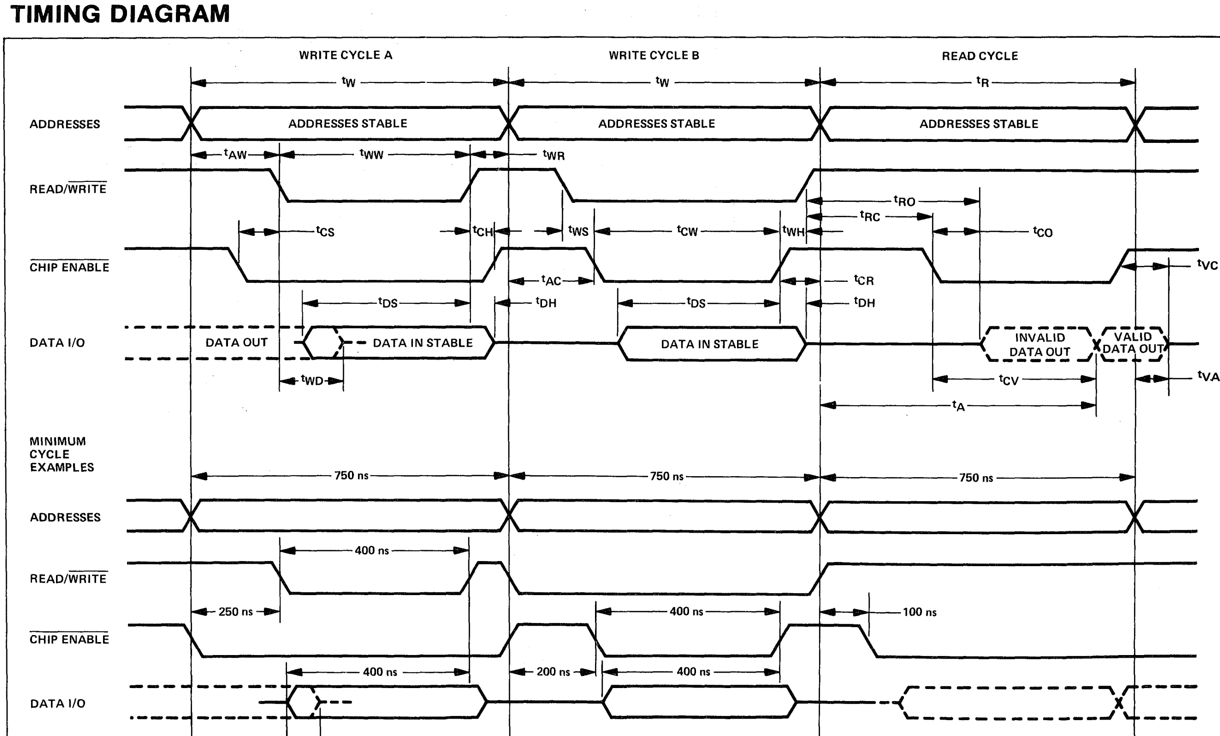
T_A = 0°C to 70°C, V_{CC} = +5V ± 5% unless otherwise specified. See Notes. E, F, G & H

		2606-1 (500 ns Cycle Time)				2606 (750 ns Cycle Time)			
WRITE CYCLE A		MIN	MAX	UNITS	NOTES	MIN	MAX	UNITS	NOTES
t_{AW}	Address to write time	150		ns		250		ns	
t_{WW}	Write pulse width	300		ns		400		ns	
t_{WR}	Write recovery time	50		ns		100		ns	
t_{CS}	Chip enable set-up	0		ns		0		ns	
t_{CH}	Chip enable hold	0		ns		0		ns	
t_{DS}	Data in set-up	280		ns		380		ns	
t_{DH}	Data in hold	0		ns	Note A	0		ns	Note A
t_{WD}	Write to data out disable delay		100	ns	Note D		125	ns	Note D
t_W	Write cycle time	500		ns		750		ns	
WRITE CYCLE B									
t_{AC}	Address to chip enable time	150		ns		250		ns	
t_{CW}	Chip enable pulse width	300		ns		400		ns	
t_{CR}	Chip enable recovery time	50		ns		100		ns	
t_{WS}	Write set-up	100		ns	Note B	200		ns	Note B
t_{WH}	Write hold	0		ns		0		ns	
t_{DS}	Data in set-up	280		ns		380		ns	
t_{DH}	Data in hold	0		ns	Note A	0		ns	Note A
t_W	Write cycle time	500		ns		750		ns	
READ CYCLE									
t_R	Read cycle time	500		ns		750		ns	
t_A	Access time		500	ns			750	ns	
t_{RO}	Read to output enabled	75		ns	Note C	100		ns	Note C
t_{CO}	Chip enable to output enable	0		ns	Note C	0		ns	Note C
t_{VC}	Previous data valid with respect to chip disable	0	100	ns		0	150	ns	
t_{VA}	Previous data valid with respect to address change	50		ns		50		ns	
t_{CV}	Chip enable to data valid delay		300	ns			400	ns	
t_{RC}	Read to chip enable	50		ns		100		ns	

NOTES

A. Maximum t_{DH} goverend by potential conflict with data out during next cycle.
B. Write set up required to prevent data overlap. For write cycle B the R/$\overline{W}$ line will typically change with the addresses.
C. R/$\overline{W}$ must be high and $\overline{CE}$ must be low in order for output buffers to turn on.
D. The output buffers will turn off within the specified time after write mode is selected.
E. Input levels swing between 0.65 volt and 2.2 volts.
F. Input signal transition times are 20 ns.
G. Timing reference level is 1.5 volts.
H. Bus load is 100 pF, one TTL input and one TTL tristate output.

TIMING DIAGRAM

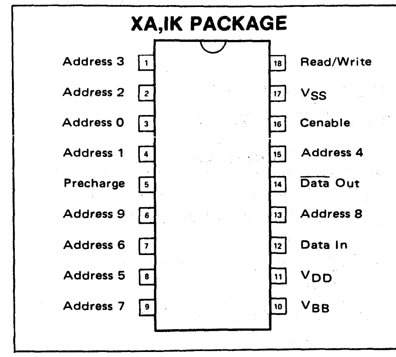


1103-XA, IK • 1103-1-XA, IK

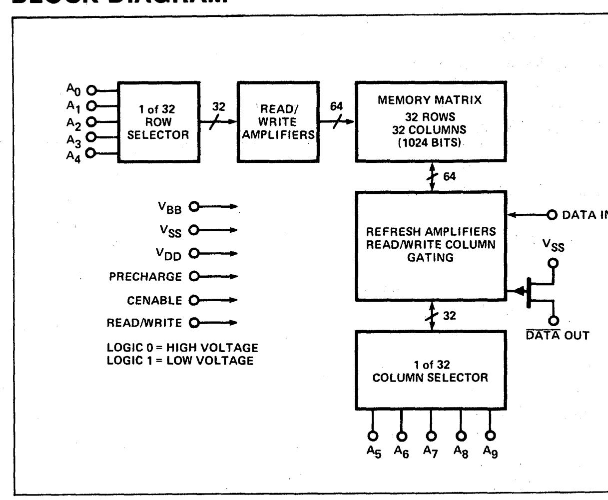
DESCRIPTION

The 1103 is designed for main memory applications where high performance, low cost and large bit storage are important design objectives. It is a 1024 word by 1 bit random access memory element using enhancement mode P-channel MOS devices integrated on a monolithic array. It is fully decoded, permitting the use of an 18-pin dual in-line package. The dynamic circuitry dissipates significant power only during precharge. Information stored in the memory is nondestructively read. Refreshing of all 1024 bits is accomplished in 32 read cycles and is required every two milliseconds. A separate cenable (chip enable) lead allows easy selection of an individual package when outputs are OR-tied. Use Signetics 8T25 Sense Amp, and 3207 Clock Driver.

PIN CONFIGURATION



BLOCK DIAGRAM



AC CHARACTERISTICS

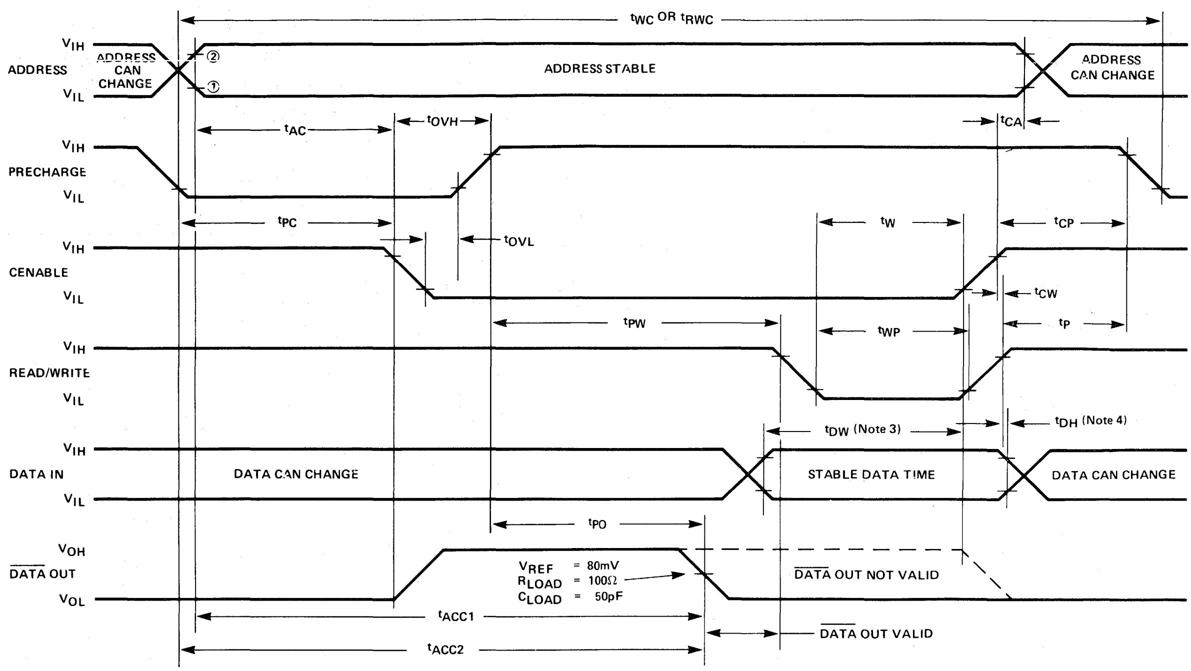
READ, WRITE, AND READ/WRITE CYCLE		1103 (1) T_A = D'C to +70°C V_{SS} = 16V ± 5% (V_{BB} - V_{SS}) = 3V to 4V V_{DD} = OV		1103-1 (3) T_A = 0°C to +55°C V_{SS} = 19V ± 5% (V_{BB} - V_{SS}) = 3V T04V V_{DD} = OV		
PARAMETER	**CONDITIONS**	**MIN**	**MAX**	**MIN**	**MAX**	**UNIT**
t_{REF} Time Between Refresh			2		1	ms
t_{AC} Address to Cenable Set Up Time		115		30		ns
t_{CA} Cenable to Address Hold Time		20		10		ns
t_{PC} Precharge to Cenable Delay		125		60		ns
t_{OVL} Precharge & Cenable Overlap, Low		25	75	5	30	ns
t_{CP} Cenable to Precharge Delay		85		40		ns
t_{OVH} Precharge & Cenable Overlap, High			140		85	ns
READ CYCLE						
t_{RC} Read Cycle	t_T = 20 ns; C_{LOAD} = 50 pF (100pF)*; R_{LOAD} = 100; V_{REF} = 80mV (40mV)*; *1103 only	480		300		ns
t_{POV} Precharge to End of Cenable	t_{ACmin} + t_{OVLmin} +t_{POmax} = 2t_T	165	500	115	500	ns
t_{PO} End of Precharge to Output Delay			120		75	ns
t_{ACC1} Address to Output Access	t_{PCmin} + t_{OVLmin} +t_{POmax} + 2 t_T	300		150		ns
t_{ACC2} Precharge to Output Access		310		180		ns
WRITE OR READ/WRITE CYCLE						
t_{WC} Write Cycle	t_T = 20 ns	580		340		ns
t_{RWC} Read/Write Cycle		580		340		ns
t_{PW} Precharge to Read/Write Delay		165	500	115	500	ns
t_{WP} Read/Write Pulse Width		50		20		ns
t_W Read/Write Set Up Time		80		20		ns
t_{DW} Data Set Up Time		105		40		ns
t_{DH} Data Hold Time		10		10		ns
t_{PO} End of Precharge to Output Delay			120		75	ns
t_{PO} End of Precharge to Output Delay	C_{LOAD} = 50pF (100pF)-*; R_{LOAD} = 100		120		75	ns
t_P Time to Next Precharge	V_{REF} = 80 mV (40mV)*	0		0		ns
t_{CW} Read/Write Hold Time	*1103 only		10		15	ns
CAPACITANCE (2)						
C_{AD} Address Capacitance	V_{IN} = V_{SS}; f =1MHz, All Unused Pins are at A.C. Ground		7		7	pF
C_{PR} Precharge Capacitance	V_{IN} = V_{SS}		18		18	pF
C_{CE} Cenable Capacitance	V_{IN} = V_{SS}		18		18	pF
C_{RW} Read/Write Capacitance	V_{IN} = V_{SS}		15		15	pF
C_{IN1} Data Input Capacitance	Cenable = 0V, V_{IN} = V_{SS}		5		5	pF
C_{IN2} Data Input Capacitance	Cenable = V_{SS}, V_{IN} = V_{SS}		4		4	pF
C_{OUT} Data Output Capacitance	V_{OUT} = 0V		3		3	pF

NOTES:

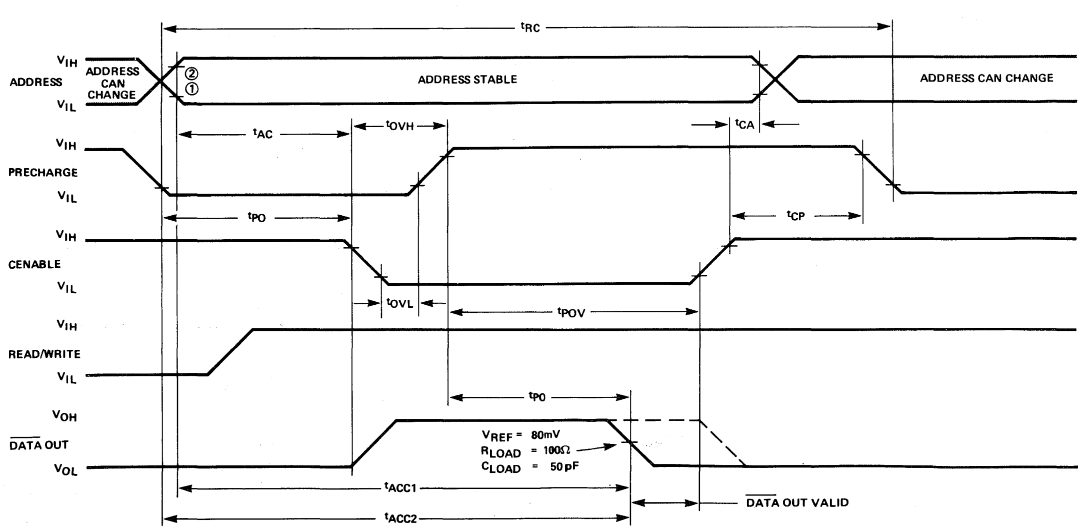
1. These times will degrade by 40ns (worst case) if the maximum values for VIL (for precharge, cenable and read/write inputs) go to V_{SS} - 14.2V @ 0°C and V_{SS} - 14.5V @ 70°C.
2. Thes parameter is periodically sampled and is not 100% tested. It is measured at worst case operating conditions. Capacitance measurements for plastic package only.
3. These times will degrade by 35ns if V_{REF} point of 40mV is chosen instead of the 80mV point defined in this specification.

TIMING DIAGRAM

WRITE CYCLE OR READ/WRITE CYCLE



READ CYCLE



NOTES:

1 $V_{DD}+2V$ ⎤ t_T is defined as the transitions between these two points.
2 $V_{SS}-2V$ ⎦

3 t_{DW} is referenced to point **1** of the rising edge of cenable or read/write whichever occurs first.

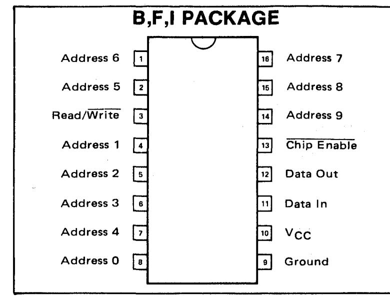
4 t_{DH} is referenced to point **2** of the rising edge of cenable or read/write whichever occurs first.

DESCRIPTION

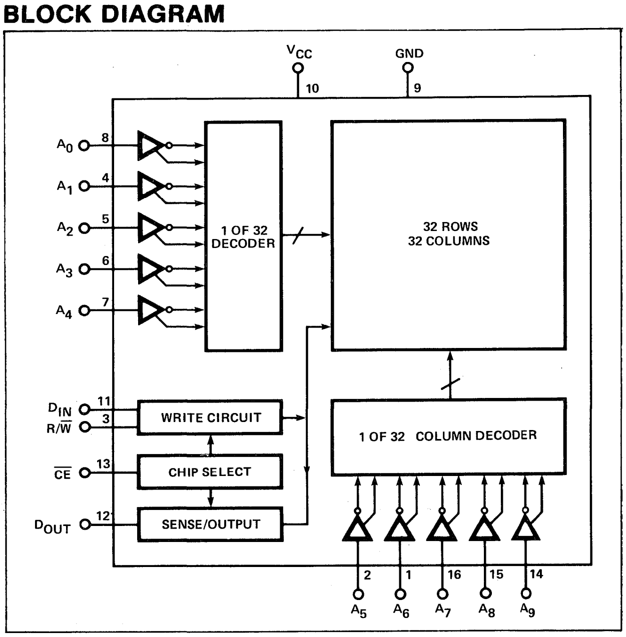
The Signetics 2102 is a static random access read/write memory offering a 1024x1 organization. Fabricated with low threshold N-Channel silicon gate technology.

The 2102 is fully static, requiring no clocks and is completely DTL/TTL compatible including the single +5V power supply requirement.

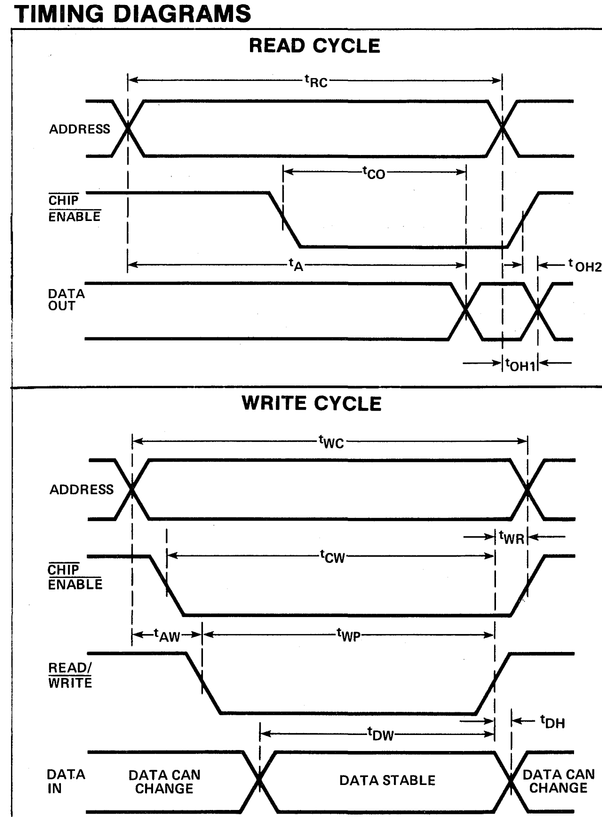
PIN CONFIGURATION



BLOCK DIAGRAM



TIMING DIAGRAMS



A.C. CONDITIONS OF TEST

Input Pulse Levels:	+0.65 Volt to +2.2 Volt
Input Pulse Rise and Fall Times:	20ns
Timing Measurement Reference Level:	1.5 Volt
Output Load:	1 TTL Gate and CL = 100pF

AC CHARACTERISTICS FOR THE 2102, 21L02-1, 21L02-2, 21F02

T_A-0°C to +70°C, V_{CC} = 5V ±5% unless otherwise specified

	READ CYCLE					WRITE CYCLE							Unit
	Read Cycle	Access Time	Chip Enable to Output Time	Previous Read Data Valid With Respect to Address	Previous Read Data Valid With Respect to Chip Enable	Write Cycle	Address to Write Set-up Time	Write Pulse Width	Write Recovery Time	Data Setup Time	Data Hold Time	Chip Enable to Write Set-up Time	
	tRC MIN	tA MAX	tCO MAX	tOH1 MIN	tOH2 MIN	tWC MIN	tAW MIN	tWP MIN	tWR MIN	tDW MIN	tDH MIN	tCW MIN	
2102	1000	1000	500	50	0	1000	200	750	50	800	100	900	ns
21L02-1	500	500	350	50	0	500	150	300	50	330	100	400	ns
21L02-3	400	400	300	50	0	400	100	250	50	300	50	300	ns
21F02	350	350	(180 TYP)[1]	(40TYP)[1]	0	350	(20 TYP)	(250 TYP)[1]	(20 TYP)[1]	(250 TYP)[1]	0	(250 TYP)[1]	ns

NOTE: 1. Typical values are for T_A = 25°C and nominal supply voltage

MEMORIES

2680 • 2680-1 • 2680-2-F

DESCRIPTION

Signetics 2680 is a 4096 word by 1 bit dynamic RAM. It incorporates the latest memory design features and can be used in a wide variety of applications, from those which require very high speed to ones where low cost and large bit capacity are the prime criteria.

The 2680 must be refreshed every 2 ms. This can be accomplished by performing a read cycle at each of the 64 row addresses (A0-A5). The chip select input can be either high or low for refresh.

The 2680 has been designed with minimum production costs as a prime criterion. It is fabricated using N-channel silicon gate MOS technology, which is an ideal choice for high density integrated circuits. The 2680 uses a single transistor cell to minimize the device area. The single device cell, along with unique design features in the on-chip peripheral circuits, yields a high performance and low cost memory device.

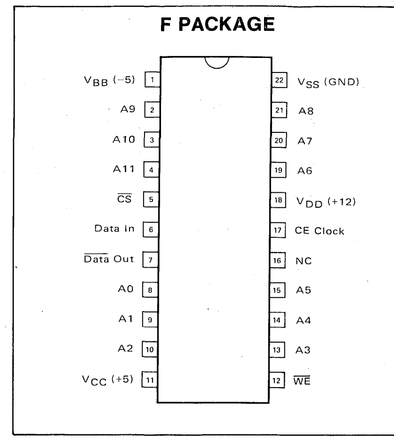
ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias	o° C to 70°C
Storage Temperature	-65°C to +150°C
All Input or Output Voltages with Respect to the most Negative Supply Voltage, V_{BB}	-20V to -0.3V
Supply Voltages V_{DD}, V_{CC}, and V_{SS} with Respect to V_{BB}	-20V to -0.3V
Power Dissipation	1.25W

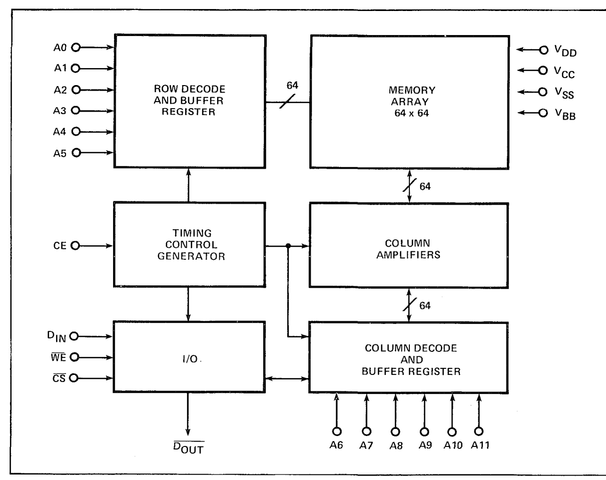
*COMMENT:

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PIN CONFIGURATION



BLOCK DIAGRAM



2680 • 2680-1 • 2680-2-F

RECOMMENDED OPERATING CONDITIONS (See Note)

PARAMETER	Min	Typ	Max	Unit
Supply voltage, V_{CC}	4.75	5	5.25	V
Supply voltage, V_{DD}	11.4	12	12.6	V
Supply voltage, V_{SS}		0		
Supply voltage, V_{BB}	-4.5	-5	-5.5	V

DC ELECTRICAL CHARACTERISTICS OVER FULL RANGES OF REC. OPER. COND.

Parameter		Limits			Unit	Conditions
		Min	Typ(2)	Max		
I_{LI}	Input Load Current (all inputs except CE)		.01	10	μA	$V_{IN} = V_{IL}$ Min to V_{IH} Max CE = V_{ILC} or V_{IHC}
I_{LC}	Input Load Current		.01	2	μA	$V_{IN} = V_{IL}$ Min to V_{IH} Max
I_{LO}	Output Leakage Current for high impedance state		.01	10	μA	CE = V_{ILC} or $\overline{CS} = V_{IH}$ V_O = 0V to 5.25V
I_{DD1}	VDD Supply Current during CE off(3)		50	200	μA	CE = -1V to +.6V
I_{DD2}	VDD Supply Current during CE on			60	mA	CE = V_{IHC}, $\overline{CS} = V_{IL}$
$I_{DD\ AV1}$	Average VDD Current		35	54	mA	Cycle time = 400ns, $\overline{CS} = V_{IL}$ t_{CE} = 230ns T_A = 25°C
I_{CC1} (4)	VCC Supply Current during CE off		.01	10	μA	CE = V_{ILC} or $\overline{CS} = V_{IH}$
I_{BB}	VBB Supply Current		5	100	μA	
V_{IL}	Input Low Voltage	-1.0		0.6	V	
V_{IH}	Input High Voltage	2.4		V_{CC} +1	V	
V_{ILC}	CE Input Low Voltage	-1.0		+1.0	V	
V_{IHC}	CE input High Voltage	V_{DD}-1		V_{DD} +1	V	
V_{OL}	Output Low Voltage	0.0		0.45	V	I_{OL} = 2.0mA
V_{OH}	Output High Voltage	2.4		V_{CC}	V	I_{OH} = -2.0mA

T_A = 0°C to 70°C (unless otherwise noted)

NOTES:

1. The only requirement for the sequence of applying voltage to the device is that V_{DD}, V_{CC}, and V_{SS} should never be .3V more negative than V_{BB}.
2. Typical values are for T_A = 25°C and nominal power supply voltages.
3. The I_{DD} and I_{CC} currents flow to V_{SS}. The I_{BB} current is the sum of all leakage currents.
4. During CE on V_{CC} supply current is dependent on output loading V_{CC} is connected to output buffer only.

CAPACITANCE[1] T_A = 25°C

Test		Typ	Max	Unit	Conditions
C_{AD}	Address Capacitance, CS	4	6	pF	$V_{IN} = V_{SS}$
C_{CE}	CE Capacitance	13	25	pF	$V_{IN} = V_{SS}$
C_{OUT}	Data Output Capacitance	4	7	pF	V_{OUT} = 0V
C_{IN}	Data Input and $\overline{WE}$ Capacitance	5	10	pF	$V_{IN} = V_{SS}$

Notes:

1. Capacitance measured with Boonton Meter or effective capacitance calculated from the equation

$$C = \frac{I \Delta t}{\Delta V}$$

with the current equal to a constant 20mA

MEMORIES

AC CHARACTERISTICS:
READ, MODIFY, WRITE CYCLE Over recommended supply voltage range, TA = 0°C to 70°C

PARAMETER		2680		2680-1		2680-2		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{RWC}	Read, Modify, Write (RMW) Cycle Time	520		590		960		ns
t_{CRW}	CE Width During RMW	350	4000	420	4000	540	4000	ns
t_{WC}	$\overline{WE}$ to CE ON	0		0		0		ns
t_W	$\overline{WE}$ to CE Off	150		150		200		ns
t_{WP}	$\overline{WE}$ Pulse Width	50		50		100		ns
t_{DW}	DIN to WE Set Up	0		0		0		ns
t_{DH}	DIN Hold Time	0		0		0		ns
t_{CO}	CE to Output Delay		180		250		320	ns
t_{ACC}	Access Time		200		270		350	ns

CONDITION:
t_T = 20ns, C_{load} = 50pf, Load = One TTL Gate, $t_{ACC} = t_{AC} + t_{CO} + 1t_T$.

READ CYCLE OVER REC. SUPPLY VOLTAGE RANGE TA = 0°C to 70°C

PARAMETER		2680		2680-1		2680-2		Unit
		Min	Max	Min	Max	Min	Max	
t_{CY}	Cycle Time	400		470		800		ns
t_{CE}	CE On Time	230	4000	300	4000	380	4000	ns
t_{CO}	CE Output Delay		180		250		320	ns
t_{ACC}	Address to Output Access		200		270		350	ns
t_{WL}	CE to $\overline{WE}$	0		0		0		ns
t_{WC}	$\overline{WE}$ to CE on	0		0		0		ns

t_T = 20ns, C_{load} = 50pF, Load = One TTL Gate, $t_{ACC} = t_{AC} + t_{CO} + 1t_T$

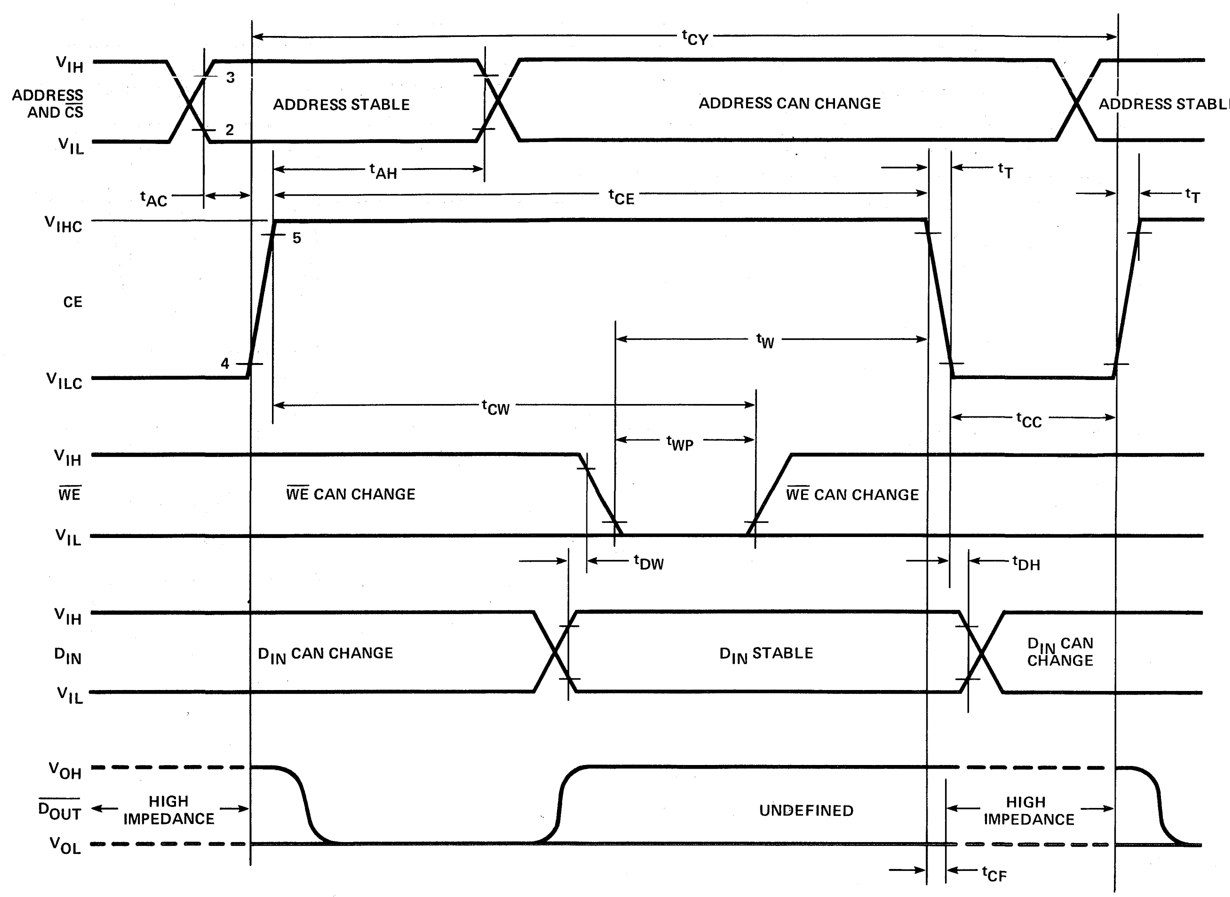
WRITE CYCLE OVER REC. SUPPLY VOLTAGE RANGE TA = 0°C to 70°C

PARAMETER		2680		2680-1		2680-2		Unit
		Min	Max	Min	Max	Min	Max	
t_{CY}	Cycle Time	400		470		800		ns
t_{CE}	CE On Time	230	4000	300	4000	380	4000	ns
t_W	WE to CE Off	150		150		200		ns
t_{CW}	CE to $\overline{WE}$	150		150		150		ns
$t_{DW(1)}$	DIN to $\overline{WE}$ Set Up	0		0		0		ns
t_{DH}	DIN Hold Time	0		0		0		ns
t_{WE}	$\overline{WE}$ Pulse Width	50		50		100		ns

t_T = 20ns

NOTE:
1. If $\overline{WE}$ is low before CE goes high then DIN must be valid when CE goes high.

WRITE CYCLE

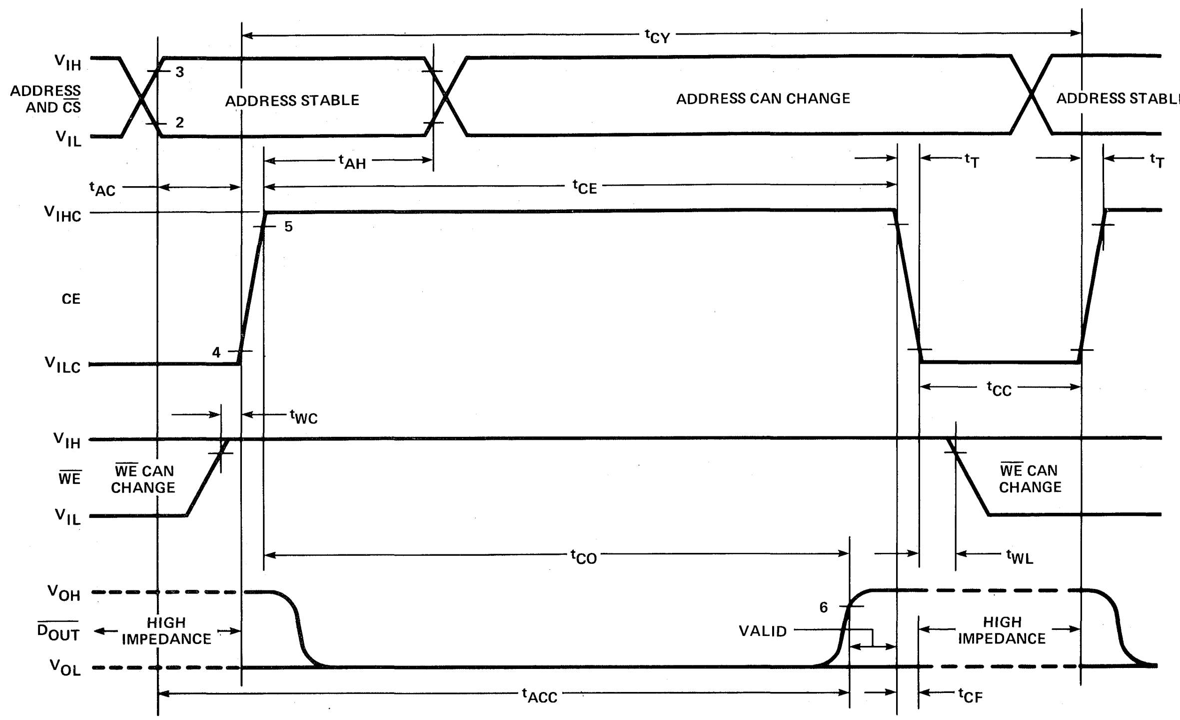


NOTES:

1. For Refresh cycle row and column addresses must be stable before t_{AC} and remain stable for entire t_{AH} period.
2. V_{IL} MAX is the reference level for measuring timing of the addresses, $\overline{CS}$, $\overline{WE}$, and D_{IN}.
3. V_{IH} MIN is the reference level for measuring timing of the addresses, $\overline{CS}$, $\overline{WE}$, and D_{IN}.
4. V_{SS} +2.0V is the reference level for measuring timing of CE.
5. V_{DD} -2V is the reference level for measuring timing of CE.
6. V_{SS} +2.4V is the reference level for measuring the timing of D_{OUT}.

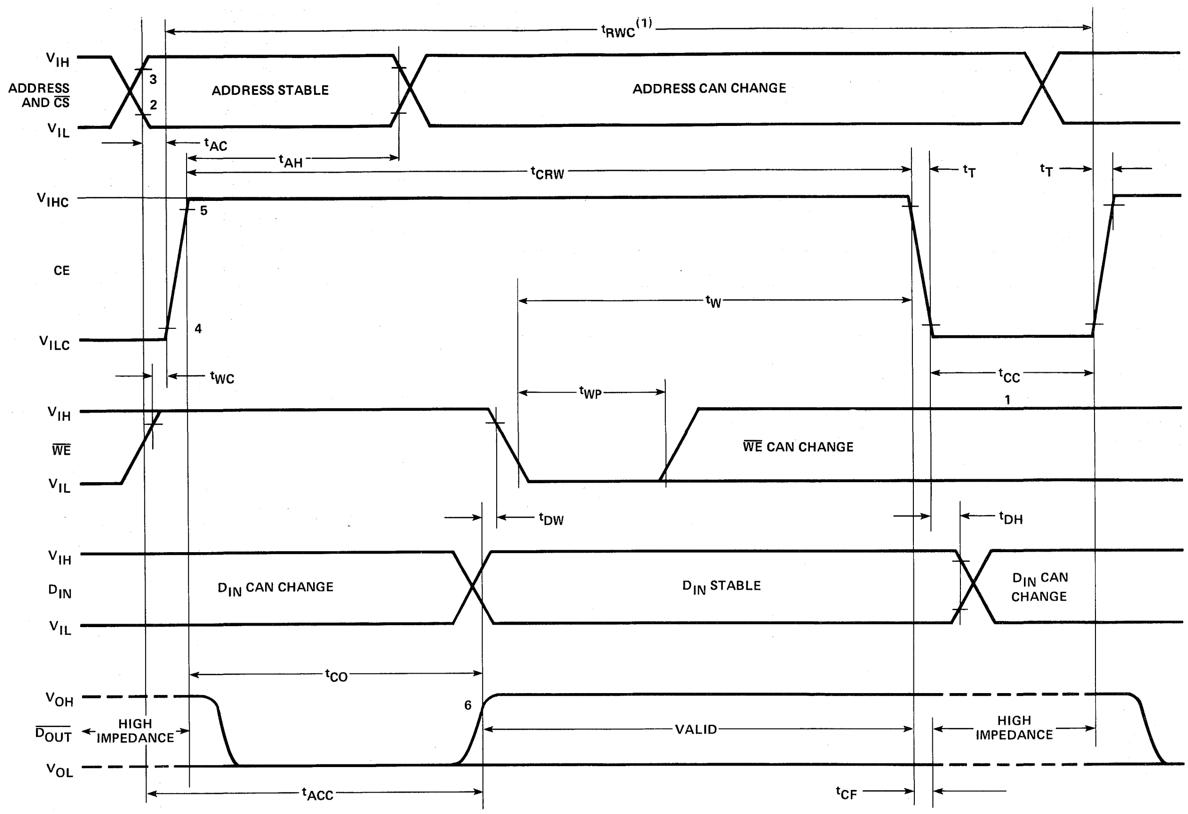
2680 • 2680-1 • 2680-2-F

READ AND REFRESH CYCLE[1]



NOTES:
1. For Refresh cycle row and column addresses must be stable before t_{AC} and remain stable for entire t_{AH} period.
2. V_{IL} MAX is the reference level for measuring timing of the addresses, $\overline{CS}$, $\overline{WE}$, and D_{IN}.
3. V_{IH} MIN is the reference level for measuring timing of the addresses, $\overline{CS}$, $\overline{WE}$, and D_{IN}.
4. V_{SS} +2.0V is the reference level for measuring timing of CE.
5. V_{DD} -2V is the reference level for measuring timing of CE.
6. V_{SS} +2.4V is the reference level for measuring the timing of D_{OUT}.

READ, MODIFY, WRITE CYCLE



NOTES:
1. For refresh cycle row and column addresses must be stable before t_{AC} and remain stable for entire t_{AH} period.
2. V_{IL} MAX is the reference level for measuring timing of the addresses, $\overline{CS}$, $\overline{WE}$, and DI_N.
3. V_{IH} MIN is the reference level for measuring timing of the addresses, $\overline{CS}$, $\overline{WE}$, and DI_N.
4. V_{SS} +2.0V is the reference level for measuring timing of CE.
5. V_{DD} -2.0V is the reference level for measuring timing of CE.
6. V_{SS} +2.4V is the reference level for measuring the timing of D_{OUT}.
7. $\overline{WE}$ must be at V_{IH} until end of t_{CO}.

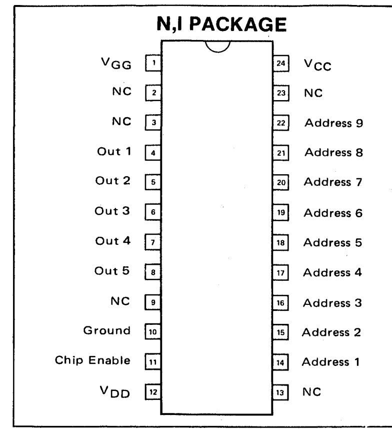
2513-N,I

DESCRIPTION

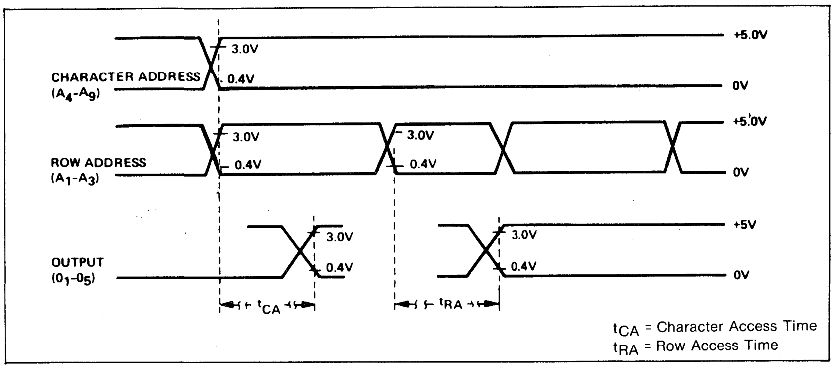
The Signetics 2513 is a high speed 2560-bit Static ROM organized as 64x8x5. A standard 7x5 dot matrix fits well in the 2513. The product uses +5V, -5V and -12V power supplies, TTL level interface signals and Tri-State Outputs for direct, low cost interfacing with TTL, DTL, CMOS and 2500 Series MOS.

CE	OUTPUT
0	DATA
1	OPEN

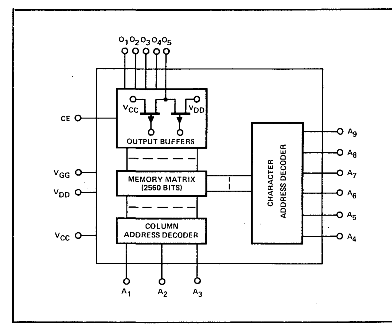
PIN CONFIGURATION



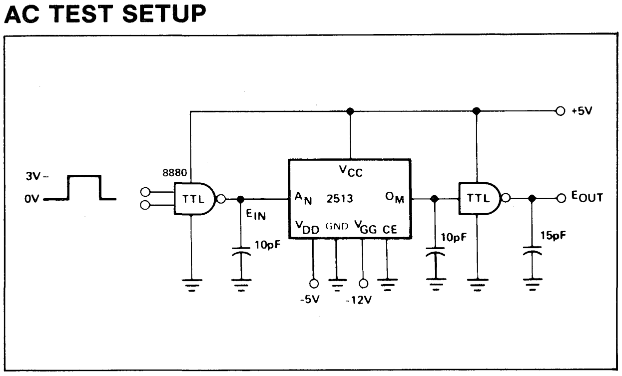
TIMING DIAGRAM



BLOCK DIAGRAM



AC TEST SETUP



AC CHARACTERISTICS

SYMBOL	TEST	MIN	TYP	MAX	UNIT
$t_{CA(CM2140)}$	Character Access Time			600	ns
t_{RA}	Row Access Time (A_1 - A_3)			500	ns
t_{CE}	Chip Enable to Output				ns

T_A = 0°C to •70°C; V_{CC} = 5V (Note 8): V_{DD} = -5V ± 5%; V_{GG} = -12V ± 5%; unless otherwise noted.

COMPANY____________________

ADDRESS____________________

CITY__________ STATE ______ ZIP______

TELEPHONE____________________

AUTHORIZED SIGNATURE ____________________

DATE ____________________

CUSTOMER PRINT OR ID NO.____________________

PURCHASE ORDER NUMBER____________________

DEVICE TYPE________2513________

CUSTOM PATTERN NUMBER (TO BE ENTERED BY SIGNETICS)____________________

CHARACTER FORMAT

ROW ADDRESS

ROW ADDRESS			OUTPUTS				
A_3	A_2	A_1	O_5	O_4	O_3	O_2	O_1
0	0	0	0	0	0	0	0
0	0	1	0	1	1	1	0
0	1	0	1	0	0	0	1
0	1	1	1	0	0	0	0
1	0	0	0	1	1	1	0
1	0	1	0	0	0	0	1
1	1	0	1	0	0	0	1
1	1	1	0	1	1	1	0

EXAMPLE 'S'

FIGURE 1

ORGANIZATION AS CHARACTER GENERATOR

A six-bit binary address (A4 through A9) selects 1-of-64 matrix characters arranged 5 dots horizontally and 8 dots vertically. A three bit binary address code (A1 through A3) selects 1 of 8 rows. Five outputs display a complete row of the character matrix. See Figure 1. The devices may also be used in pairs to provide 9 X 7 and 10 X 8 vertical scan formats.

CHARACTER ADDRESS

	COLUMN ADDRESS					
	A_4	A_5	A_6	A_7	A_8	A_9
ASCII CHARACTER	1	1	0	0	1	0

FIGURE 2

ORGANIZATION AS READ-ONLY MEMORY

For a straight 512 X 5 read-only memory, the five outputs will display any one of 512 5-bit stored words corresponding to a 9-bit address applied to A_1 through A_9.

CUSTOM DEVICES

For unique custom memory patterns, this form should be used to transmit coding instructions. The nomenclature for a custom device will consist of he basic product type followed by a unique CM number assigned by Signetics. For example, "2513N/CM2141".

- **PROGRAMMING WITH PUNCHED CARDS**

For maximum accuracy and minimum cost and turn-around time, the truth table should be transmitted to Signetics in the form of punched cards according to the format indicated on the following pages.

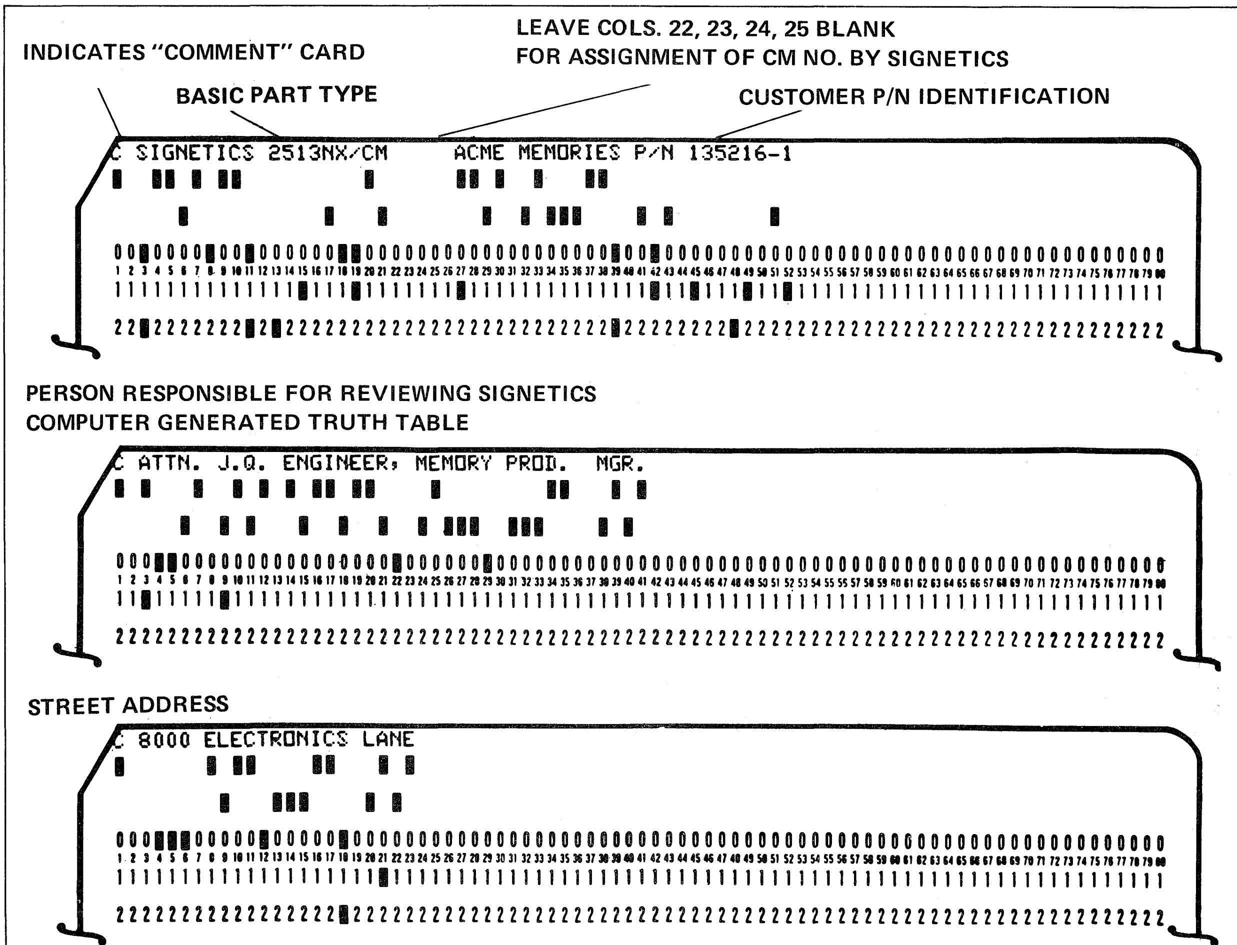
VERIFICATION

Upon receipt of either punched card or written truth table information, Signetics will prepare a computer tabulation of the instructions and return to the address indicated. If errors are detected, they should be transmitted to Signetics as quickly as possible.

LOGIC CONVENTION

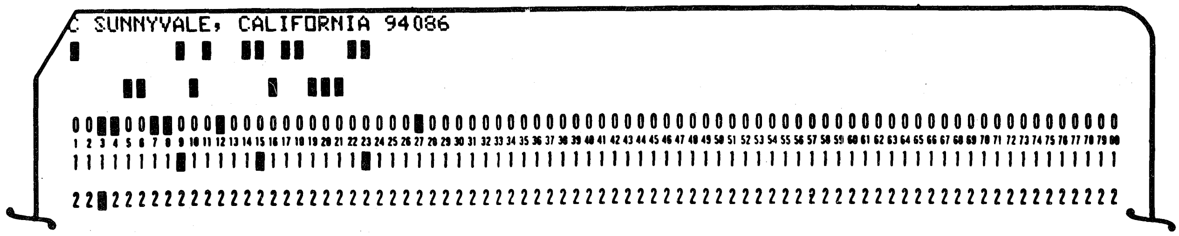
Logic "1"s or blackened squares in the truth table will result in "high" output from the indicated output terminal (i.e. 3.2V minimum). Similarly, a "1" address input level is interpreted as 3.2V minimum.

IDENTIFICATION CARDS

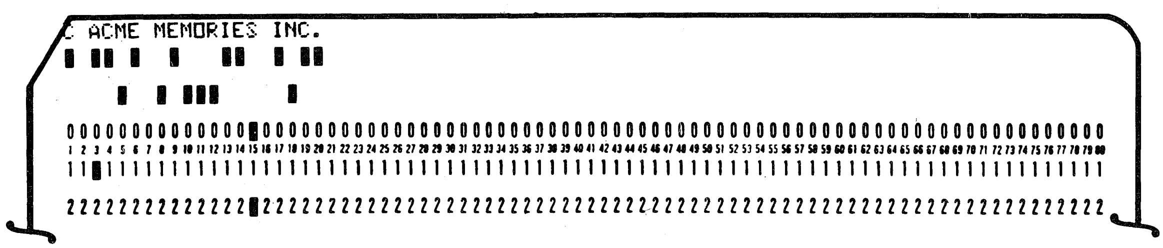


IDENTIFICATION CARDS (Cont'd)

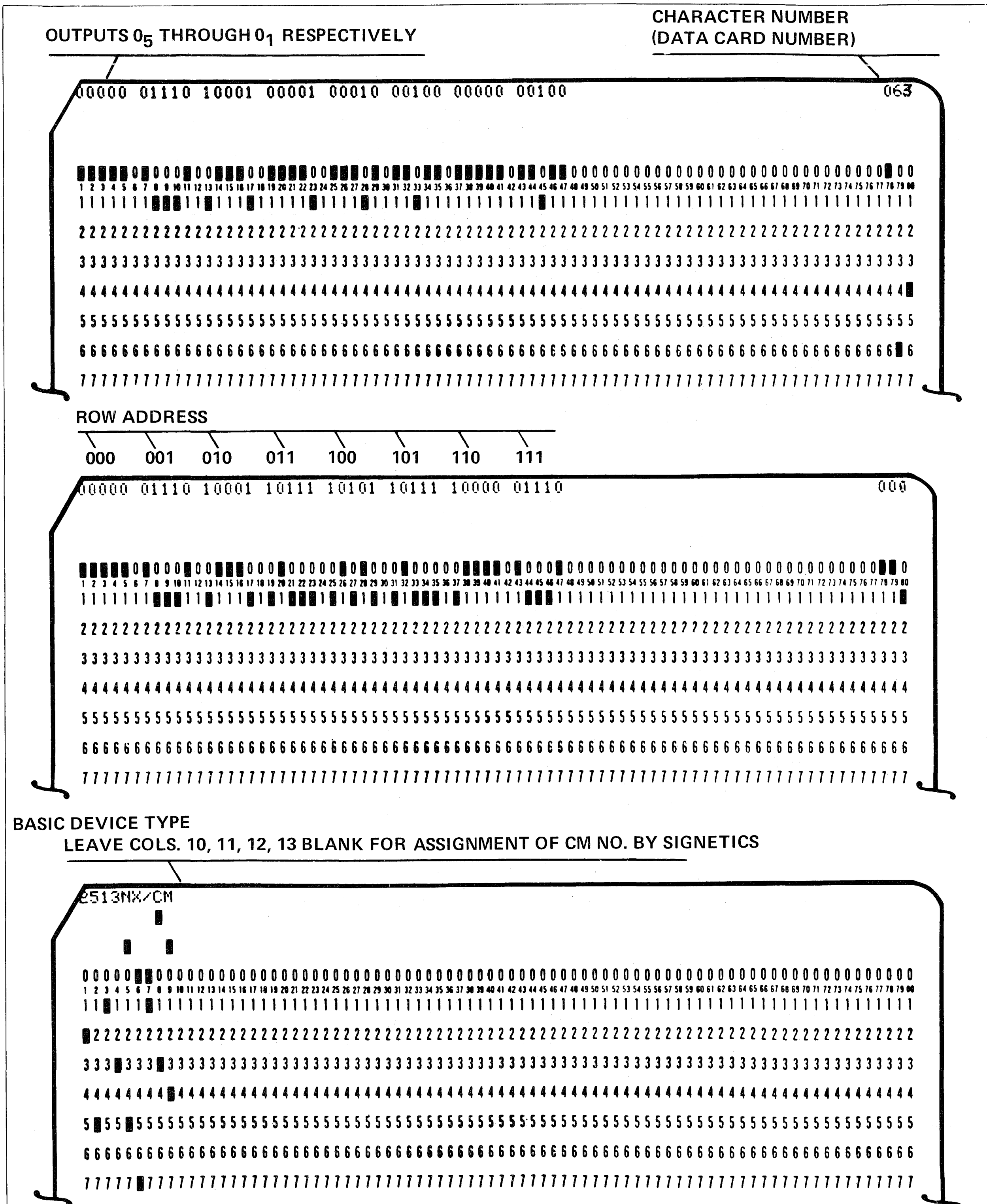
CITY STATE ZIP



COMPANY NAME

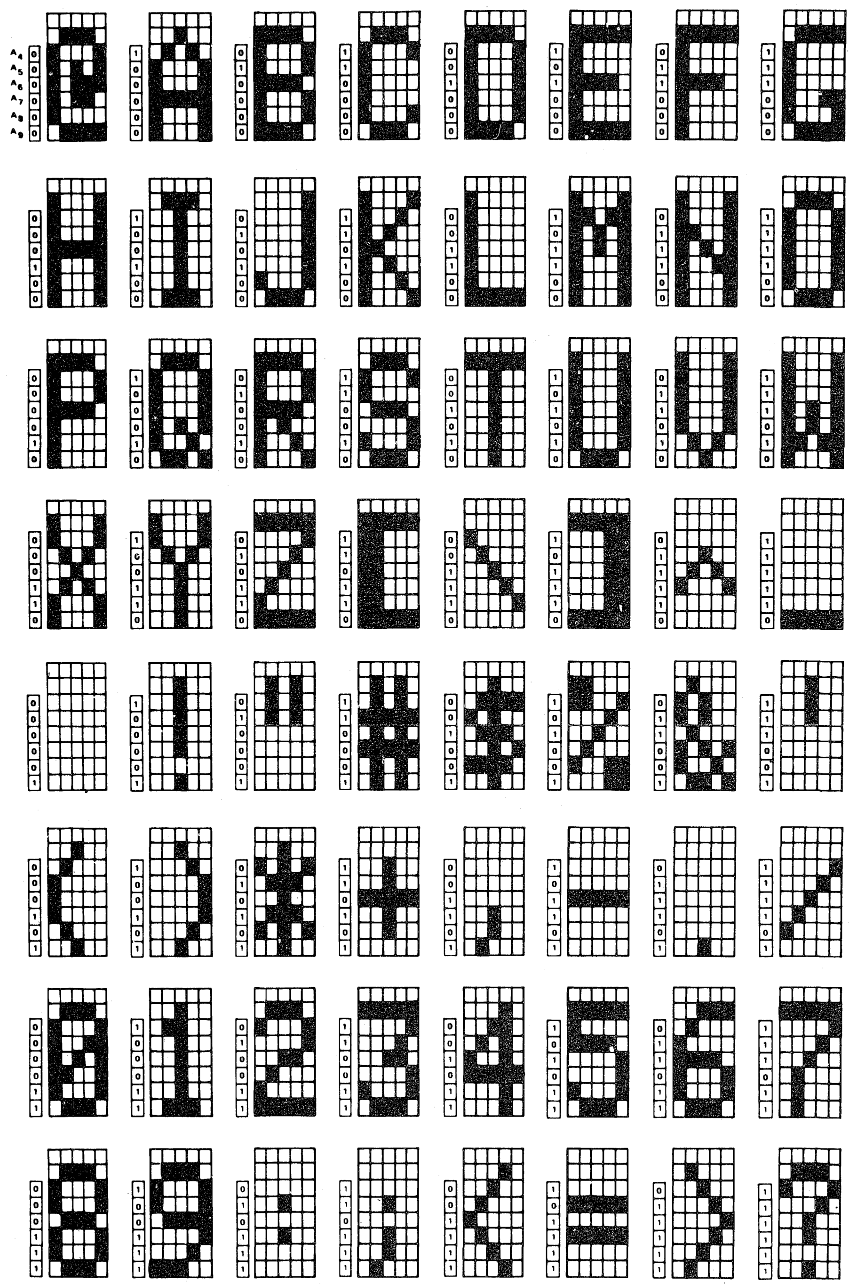


DATA CARDS



NOTE:
"Character" number is in columns 78, 79, and 80. Note that each group of eight 5-bit words is treated as a character for convenience of coding.

ASCII CHARACTER FONT CM2140 (Upper Case); For Lower Case Order CM3021



2516-N,I

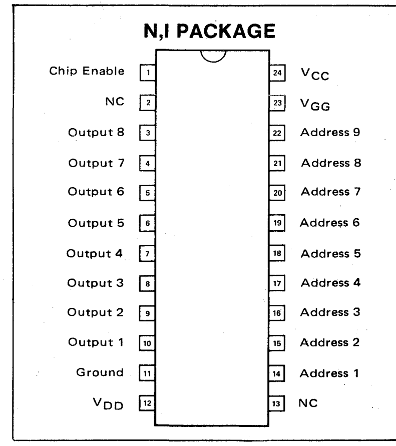
DESCRIPTION

The 2516 is a 3072-bit Static ROM organized as 64x6x8. The product uses +5V, -5V and -12V power supplies, 5V TTL level input signals and Tri-State outputs for direct, low cost interfacing with TTL, DTL and 2500 Series MOS.

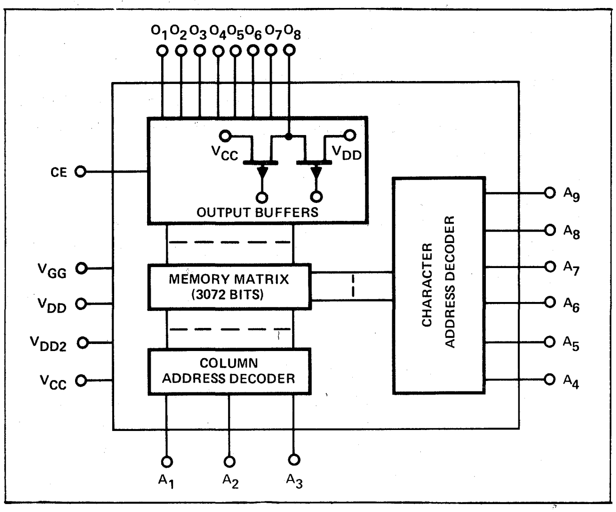
TRUTH TABLE

CE	OUTPUT
0	DATA
1	OPEN

PIN CONFIGURATION



BLOCK DIAGRAM



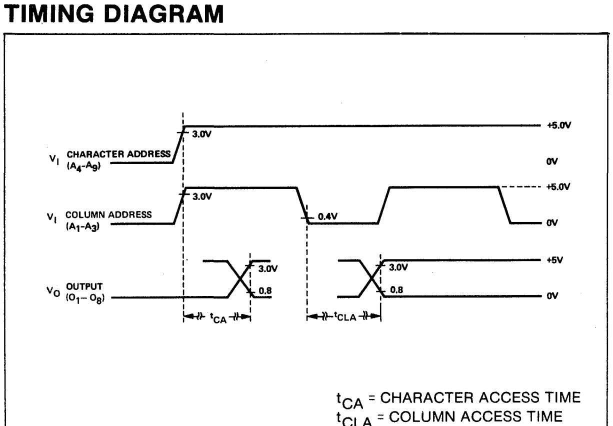
AC CHARACTERISTICS (NOTE 8)

T_A = 0°C to +70°C; V_{CC} = 5V (Note 8); V_{DD} = -5V ± 5%; V_{GG} = -12V ± 5%; unless otherwise noted.

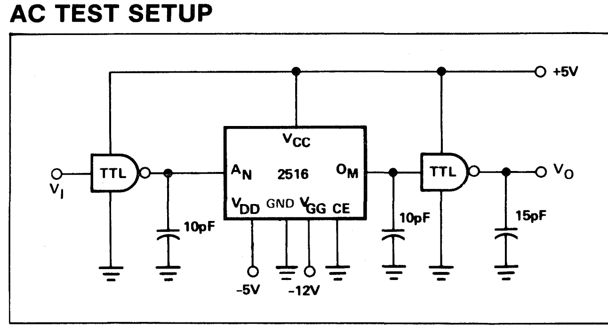
SYMBOL	TEST	MIN	MAX	UNIT	CONDITIONS
t_{CA}	Character Access Time	600		ns	See AC Test Setup*
t_{CA}	Column Access Time (A_1 - A_3)	500		ns	See AC Test Setup*

TA = 0° to +70°C

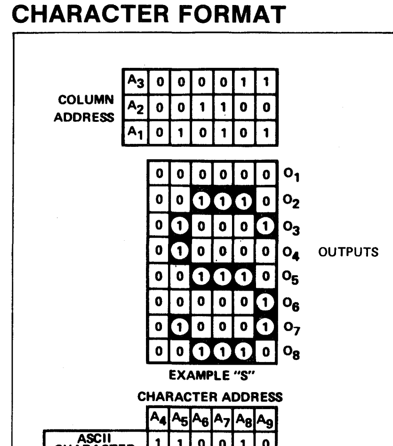
TIMING DIAGRAM



AC TEST SETUP



CHARACTER FORMAT



NOTE:
Undefined (column) addresses result in "1" level (high) outputs.

memories

APPLICATIONS DATA:

OUTPUT INTERFACING NOTES

The tri-state outputs on this device exhibit three states:

"1" — low impedance to +5V
"0" — low impedance to -5V
OFF — high impedance 10 megohm

The "off" state is controlled by the chip enable control input.

CUSTOM ROM ORGANIZATIONS

The 2516 is a static ROM with a total 64 x 6 x 8 bit capacity. This allows a standard 5 x 7 font to be encoded in the ROM, e.g., the 2516/CM2150 ASCII font standard product. A custom coding configuration may make use of the full 6x8 dot matrix if desired.

ORGANIZATION AS CHARACTER GENERATOR

A six-bit binary address (A4 through A9) selects 1-of-64 matrix characters arranged 6 dots horizontally and 8 dots vertically. A three bit-binary address code (A1 through A3) selects 1 of 6 columns. Eight outputs display a complete column of the character matrix.

STANDARD PATTERN

A standard ASCII Character Font is available for the 2516. This device (2516N / CM2150) may be used for ASCII character generation or for device evaluation.

CUSTOM DEVICES

For unique custom memory patterns, the following formats should be used to transmit coding instructions. The nomenclature for each custom device will consist of the basic product type followed by a unique "CM" number assigned by Signetics. For example, "2516N/CM2151",

- **Programming with punched cards.**
  For maximum accuracy and minimum cost and turn-around time, the truth table should be transmitted to Signetics in the form of punched cards according to the format indicated on the following pages.

- **Programming with written truth table.**
  When punched data cards cannot be supplied, the truth table may be transmitted in written form using the attached blank truth table.

VERIFICATION

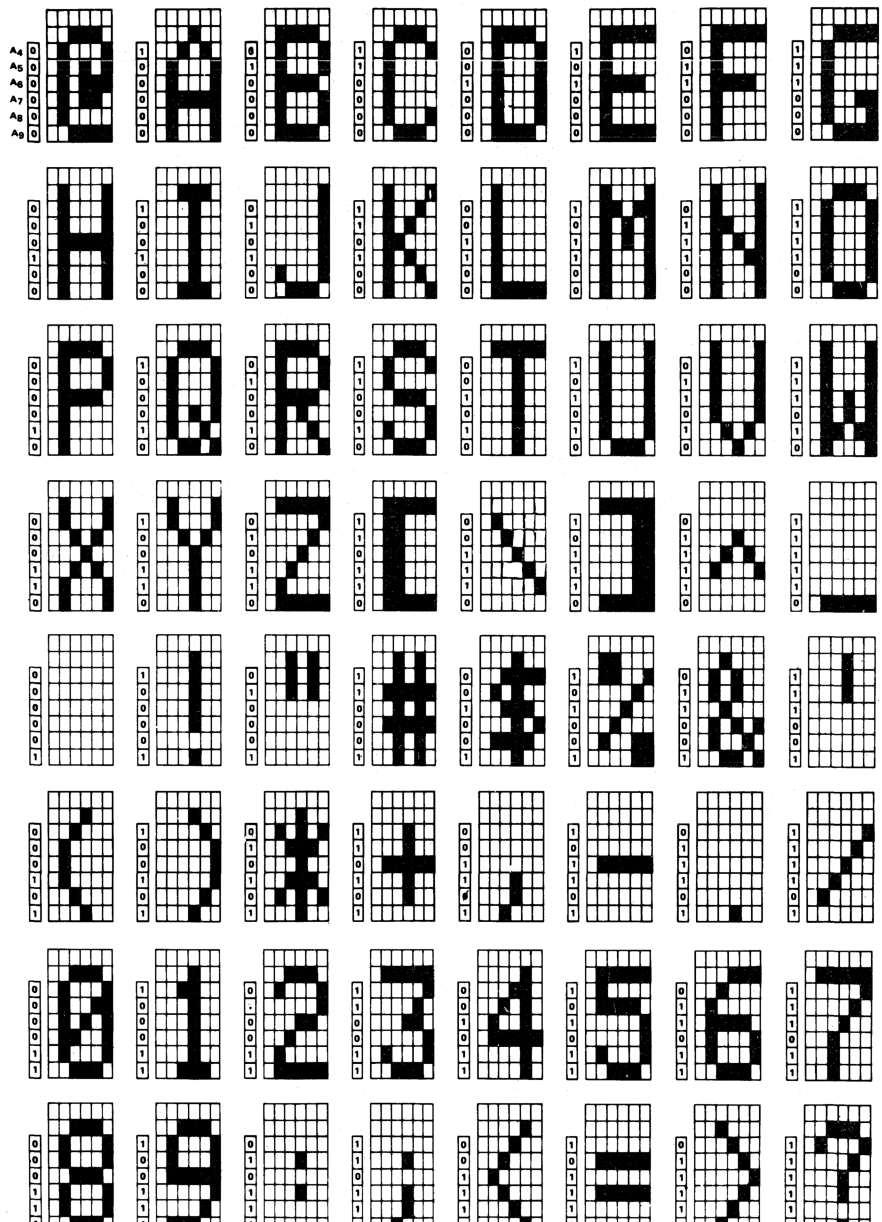
Upon receipt of either punched card or written truth table information, Signetics will prepare a computer tabulation of the instructions and return to the address indicated. If errors are detected, they should be transmitted to Signetics as quickly as possible.

LOGIC CONVENTION

Logic "1"s of blackened squares in the truth table will result in "high" output from the indicated output terminal (i.e. +3.6V minimum). Similarly, a "1" address input level is interpreted as +3.2V minimum.

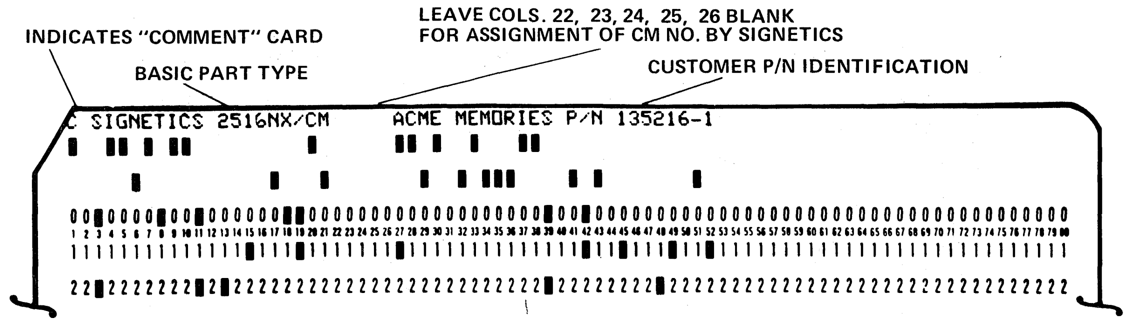
Undefined addresses result in "1" level outputs.

ASCII CHARACTER FONT

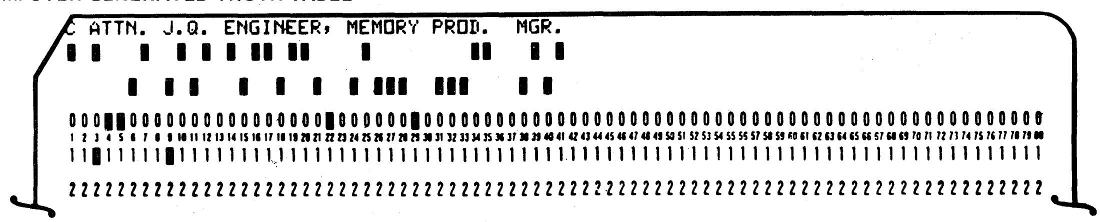


NOTE: Excess addresses yield logic "1" outputs.

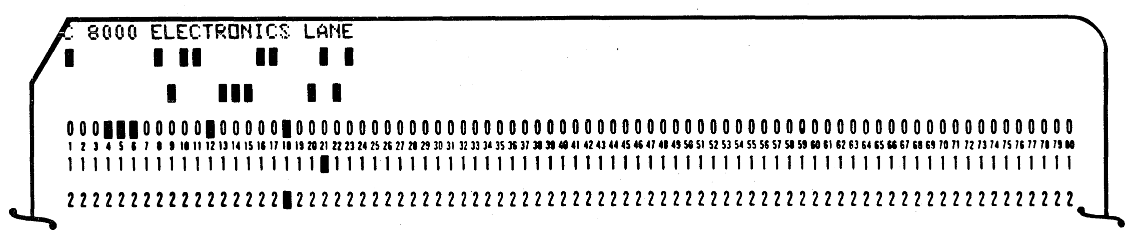
IDENTIFICATION CARDS



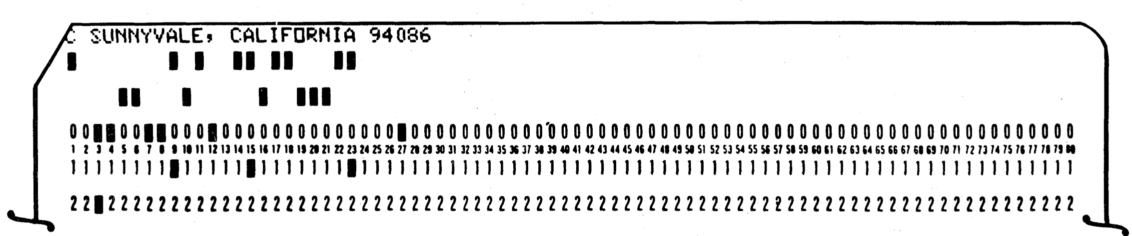
PERSON RESPONSIBLE FOR REVIEWING SIGNETICS COMPUTER GENERATED TRUTH TABLE



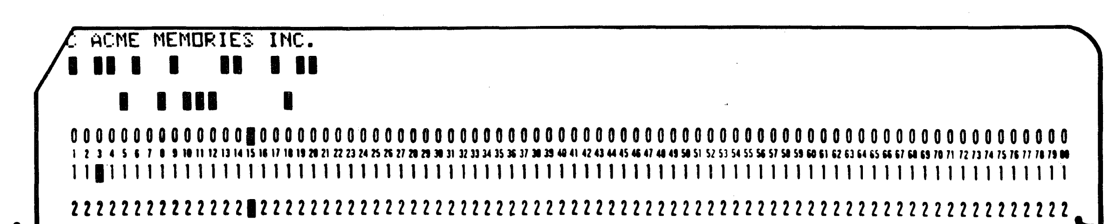
STREET ADDRESS



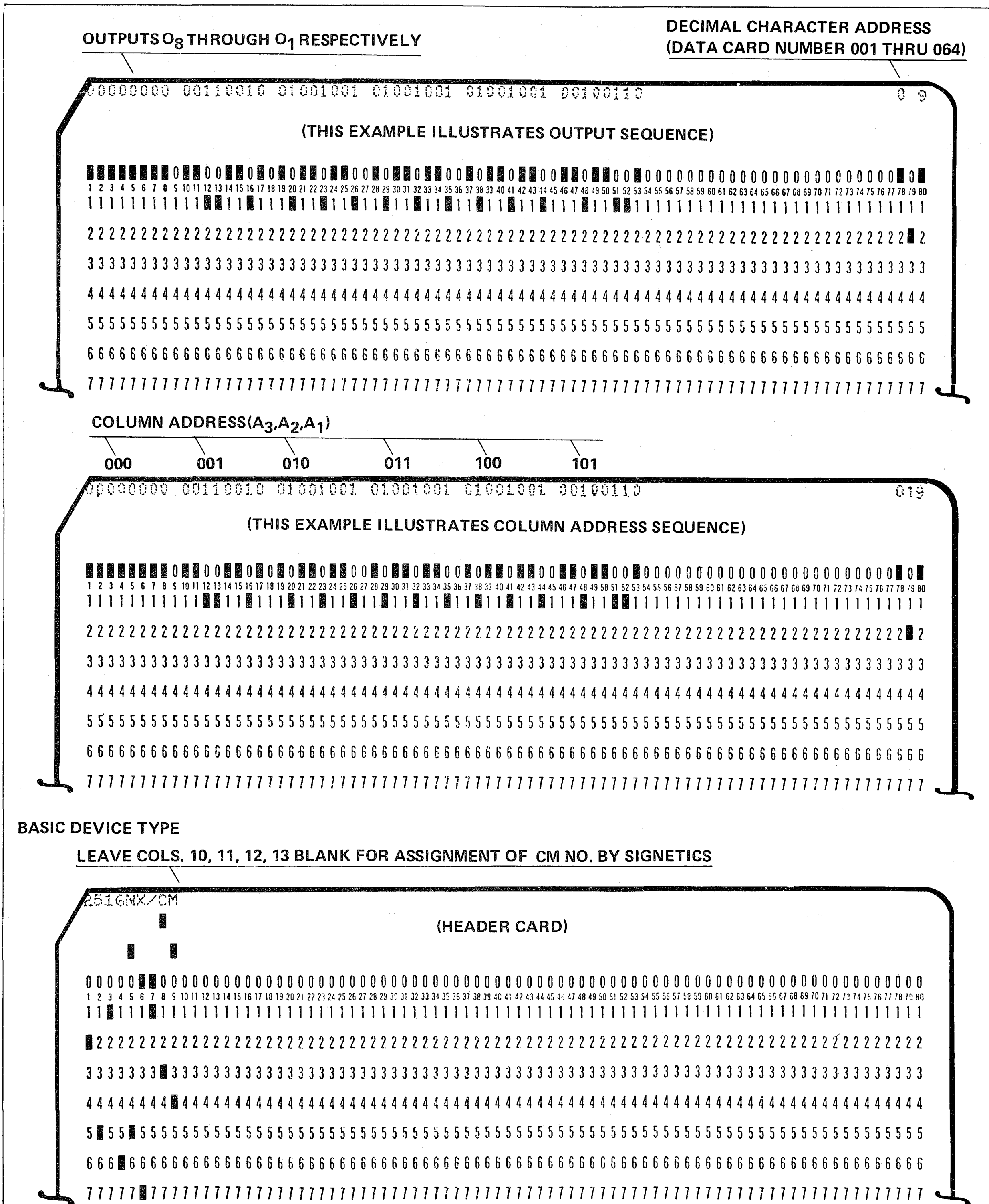
CITY STATE ZIP



COMPANY NAME



DATA CARDS

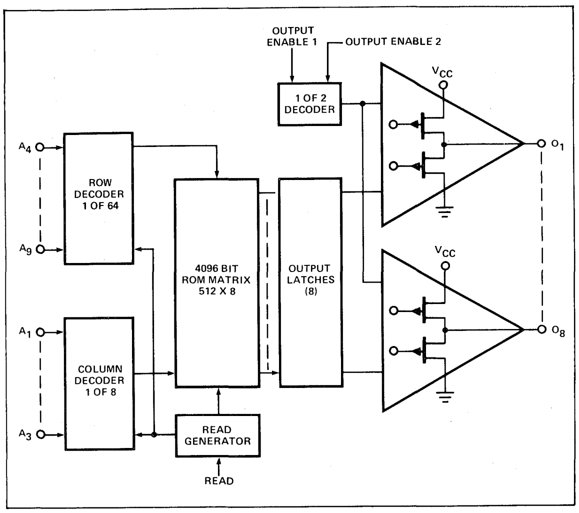


NOTE
"Character" number is in columns 78, 79, and 80.

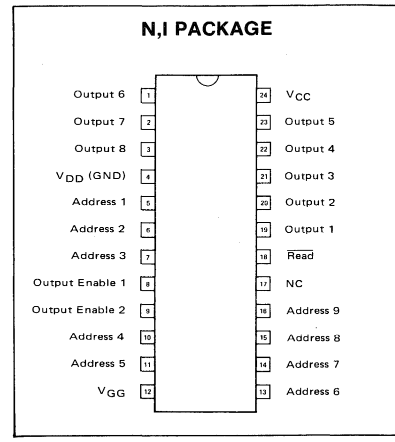
DESCRIPTION

The 2530 is a high speed 4,096-bit Static Read-Only Memory available in a 512x8 organization. This device has TTL compatible inputs and outputs and requires +5V and -12V power supplies. A READ input controls the entry of data from the ROM into output latches. Three-state outputs allow OR tying for implementing larger memories. Two-mask programmable OUTPUT ENABLES control the eight output devices without affecting address circuitry.

BLOCK DIAGRAM



PIN CONFIGURATION

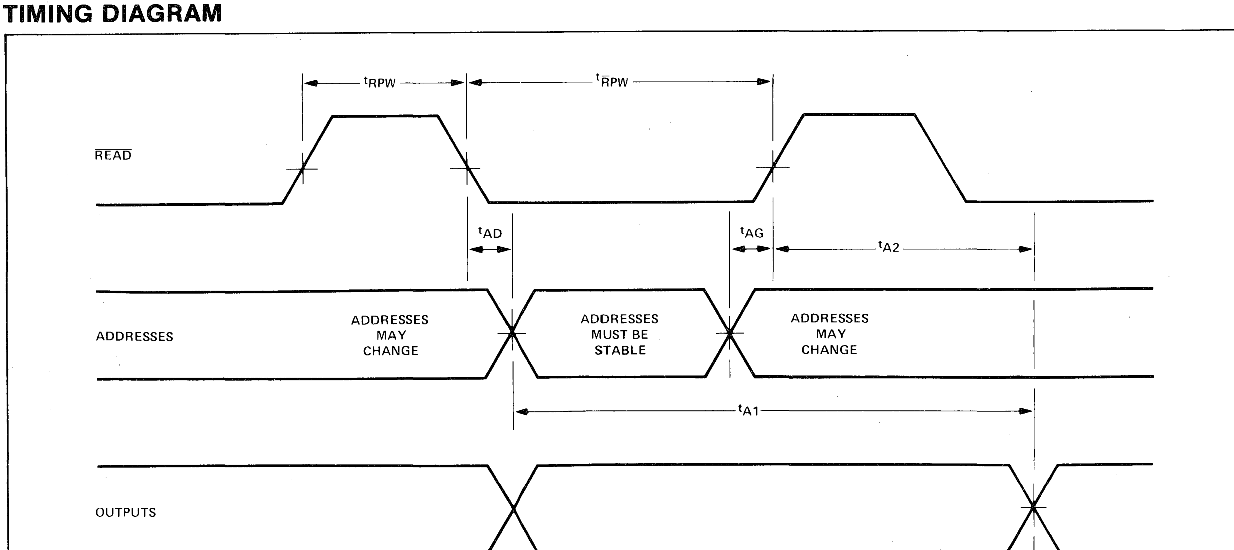


AC CHARACTERISTICS (8)

T_A = 0°C to 70°C; V_{CC} = 5V (Note 8) V_{GG} = -12V ± 5%; unless otherwise noted.

SYMBOL	TEST	MIN	MAX	UNIT	CONDITIONS
t_{RPW}	Read Pulse Width	250		ns	Note 19
t_{RPW}	Read Pulse Width	500		ns	Note 18
t_{AD}	Address Delay Time (12)		50	ns	
t_{AG}	Address-Read Pulse Gap (12)		50	ns	
t_{A1}	Address to Output Delay		700	ns	Note 17
t_{A2}	End of Read Pulse to Output Delay		250	ns	
t_{OE}	Output Enable to Output Delay		250	ns	V_{AC} = 25m V_{p-p} $V_{IN} = V_{CC}$

TIMING DIAGRAM



Note: All times measured from 50% points, for all input waveforms tr = tf 10nsec.

2530 CUSTOM CODING INFORMATION

PUNCHED CARD INPUT

Header Card

Card No.	Column	Information
1	1-5	"2530N" or "25301"
	6-14	Blank
	15-19	"CODED"
	20	Blank
	21	Logic state of Output Enable #2, (CS2) - Most Significant Bit.
	22	Logic state of Output Enable #1.
	23	Blank
	24-71	Customer company name.
	72	Blank
	73-80	Date

I.D./Comment Cards:

Card No.	Column	Information
1	1	"C"
	2	Blank
	3-80	Person responsible for reviewing Signetics truth table and Company Name.
2	1	"C"
	2	Blank
	3-80	Customer Street Address
3	1	"C"
	2	Blank
	3-80	Customer City, State, Zip.

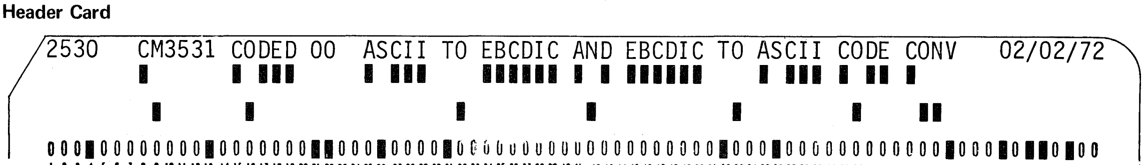
Data Cards:

Card No.	Column	Information
1	1-3	Decimal address (blank, blank, 0.)
	4	Blank
	5-12	8-digit binary output (MSB-left)
	13-20	Blank
	21-33	Decimal address, (blank, blank, 1.)
	24	Blank
	25-32	8-Digit binary output (MSB-left)
	33-40	Blank
	41-43	Decimal address, (Blank, blank, 2.)
	44	Blank
	45-52	8-digit binary output (MSB-left)
	53-60	Blank
	61-63	Decimal address, (Blank, blank, 3.)
	64	Blank
	65-72	8-digit binary output (MSB-left)
	73-80	Blank
2		Same format as data card #1.
128		Same format as data card #1.

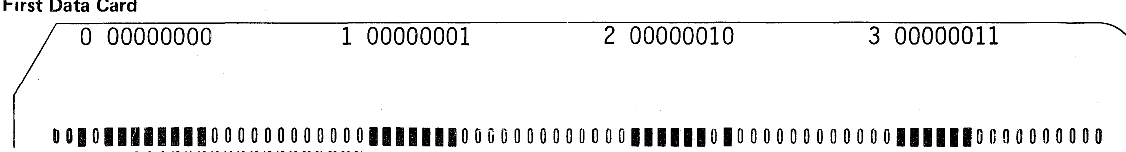
NOTE: MSB = O_9

EXAMPLES

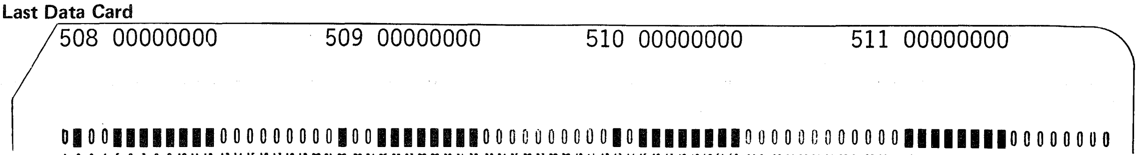
Header Card



First Data Card



Last Data Card

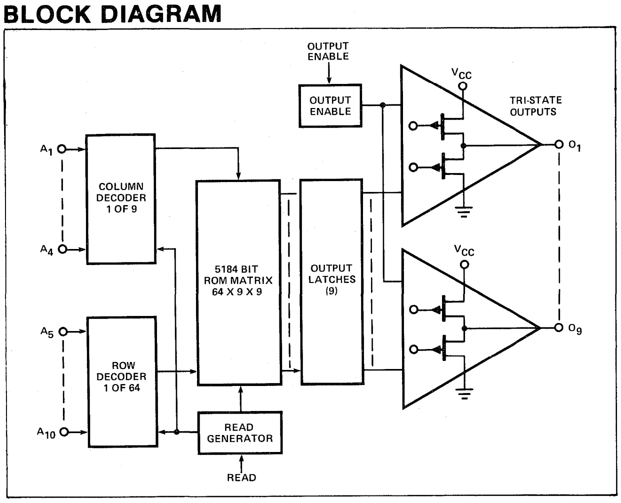


2526-N,I

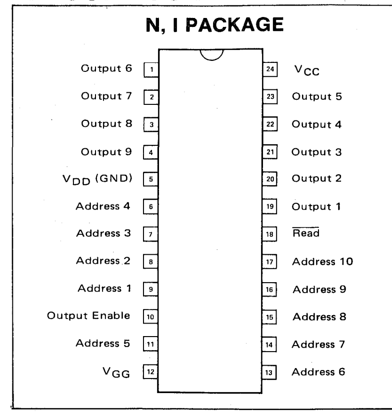
DESCRIPTION

The 2526 is a high speed 5 184-bit Static Read-Only Memory. It may be organized as 64x9x9 for use as a character generator, or as a 512x9 ROM for general purpose use. This device has TTL compatible inputs and outputs and requires +5V and −12V power supplies. A $\overline{\text{READ}}$ input controls the entry of data from the ROM into output latches. Three-state outputs allow OR tying for implementing large memories. OUTPUT ENABLE controls the nine output devices without affecting address circuitry.

BLOCK DIAGRAM



PIN CONFIGURATION

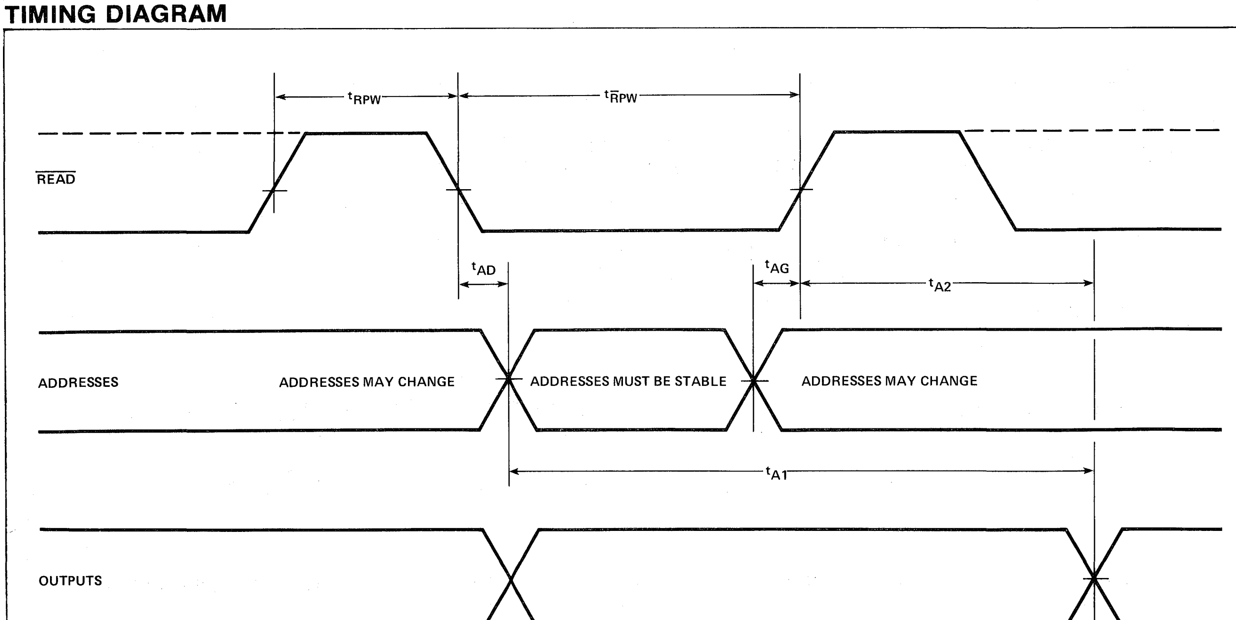


AC CHARACTERISTICS

TA = 0°C to +70°C, VCC = 5V (note 8) VGG = −12V 5%; unless otherwise noted.

	PARAMETER	MIN	MAX	UNIT	CONDITIONS
t_{RPW}	Read Pulse Width	250		ns	Note 19
$t_{\overline{RPW}}$	Read Pulse Width	500		ns	Note 18
t_{AD}	Address Delay Time		50	ns	Note 20
t_{AG}	Address-Read Pulse Gap		50	ns	Note 20
t_{A1}	Adress to Output Delay		700	ns	Note 17
t_{A2}	End of Read Pulse to Output Delay		250		Note 17
t_{OE}	Output Enable to Output Delay		250	ns	V_{AC} = 25mV p-p $V_{IN} = V_{CC}$

TIMING DIAGRAM

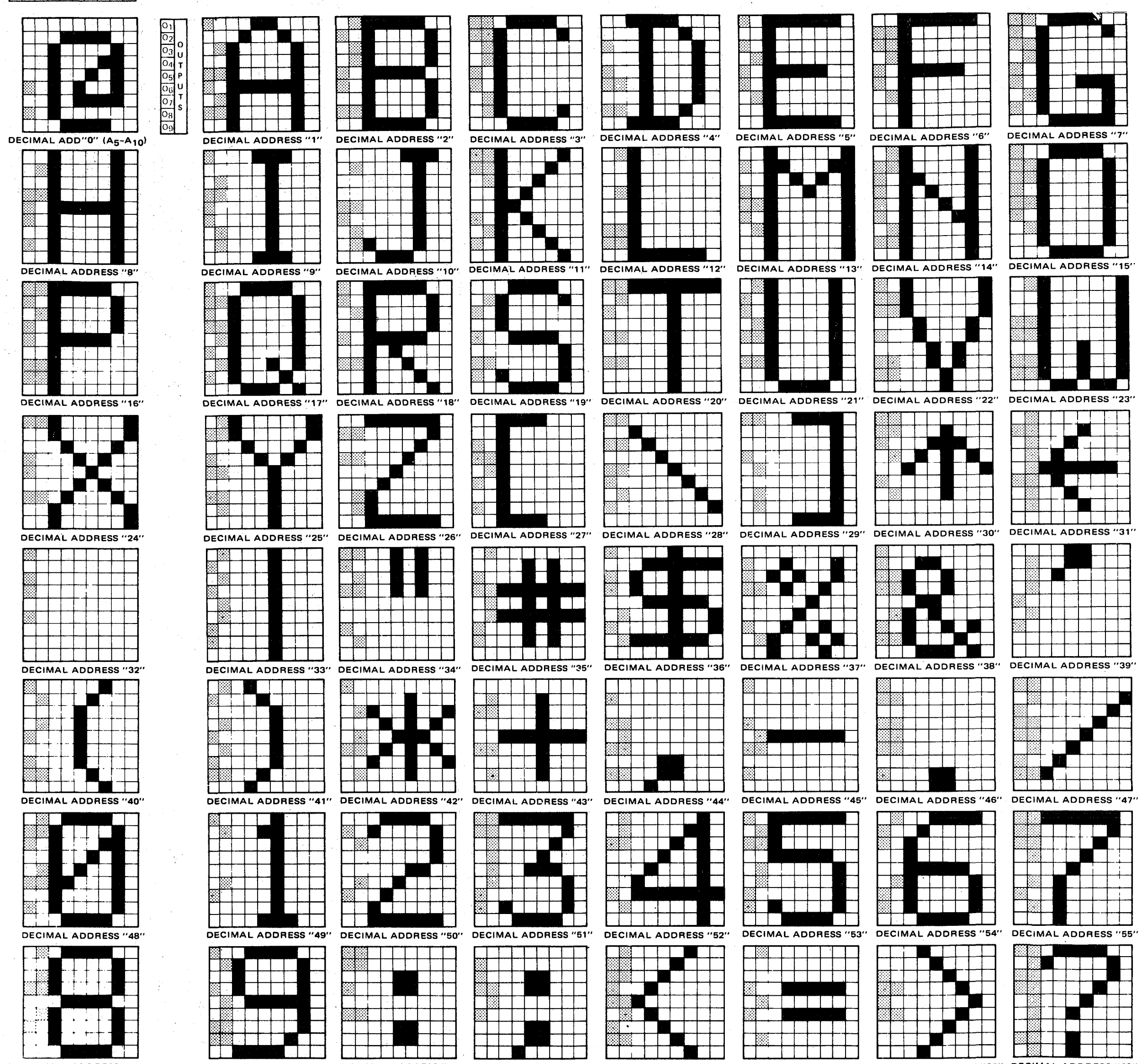


NOTE:
All Times Measured from 50% Points.
tr = tf = 10 ns or less

STANDARD CHARACTER FONT

CM 3400
ASCII SET, VERTICAL SCAN 7X9 WITH CODE CONVERSION

COLUMN ADDRESSES									
A_1	0	1	0	1	0	1	0	1	0
A_2	0	0	1	1	0	0	1	1	0
A_3	0	0	0	0	1	1	1	1	0
A_4	0	0	0	0	0	0	0	0	1



NOTES:
1. BCDIC to ASCII in leftmost column, Baudot to ASCII in next column to right.
2. Underfined addresses result in all outputs going low (TTL "0").
3. Black squares in character font are high (TTL "1").

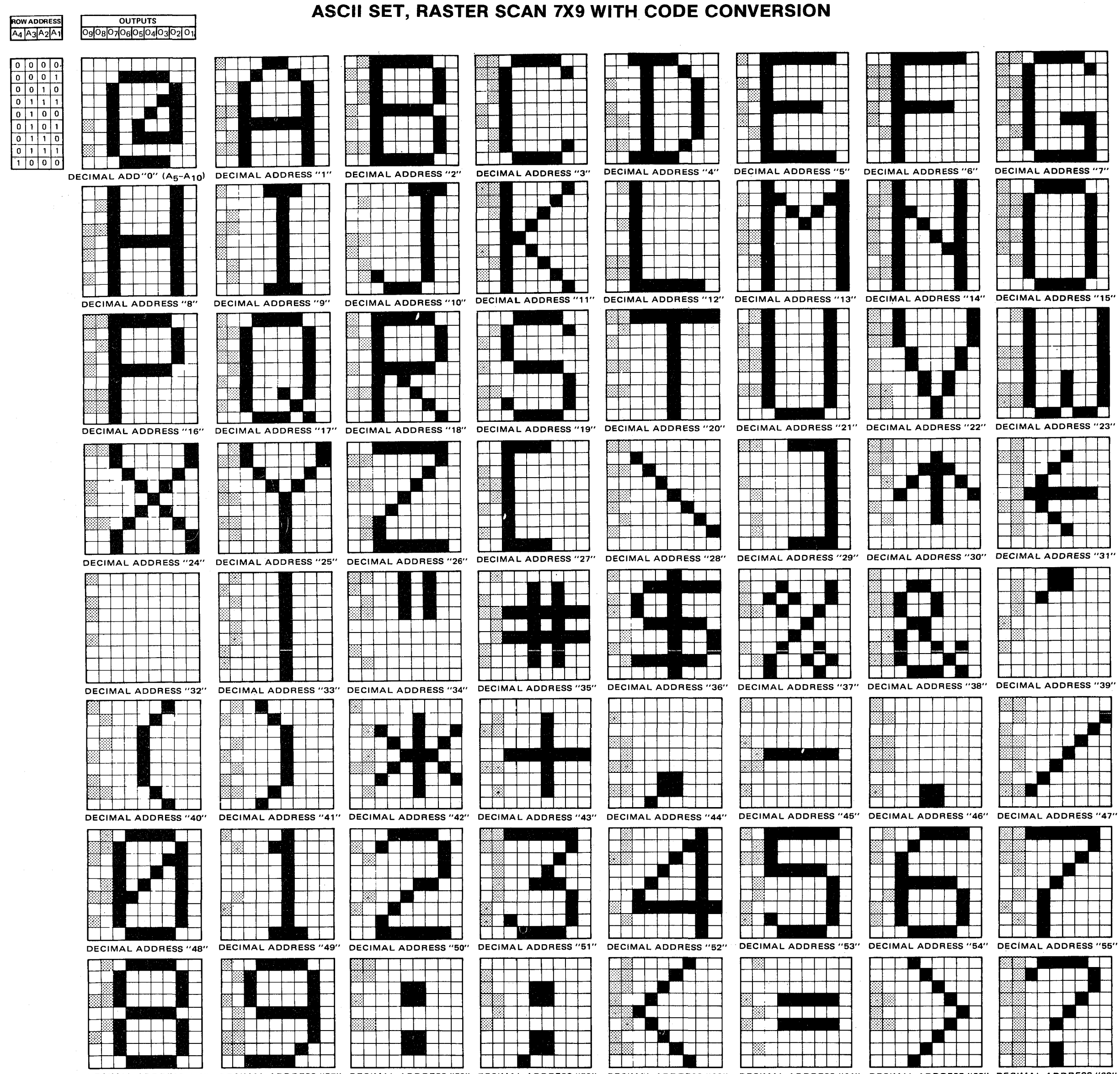
MEMORIES

2526-N,I

STANDARD CHARACTER FONT

CM 3941

ASCII SET, RASTER SCAN 7X9 WITH CODE CONVERSION



NOTES:
1. BCDIC to ASCII in leftmost column, Baudot to ASCII in next column to right.
2. Undefined addresses result in all outputs going low (TTL "0").
3. Black squares in character font are high (TTL "1").

CUSTOM CODING INFORMATION

2526-N,I

PUNCHED CARD INPUT

Comment/I.D. Cards:

Card. No.	Column	Information
1	1	"C"
	2	Blank
	3-17	"SIGNETICS 2526N/CM"
	18-26	Blank
	27-71	Customer I'D' (Company, Project, Part No., etc.)
	72	Blank
	73-80	Date
2	1	"C"
	2	Blank
	3-80	Person responsible for reviewing Signetics truth table.
3	1	"C"
	2	Blank
	3-80	Customer Street Address
4	1	"C"
	2	Blank
	3-80	Customer City, State, Zip.
5	1	"C"
	2	Blank
	3-80	Name

Data Cards

Card No.	Column	Information
1	1-9	Binary outputs of rows 9 through 1, (MSB at 9), first column, first character, (first character is "000"). Logic "1" is high output (3.2V, min.).
	10	Blank
	11-19	Binary outputs of second column, first character.
	20	Blank
	21-29	Third column

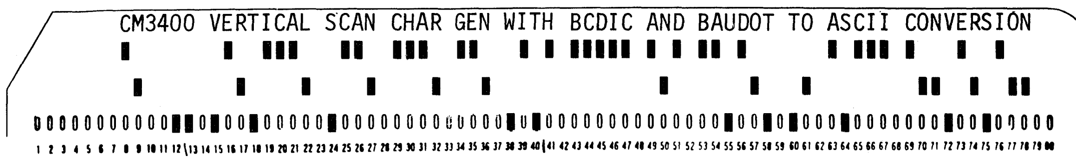
Data Cards (Continued)

Card No.	Column	Information
1 (cont'd)	30	Blank
	31-39	Fourth column
	40	Blank
	41-49	Fifth column
	50	Blank
	51-59	Sixth column
	60	Blank
	61-69	Seventh column
	70-71	Blank
	72	Data card number of first character, ("1").
	73	Blank
	74-76	Anything—customer option.
	77	Blank
	78-80	Decimal character number, ("000")
2	1-9	Eight column
	10	Blank
	11-19	Ninth column
	20-70	Anything—customer option.
	71	Blank
	72	Data card number of first character, ("2").
	73	Blank
	74-76	Customer option
	77	Blank
	78-80	Decimal character number, ("000").
3	1-9 (etc.,as Card 1)	First column, second character, rows 9 through 1 (MSB at 9). Second character is "001".
4	(etc.,as Card 2)	
128	78-80	Decimal character number, ("063").

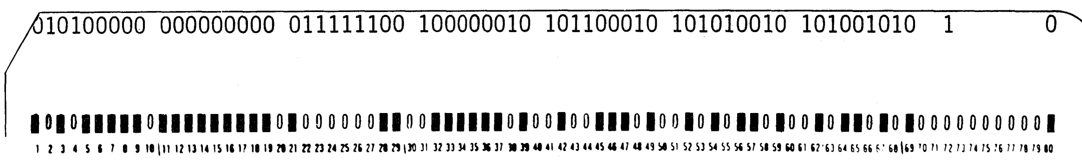
MEMORIES

EXAMPLES

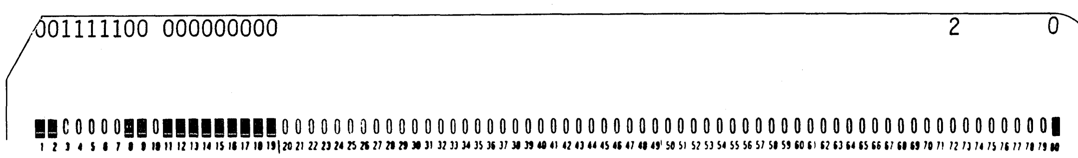
I.D. Card



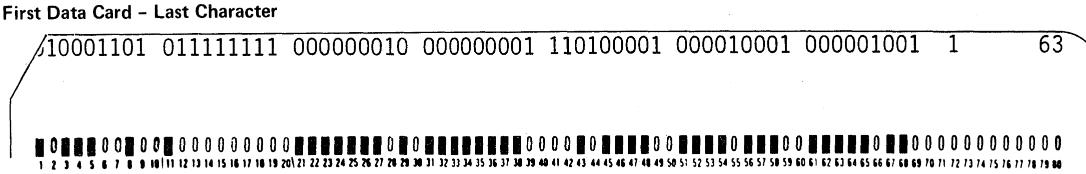
First Data Card – First Character



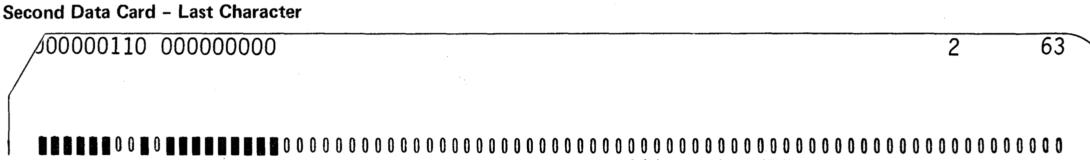
Second Data Card – First Character



First Data Card – Last Character



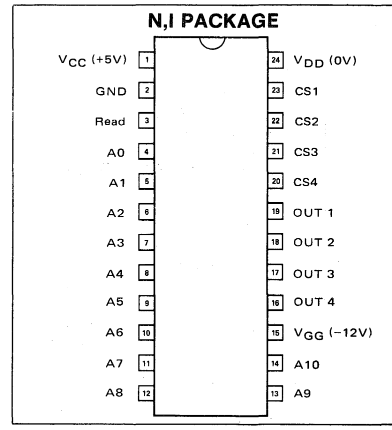
Second Data Card – Last Character



DESCRIPTION

The 2580 is an 8192-Bit Read-Only Memory available in a 2048x4 organization. This device has TTL compatible inputs and outputs and requires +5V and -12V power supplies. A READ input controls the entry of data from the ROM into output latches. Three-state outputs allow OR tying for implementing larger memories. The outputs are enabled by a programmable four bit select code applied to four binary chip select terminals.

PIN CONFIGURATION



AC CHARACTERISTICS

$T_A = 25°C$; $V_{CC} = 5V$ (Note 8) VDD = OV, $V_{GG} = -12V$ ±5% unless otherwise noted

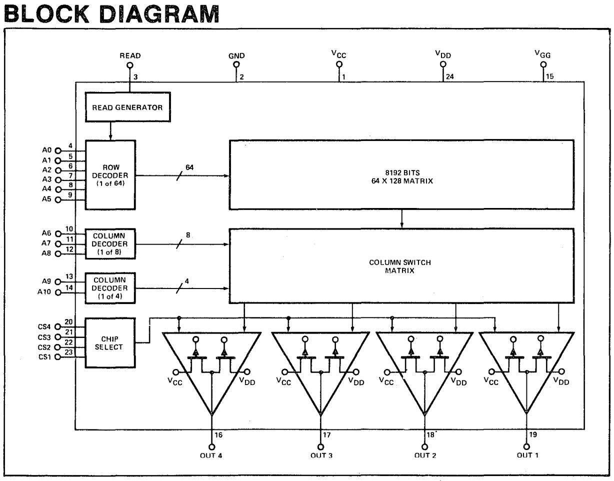
	PARAMETER	MIN	MAX	UNIT
t_{RPW}	Read Pulse Width[14]	650		ns
t_{RPW}	Read Pulse Width[13]	500		ns
t_{AD}	Address Delay Time[15]		50	ns
t_{AH}	Address Hold Time	0		ns
t_{A1}	Address to Output Delay		950	ns
t_{A2}	End of Read Pulse to Output Delay		350	

CODING FORMAT

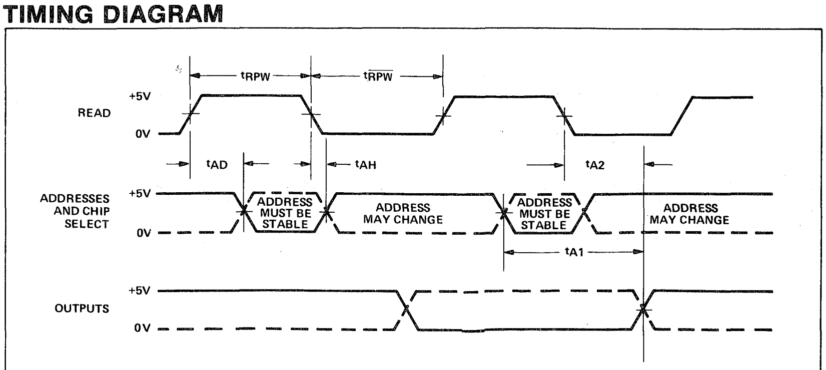
Coding data for the 2580 may be sent to Signetics via punched cards or via a written truth table. Cards are preferred since errors are essentially eliminated.

On receipt of a card deck, Signetics will translate the card deck to a truth table using the Signetics Computor Aided Design (CAD) facility. The truth table will then be sent to the customer requesting engineer for final approval. On receipt of final approval, Signetics will cut the rubylith mask and proceed with manufacture.

BLOCK DIAGRAM

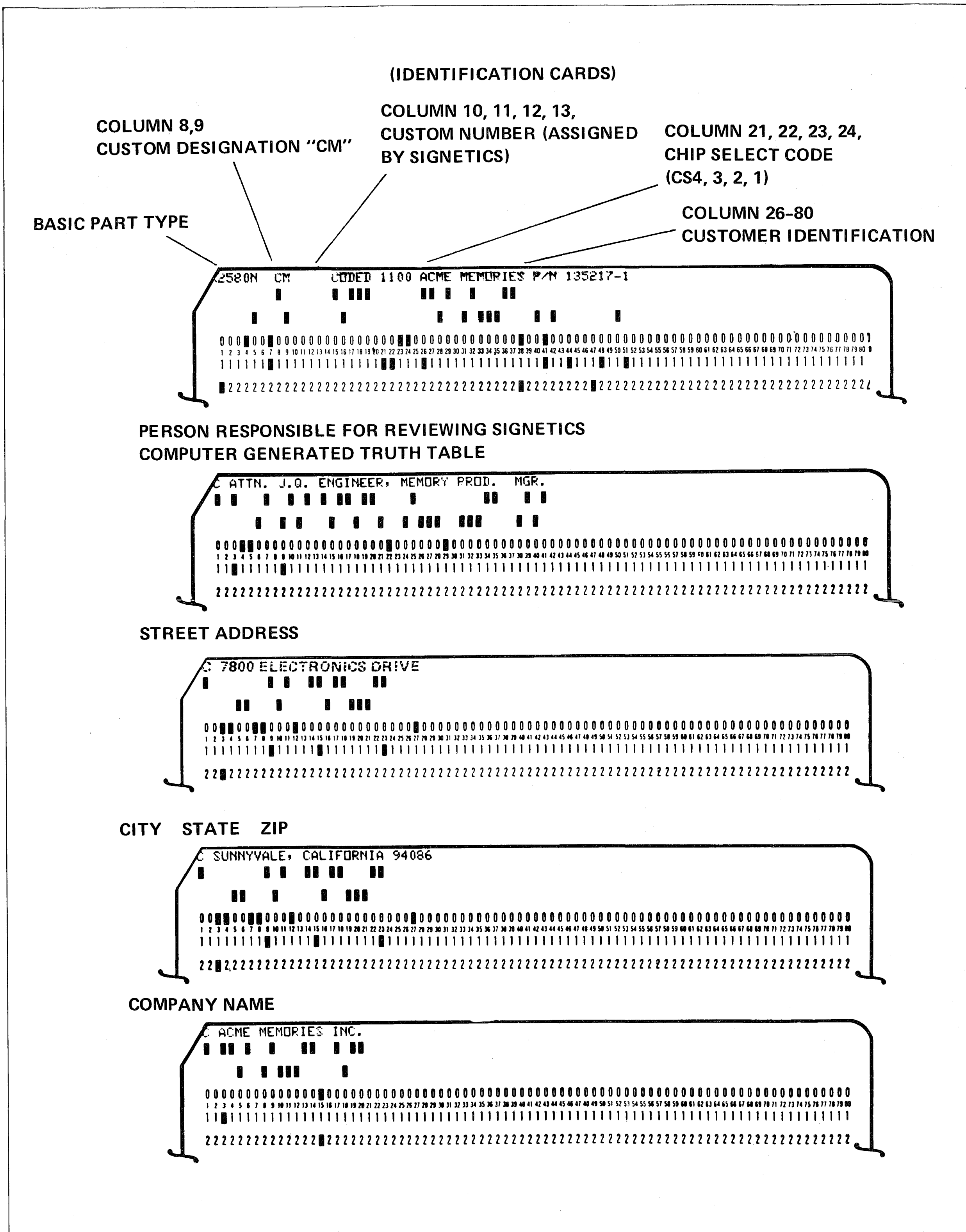


TIMING DIAGRAM



2580-N,I

CARD FORMAT

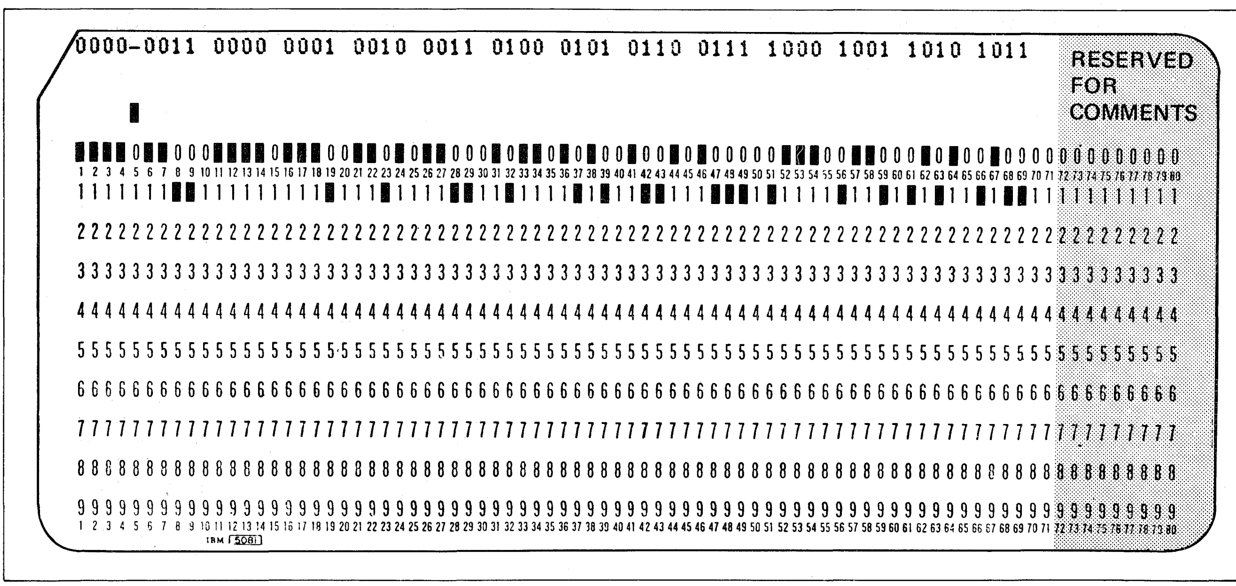


DATA CARD FORMAT

Col 1-4	Decimal equivalent of first data word location. Example: 0124 Note: leading zeros must be used for addresses from 0000 to 0999.
Col 5	Dash (-) to separate numbers
Col 6-9	Address of last word on card
Col 10	Blank
Col 11-14	First data word (0_4, 0_3, 0_2, 0_1)
Col 15	Blank
Col 16-19	Second data word
Etc. thru column 71	
Col 72-80	Reserved for comments (These columns are ignored by the computer)

Up to twelve (12) data words can be coded on one card. Less than 12 may be used as long as the first and last addresses are given in columns 1-9.

EXAMPLE



MEMORIES

8192-BIT STATIC MOS ROM (1024X8) — 2608/2608-1

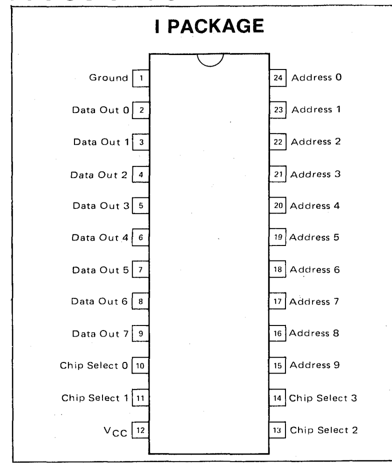
2608 • 2608-1-I

DESCRIPTION

The 2608 is a fully decoded, static, mask programmable read-only memory. It has a capacity of 8192 bits organized 1024 X 8. The 2608 is fabricated with low threshold N-Channel silicon gate MOS technology which allows extreme ease of use with low voltage logic families such as transistor-transitor logic.

Requiring only 5 volts and ground power connections, the 2608 features a maximum access time of 650ns. Since the 2608 uses static logic throughout, no clocks are required. Four mask programmable chip selects are provided for easy word expansion. All 2608 inputs and outputs are TTL-compatible.

PIN CONFIGURATION



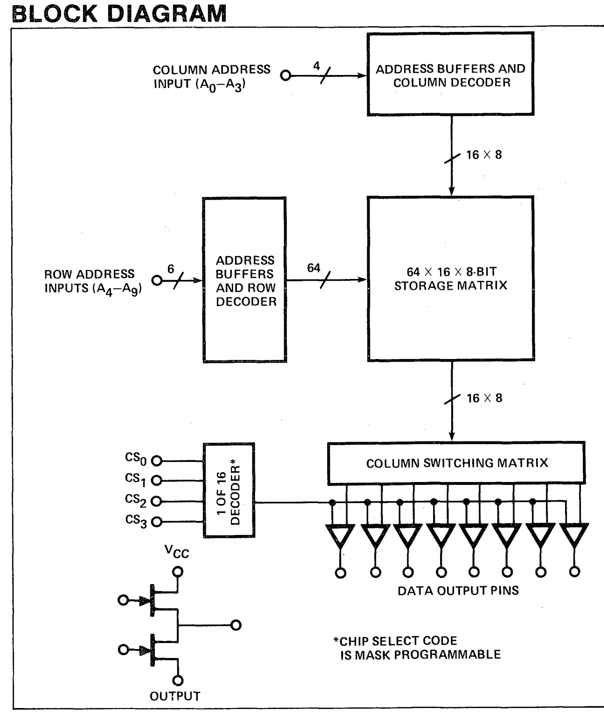
AC OPERATING CHARACTERISTICS

T_A = 0°C to +70°C, V_{CC} = +5V 5% (See Notes A, B & C)

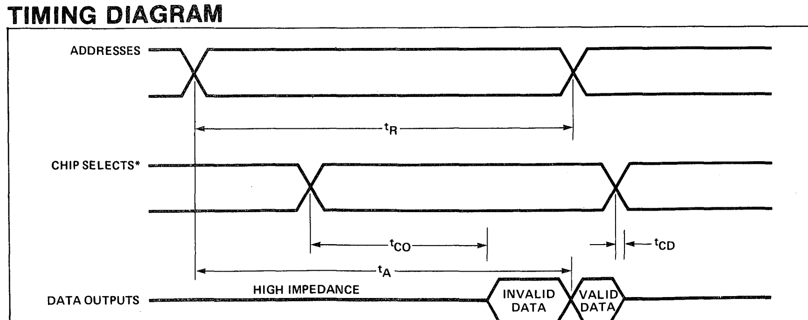
SYMBOL	PARAMETER	MIN	MAX	UNITS	NOTES
t_R	Read Cycle Time	650		ns	
t_{CO}	Chip Select to Output Enable		300	ns	Note D
t_{CD}	Chip Select to Output Disable	10	150	ns	Note D
t_A	Access Time (2608)	100	550	ns	Note D
	Access Time (2608-1)	100	450	ns	Note D

NOTES:
A. Input levels swing between 0.65 volts and 2.2 volts.
B. Input signal transition times are 20 nsec.
C. Timing reference level is 1.5 volts.
D. Output load is one standard TTL load plus 130pF.

BLOCK DIAGRAM



TIMING DIAGRAM



*CUSTOMER CHOOSES PARTICULAR CHIP SELECT CODE DESIRED. THE OTHER FIFTEEN COMBINATIONS OF FOUR CHIP SELECT INPUTS DISABLE THE OUTPUTS.

PIN DESCRIPTION

ADDRESS

These ten TTL-compatible inputs are decoded on-chip to select one of 1024 eight-bit bytes. Since the 2608 utilizes static logic throughout, a change in addresses results in a change in data as long as the chip is selected. Access time is measured from the point where the last address input became stable. Cycle time and access time are equal in a static ROM design.

CHIP SELECTS

There are four TTL-compatible chip select inputs for the 2608. Only one combination of these four signals enables enabling combination is chosen by the customer and specified on the first punched card of the customer card deck (see following page). A positive logic convention is assumed.

DATA OUTPUTS

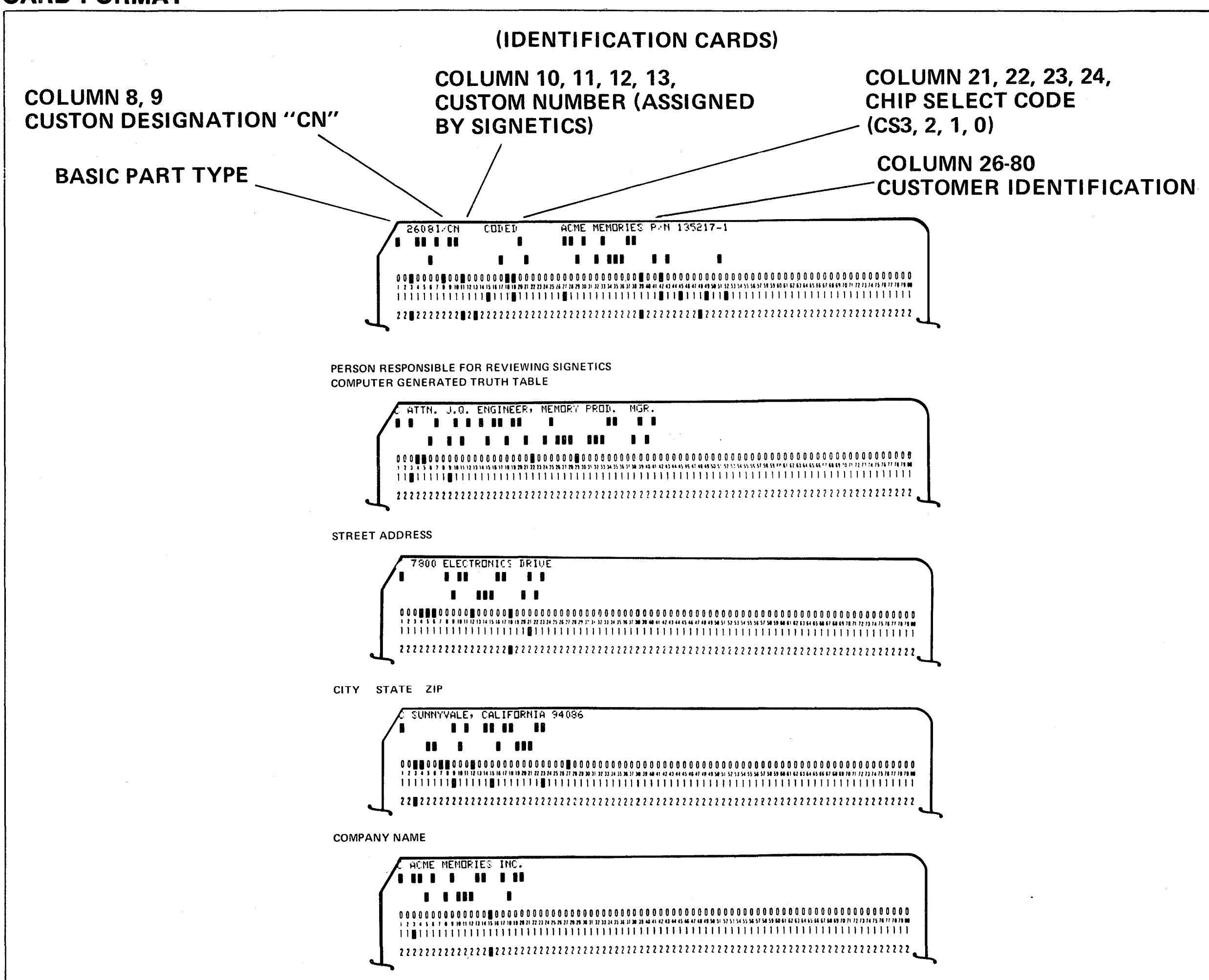
The eight data outputs are push-pull buffers capable of driving one standard TTL-load plus a 130pF load capacitance. These outputs are placed in the high impedance state when any one of the disabling combinations of the chip select inputs is present.

CODING FORMAT

Coding data for the 2608 may be sent to Signetics via punched cards or via a written truth table. Cards are preferred since errors are essentially eliminated.

On receipt of a card deck, Signetics will translate the card deck to a truth table using the Signetics Computer Aided Design (CAD) facility. The truth table will then be sent to the customer for final approval. On receipt of final approval, Signetics will produce masks and proceed with manufacturing.

CARD FORMAT



DATA CARDS

12——75 Hexadecimal data coding
77——78 Card number (starting 01)
79——80 Total number of cards (32)

Column 12 on the first card contains the hexadecimal equivalent of bits D7 thru D4 of byte 0, while column 13 contains the hexadecimal equivalent of bits D3 thru D0. Columns 14 and 15 contain byte 1, columns 16 and 17 byte 2, and so on.

The first card contains the first 32 bytes. Columns 12 and 13 on the second card will contain byte 32 (the 33rd byte). A total of 32 cards will contain 1024 bytes of 8 bits.

BINARY TO HEXADECIMAL CONVERSION

BINARY COMBINATION D0-D3 OR D4-D7				HEXADECIMAL CHARACTER
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	A
1	0	1	1	B
1	1	0	0	C
1	1	0	1	D
1	1	1	0	E
1	1	1	1	F

INTERFACE 3

Interface

TABLE OF CONTENTS

INTERFACE-LOGIC

	INPUT VOLTAGE																		OUTPUT VOLTAGE		
PARAMETER		V_{IL} (V) LOW LEVEL			V_{IH} (V) HIGH LEVEL			V_{IC} CLAMP VOLTAGE			VOLTAGE RATING			VT_L (mV)[20] LOW LEVEL THRESHOLD VOLTAGE			VT_H (mV)[20] HIGH LEVEL THRESHOLD VOLTAGE			V_{OL} (V)[7] LOW LEVEL	
TEST CONDITIONS								V_{CC}=MIN I_{IN}=−12mA			V_{IN}=10mA			V_{CC}=MIN V_{IN}=0.8V I_{OL}=−400μA			V_{CC}=MAX V_{IN}=0.8V I_{OH}=16mA			V_{CC}=MIN	
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
8T04		For a, b, c, d	0.8	2.0	1 For a, b, c, d				−1.5	5.5				N/A			N/A			RBO/B1=4.8mA RB1, Driven Inputs=0.8V RBO 0.4 Outputs=40mA LT, RB1, RBO/B1=0.4V A-G 0.5	
8T05		For a, b, c, d	0.8	2.0	For a, b, c, d				−1.5	5.5				N/A			N/A			LT=4.5V V_{IN}=0.4V I_{OL}=500μA A-G 0.3 RBO/B1=4.8mA Others=0.8V RBO 0.4	
8T06		For a, b, c, d	0.8	2.0	For a, b, c, d				−1.5	5.5				N/A			N/A			A-G Outputs=40mA LT=4.5V RB1, RBO/B1=0.4V 0.5 RBO RBO/B1=4.8mA RB1, Driven Inputs=0.8V 0.4	
8T09			0.8	2.0					−1.5	5.5				N/A			N/A			Outputs=40mA Data=2.0V Disable=0.8V 0.2 0.4	
8T10			0.8	2.0					−1.5	5.5				N/A			N/A			V_{IN}=0.8V I_{OL}=32mA 0.4	
8T13			0.8	2.0					−1.5	5.5				N/A			N/A			N/A	
8T14			0.8	2.0				NOTE: Hysteresis is 0.3V MIN, 0.5V TYP	−1.5	5.5				N/A			N/A			I_{OL}=16mA R=0.8V, S=2.0V A, B=0V 0.4 Note 10 R, S=0V, A, B=2.0V 0.4 Note 10	
8T15			0.8	2.0					−1.5	5.5	Note 23			N/A			N/A		−5.0	V_{IN}=2.0V I_{OL}=4.0mA −6.0	−7.0
8T16	See Data Sheet for Electrical Characteristics																				
8T18		N/A			N/A				−1.5	50	Driven Input=100μA Others=0V			N/A			N/A			V_{CC1}=4.75V V_{CC2}=20.0V Others=9.0V I_{OL}=7.2mA 0.35	
8T20								$V_{(REF)}$=0.8V MIN, 2.0V MAX, Pin 6 tied to Pin 7	−1.5	5.5					±4					I_{OL}=16mA 0.4	
8T22			0.9	1.9					−1.5		N/A			N/A			N/A			I_{OL}=12.8mA 0.2	0.45
8T23			0.8	2.0					−1.5	5.5				N/A			N/A			Gate #1 Input Under Test=0.8V Other=4.5V Gate #2=0V I_{OL}=−240μA 0.15 Note 15	
8T24			0.7	1.7				S, A, B	−1.5	5.5 S, A, B				N/A			N/A			R=0.7V, S=1.7V A, B=0V, I_{OL}=16mA 0.2 0.4 R, S=0V, A, B=1.7V 0.2 0.4 I_{OL}=16mA	
8T25			0.8	2.0				DIS, STR	−1.5	5.5 IBUI=1mA DIS, STR				N/A			N/A			A, B=200μA Disable, Strobe=0.8V 0.4 I_{OL}=16mA	

INTERFACE-LOGIC (Cont'd)

		INPUT CURRENT		OUTPUT CURRENT		POWER SUPPLY		
PARAMETER	V_{OH} (V)* HIGH LEVEL	I_{IL} (mA) LOW LEVEL	I_{IH} (μA) HIGH LEVEL	I_{CBO} (μA)* LEAKAGE CURRENT	I_{OS}* SHORT CIRCUIT CURRENT	I_{CC} POWER/CURRENT CONSUMPTION (mW/mA)		I_{CC} (mA) V_{IN}=2.0V
TEST CONDITIONS	V_{CC}=MIN I_{OH}=−160μA	V_{CC}=MAX V_{IN}=0.4V	V_{CC}=MAX V_{IN}=4.5V	V_{IN}=2.0V	V_{CC}=MAX V_{IN}=0V V_{OUT}=0V	V_{CC}=MAX V_{IN}=0V MILITARY	COMMERCIAL	V_{CC}=MAX
	MIN TYP MAX	MIN TYP MAX	MIN TYP MAX	MIN TYP MAX	MIN TYP MAX	TYP MAX	TYP MAX	MIN TYP MAX
8T04	RBO 3.1	RB1 −.1 −1.2 B1 −.1 −2.2 LT −.1 −10 Others −.1 −1.6	RB1 40 LT 160 Others 80	V_{IN}=0.8V A-G 100 Outputs=6.0V	N/A	394/75	446/85	N/A
8T05	A-G Outputs=−500μA LT=0.4V 3.9 RBO RBO/B1=−160μA 3.1	RB1 −.1 −1.2 B1 −.1 −2.2 LT −.1 −1.0 Others −.1 −1.6	RB1 40 LT 160 Others 80	N/A	N/A	394/75	110/85	N/A
8T06	RBO 3.1	RB1 −.1 −1.2 B1 −.1 −2.2 LT −.1 −10 Others −.1 −1.6	RB1 40 LT 160 Others 80	A-G LT=0.4V Outputs=6.0V 100	N/A	394/75	446/85	N/A
8T09	Outputs=−5.2mA V_{IN}=0.8V 2.4 3.0	−2.0	40	Outputs=0.4V or 2.4V Disable=2.0V −40 +40	−40 −120	N/A	236/45 340/65	N/A
8T10	D_N=2.0V Others=0.8V I_{OH}=−5.2mA 2.4 3.0	D_N −.100 −3.2 Others −.100 −2.0	D_N 50 Others 40	Outputs=0.4V or 2.4V Outdis=2.0V Others=0.8V −40 +40	D_N=4.5V V_{IN}=0.4V −40 −120	N/A	619/118	N/A
8T13	Gate #1 V_{IN}=2.0V Gate #2 V_{IN}=0.8V I_{OH}=−75mA 2.4	−.1 −1.6	40	HIGH Level Outputs=3.0V V_{IN}=0V 80 LOW Level Outputs=0.4V Gate #1 Input Under Test V_{IN}=0.8V Others V_{IN}=4.5V Gate #2 V_{IN}=0V −800	Gate #1 V_{IN}=4.5V Gate #2 V_{IN}=0V −30	N/A	HIGH Level V_{IN}=2.0V 150/28 LOW Level V_{IN}=0.8V 315/60	
8T14	I_{OH}=−800μA R=2.0V, S=4.5V A, B=0V 2.6 3.5 Note 11 R, A, B=0V, S=0.8V 2.6 3.5 Note 11	−.1 −1.6 SN, AN, BN	SN, AN, BN 40 R=3.8V R_N .17mA R=3.8V	N/A	−50 −100	N/A	315/60 380/76	N/A
8T15	V_{IN}=0.8V I_{OH}=−4.0mA 5.0 6.0 7.0	−0.1 −0.8 −1.6	40	N/A	Out=−25V −25 Out=+25V +25 Note 23	N/A Positive Supply Negative Supply Note 23	Per Driver 275/16 28	N/A
8T16								
8T18	V_{CC1}=4.75V V_{CC2}=24.0V Driven Input=6.5V I_{OH}=−225μA 3.4	N/A	N/A	N/A	Driven Input=0V −75	V_{CC1}=5.25V V_{CC2}=24V N/A	(Per Gate) V_{CCIL} 44 V_{CCIH} 1 V_{CC2L} 39 V_{CC2H} 38	N/A
8T20	I_{OL}=−800μA 2.6	REC, NEC −0.1 −2.4 Clear −0.1 −1.6 Common Mode Range[21] −3.2 4.2	40 Bias 125 Offset 2		−20 −70	N/A	N/A	37 55 I_{EE} V_{CC}=−5.25V −12 −20
8T22	I_{OH}=−960μA 2.4 3.4	−1.6 V_{IN}=.45V	60	N/A	−10 −40	N/A	N/A	25
8T23	Gate #1=2.0V Gate #2=0.8V I_{OH}=−59.3mA 3.11	−.1 −1.6	40	40	Gate #1=4.5V Gate #2=0V −100 −250 V_{OUT}=2.0V	N/A	HIGH Level[14] V_{IN}=2.0V 150/28 LOW Level[14] V_{IN}=0.8V 315/60	N/A
8T24	R=1.7V, S=4.5V A, B=0V 2.6 3.4 I_{OH}=−800μA R, A, B=0V, S=0.7V 2.6 3.4 I_{OH}=−800μA	−.1 −1.6 SN, AN, BN	V_{CC}=0V SN, AN, BN 40 R=3.11V RN 0.17mA R=7.0V RN 5.0mA R=6.0V RN 5.0mA		−50 −100 R=3.11V S, A, B=0V	N/A	315/60 380/72	N/A
8T25	A, B=400μA Disable, Strobe=0.8V 2.8 3.5 I_{OH}=−1.5mA	−.1 −1.6 V_{IN}=0V STR, PRE/DIS	STR, DIS 40	DIS=2V, STR=.8V OUT=3.9V 100 Output A A=200μA, B=1.5mA Output B A=1.5mA, B=200μA	−20 −70 STR=0V	N/A	A, B=400μA Disable=4.5V Strobe=0V 210/40	N/A

INTERFACE-LOGIC (Cont'd)

PARAMETER	INPUT VOLTAGE																		OUTPUT VOLTAGE		
	V_{IL} (V) LOW LEVEL			V_{IH} (V) HIGH LEVEL			V_{IC} CLAMP VOLTAGE			VOLTAGE RATING			V_{TL} (mV)[20] LOW LEVEL THRESHOLD VOLTAGE			V_{TH} (mV)[20] HIGH LEVEL THRESHOLD VOLTAGE			V_{OL} (V)[7] LOW LEVEL		
TEST CONDITIONS							V_{CC}=MIN I_{IN}=-12mA			V_{IN}=10mA			V_{CC}=MIN V_{IN}=0.8V I_{OL}=-400µA			V_{CC}=MAX V_{IN}=0.8V I_{OH}=16mA			V_{CC}=MIN		
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
8T26A		N/A			N/A				-1.0		N/A		0.85					2		Driver I_{OL}=48mA Receiver I_{OL}=20mA	 0.5 0.5
8T28		N/A			N/A				-1.0		N/A		0.85					2		Driver I_{OL}=48mA Receiver I_{OL}=20mA	 0.5 0.5
8T30			0.8	2.0				N/A			N/A			N/A			N/A		 -1.2	V_{IN}=0.8V, 2.0V Transmit Outputs I_{OL}=60mA TTL/DTL Transceivers I_{OL}=24mA MOS Transceivers I_{OL}=-1mA	 0.4 0.4 0.4
8T31		N/A			N/A		I_{IN}=-5mA		-1		N/A			N/A			N/A			I_{OL}=20mA	0.55
8T32[16]			.8	2.0			I_{IN}=-5mA		-1		N/A			N/A			N/A			I_{OL}=16mA	0.55
8T33[16]			.8	2.0			I_{IN}=-5mA		-1		N/A			N/A			N/A			I_{OL}=16mA	0.55
8T34			0.8	2.0				-1	-1.5	5.5	I_{IN}≤1mA		1.05	1.30 Receiver	1.55	1.80	2.25 Receiver	2.50		Receiver I_{OL}=16mA 0.25 Bus I_{OL}=50mA	 0.4 0.7
8T37	Disable		0.8	Disable 2.0				-1	-1.5		N/A		1.05	1.30 Receiver	1.55	1.80	2.25 Receiver	2.50		Receiver=4.0V, 0.5V Disable=0.8V, 2.0V I_{OL}=16mA	 0.4
8T38			0.8	2.0				-1	-1.5	5.5	I_{IN}≤1mA		1.05	1.30	1.55	1.80	2.25 Receiver	2.50		Bus Driver I_{OL}=50mA Receiver I_{OL}=16mA 0.25	 0.7 0.4
8T80			0.6	2.0					-1.5		N/A			N/A			N/A			V_{IN}=2.0V[19] I_{OL}=20mA	 1.0
8T90			0.6	2.0					-1.5		N/A			N/A			N/A			V_{IN}=2.0V[19] I_{OL}=7.2mA I_{OL}=20mA	 0.35
8T93			0.8	2.0				I_{IN}=-18mA	-1.2	5.5	I_{IN}=1mA			N/A			N/A			V_{IN}=2.0V I_{OL}=20mA	 0.5
8T94			0.8	2.0				I_{IN}=-18mA	-1.2	5.5	I_{IN}=1mA			N/A			N/A			V_{IN}=2.0V I_{OL}=20mA	 0.5
8T95			0.8	2.0				Input Output to Ground	-1.5 -1.5	5.5	I_{IN}=1mA			N/A			N/A			I_{OL}=48mA	0.5
8T96			0.8	2.0				Input Output to Ground	-1.5 -1.5	5.5	I_{IN}=1mA			N/A			N/A.			I_{OL}=48mA	0.5

INTERFACE

INTERFACE-LOGIC (Cont'd)

PARAMETER	V_{OH} (V)* HIGH LEVEL	INPUT CURRENT: I_{IL} (mA) LOW LEVEL	INPUT CURRENT: I_{IH} (µA) HIGH LEVEL	OUTPUT CURRENT: I_{CBO} (µA)* LEAKAGE CURRENT	OUTPUT CURRENT: I_{OS}* SHORT CIRCUIT CURRENT	POWER SUPPLY: I_{CC} POWER/CURRENT CONSUMPTION (mW/mA) – MILITARY	POWER SUPPLY: I_{CC} POWER/CURRENT CONSUMPTION (mW/mA) – COMMERCIAL	POWER SUPPLY: I_{CC} (mA) V_{IN}=2.0V
TEST CONDITIONS	V_{CC}=MIN I_{OH}=−160µA	V_{CC}=MAX V_{IN}=0.4V	V_{CC}=MAX V_{IN}=4.5V	V_{IN}=2.0V	V_{CC}=MAX V_{IN}=0V V_{OUT}=0V	V_{CC}=MAX V_{IN}=0V	V_{CC}=MAX V_{IN}=0V	V_{CC}=MAX
	MIN TYP MAX	MIN TYP MAX	MIN TYP MAX	MIN TYP MAX	MIN TYP MAX	TYP MAX	TYP MAX	MIN TYP MAX
8T26A	Driver I_{OL}=−10mA 2.4 Receiver I_{OL}=−100µA 3.5 I_{OL}=−2.0mA 2.4	Driver LOW Level −200 LOW Level (Disabled) −25 Receiver −200	Driver/Receiver 25	HIGH Level V_{OUT}=2.4V 100 LOW Level V_{OUT}=0.5V −100	Driver −50 −150 Receiver −30 −75	N/A	457/87	N/A
8T28	Driver I_{OL}=−10mA 2.4 Receiver I_{OL}=−100µA 3.5 I_{OL}=−2.0mA 2.4	Driver LOW Level −200 LOW Level (Disabled) −25 Receiver −200	Driver/Receiver 25	HIGH Level V_{OUT}=2.4V 100 LOW Level V_{OUT}=0.5V −100	Driver −50 −150 Receiver −30 −75	N/A	578/110	N/A
8T30	V_{IN}=0.8V, 2.0V TTL/DTL Transceivers I_{OL}=−150µA 3.0 MOS Transceivers I_{OL}=−1.6mA 4.25	Enable/Wraparound Inputs −1.6 TTL/DTL Transceivers/ Receive Inputs −3.2 MOS Transceivers −0.5	Enable/Wraparound Inputs 40 Receive Inputs 80 MOS Transceivers 200	V_{IN}=0.8V, 2.0V 250 V_{OUT}=V_{CC}	N/A	N/A	370/70 Rec Enable=0V	N/A
8T31	I_{OL}=−3.2mA 2.4	V_{IN}=0.55V −500	V_{IN}=5.5V 100	−10	−20 −200	N/A	N/A	150
8T32[16]	I_{OH}=−3.2mA 2.4	V_{IL}=.5V[17] −350 −550	V_{IH}=5.25V[17] <10 100	N/A	VD Bus 10 IV Bus 20	N/A	N/A	100 150
8T33[16]	I_{OH}= 3.2mA 2.4	V_{IL}=.5V[17] −350 −550	V_{IH}=5.25V[17] <10 100	N/A	VD Bus 10 IV Bus 20	N/A	N/A	100 150
8T34	Receiver I_{OL}=−400µA 2.4 Bus I_{OL}=10.4mA 2.4	−1.6	Disable & Driver V_{IN}=2.4V 50 V_{IN}=4.0V Bus–Power ON 20 100 Bus–Power OFF 20 100 V_{CC}=0V	N/A	Receiver −18 −33 −55 Driver −60 −80 −105	N/A	N/A	40 60 Power Dissipation 210mW 315mW
8T37	Receiver=0.5V Disable=0.8V I_{OL}=−400µA 2.4	Disable −3.2	V_{IN}=2.4V Disable 80 Receiver 15 50 V_{CC}=0V Receiver 1 50	N/A	−18 −55	N/A	315/16	N/A
8T38	Receiver I_{OL}=−400µA 2.4	−1.6	V_{IN}=2.4V Disable/Driver 50 V_{IN}=4.0V Bus–Power ON 20 100 Bus–Power OFF V_{CC}=0V 2 100	N/A	−18 −33 −55	N/A	N/A	40 60 Power Dissipation 210mW 315mW
8T80	N/A	−.1 −1.6	25	V_{IN}=0.6V[18] 100	N/A	N/A	(Per Gate) HIGH Level 7.9 LOW Level 20	N/A
8T90	N/A	−.1 −1.6 V_{IN}=.35V	25	V_{IN}=0.6V[18] 100	N/A	N/A	(Per Gate) HIGH Level 7.9/1.51 LOW Level 20/3.81	N/A
8T93	V_{IN}=0.8V I_{OL}=−1mA 2.7 3.3	V_{IN}=0.5V −400	10	N/A	−40 −100	N/A	N/A	15 24 I_{CCL} 30 54
8T94	N/A	V_{IN}=0.5V −400	10	V_{IN}=0.8V[8] 250 V_{OUT}=5.5V	−40 −100	N/A	N/A	I_{CCL} 30 54 I_{CCH} 9 20
8T95	I_{OL}=−5.2mA 2.4	V_{IN}=0.5V DIS=0.5V −400 DIS=2.0V Third State −40 V_{IN}=.5V	V_{IN}=2.4V 40	N/A Third State Output Current V_{OUT}=2.4V 40 V_{OUT}=0.5V −40	−40 −80 −115	N/A	N/A	65 98
8T96	I_{OL}=−5.2mA 2.4	V_{IN}=0.5V DIS=0.5V −400 DIS=2.0V Third State −40 V_{IN}=.5V	V_{IN}=2.4V 40	N/A Third State Output Current V_{OUT}=2.4V 40 V_{OUT}=0.5V −40	−40 −80 −115	N/A	N/A	59 89

INTERFACE-LOGIC (Cont'd)

	INPUT VOLTAGE																					OUTPUT VOLTAGE		
PARAMETER	V_{IL} (V) LOW LEVEL			V_{IH} (V) HIGH LEVEL			V_{IC} CLAMP VOLTAGE			VOLTAGE RATING			VT_L (mV)[20] LOW LEVEL THRESHOLD VOLTAGE			VT_H (mV)[20] HIGH LEVEL THRESHOLD VOLTAGE			V_{OL} (V)[7] LOW LEVEL					
TEST CONDITIONS							V_{CC}=MIN I_{IN}=−12mA			V_{IN}=10mA			V_{CC}=MIN V_{IN}=0.8V I_{OL}=−400μA			V_{CC}=MAX V_{IN}=0.8V I_{OH}=16mA			V_{CC}=MIN					
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
8T97			0.8	2.0				Input Output to Ground	−1.5 −1.5	5.5	I_{IN}=1mA			N/A			N/A			I_{OL}=48mA	0.5			
8T98			0.8	2.0				Input Output to Ground	−1.5 −1.5	5.5	I_{IN}=1mA			N/A			N/A			I_{OL}=48mA	0.5			
8T100		N/A			N/A			I_{IN}=−18mA	−1.5		N/A			N/A			N/A			I_{OL}=20mA I_{OL}=40mA	.45 0.5			
8T101		N/A			N/A			I_{IN}=−18mA	−1.5		N/A			N/A			N/A			I_{OL}=20mA I_{OL}=40mA	.45 0.5			
8T110			0.8	2.0				N/A			Common Mode Voltage Range	±15		−15V≤V_{CM}≤+15V V_{OUT}≤0.5V I_{OL}=20mA	−1.0		−15V≤V_{CM}≤+15V V_{OUT}≥2.7V I_{OH}=−1.0mA	1.0		V_{DIFF}=−1V I_{OL}=20mA	0.5			
8T111			0.8	2.0				N/A			Common Mode Voltage Range	±15		−15V≤V_{CM}≤+15V V_{OUT}≤0.5V I_{OL}=20mA	−1.0		−15V≤V_{CM}≤+15V V_{OUT}≥2.7V I_{OH}=−1.0mA	1.0		V_{DIFF}=−1V I_{OL}=20mA	0.5			
8T363	See Data Sheet for Electrical Characteristics																							
8T380		N/A			N/A				−1.5		N/A		1.1	1.3	1.5	2	2.25	2.5		I_{OL}=16mA	0.4			

NOTES:
1. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. All measurements are taken with ground pin tied to zero volts.
3. Positive current is defined as into the terminal referenced.
4. Precautionary measures should be taken to insure current limiting in accordance with absolute maximum ratings.
5. Measurements apply to each gate element independently.
6. Output source current is supplied through a resistor to ground.
7. Output sink current is supplied through a resistor to V_{CC}.
8. Connect an external 1k±1% resistor to the output for this test.
9. Not more than one output should be shorted at one time.
10. Previous condition is a HIGH level output state.
11. Previous condition is a LOW level output state.
12. Test each driver separately.
13. For more electrical specifications see data sheet.
14. I_{CC} is dependent upon loading. I_{CC} limit specified is for no-load test condition for both drivers.
15. With forced output current of 240μA, the output voltage must not exceed 0.15V.
16. These limits do not apply during address programming.
17. The input current includes the tri-state/open collector leakage current of the output driver on the data lines.
18. Output leakage current is supplied through a 2kΩ resistor to 30V.
19. Output sink current is supplied through a resistor to 30V.
20. The differential input threshold voltage is defined as the maximum DC voltage duration from the reference level necessary to trigger the one-shot.
21. Common mode voltages that are confined within the dynamic range as specified will not cause false triggering of the one-shot.
22. Hysteresis is defined as voltage difference between R input level at which output begins to go from "0" to "1" state and level at which output begins to go from "1" to "0". Refer to Hysteresis test circuit.
23. V_{CC}=+12.6V, V_{EE}=−12.6V.

INTERFACE

INTERFACE-LOGIC (Cont'd)

		INPUT CURRENT		OUTPUT CURRENT		POWER SUPPLY		
PARAMETER	V_{OH} (V) HIGH LEVEL	I_{IL} (mA) LOW LEVEL	I_{IH} (μA) HIGH LEVEL	I_{CBO} (μA) LEAKAGE CURRENT	I_{OS} SHORT CIRCUIT CURRENT	I_{CC} POWER/CURRENT CONSUMPTION (mW/mA)		I_{CC} (mA) V_{IN}=2.0V
TEST CONDITIONS	V_{CC}=MIN I_{OH}=−160μA	V_{CC}=MAX V_{IN}=0.4V	V_{CC}=MAX V_{IN}=4.5V	V_{IN}=2.0V	V_{CC}=MAX V_{IN}=0V V_{OUT}=0V	V_{CC}=MAX V_{IN}=0V MILITARY	COMMERCIAL	V_{CC}=MAX
	MIN TYP MAX	MIN TYP MAX	MIN TYP MAX	MIN TYP MAX	MIN TYP MAX	TYP MAX	TYP MAX	MIN TYP MAX
8T97	I_{OL}=−5.2mA 2.4	V_{IN}=0.5V DIS=0.5V −400 DIS=2.0V Third State −40 V_{IN}=.5V	V_{IN}=2.4V 40	N/A Third State Output Current V_{OUT}=2.4V 40 V_{OUT}=0.5V −40	−40 −80 −115	N/A	N/A	65 98
8T98	I_{OL}= 5.2mA 2.4	V_{IN}=0.5V DIS=0.5V −400 DIS=2.0V Third State −40 V_{IN}=.5V	V_{IN}=2.4V 40	N/A Third State Output Current V_{OUT}=2.4V 40 V_{OUT}=0.5V −40	−40 −80 −115	N/A	N/A	59 89
8T100	I_{OH}=20mA 2.6 I_{OH}=40mA 1.8	Data Inputs −400 Mode Control 1200	Data Inputs 40 Mode Control 120	N/A	N/A	N/A	N/A	100
8T101	I_{OH}=20mA 2.6 I_{OH}=40mA 1.8	Data Inputs −400 Mode Control 1200	Data Inputs 40 Mode Control 120	N/A	100	N/A	N/A	100
8T110	V_{DIFF}=+1V I_{OH}=−1mA 2.7	V_{IN}=0.5V 400 Data-Inverting V_{CM}=+.15V 1.5 V_{CM}=0V −0.5 V_{CM}=−15V −1.5 Data-Non-Inverting V_{CM}=+15V 1.7 2.1 V_{CM}=0V −0.4 −0.6 V_{CM}=−15V −2.5 −3.1	V_{IN}=2.7V −40	HIGH Level V_O=2.7V V_{IN}(DIS)=2.0V V_{IN}=0.5V −50 LOW Level V_O=0.5V V_{IN}(DIS)=2.0V V_{IN}=2.7V +50	−40 −100	N/A	N/A	40 55
8T111	V_{DIFF}=+1V I_{OH}=−1mA 2.7	V_{IN}=0.5V 400 Data-Inverting V_{CM}=+.15V 1.5 V_{CM}=0V −0.5 V_{CM}=−15V −1.5 Data-Non-Inverting V_{CM}=+15V 1.7 2.1 V_{CM}=0V −0.4 −0.6 V_{CM}=−15V −2.5 −3.1	V_{IN}=2.7V −40	HIGH Level V_O=2.7V, V_{IN}=0.5V V_{IN}(DIS)=2.0V −50 LOW Level V_O=0.5V, V_{IN}=2.7V V_{IN}(DIS)=2.0V +50	−40 −100	N/A	N/A	40 55
8T363								
8T380	I_{OH}= 400μA 2.4	N/A	15 50 V_{CC}=0V 1 50	N/A	V_{IN}=0.5V −18 −55	N/A	132/25 210/40	

ANALOG INTERFACE - GENERAL
AC ELECTRICAL CHARACTERISTICS

	Input Voltage			Output Voltage		Threshold Voltage		Input Current
PARAMETER	V_{IL}(V) Low Level	V_{IH}(V) High Level	V_{IC}(V) Clamp Voltage	V_{OL}(V) Low Level	V_{OH}(V) High Level	V_{TL}(V) Low Level	V_{TH}(V) High Level	I_I(mA) Input Current At Max Input Voltage
TEST CONDITIONS	V_{CC}=MIN	V_{CC}=MIN	V_{CC}=MAX I_{IN}=−12mA	V_{CC}=MIN V_{IN}=2.0V	V_{CC}=MIN V_{IN}=0.8V	T_A=25°C V_{OUT}≤2.5V I_{OUT}=−0.5mA	T_A=25°C V_{OUT}≤0.45V I_{OUT}=10mA	V_{CC}=5.5V V_{IN}=5.5V
	Min Typ Max	Min Typ Max	Min Typ Max	Min Typ Max	Min Typ Max	Min Typ Max	Min Typ Max	Min Typ Max
NE582	N/A	N/A	N/A	N/A	V_{IN}=2V, I_R=2mA I_{OL}=20mA .025 .060 V_{IN}=6.5V, I_R=12mA I_{OL}=250mA .320 .450 V_{IN}=6.5V, I_R=20mA I_{OL}=400mA .500 .750			V_{IN}=10V I_R=2mA I_{OL}=20mA 2.2 3.3
NE584	See Data Sheet For Electrical Specifications							
NE585	See Data Sheet For Electrical Specifications							
DM7820/8820	See Data Sheet For Electrical Specifications							
DM7830/8830[1]	0.8	2.0	N/A	I_{OUT}=32mA 0.2 0.4 I_{OUT}=40mA 0.22 0.5	I_{OUT}=−0.8mA 2.4 I_{OUT}=40mA 1.8 2.9	N/A	N/A	
DM8880	0.8	2.0	−0.9 −1.5	I_{OUT}=SmA RBO 0.13 0.4	I_{OUT}=200μA 2.4 3.7	N/A	N/A	N/A
MC1488[4]	N/A	N/A	N/A	R_L=3.0K V+=9.0V, V−=−9.0V −6.0 −6.8 V+=13.2V, V−=−13.2V −9.0 −10.5	R_L=3.0K V+=9.0V, V−=−9.0V 6.0 7.0 V+=13.2V, V−=−13.2V 9.0 10.5	N/A	N/A	N/A

ANALOG INTERFACE - GENERAL
AC ELECTRICAL CHARACTERISTICS (Cont'd)

	Input Current		Output Current		Power Supply		
PARAMETER	I_{IL}(mA) Low Level	I_{IH}(μA) High Level	I_{OL} Low Level	I_{OH}(μA) High Level	I_{OS}(mA) Short Circuit	I_{CCL}(mA) Low Level	I_{CCH}(mA) High Level
TEST CONDITIONS	V_{CC}=5.25V V_{IN}=0.4V	V_{CC}=5.25V V_{IN}=2.0V		V_{CC}=MIN V_{IN}=2V V_{OH}=30V	V_{OUT}=0V	T_A=25°C V_{CC}=MAX V_{IN}=0V	T_A=25°C V_{CC}=MAX V_{IN}=5V
	Min Typ Max	Min Typ Max	Min Typ Max	Min Typ Max	Min Typ Max	Min Typ Max	Min Typ Max
NE582	N/A	N/A	N/A	N/A	N/A	N/A	N/A
NE584 NE585 DM7820/8820							
DM7830/8830[1]	4.8	120 V_{IN}=5.5V 2mA	N/A	N/A	–40 –100	(Each Driver)	N/A
DM8880	B1 –1.2 –2.0 Except B1 –300 –600	Except B1 2 15 V_{IN}=5.5V 4 400	N/A	N/A	N/A	Rp=2.2K 27 43	N/A
MC1488[4]	V_{IN}=0V –1.0 –1.3	V_{IN}=5V .005 10.0	N/A	N/A	High Level V_{IN}=0.8V –6.0 10.0 –12.0 Low Level V_{IN}=1.9V 6.0 10.0 12.0	V_{IN}=1.9V V+=9.0V, V–=–9.0V –13.0 –17.0 V+=12V, V–=12V –18.0 –23.0 V+=15V, V–=–15V –25.0 –34.0 V_{IN}=0.8V V+=9.0V, V–=9.0V –.001 –1.0 V+=12V, V–=–12V –.001 –1.0 V+=15V, V–=–15V –.01 –2.5	 15.0 20.0 19.0 25.0 25.0 34.0 4.5 6.0 5.5 7.0 8.0 12.0

ANALOG INTERFACE - GENERAL
AC ELECTRICAL CHARACTERISTICS (Cont'd)

	Input Voltage									Output Voltage						Threshold Voltage						Input Current		
PARAMETER	V_{IL}(V) Low Level			V_{IH}(V) High Level			V_{IC}(V) Clamp Voltage			V_{OL}(V) Low Level			V_{OH}(V) High Level			V_{TL}(V) Low Level			V_{TH}(V) High Level			I_I(mA) Input Current At Max Input Voltage		
TEST CONDITIONS	V_{CC}=MIN			V_{CC}=MIN			V_{CC}=MAX I_{IN}=−12mA			V_{CC}=MIN V_{IN}=2.0V			V_{CC}=MIN V_{IN}=0.8V			T_A=25°C V_{OUT}≤2.5V I_{OUT}=−0.5mA			T_A=25°C V_{OUT}≤0.45V I_{OUT}=10mA			V_{CC}=5.5V V_{IN}=5.5V		
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max
MC1489[5]	N/A			N/A			N/A			V_{IN}=3.0V I_{OUT}=10mA			V_{IN}=0.75V I_{OUT}=−0.5mA									N/A		
											0.33	0.45	2.6	3.8	5.0	0.75		1.25	1.75		2.2			
75S107	N/A			N/A			N/A			N/A			N/A			N/A			N/A			N/A		
75S108	N/A			N/A			N/A			I_{OUT}=20mA			N/A			N/A			N/A			N/A		
												0.5												

INTERFACE

ANALOG INTERFACE - GENERAL
AC ELECTRICAL CHARACTERISTICS (Cont'd)

	Input Current		Output Current		Power Supply		
PARAMETER	I_{IL}(mA) Low Level	I_{IH}(μA) High Level	I_{OL} Low Level	I_{OH}(μA) High Level	I_{OS}(mA) Short Circuit	I_{CCL}(mA) Low Level	I_{CCH}(mA) High Level
TEST CONDITIONS	V_{CC}=5.25V V_{IN}=0.4V	V_{CC}=5.25V V_{IN}=2.0V		V_{CC}=MIN V_{IN}=2V V_{OH}=30V	V_{OUT}=0V	T_A=25°C V_{CC}=MAX V_{IN}=0V	T_A=25°C V_{CC}=MAX V_{IN}=5V
	Min Typ Max	Min Typ Max	Min Typ Max	Min Typ Max	Min Typ Max	Min Typ Max	Min Typ Max
MC1489[5]	V_{IN}=25V 3.6 5.6 8.3 V_{IN}=25V −3.6 −5.6 −8.3 V_{IN}=3V 0.43 0.53 V_{IN}=3V −0.43 −0.53	N/A	N/A	N/A	V_{IN}=0.75V 3.0	V_{IN}=5.0V 20 26	N/A
75S107	V_{IL}=0.5V 1G or 2G Strobe −2.0 Common Strobe S −4.0	V_{IH}=2.7V 1 G or 2 G Strobe 50 Common Strobe S 100 V_{IH}=5.5V 1G or 2G Strobe 1mA Common Strobe S 2mA	N/A	N/A	−40 −100	−11 −15	20 30
75S108	V_{IN}=0.5V 1G or 2G Strobe −2.0 Common Strobe S −4.0	V_{IH}=2.7V 1G or 2G Strobe 50 Common Strobe S 100 V_{IH}=5.5V 1G or 2G Strobe .1mA Common Strobe S 2mA	N/A		N/A	−11 −15	20 30

ANALOG INTERFACE - GENERAL
AC ELECTRICAL CHARACTERISTICS (Cont'd)

	Input Voltage						Output Voltage									Threshold Voltage						Input Current		
PARAMETER	V_{IL}(V) Low Level			V_{IH}(V) High Level			V_{IC}(V) Clamp Voltage			V_{OL}(V) Low Level			V_{OH}(V) High Level			V_{TL}(V) Low Level			V_{TH}(V) High Level			I_I(mA) Input Current At Max Input Voltage		
TEST CONDITIONS	V_{CC}=MIN			V_{CC}=MIN			V_{CC}=MAX I_{IN}=−12mA			V_{CC}=MIN V_{IN}=2.0V			V_{CC}=MIN V_{IN}=0.8V			T_A=25°C V_{OUT}≤2.5V I_{OUT}=−0.5mA			T_A=25°C V_{OUT}≤0.45V I_{OUT}=10mA			V_{CC}=5.5V V_{IN}=5.5V		
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max
75450B6			0.8	2.0					−1.5	I_{OL}=16mA	0.22	0.5	I_{OH}=−400µA 2.4	3.3			N/A			N/A		A G		1 2
75451B6			0.8	2.0					−1.5	V_{IL}=0.8V I_{OL}=100mA I_{OL}=300mA	0.25 0.5	0.5 0.8		N/A			N/A			N/A				1
75452B6			0.8	2.0					−1.5	I_{OL}=100mA I_{OL}=300mA	0.25 0.5	0.5 0.8		N/A			N/A			N/A				1
75453B6			0.8	2.0					−1.5	I_{OL}=100mA I_{OL}=300mA	0.25 0.5	0.5 0.8		N/A			N/A			N/A				1
75454B6			0.8	2.0					−1.5	I_{OL}=100mA I_{OL}=300mA	0.25 0.5	0.5 0.8		N/A			N/A			N/A				1

INTERFACE

ANALOG INTERFACE - GENERAL
AC ELECTRICAL CHARACTERISTICS (Cont'd)

	Input Current						Output Current						Power Supply								
PARAMETER	I_{IL}(mA) Low Level			I_{IH}(μA) High Level			I_{OL} Low Level			I_{OH}(μA) High Level			I_{OS}(mA) Short Circuit			I_{CCL}(mA) Low Level			I_{CCH}(mA) High Level		
TEST CONDITIONS	V_{CC}=5.25V V_{IN}=0.4V			V_{CC}=5.25V V_{IN}=2.0V						V_{CC}=MIN V_{IN}=2V V_{OH}=30V			V_{OUT}=0V			T_A=25°C V_{CC}=MAX V_{IN}=0V			T_A=25°C V_{CC}=MAX V_{IN}=5V		
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max
75450B[6]	A G		-1.6 -3.2	A G		40 80		N/A			N/A		-18			V_{IN}=5V	6	11	V_{IN}=0V	2	4
75451B[6]		-1	-1.6			40		N/A				300		N/A			52	85		7	11
75452B[6]		-1	-1.6			40		N/A				300		N/A		V_{IN}=5V	56	71	V_{IN}=0V	11	14
75453B[6]		-1	-1.6			40		N/A				300					54	68		8	11
75454B[6]		-1	-1.6			40		N/A				300				V_{IN}=5V	61	79	V_{IN}=0V	13	17

NOTES FOR ELECTRICAL CHARACTERISTICS TABLE

1. Specifications apply for DM7830: $-55°C \leq T_A \leq +125°C$, V_{CC} = +5V ± 10%, DM8830: $0°C \leq T_A \leq 70°C$, V_{CC} = +5V ± 5% unless otherwise specified.
2. Applies for T_A = +125°C only.
3. Voltage values shown are with respect to network ground terminal. Positive current is defined as current into the referenced pin.
4. These specifications apply for V+ = +9.0V ± 1%, V− = −9.0V ± 1% and T_A = 25°C.
5. These specifications apply for response control pin = open.
6. For additional electrical specifications, see data sheet.

ANALOG INTERFACE-MEMORIES
AC ELECTRICAL CHARACTERISTICS

	Input Voltage									Output Voltage									Input Current		
Parameter Test Conditions	V_{IL} (V) Low Level V_{CC}=4.75V V_{IN}=2V			V_{IH} (V) High Level V_{CC}=4.75V V_{IL}=0.8V			V_{IC} (V) Clamp Voltage I_{IL}=−12mV			V_{OL} (V) Low Level V_{CC}=4.75V V_{IN}=2V I_{OL}=16mA			V_{OH} (V) High Level V_{CC}=5V V_{IN}=0.85V I_{OH}=−400µA			V_{OL} (V) Clamp Voltage V_{IN}=0V I_{OH}=20mA			I_I (mA) V_{IN}=5.5V		
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max
3207A[1] V_{SS}=16V, V_{BB}=19V		V_{CC}=5V	1.0	2.0	V_{CC}=5V			N/A		0°C 25°C	I_{OL}=500µA	0.8 0.7	V_{SS}−0.7 V_{SS}−0.6 V_{SS}−0.5	I_{OH}=−500µA	0°C 25°C 75°C		N/A			N/A	
3207A−1[1] V_{SS}=19V, V_{BB}=23V		V_{CC}=5V	1.0	2.0	V_{CC}=5V			N/A		0°C 25°C 75°C	I_{OL}=500µA	0.8 0.7 0.6	V_{SS}−0.7 V_{SS}−0.6 V_{SS}−0.5	I_{OH}=−500µA	0°C 25°C 75°C		N/A			N/A	
75S207			0.8	2.0				N/A			I_{OL}=20mA	0.5	2.7	I_{OH}=−1mA 3.4							
75S208			0.8	2.0				N/A			I_{OL}=20mA	0.5		N/A			N/A			N/A	
7520[1]			0.8	2.0				N/A			0.25	0.4	2.4	3.9			N/A			N/A	
7521[1]			0.8	2.0				N/A			0.25	0.4	2.4	3.9			N/A			N/A	
7522[1]			0.8	2.0				N/A			0.2	0.4	2.4	3.9			N/A			N/A	
7523[1]			0.8	2.0				N/A			0.2	0.4	2.4	3.9			N/A			N/A	
7524[1]			0.8	2.0				N/A			0.25	0.4	2.4	3.9			N/A			N/A	
7525[1]			0.8	2.0				N/A			0.25	0.4	2.4	3.9			N/A			N/A	
75324			0.8	3.5				N/A			N/A			N/A			N/A			N/A	

ANALOG INTERFACE-MEMORIES
AC ELECTRICAL CHARACTERISTICS (Cont'd)

	Input Current		Output Current		Power Supply		
Parameter Test Conditions	I_{IL} (mA) Low Level V_{CC}=5.25V V_{IL}=0.4V	I_{IH} (μA) High Level V_{CC}=5.25V V_{IH}=2.4V	I_{OL} Low Level V_{CC}=5V V_{NT}=4V V_{IN}=2V	I_{OH} (μA) V_{CC}=5V V_{OUT}=V_{SS}−4V V_{IN}=0.85V	I_{CCL} Low Level V_{IN}=0V	I_{CCH} High Level	I_{OS}
	Min Typ Max	Min Typ Max	Min Typ Max	Min Typ Max	Min Typ Max	Min Typ Max	Min Typ Max
3207A[1] V_{SS}=16V, V_{BB}=19V	V_D=0.45V Others =5.25V Data −.25 Enable −.50	N/A	100	−100	See Data Sheet See Data Sheet		N/A
3207A−1[1] V_{SS}=19V, V_{BB}=23V	V_D=0.45V Others=5.25V Data −.25 Enable −.50	N/A	100	−100	See Data Sheet		N/A
75S207	V_{IL}=0.5V 16 or 26 Strobe −2 Common Strobe S −4	V_{IH}=2.7V 16 or 26 Strobe 50 Common Strobe S 100 V_{IH}=5.5V 16 or 26 Strobe 1mA Common Strobe S 2mA	N/A	N/A	See Data Sheet		−40 −100
75S208	V_{IL}=0.5V 16 or 26 Strobe −2 Common Strobe S −4	V_{IH}=2.7V 16 or 26 Strobe 50 Common Strobe S 100 V_{IH}=5.5V 16 or 26 Strobe 1mA Common Strobe S 2mA	N/A	N/A	See Data Sheet		−40 −100
7520[1]	−1.6	1mA	N/A	N/A	See Data Sheet		2.1 3.5
7521[1]	−1.6	1mA	N/A	N/A	See Data Sheet		2.1 3.5
7522[1]	−1.6	1mA	N/A	N/A	See Data Sheet		2.1 3.5
7523[1]	−1.6	1mA	N/A	N/A	See Data Sheet		2.1 3.5
7524[1]	−1.6	1mA	N/A	N/A	See Data Sheet		2.1 3.5
7525[1]	−1.6	1mA	N/A	N/A	See Data Sheet		2.1 3.5
75324	V_{IL}=0V Address −6 Timing −12	V_{IH}=5V Address 200 Timing 100			All sources/sinks off 12.5 15 Either sink selected 30 42 Either source selec'd 25 35		N/A

ANALOG INTERFACE-MEMORIES
AC ELECTRICAL CHARACTERISTICS

	Input Voltage									Output Voltage									Input Current		
Parameter	V_{IL} (V) Low Level			V_{IH} (V) High Level			V_{IC} (V) Clamp Voltage			V_{OL} (V) Low Level			V_{OH} (V) High Level			V_{OL} (V) Clamp Voltage			I_I (mA)		
Test Conditions	V_{CC}=4.75V V_{IN}=2V			V_{CC}=4.75V V_{IL}=0.8V			I_{IL}=−12mV			V_{CC}=4.75V V_{IN}=2V I_{OL}=16mA			V_{CC}=5V V_{IN}=0.85V I_{OH}=−400μA			V_{IN}=0V I_{OH}=20mA			V_{IN}=5.5V		
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max
75325[1]			0.8	2.0				I_{IL}=−10mA	−1.3	−1.7	N/A		19	V_{CC}=4.5V I_{OH}=0V 23			N/A			Address	1 Strobe 2
75361A			0.8	2.0						−1.5	I_{OL}=10mA 0.15	0.3	V_{CC2}	I_{OH}=−50μA V_{CC}			V_{CC}=+15V				A

INTERFACE

ANALOG INTERFACE-MEMORIES
AC ELECTRICAL CHARACTERISTICS (Cont'd)

	Input Current						Output Current						Power Supply								
Parameter Test Conditions	I_{IL} (mA) Low Level V_{CC}=5.25V V_{IL}=0.4V			I_{IH} (μA) High Level V_{CC}=5.25V V_{IH}=2.4V			I_{OL} Low Level V_{CC}=5V V_{NT}=4V V_{IN}=2V			I_{OH} (μA) V_{CC}=5V V_{OUT}=V_{SS}−4V V_{IN}=0.85V			I_{CCL} Low Level V_{IN}=0V			I_{CCH} High Level			I_{OS}		
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max
75325[1]	Address −1 Strobe −2	 −1.6 −3.2		Address	 3 Strobe 6	 40 80		N/A			N/A				See Data Sheet						N/A	
75361A	−1	−1.6			A	40		N/A			N/A		V_{CC1}=5.25V V_{CC2}=24V V_{IN}=5V I_{CC1} I_{CC2}	 16 7	 24 11	V_{CC1}=5.25V V_{CC2}=24V V_{IN}=0V I_{CC1} I_{CC2}	 2	 4 0.5		N/A	

NOTES:
1. For additional electrical specifications, see data sheet.

DESCRIPTION

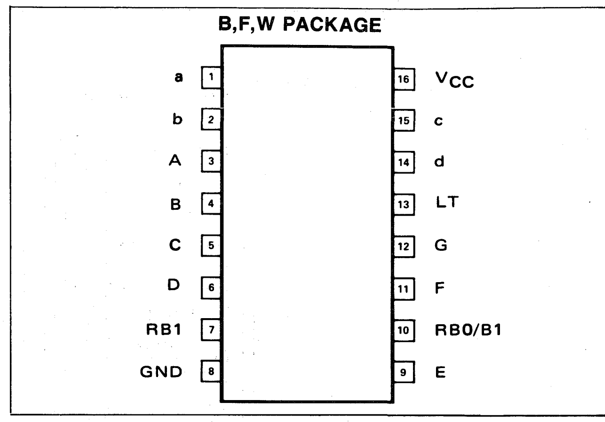
The 8T04 consists of the necessary logic to decode a 4-bit BCD code to seven segment (0 through 9) readout, as well as some selected signs and letters.

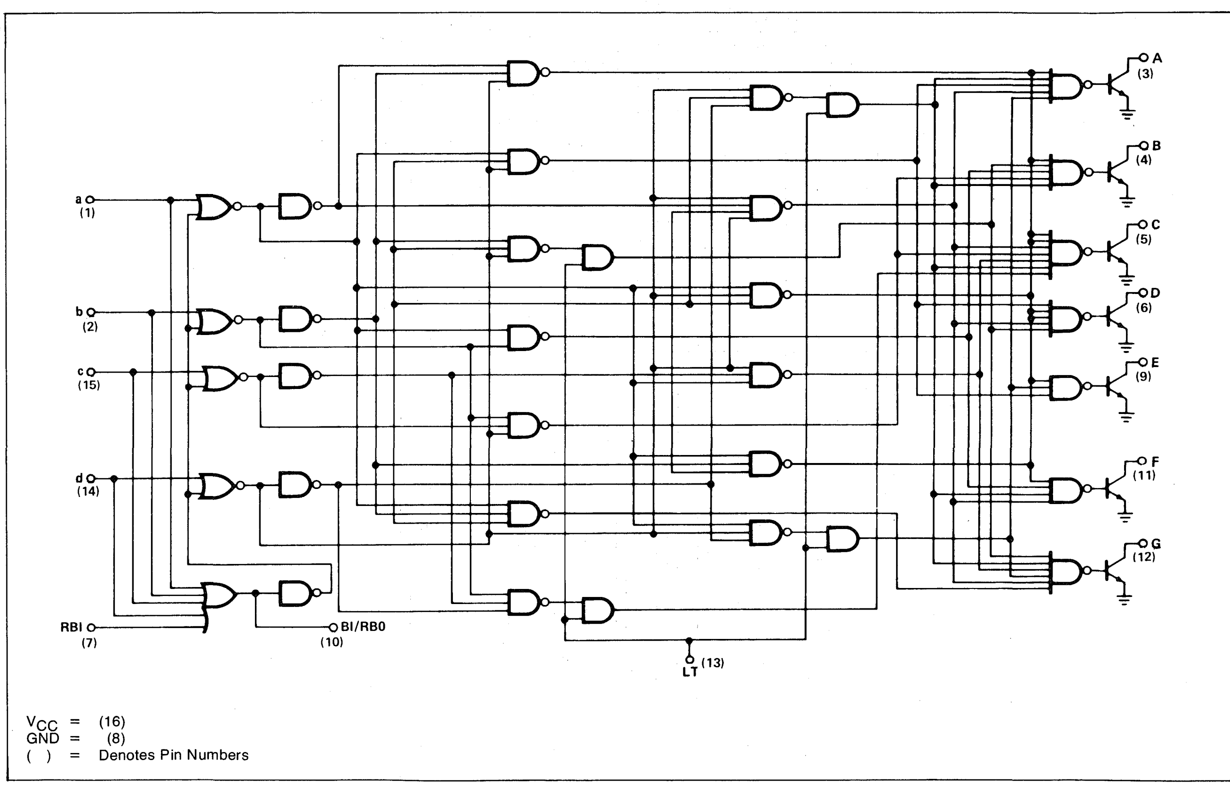
Incorporated in this device is a blanking circuit which turns all segments off when activated. The blanking circuit allows suppression of all numerically insignificant zeros, thereby presenting an easily read display.

Also included is the necessary circuitry to implement suppression of leading and/or trailing zeros. A Lamp Test control is provided to turn all segments on. The Lamp Test allows the viewer to check the validity of the display lamps.

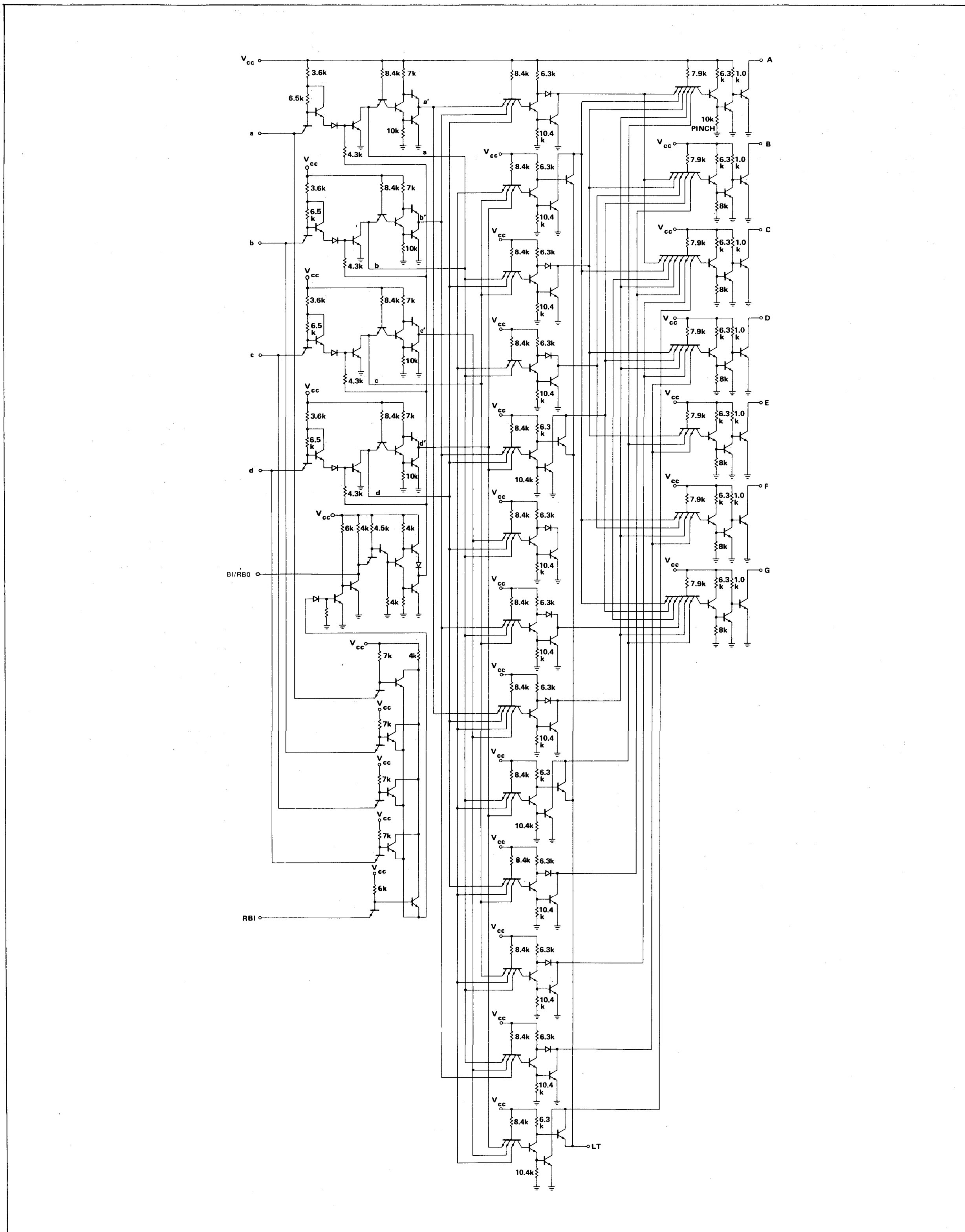
High performance bare collector output transistors are used in the 8T04 for directly driving incandescent lamps or common anode LED displays.

PIN CONFIGURATION





SCHEMATIC DIAGRAM



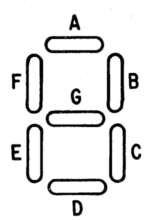
TRUTH TABLE

INPUTS						BI/RBO	OUTPUTS							DISPLAY CHARACTER
INPUT CODE				LAMP TEST	RBI		OUTPUT STATE							
d	c	b	a	LT		Note	A	B	C	D	E	F	G	
X	X	X	X	0	X	X	0	0	0	0	0	0	0	8
X	X	X	X	1	X	0 [1,2]	1	1	1	1	1	1	1	BLK
0	0	0	0	1	0	0 [2]	1	1	1	1	1	1	1	BLK
0	0	0	0	1	1	1 [2]	0	0	0	0	0	0	1	0
0	0	0	1	1	X	1	1	0	0	1	1	1	1	1
0	0	1	0	1	X	1	0	0	1	0	0	1	0	2
0	0	1	1	1	X	1	0	0	0	0	1	1	0	3
0	1	0	0	1	X	1	1	0	0	1	1	0	0	4
0	1	0	1	1	X	1	0	1	0	0	1	0	0	5
0	1	1	0	1	X	1	1	1	0	0	0	0	0	6
0	1	1	1	1	X	1	0	0	0	1	1	1	1	7
1	0	0	0	1	X	1	0	0	0	0	0	0	0	8
1	0	0	1	1	X	1	0	0	0	1	1	0	0	9
1	0	1	0	1	X	1	1	1	1	1	1	1	0	—
1	0	1	1	1	X	1	1	1	1	1	1	1	1	BLK
1	1	0	0	1	X	1	0	0	0	1	0	0	0	A
1	1	0	1	1	X	1	1	1	0	1	1	1	1	ı*
1	1	1	0	1	X	1	1	1	1	0	0	0	1	L
1	1	1	1	1	X	1	1	1	1	1	1	1	1	BLK

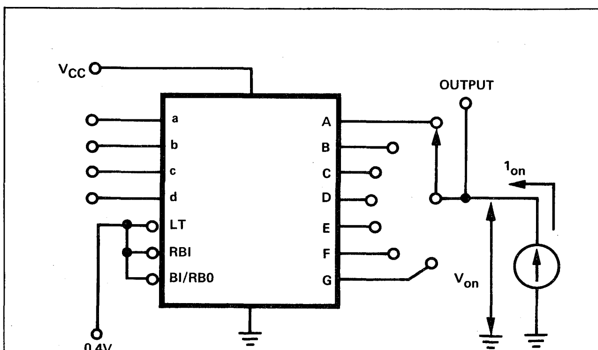
*COMMA

X = Don't care, either "1" or "0".
BI/RBO is an internally wired OR output.

NOTE:
1. BI/RBO used as input.
2. BI/RBO should not be forced high when a,b,c,d, RBI terminals are low, or damage may occur to the unit.



TEST FIGURE FOR "0" OUTPUT VOLTAGE



Each output is tested separately in the ON state.

8T05 B,F,W

DESCRIPTION

The 8T05 consists of the necessary logic to decode a 4-Bit BCD code to seven segment (0 through 9) readout as well as some selected signs and letters.

A Ripple Blanking input is provided to implement suppression of leading and/or trailing zeros. The suppression of all numerically insignificant zeros provides an easily read display.

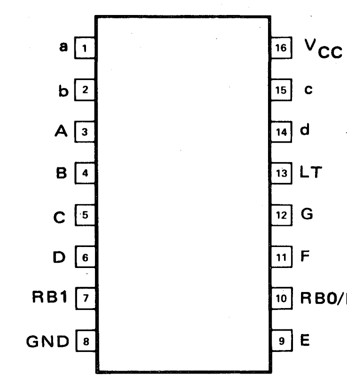
Incorporated in the Ripple Blanking output (BI/RBO) is the facility to ground all the outputs. Blanking of the outputs allows for intensity modulation.

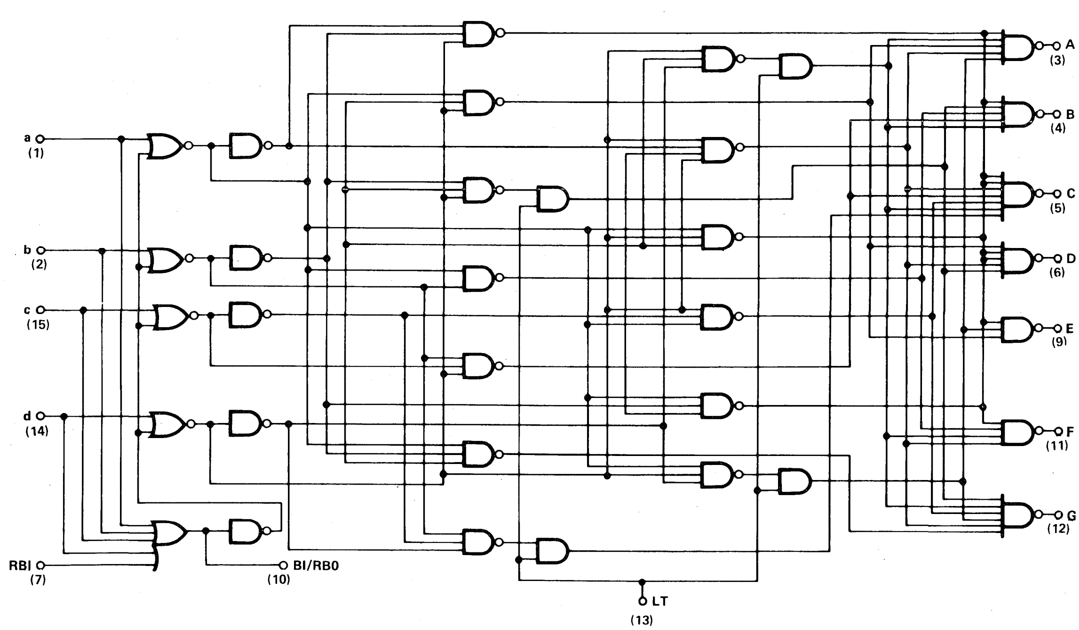
A Lamp Test input is provided which, when grounded forces all segment outputs high. This allows the viewer to check the validity of the display presentation by testing the integrity of the lamps.

The 8T05 has resistor pullups on the outputs to provide source current sufficient to drive interfacing elements. This allows the unit to drive high voltage transistors for neon displays. The 8T05 can also be used to drive common cathode LED displays without the need for external resistors.

PIN CONFIGURATION

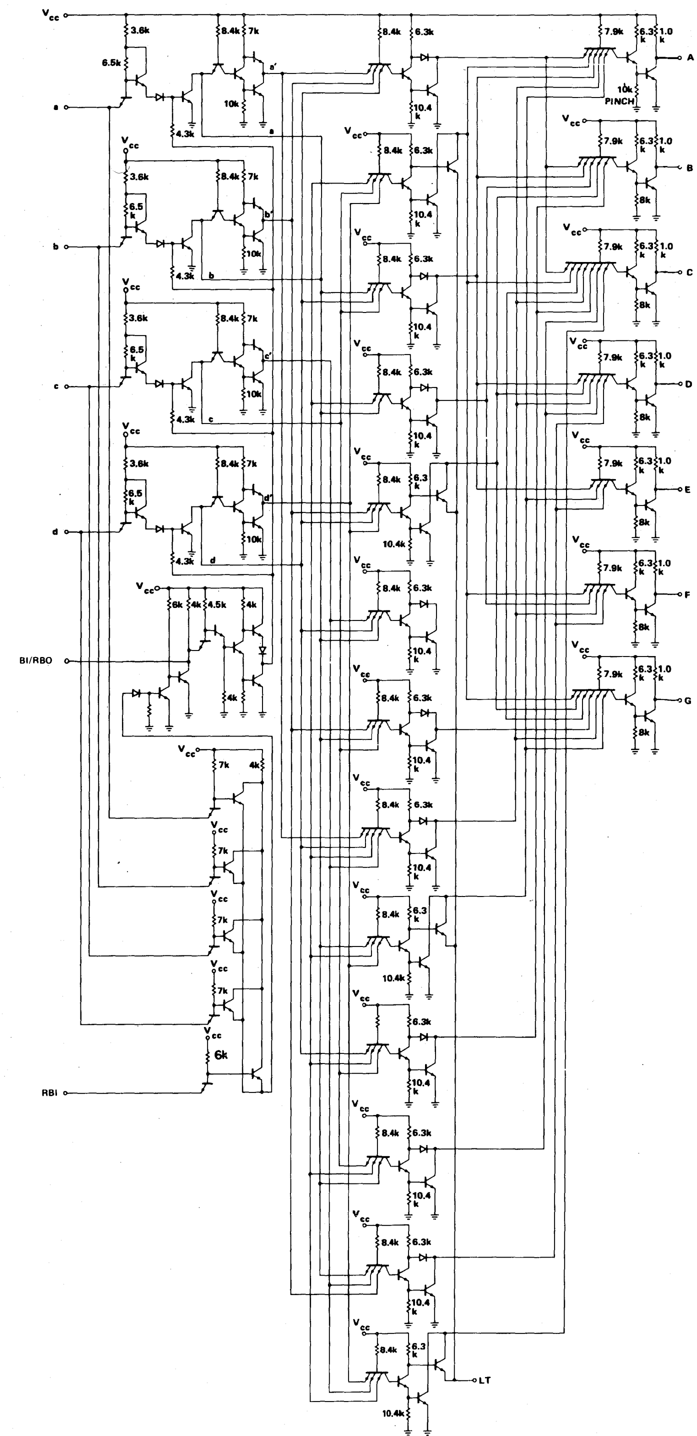
B,F,W PACKAGE





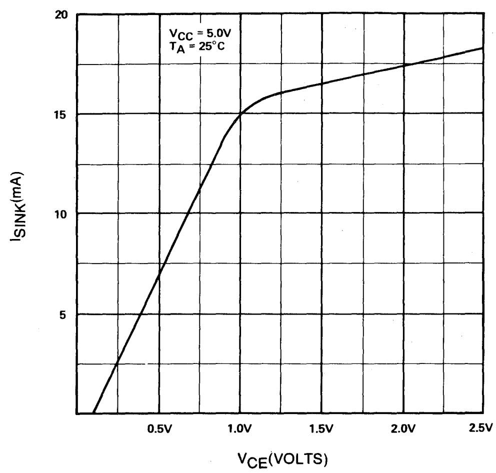
V_{CC} = (16)
GND = (8)
( ) = Denotes Pin Numbers

SCHEMATIC DIAGRAM

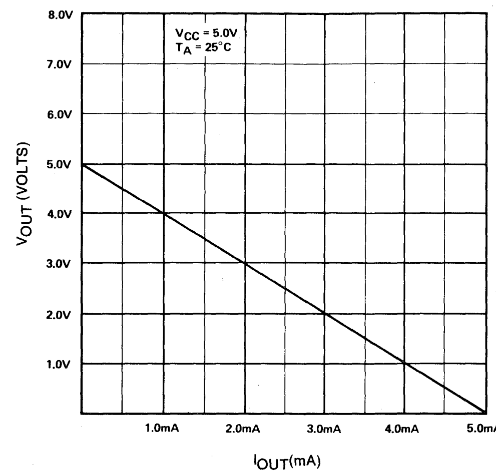


TYPICAL CHARACTERISTIC CURVES

TYPICAL CURRENT SINK CAPABILITY VERSUS VCE (SAT) (OUTPUTS A-G)



TYPICAL OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (OUTPUTS A-G)

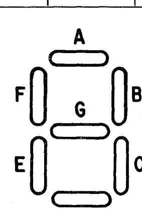


TRUTH TABLE

INPUTS						BI/RBO	OUTPUTS							DISPLAY CHARACTER
INPUT CODE				LAMP TEST	RBI		OUTPUT STATE							
d	c	b	a	LT		Note	A	B	C	D	E	F	G	
X	X	X	X	0	X	X	1	1	1	1	1	1	1	8
X	X	X	X	1	X	0	0	0	0	0	0	0	0	BLK
0	0	0	0	1	0	0 [1,2]	0	0	0	0	0	0	0	BLK
0	0	0	0	1	1	1 [2]	1	1	1	1	1	1	0	0
0	0	0	1	1	X	1	0	1	1	0	0	0	0	1
0	0	1	0	1	X	1	1	1	0	1	1	0	1	2
0	0	1	1	1	X	1	1	1	1	1	0	0	1	3
0	1	0	0	1	X	1	0	1	1	0	0	1	1	4
0	1	0	1	1	X	1	1	0	1	1	0	1	1	5
0	1	1	0	1	X	1	0	0	1	1	1	1	1	6
0	1	1	1	1	X	1	1	1	1	0	0	0	0	7
1	0	0	0	1	X	1	1	1	1	1	1	1	1	8
1	0	0	1	1	X	1	1	1	1	0	0	1	1	9
1	0	1	0	1	X	1	0	0	0	0	0	0	1	–
1	0	1	1	1	X	1	0	0	0	0	0	0	0	BLK
1	1	0	0	1	X	1	1	1	1	0	1	1	1	A
1	1	0	1	1	X	1	0	0	1	0	0	0	0	,*
1	1	1	0	1	X	1	0	0	0	1	1	1	0	L
1	1	1	1	1	X	1	0	0	0	0	0	0	0	BLK

* COMMA

X = Don't care, either "1" or "0".
BI/RBO is an internally wired OR output.



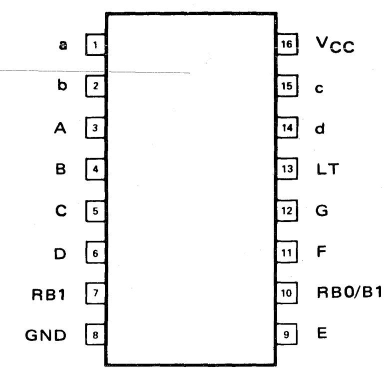
NOTE:
1. BI/RBO used as input.
2. BI/RBO should not be forced high when ab,c,d, RBI terminals are low, or damage may occur to the unit.

DESCRIPTION

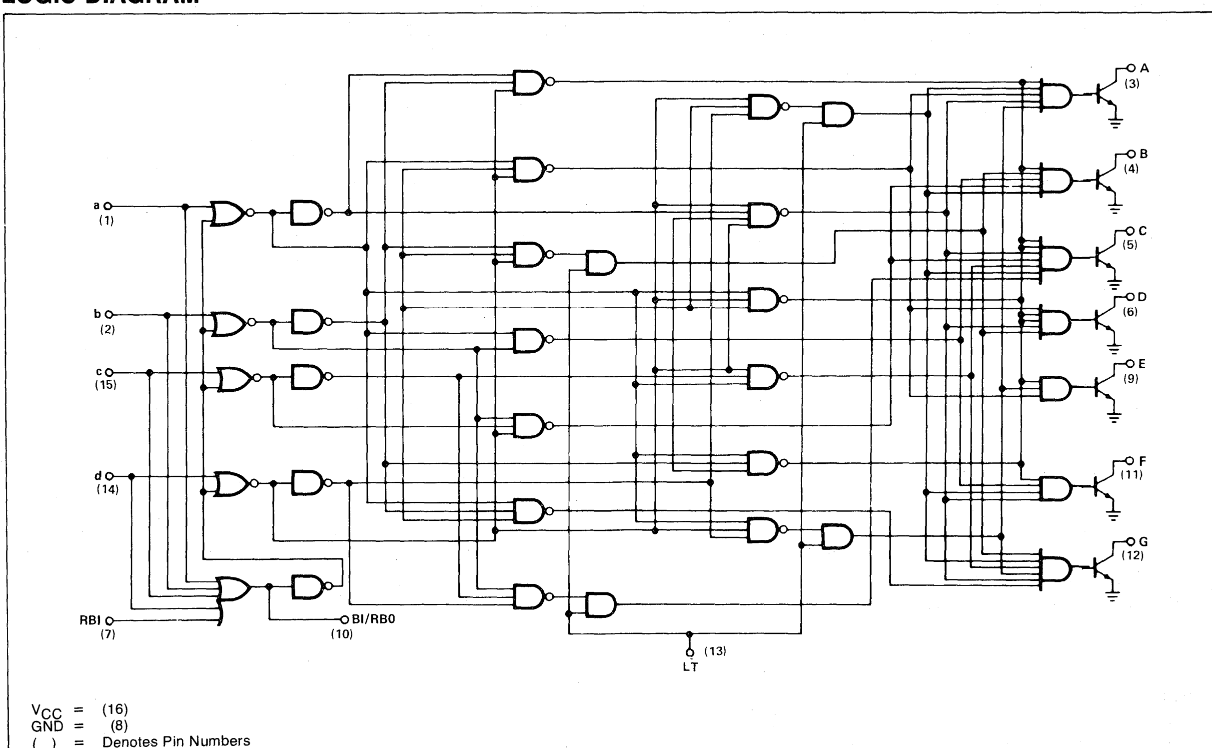
The 8T06 is a monolithic MSI circuit consisting of the necessary logic to decode a 4-bit BCD code to drive 7-segment indicators directly. Open-collector outputs are used for high current source applications, such as driving common cathode LED displays and discrete active components. The 8T06 seven segment decoder/driver accepts a 4-bit binary code and decodes all possible inputs as decimals 0-9 or selected signs and letters. Auxiliary inputs are provided for maximum versatility. The ripple blanking inputs (RBI) and the ripple blanking output (RBO) may be used for automatic leading and/or trailing-edge zero suppression. The RBO output also acts as an overriding blanking input (BI) which may be used for intensity modulation or strobing of the display. A lamp test (LT) input is provided to check the integrity of the display by activating all outputs independent of the input code.

PIN CONFIGURATION

B,F,W PACKAGE

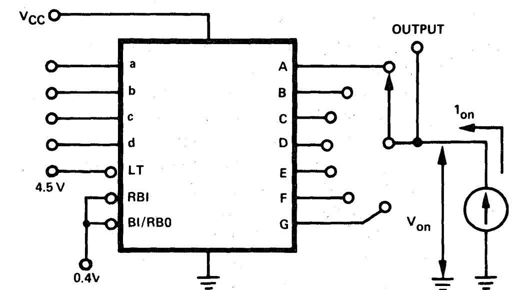


LOGIC DIAGRAM



8T06 B,F,W

TEST FIGURE FOR "0" OUTPUT VOLTAGE



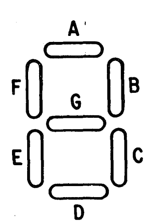
Each output is tested separately in the ON state.

TRUTH TABLE

INPUTS						OUTPUTS							
INPUT CODE				LAMP TEST	RBI	BI/RBO	OUTPUT STATE							DISPLAY CHARACTER
d	c	b	a	LT		Note	A	B	C	D	E	F	G	
X	X	X	X	0	X	X	1	1	1	1	1	1	1	8
X	X	X	X	1	X	0[1,2]	0	0	0	0	0	0	0	BLK
0	0	0	0	1	0	0[2]	0	0	0	0	0	0	0	BLK
0	0	0	0	1	1	1	1	1	1	1	1	1	0	0
0	0	0	1	1	X	1	0	1	1	0	0	0	0	1
0	0	1	0	1	X	1	1	1	0	1	1	0	1	2
0	0	1	1	1	X	1	1	1	1	1	0	0	1	3
0	1	0	0	1	X	1	0	1	1	0	0	1	1	4
0	1	0	1	1	X	1	1	0	1	1	0	1	1	5
0	1	1	0	1	X	1	0	0	1	1	1	1	1	6
0	1	1	1	1	X	1	1	1	1	0	0	0	0	7
1	0	0	0	1	X	1	1	1	1	1	1	1	1	8
1	0	0	1	1	X	1	1	1	1	0	0	1	1	9
1	0	1	0	1	X	1	0	0	0	0	0	0	1	—
1	0	1	1	1	X	1	0	0	0	0	0	0	0	BLK
1	1	0	0	1	X	1	1	1	1	0	1	1	1	A
1	1	0	1	1	X	1	0	0	1	0	0	0	0	,*
1	1	1	0	1	X	1	0	0	0	1	1	1	0	L
1	1	1	1	1	X	1	0	0	0	0	0	0	0	BLK

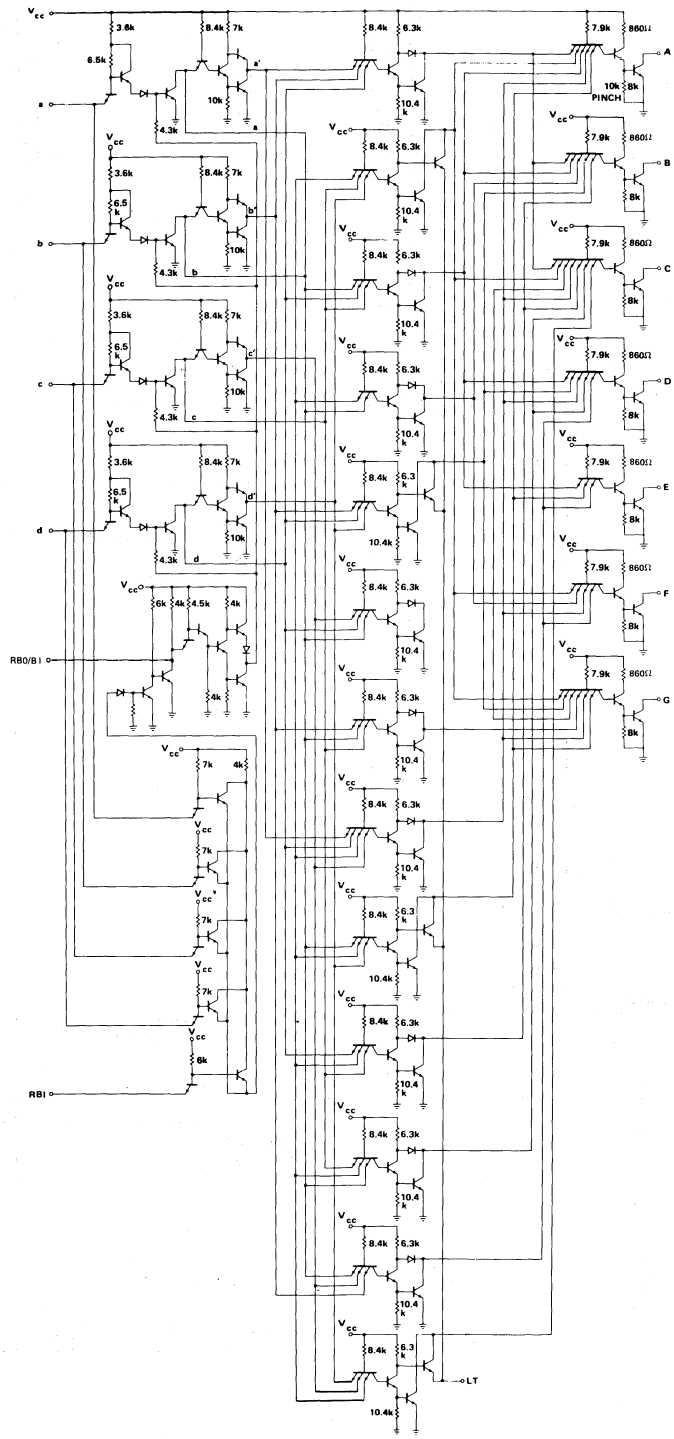
* COMMA

X = Don't care, either "1" or "0".
BI/RBO is an internally wired OR output.



NOTE:
1. BI/RBO used as input.
2. BI/RBO should not be forced high when ab,c,d, RBI terminals are low, or damage may occur to the unit.

SCHEMATIC DIAGRAM



TRI-STATE QUAD BUS DRIVER — 8T09

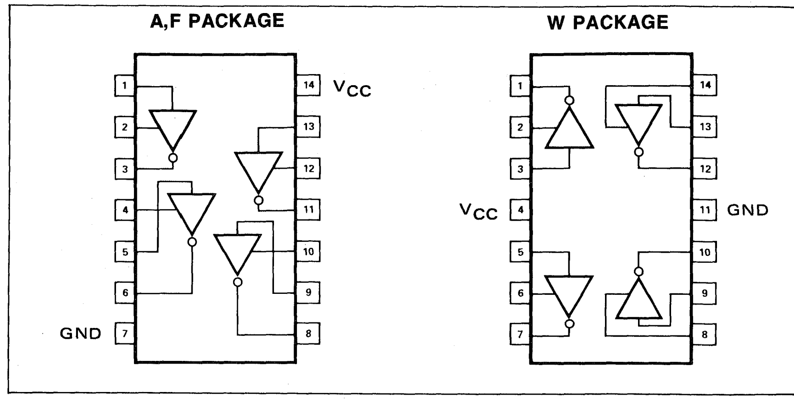
8T09 A,F,W

DESCRIPTION

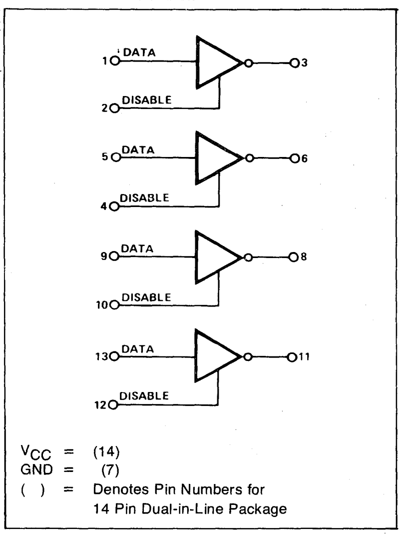
The 8T09 is a high speed quad bus driver device for applications requiring up to 25 loads interconnected on a single bus.

The tri-state outputs present a high impedance to the bus when disabled, (control input "1") and active drive when enabled (control input "0"). This eliminates the resistor pullup requirement while providing performance superior to open collector schemes. Each output can sink 40mA and drive 300pF loading with guaranteed propagation delay less than 20 nanoseconds.

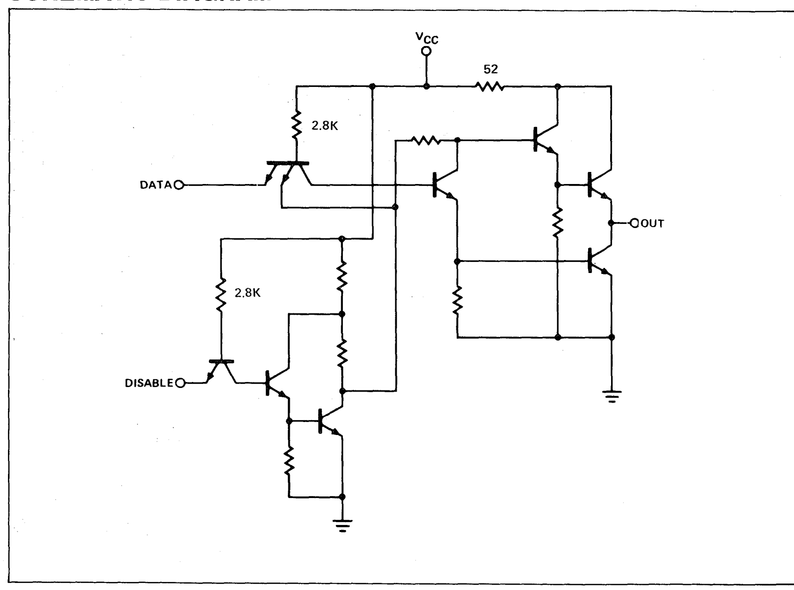
PIN CONFIGURATIONS



LOGIC DIAGRAM



SCHEMATIC DIAGRAM



TRUTH TABLE

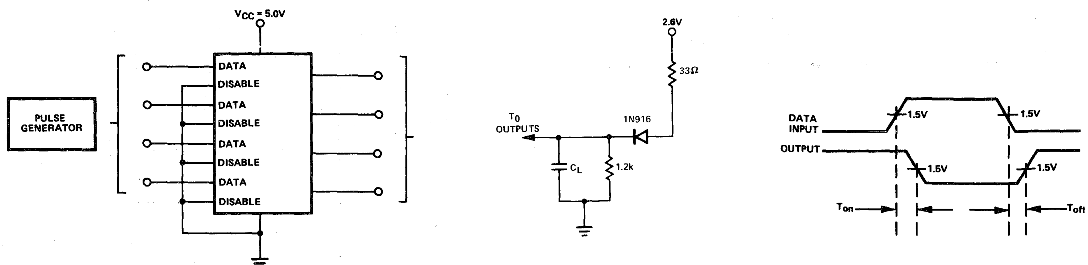
Data	Disable	Output
0	0	1
1	0	0
0	1	Hi-Z
1	1	Hi-Z

T_A = 25°C and V_{CC} = 5.0V

CHARACTERISTICS	LIMITS MAX	UNITS	TEST CONDITIONS OUTPUTS	TEST CONDITIONS NOTES
Propagation Delay				
Data to Output				
t_{on}, t_{off}	10	ns	30pF load	9
	20	ns	300pF load	9
Disable to Output				
High Z to 0, 0 to High Z	14	ns	30pF load	9
	22	ns	300pF load	9
High Z to 1, 1 to High Z	14	ns	30pF load	9
	22	ns	300pF load	9

AC TEST FIGURES AND WAVEFORMS

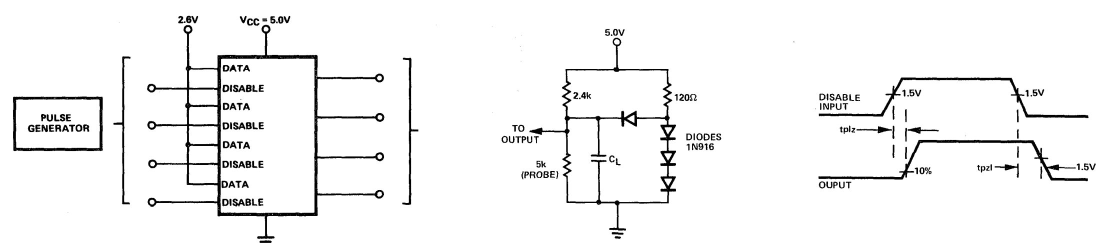
PROPAGATION DELAY (DATA TO OUTPUT)



INPUT PULSE:
$t_r = t_f =$ 5ns (10% TO 90%)
FREQ. = 1MHz (50% DUTY CYCLE)
AMP. = 2.6V

FIGURE 1

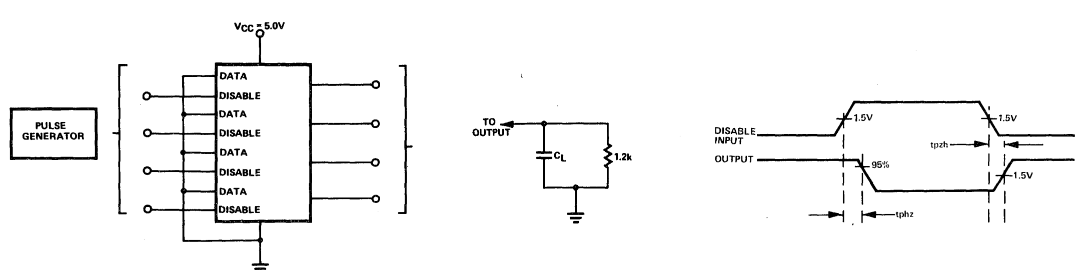
PROPAGATION DELAY
("0" TO HIGH Z, t_{pLZ}; HIGH Z TO 0, t_{pZL})



INPUT PULSE:
$t_r = t_f =$ 5ns (10% TO 90%)
FREQ. = 200kHz
AMP. = 2.6V

FIGURE 2

PROPAGATION DELAY
("1" TO HIGH Z, t_{pHZ}; HIGH Z to "1", t_{pZH})

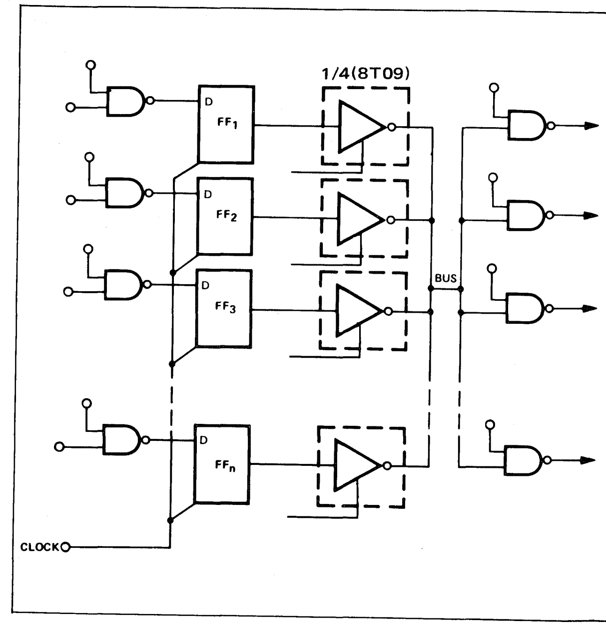


INPUT PULSE:
$t_r = t_f =$ 5ns (10% TO 90%)
FREQ. = 200kHz
AMP = 2.6V

FIGURE 3

The figure to right illustrates usage of the 8T09 in data processing logic. For example, FF_1 thru FF_n may represent bit X in each of several functions in a minicomputer (accumulators, MQ register, index registers, indirect address registers, etc.). Transfer from any source to any load, including transfers from one register to another, can take place along the single path labeled "BUS".

TYPICAL APPLICATION



8T10 B,F,W

DESCRIPTION

The 8T10 is a high speed Quad D flip-flop with tri-state outputs for use in bus-organized systems. The high current sink capability permits up to 20 standard loads to be interconnected on a single bus. The outputs present a high impedance to the bus when disabled (Control Input "1") and active drive when enabled (Control Inputs "0").

All four D-type flip-flops operate from a common clock with data being transferred on the low-to-high transition of the pulse.

A common clear input resets all flip-flops upon application of a logic "1" level.

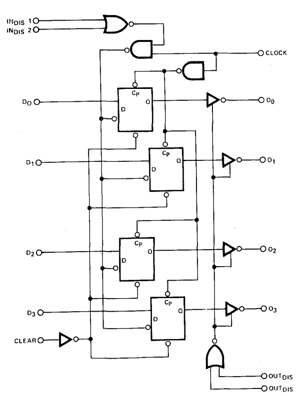
Data will be stored if either one or both inputs to the Input Disable NOR gate is a logic "1".

TRUTH TABLE

D_n	IN_{DIS}	OUT_{DIS}	O_{n+1}
0	0	0	0
1	0	0	1
X	1	0	O_n
X	X	1	High Z

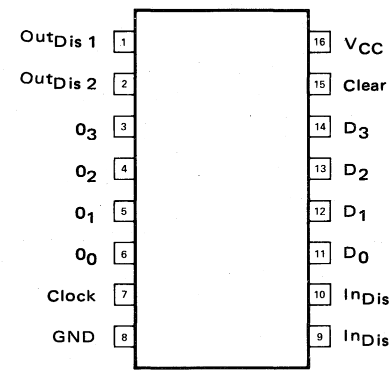
O_n refers to the output state before a clock pulse.
$O_n + 1$ refers to the output state after a clock pulse.

LOGIC DIAGRAM



PIN CONFIGURATION

B,F,W PACKAGE



$T_A = 25°$ C and $V_{CC} = 5.0V$

PARAMETER	LIMITS MIN.	TYP.	MAX.	UNITS
Propagation Delay (t_{on}, t_{off})				
Clock to Output				
C_L = 30pf		18	25	ns
C_L = 300pf		24	35	ns
Disable to Output				
High Z to Logic 0, t_{pZL} State (C_L = 300pf)		20	30	ns
Logic 0 to High Z, t_{pLZ} High Z (C_L = 300pf)		20	30	ns
Clear to Output				
C_L = 30pf		15	22	ns
C_L = 300pf		21	30	ns
Set Up Time, t_{setup}				
Data	+5	−1		ns
Input Disable		−6	0	ns
Hold Time, t_{hold}				
Data		−1	+5	ns
Reset Pulse Width	15			ns
Clock Frequency	35	50		MH_z
Clock Pulse Width				
Positive		8	12	ns
Negative		8	12	ns

1. Measured to 1.5V level of output waveform.
2. Measured to 10% level of output waveform.
3. Refer to AC Test Circuits.

AC TEST CIRCUITS AND WAVEFORMS

PROPAGATION DELAY t_{on}, t_{off} (CLOCK TO OUTPUT)

DATA SETUP TIME, t_{setup}

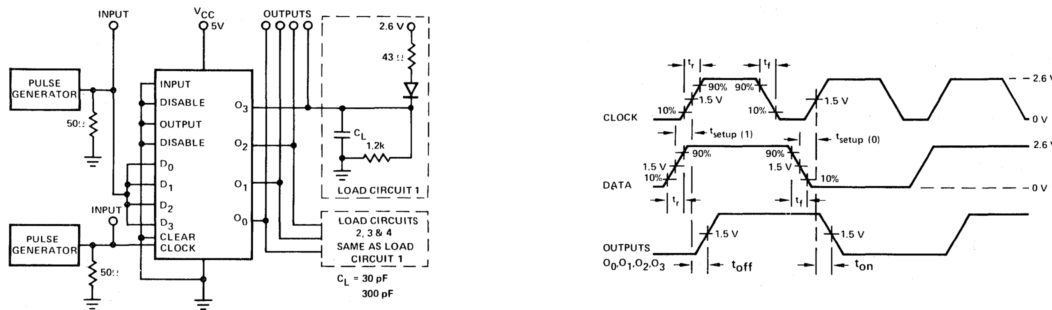


FIGURE 1

PROPAGATION DELAY (CLEAR TO OUTPUT)

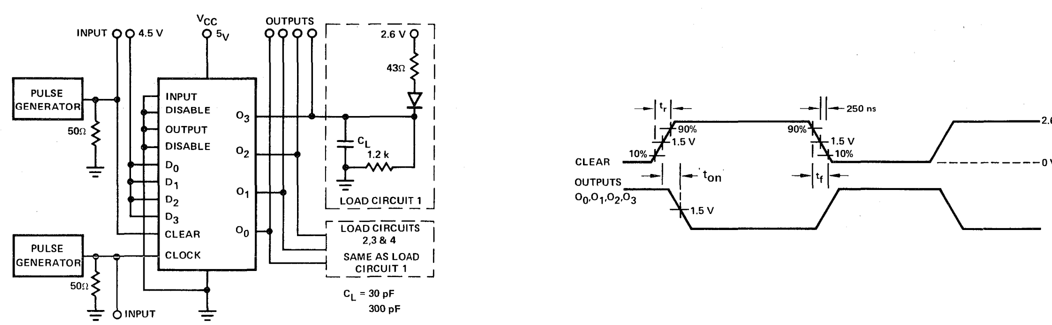


FIGURE 2

PROPAGATION DELAY (DATA HOLD TIME)

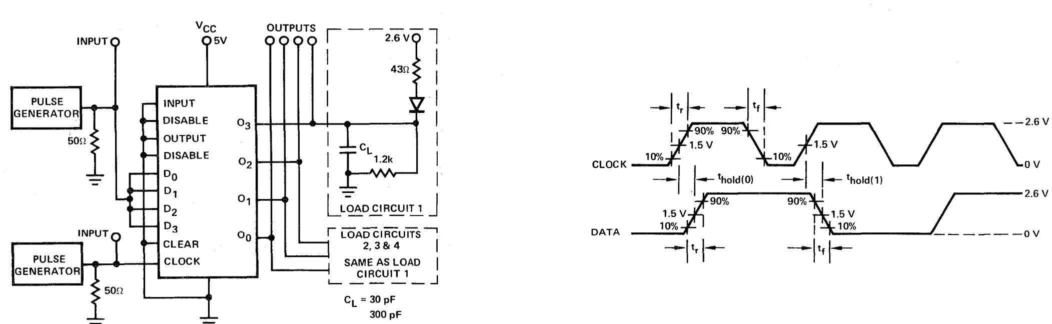


FIGURE 3

AC TEST FIGURES AND WAVEFORMS (Cont'd)

PROPAGATION DELAY (DISABLE TO OUTPUT)

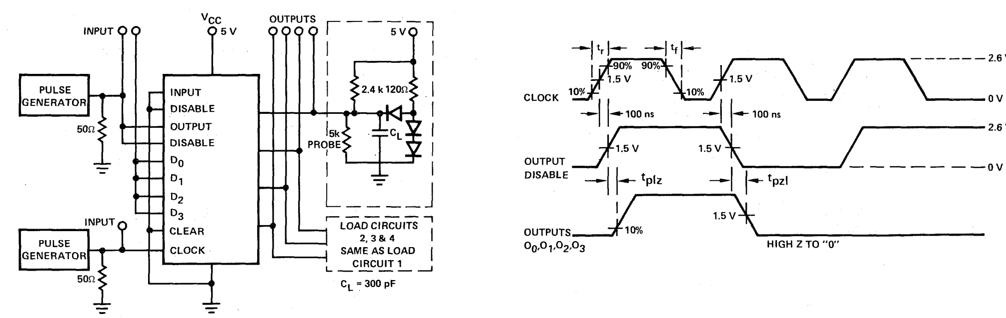
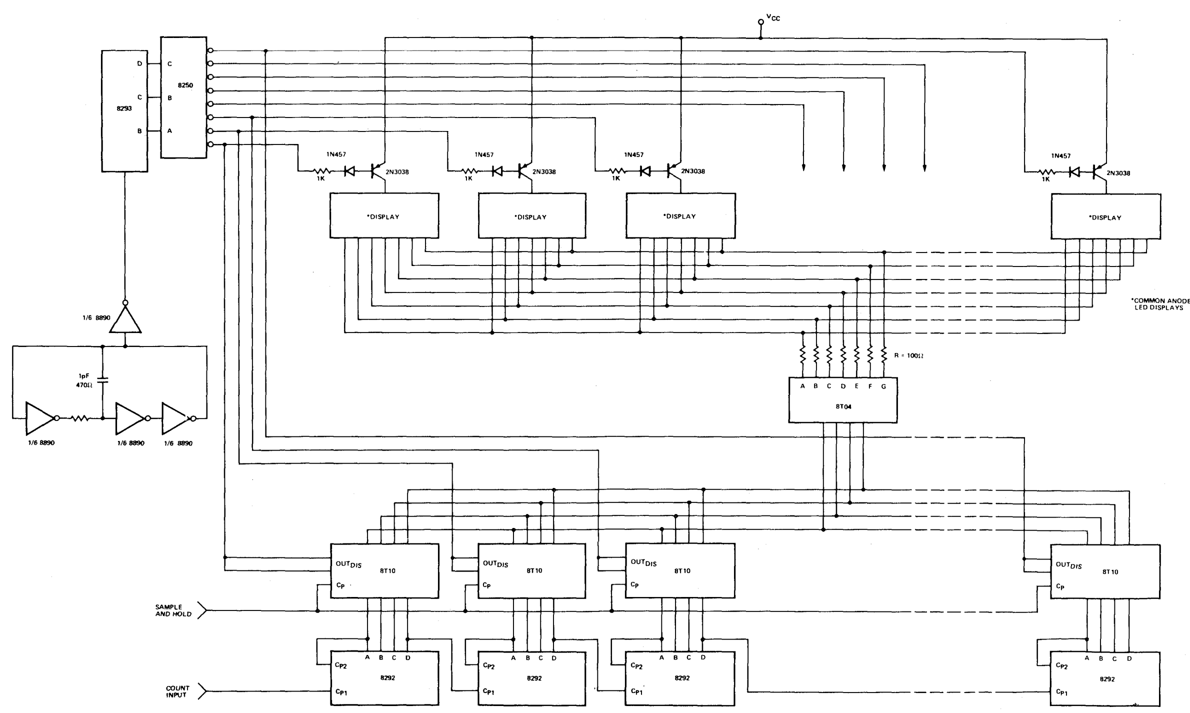


FIGURE 4

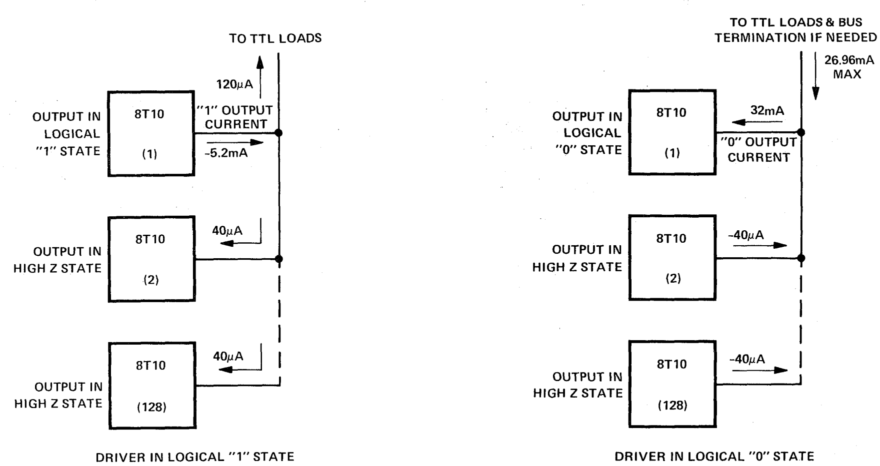
TYPICAL APPLICATIONS

MULTIPLEXING EIGHT LED DISPLAYS



8T10 B,F,W

TYPICAL APPLICATIONS



8T13 B,F,W

DESCRIPTION

The 8T13 is a monolithic Dual Line Driver designed to drive 50 ohm or 75 ohm coaxial transmission lines. TTL multiple emitter inputs allow this line driver to interface with standard TTL or DTL systems. The outputs are designed to drive long lengths of coaxial cable, strip line, or twisted pair transmission lines with impedances of 50Ω to 500Ω.

KEY DESIGN BENEFITS

- High-Power Drive Capability:
  Specified at −75mA source current rating at 2.4 volts.
- Party-Line Operation:
  Emitter-follower outputs enable two or more drivers to drive the same line. This permits multiple time-shared terminal connections since these drivers have no effect upon the transmission line unless activated.
- Input gating structure allows employment of the "OR" as well as the "AND" function.
- High Speed: $t_{on} = t_{off}$ = 20ns (max).
- Input Clamp Diodes: Protects inputs from line ringing.
- Single 5 Volt power supply.
- Short Circuit Protection:
  Incorporates a latch-back short circuit protection feature which protects the device by limiting the current it may source when operating under conditions of zero load resistance.

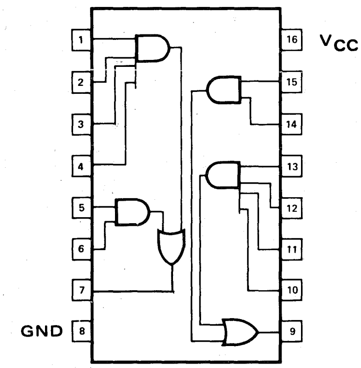
T_A = 25° C and V_{CC} = 5.0V

PARAMETER	LIMITS			UNIT
	MIN	TYP	MAX	
t_{on}, Turn-On Delay			20	ns
		32		ns
t_{off}, Turn-Off Delay			20	ns
		22		ns

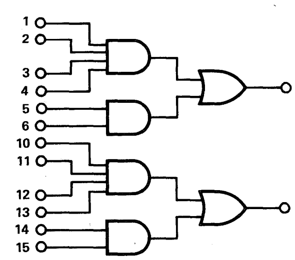
NOTES:
1. R_L = 37Ω to ground.
2. Load is 37Ω in parallel with 1000pF.
3. Reference AC Test Circuit and Pulse Requirements.

PIN CONFIGURATION

B,F,W PACKAGE

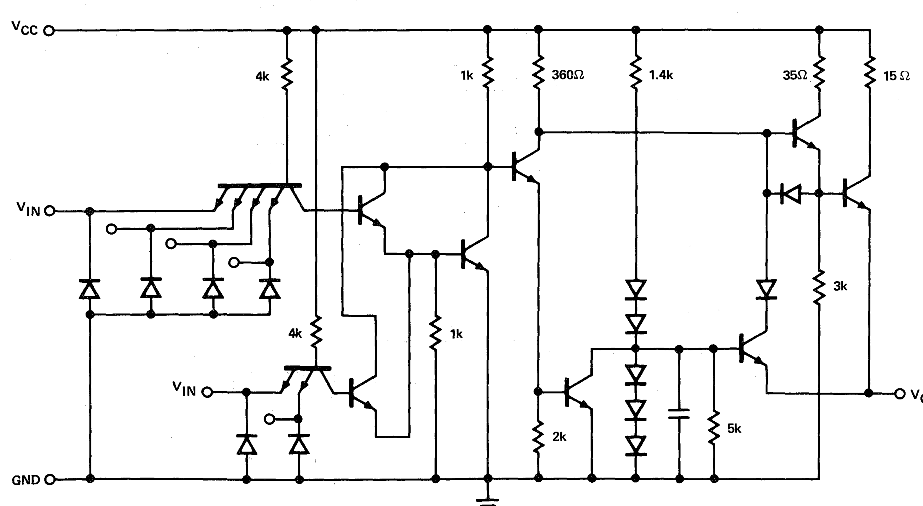


LOGIC DIAGRAM



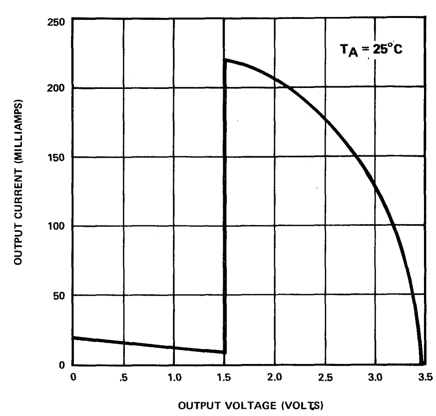
V_{CC} = (16)
GND = (8)
( ) = Denotes Pin Numbers

SCHEMATIC DIAGRAM

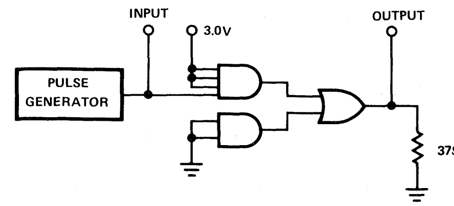


8T13 B,F,W

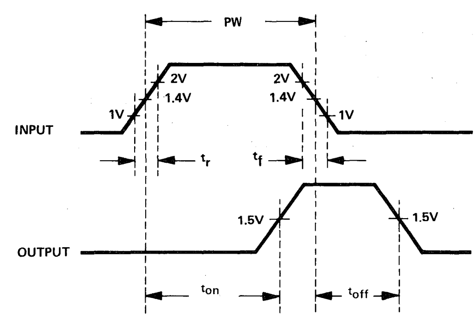
TYPICAL OUTPUT CURRENT VERSUS Ω OUTPUT VOLTAGE CURVE



AC TEST FIGURE AND WAVEFORMS



PULSE REQUIREMENTS



INPUT PULSE:
Amplitude = 3.0V
PW = 40ns (50% Duty Cycle)
$t_r = t_f \leq 5ns$ (10% and 90% measurement points)

TYPICAL APPLICATIONS

A typical application for the 8T13 is shown in Figure 1. If only one line driver is to be used for each transmission line, the line may be terminated with 50 ohms on the receiving end only. See Figure 2.

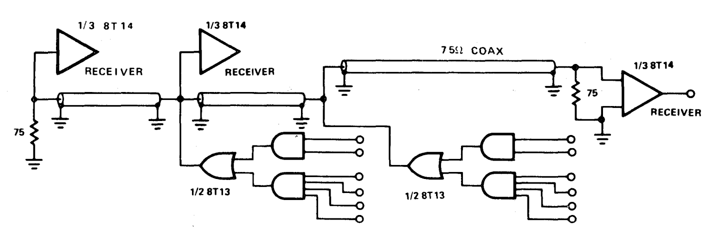


FIGURE 1

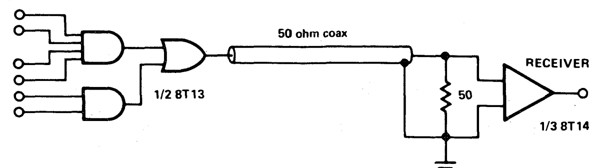


FIGURE 2

DESCRIPTION

The 8T14 is a Triple Line Receiver designed for applications requiring digital information to be transmitted over long lengths of coaxial cable, strip line, or twisted pair transmission lines. The Receiver's high impedance input structure (≈30kΩ) presents a minimal load to the driver circuit and allows the transmission line to be terminated in its characteristic impedance to minimize line reflections.

The built-in hysteresis characteristic of the 8T14 also makes it ideal for such applications as Schmitt triggers, one-shots and oscillators.

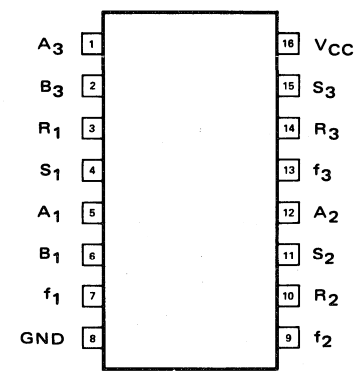
FEATURES

- BUILT-IN INPUT THRESHOLD HYSTERESIS*
- HIGH SPEED: $t_{on} = t_{off} =$ 20ns (Typical)
- EACH CHANNEL CAN BE STROBED INDEPENDENTLY
- FANOUT OF TEN (10) WITH STANDARD TTL INTEGRATED CIRCUITS
- INPUT GATING IS INCLUDED WITH EACH LINE RECEIVER FOR INCREASED APPLICATION FLEXIBILITY
- OPERATION FROM A SINGLE +5 VOLT LOGIC SUPPLY

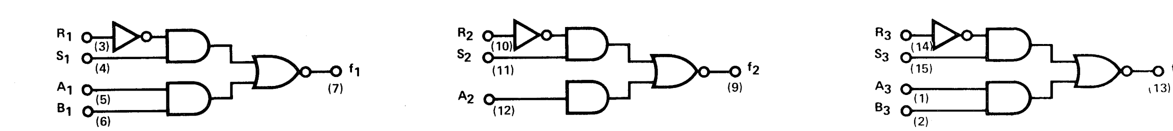
* Hysteresis is defined as the difference between the input thresholds for the "1" and "0" output states. Hysteresis is specified at 0.5 volts typically and 0.3 volts minimum over the operating temperature range.

PIN CONFIGURATION

B,F,W PACKAGES

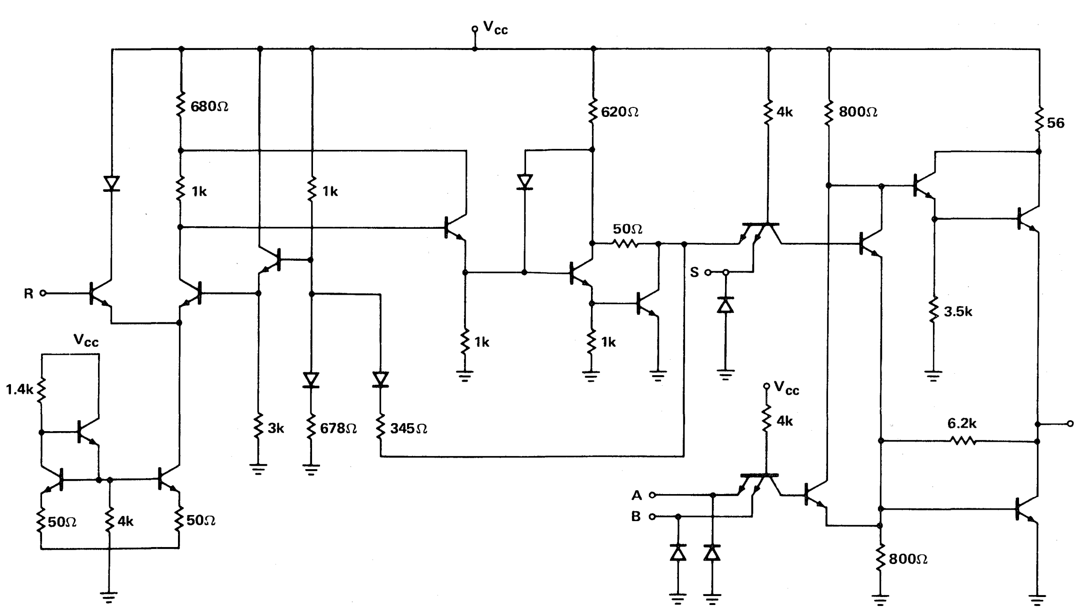


LOGIC DIAGRAMS



VCC = (16)
GND = (8)
( ) = Denotes Pin Numbers

SCHEMATIC DIAGRAM



8T14 B,F,W

$T_A = 25°$ C and $V_{CC} = 5.0V$

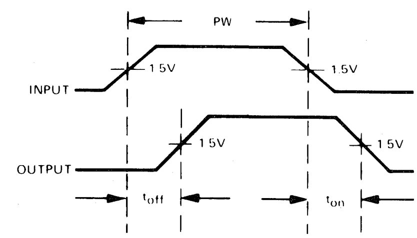
CHARACTERISTICS	LIMITS			UNITS
	MIN.	TYP.	MAX.	
t_{on}, Turn-On Delay		20	30	ns
t_{off}, Turn-Off Delay		20	30	ns

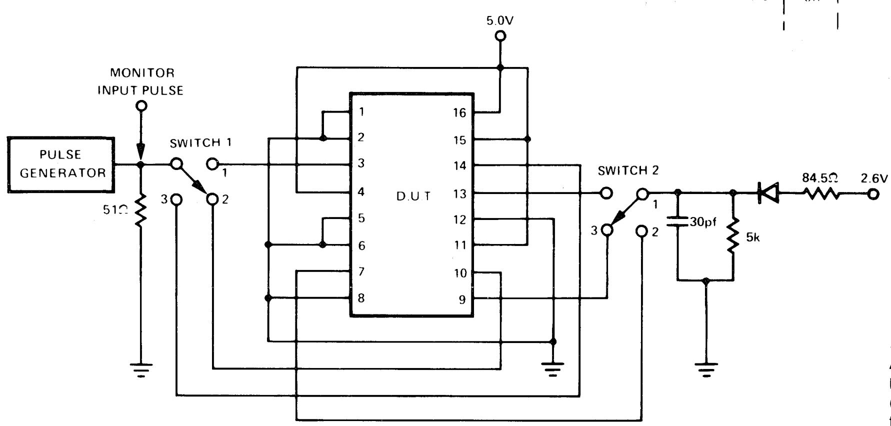
AC TEST CIRCUIT AND WAVEFORMS

3 Receivers in the package.
Test each Receiver using switch positions as shown in Table 1.

TABLE I

Receiver no.	Position	
	Switch 1	Switch 2
Receiver 1	1	1
Receiver 2	2	2
Receiver 3	3	3





Input Pulse:
Amplitude = 2.6V
Pulse width = 200nS
(50% Duty Cycle)
tr = tf = 5nS (10% to 90%)

HYSTERESIS TEST CIRCUIT

FIGURE 1

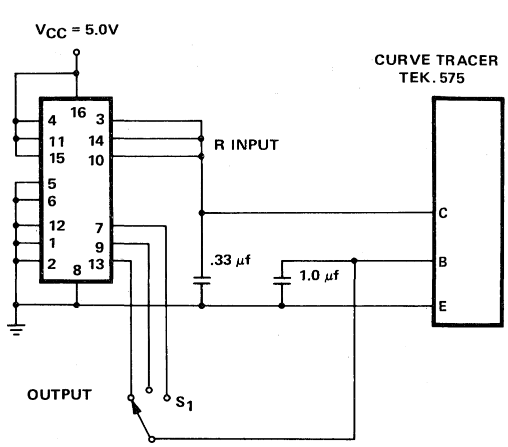
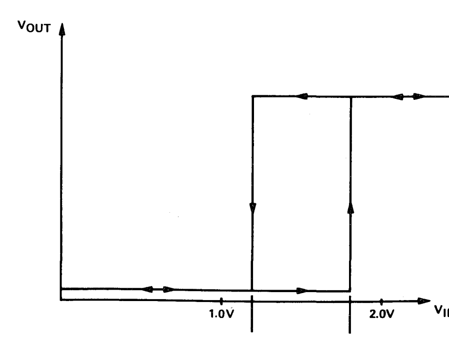


FIGURE 2

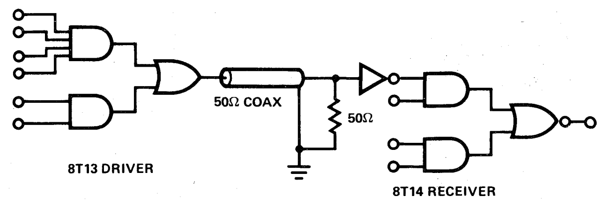


Verify in each of three (3) positions of S_1 (Figure 1) that the following occurs per Figure 2.

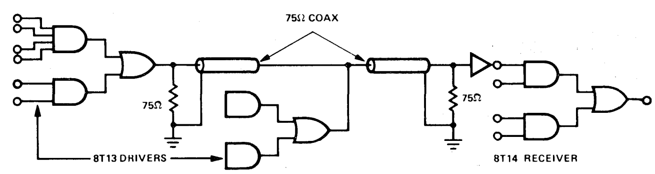
1. V_1 and V_2 must be between 0.8V minimum and 2.0V max.
2. Hysteresis = $V_1 - V_2 \geq 0.3V$.

TYPICAL APPLICATIONS

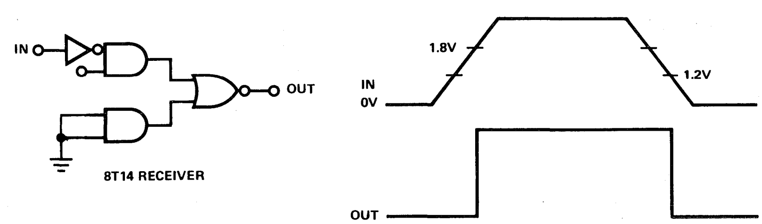
COAXIAL TRANSMISSION SYSTEM



PARTY-LINE APPLICATION



SCHMITT TRIGGER APPLICATION



INTERFACE

8T15 A,F

DESCRIPTION

The 8T15 Dual Communications Line Driver provides line driving capability for data transmission between Data Communication and Terminal Equipment. The device meets or exceeds the requirements of EIA Standard RS-232B and C, MIL STD-188B and CCITT V 24.

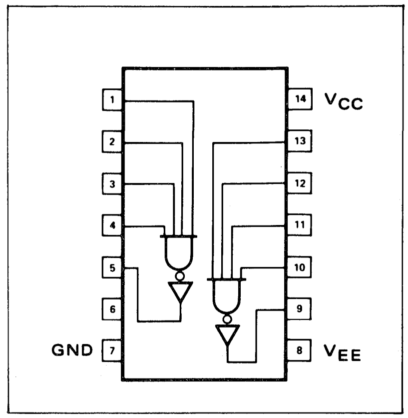
This dual 4-input NAND driver will accept standard TTL logic level inputs and will drive interface lines with nominal data levels of +6V and −6V. Output slew rate may be adjusted by attaching an external capacitor from the output terminal to ground. The outputs are protected against damage caused by accidental shorting to as high as ±25V.

ABSOLUTE MAXIMUM RATINGS*

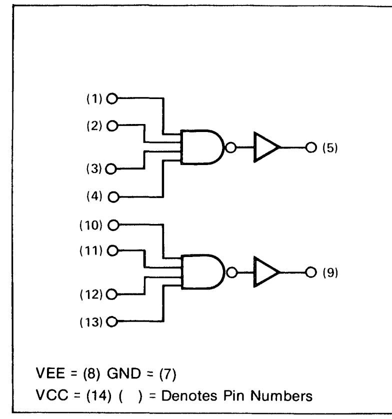
Input Voltage	+5.5V
Output Voltage	±25V
V_{CC}	+15V
V_{EE}	−15V
Storage Temperature	−65°C to +150°C
Operating Temperature	0°C to +75°C

* Limiting values above which serviceability may be impaired.

PIN CONFIGURATION



LOGIC DIAGRAM

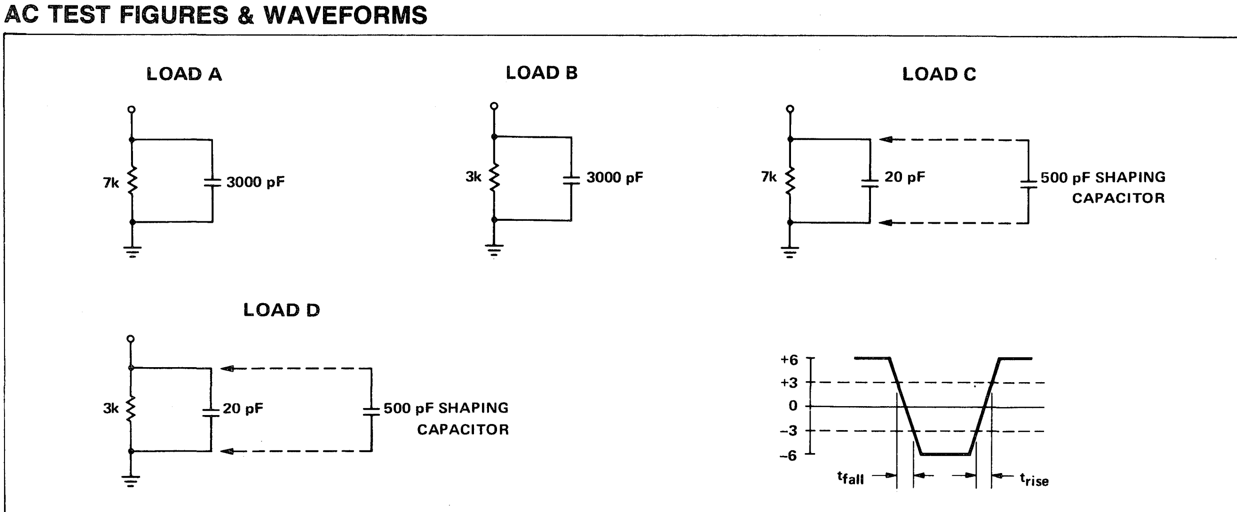


$T_A = 25°C, V_{CC} = +12.0V, V_{EE} = -12.0V$

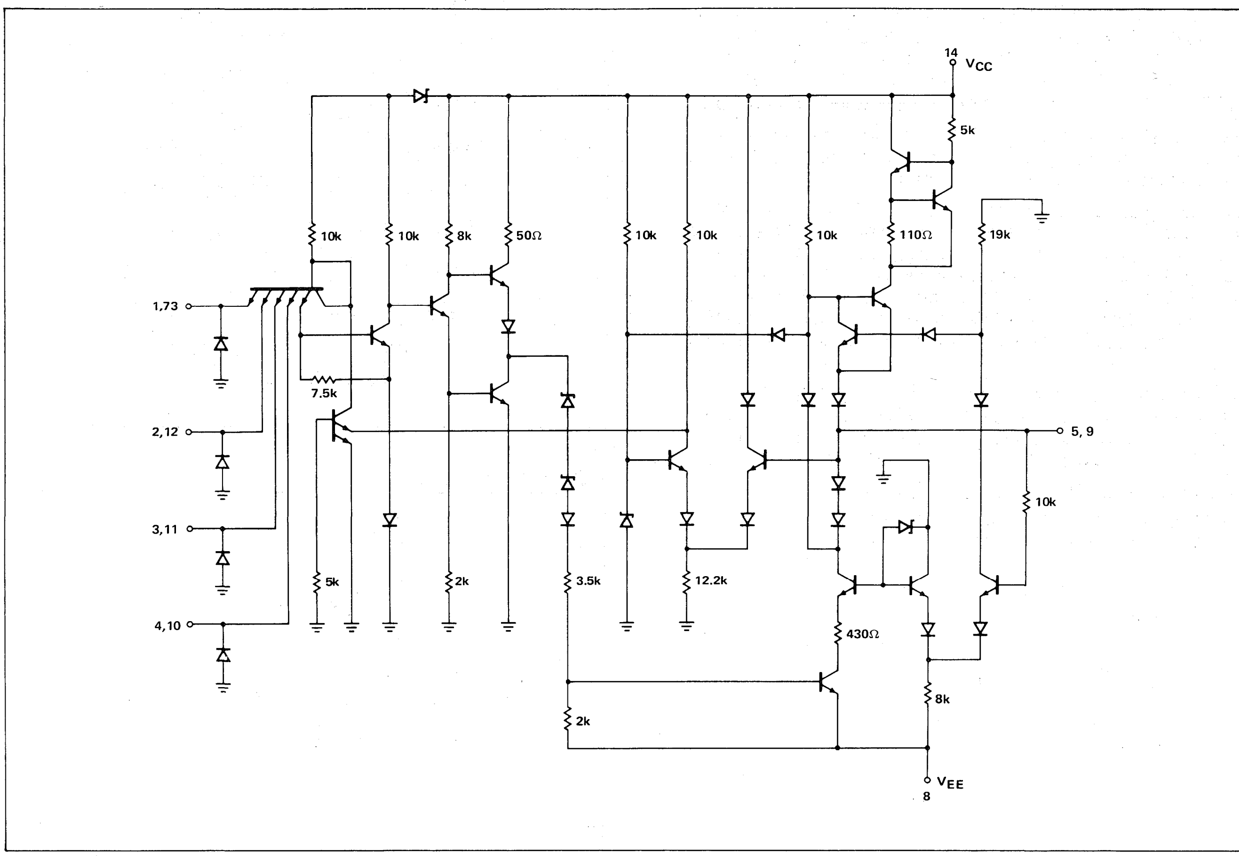
CHARACTERISTICS	TEST CONDITIONS: INPUTS: DRIVEN	INPUTS: OTHER	OUTPUTS	UNIT	LIMITS: MIN	TYP	MAX
Output Rise Time[1]			Load A	µs			4
Output Fall Time[1]			Load B	µs			4
Output Rise Time[1]			Load C	ns	200		
Output Fall Time[1]			Load D	ns	200		
Current from Positive Supply[2]				mA			16
Current from Negative Supply[2]				mA			28
Output Impedance							
(Power on)	0.0V		−3.5± 1mA	ohms		95	
(Power on)	2.0V		+3.5± 1mA	ohms		95	
(Power off)			±2V	ohms	300	2.5M	

[1] Rise and fall times are measured between the +3V and −3V points on the output waveform.
[2] $V_{CC} = +12.6V$, $V_{EE} = -12.6V$

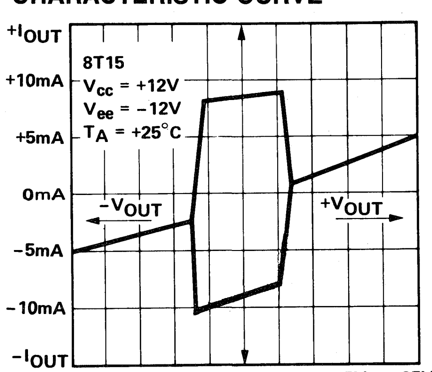
AC TEST FIGURES & WAVEFORMS



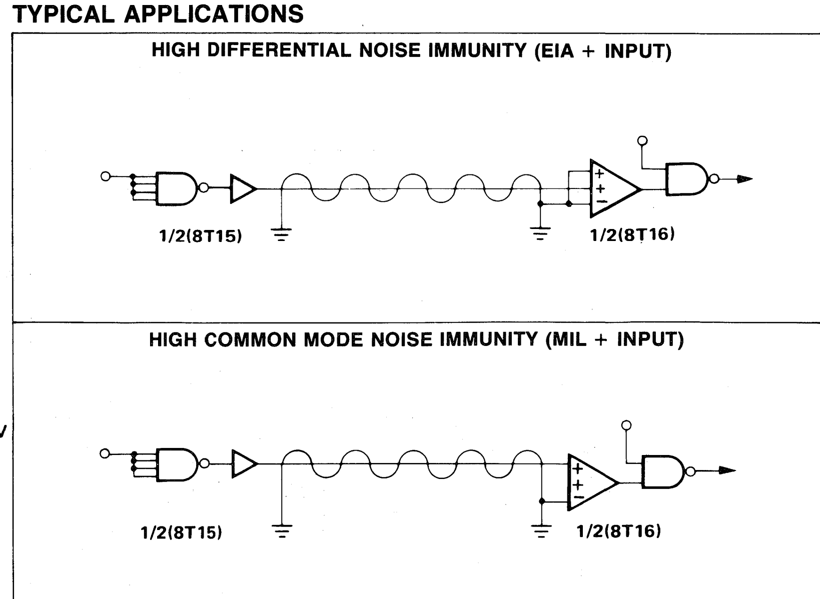
SCHEMATIC DIAGRAM



TYPICAL OUTPUT CHARACTERISTIC CURVE



TYPICAL APPLICATIONS



8T16 A,F

DESCRIPTION

The 8T16 Dual Communications Line Receiver provides receiving capability for data lines between Data Communication and Terminal Equipment. The device meets or exceeds the requirements of EIA Standard RS-232B and C, MIL-STD-188B and CCITT V24 and operates from a single 5 volt power supply.

The receivers accept single (EIA) or double ended (MIL) inputs and are provided with an output strobing control. Both EIA and MIL input standards are accommodated.

When using the EIA input terminal (with the Hysteresis terminal open), input voltage threshold levels are typically +2V and −2V with a guaranteed minimum Hysteresis of 2.4V. By grounding the "Hysteresis" terminal, the EIA input voltage threshold levels may be shifted to typically +1.0V and +2.1V with a minimum guaranteed Hysteresis of 0.75V. (Note that when using the EIA inputs, the MIL inputs — both positive and negative — must be grounded).

The MIL input voltage threshold levels are typically +0.6V and −0.6V with a minimum guaranteed Hysteresis of 0.7V. A MIL negative terminal is provided on each receiver per specification MIL-STD-188B to provide for common mode noise rejection.

Each receiver includes a strobe input so that:

a. A "1" on the strobe input allows data transfer.
b. A "0" on the strobe input holds the output high.

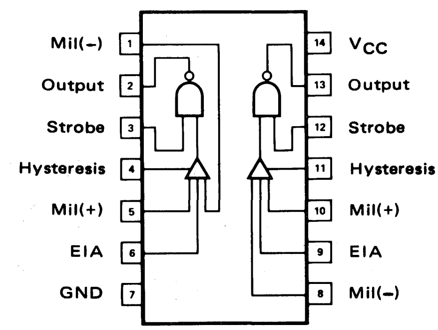
ABSOLUTE MAXIMUM RATINGS*

Input Voltage (EIA and MIL)	±25V
V_{CC}	+7.0V
Storage Temperature	−65°C to +175° C
Operating Temperature	0° C to +75° C

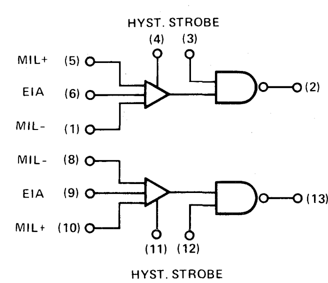
* Limiting values above which serviceability may be impaired.

PIN CONFIGURATION

A,F PACKAGE

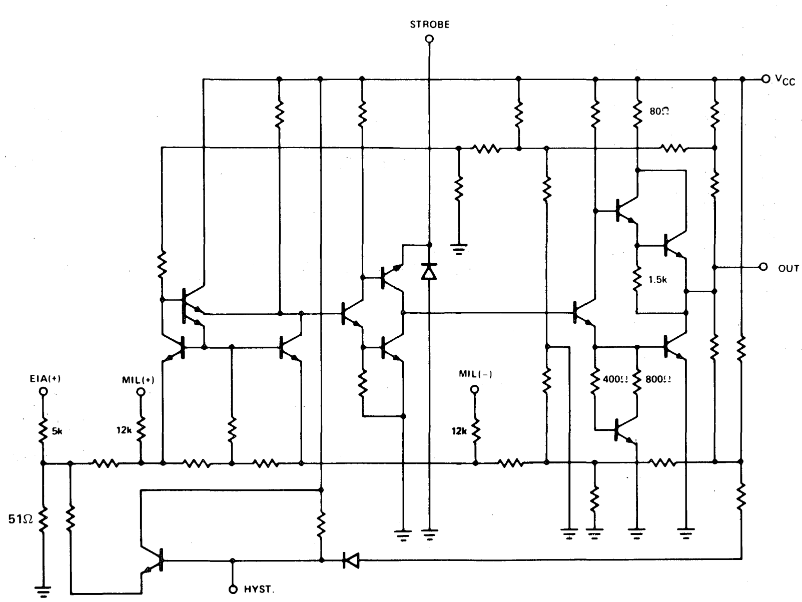


LOGIC DIAGRAM



V_{CC} = (14)
GND = (7)
( ) = Denotes Pin Numbers

SCHEMATIC DIAGRAM



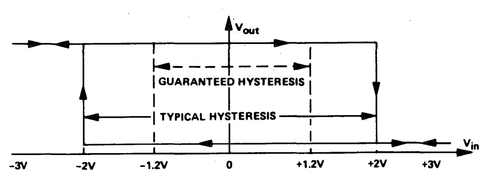
$T_A = 25°C$ and $V_{CC} = 5.0V$

PARAMETER	TEST CONDITIONS: INPUTS EIA	MIL(+)	MIL(−)	STROBE	LIMITS: MIN	TYP	MAX	UNITS
Input Resistance (EIA)	±25V	0.0V	0.0V		3	5	7	kΩ
Input Resistance (MIL)	0.0V	±25V	0.0V		7.5	11.4		kΩ
Propagation Delay				5.00V		100	150	ns
Signal Switching Acceptance				5.00V	20			kHz

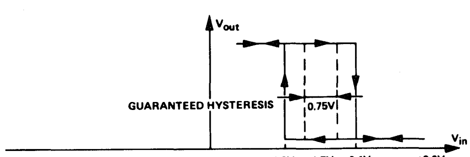
1. This test guarantees transfer of signals of up to 20kHz. Connect 1000pF between the output terminal and ground.

HYSTERESIS CURVES

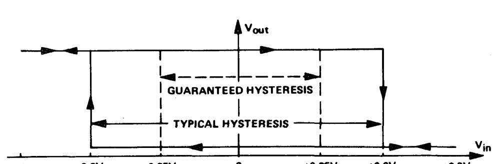
EIA — "HYSTERESIS" OPEN



EIA — "HYSTERESIS" GROUNDED

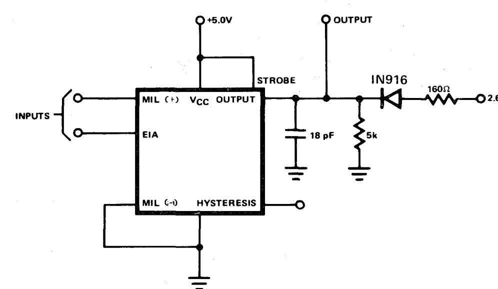


MIL — HYSTERESIS

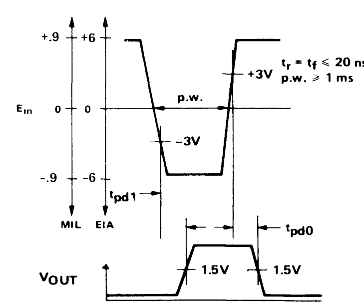


* V_{in} IS REFERENCED TO THE MIL (-) INPUT TERMINAL

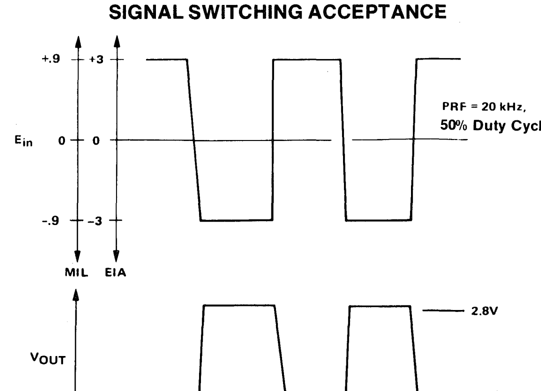
AC TEST FIGURE AND WAVEFORMS



PROPAGATION DELAY

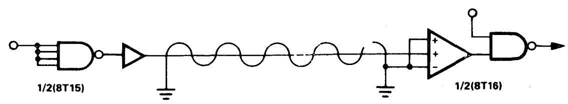


SIGNAL SWITCHING ACCEPTANCE

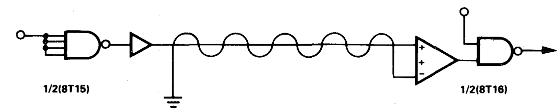


TYPICAL APPLICATIONS

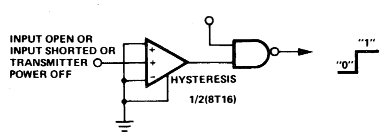
HIGH DIFFERENTIAL NOISE IMMUNITY (EIA + INPUT)



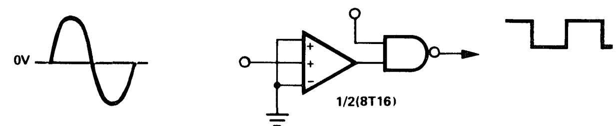
HIGH COMMON MODE NOISE IMMUNITY (MIL + INPUT)



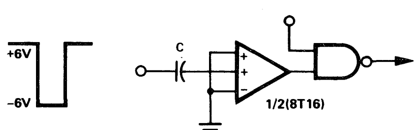
EIA FAIL-SAFE OPERATION



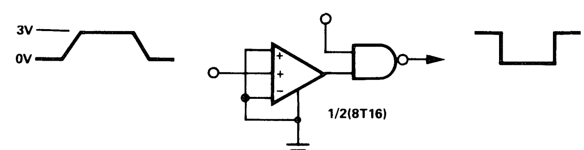
SINE TO SQUARE WAVE CONVERTER



AC COUPLED OPERATIONS



SCHMITT TRIGGER



DUAL 2-INPUT NAND GATE (HIGH VOLTAGE TO TTL INTERFACE) 8T18

8T18 A,F,W

DESCRIPTION

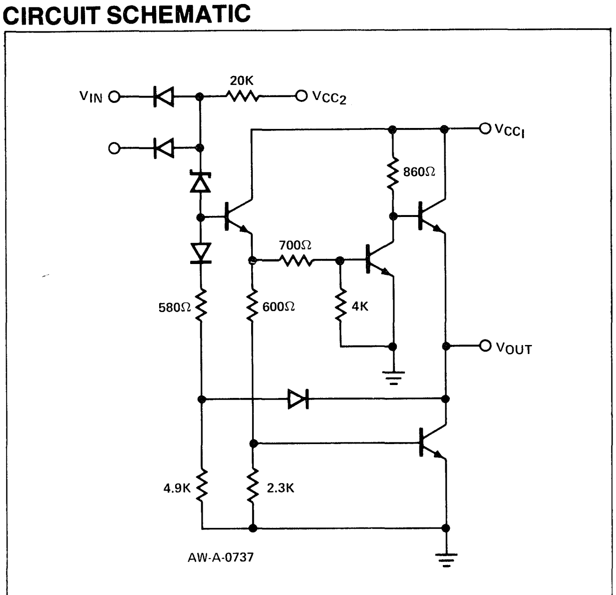
The 8T18 is a Dual 2-Input NAND Interface Gate. It is typically used as a high to low voltage translator which provides translation from up to 30-volt logic levels to standard logic levels of 5 volts.

The basic gate operates from two power supplies. The input structure functions from a high voltage supply V_{CC2}, between 20V and 30V and the second stage transistors and output structure operate from a standard 5V power supply, V_{CC1}.

The high "0" level input threshold (guaranteed at 6.5V) makes the 8T18 very attractive for noisy systems applications such as industrial interfaces.

The output structure features active pull-up and pull-down, providing a low impedance driving source in both "1" and "0" output states. This configuration is particularly suited for driving the high capacitance loads encountered in high fan-out and line driving applications.

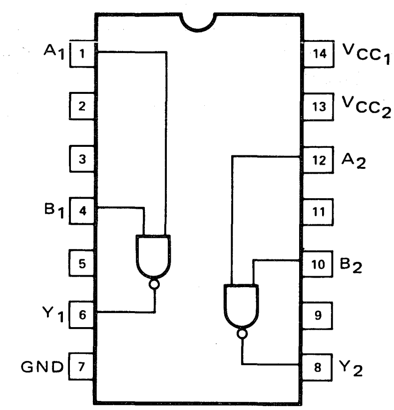
CIRCUIT SCHEMATIC



NOTE: ½ of unit shown. Component values are typical.

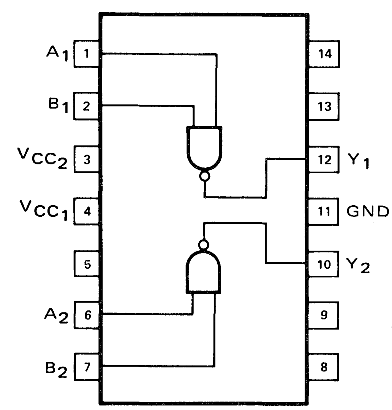
PIN CONFIGURATION

A,F PACKAGE



$AB = \overline{Y}$

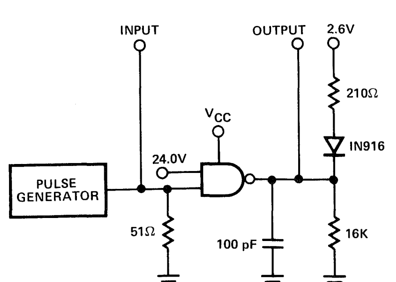
W PACKAGE



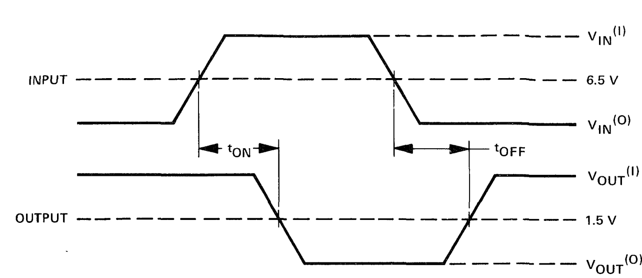
$AB = \overline{Y}$

SWITCHING PARAMETER MEASUREMENT INFORMATION

LOAD CIRCUIT



TYPICAL WAVEFORM



Input Pulse: Amplitude = 24.0 V, P.W. = 200 ns, $t_r = t_f = 10$ ns.

INTERFACE

AC ELECTRICAL CHARACTERISTICS $T_A = 25°$ C, $V_{CC1} = 5.0V$, $V_{CC2} = 24.0V$

PARAMETER		TEST CONDITIONS[9]	LIMITS			UNIT
			MIN	TYP	MAX	
t_{on}	Turn-On Delay	$R_L = 210\Omega$		27	40	ns
t_{off}	Turn-Off Delay	$C_L = 100$ pF		18	35	ns

DESCRIPTION

The Bidirectional One Shot is intended for applications where high speed low level signal processing is required.

The 8T20 Is a Monolithic Building Block, consisting of a high speed analog comparator, digital control circuitry, and a precision monostable multivibrator. The differential input threshold voltage is between ±4mV with respect to the input reference level which may range from −3.2V to +4.2V. For input frequencies up to 8MHz, the device may be conditioned to act as a frequency doubler since it can trigger on both positive and negative input transitions.

Timing pins permit using this device in a variety of applications where external control over pulse width is desirable. Pulse width (t_W) is defined by the relationship $t_W = C_X R_X$ Loge2. Pulse width stability is internally compensated and virtually independent of temperature and V_{CC} variations, thus only limited by the accuracy of external timing components.

An internal resistive divider is available on the chip to provide a voltage of 1.4V (typ.). This output can be connected directly to either of the comparator inputs as a reference voltage when interfacing with TTL outputs.

FEATURES

- DIFFERENTIAL INPUT THRESHOLD = ±4mV
- PULSE POSITION ERROR = TYPICALLY <3ns
- MAX. INPUT FREQUENCY = 8 MHz
- TRIGGERS ON POSITIVE AND/OR TRANSITIONS

APPLICATIONS

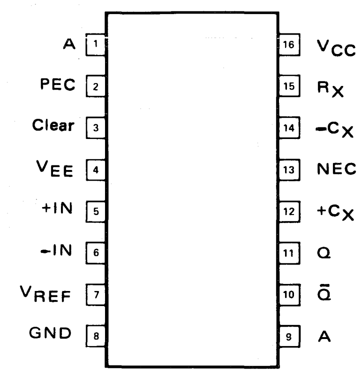
DISC, TAPE AND DRUM READERS
DIGITAL COMMUNICATIONS RECEIVERS
SIGNAL CONDITIONERS
TRANSITION DETECTORS

ABSOLUTE MAX RATINGS

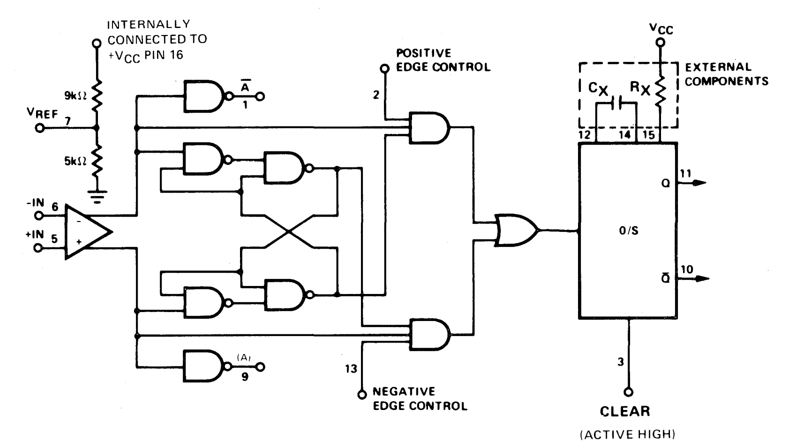
Input Voltage
V_{CC}: +7V
V_{EE}: −7V
MAX DIFF. INPUT VOLTAGE ± 5V

PIN CONFIGURATION

B,F PACKWGE



LOGIC DIAGRAM



V_{EE} = (4) (−5V ±5%)
V_{CC} = (16) (+5V ±5%)
GND = (8)
( ) = Denotes Pin Numbers

$T_A = 25°C$, $V_{CC} = +5.00V$, $V_{EE} = -5.00V$

CHARACTERISTICS	LIMITS MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
Output Frequency	16			MHz	Fig. 1, f_{in} = 8 MHz
Propagation Delay (t_{on}, t_{off})					
Input to Q, Q		30	50	ns	Fig. 2
Input to A, A		30	50	ns	Fig. 4
Clear to Q, Q		20	30	ns	
Reference Voltage (V_{REF})	0.8	1.4	2.0	V	Pin 7 tied to Pin 6
Output Pulse Width, Fig. 1	10		40	ns	Rx = 10K, Cx = Open
Output Pulse Width, Fig. 3	600		800	ns	Rx = 10K, Cx = 100pf

AC TEST CIRCUITS

MINIMUM OUTPUT PULSE WIDTH (C_X = OPEN)

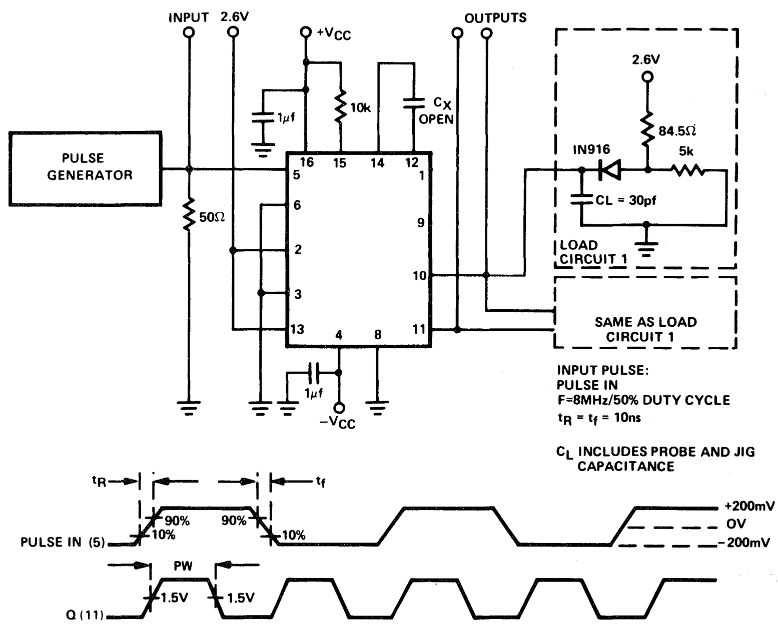


FIGURE 1

PROPAGATION DELAY (INPUT TO Q, $\overline{Q}$ OUTPUTS)

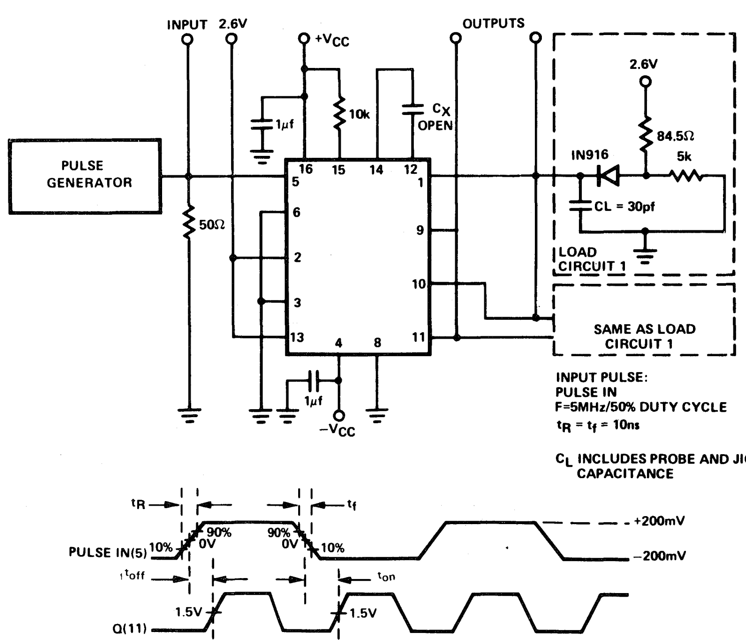


FIGURE 2

AC TEST CIRCUITS (Cont'd)

PROPAGATION DELAY (CLEAR TO Q, $\overline{Q}$)

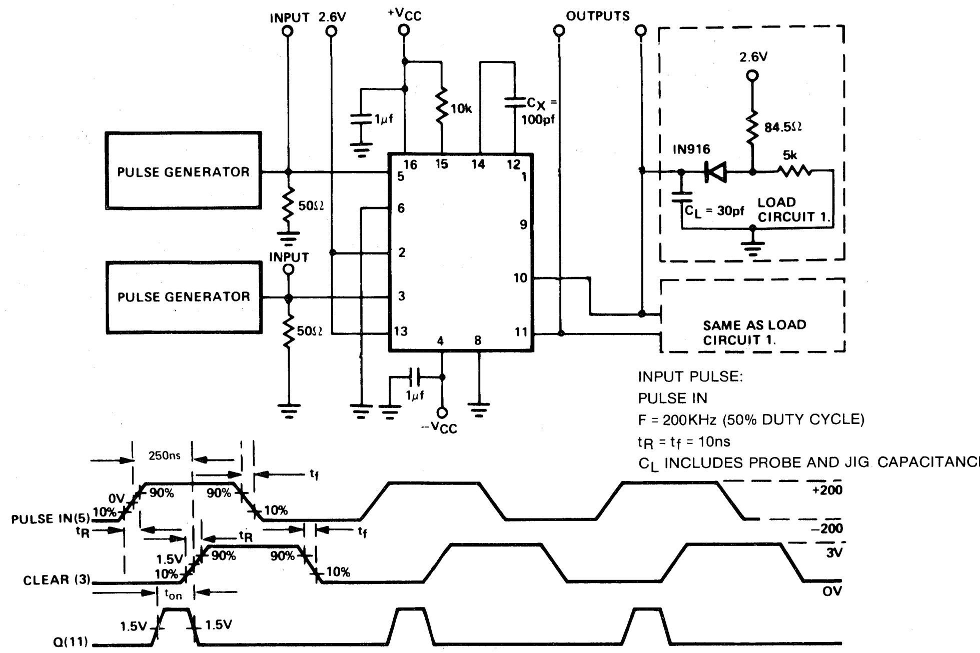


FIGURE 3

PROPAGATION DELAY (INPUT TO A, $\overline{A}$ OUTPUTS)

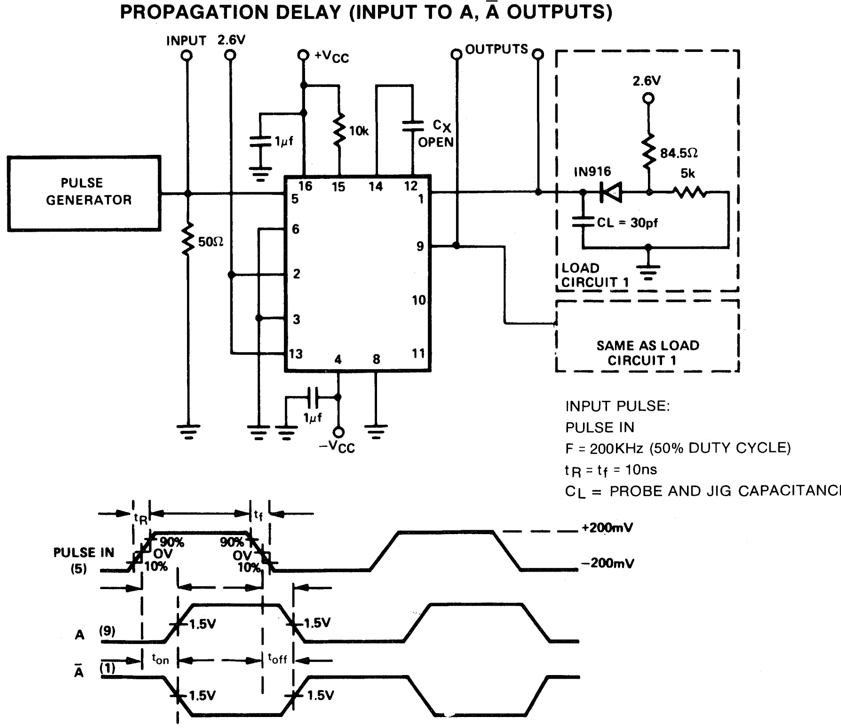


FIGURE 4

INPUT BIAS CURRENT TEST CIRCUIT

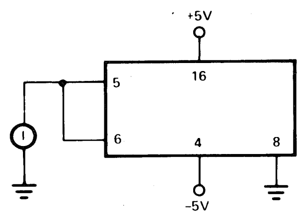


FIGURE 5

INPUT/OUTPUT WAVEFORMS

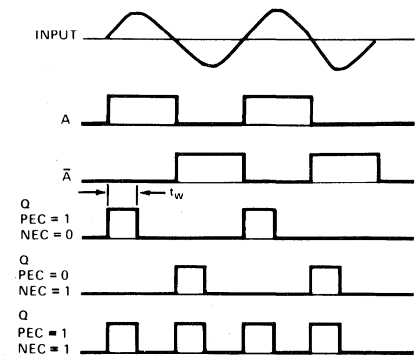


FIGURE 6

DESCRIPTION

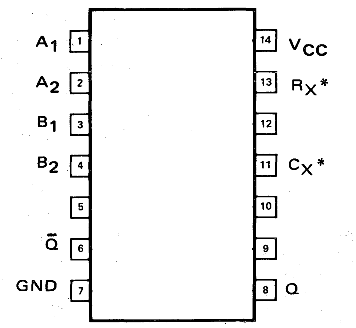
The 8T22 is a direct pin-for-pin replacement for the 9601 retriggerable one-shot. Triggering can be performed on either the leading or falling edge of the input signal through selection of the proper input terminal.

The inputs are level-sensitive making triggering independent of signal transition times. Output pulse width is determined by external timing components (R_X and C_X) with each trigger pulse initiating a complete new timing cycle.

For those applications where a dual retriggerable one-shot is required the Signetics 9602 should be considered.

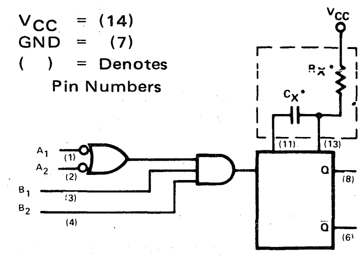
PIN CONFIGURATION

A,F PACKAGE



* PINS FOR EXTERNAL TIMING COMPONENTS

LOGIC DIAGRAM



*External Components

TRUTH TABLE

Pin Number			
1	2	3	4
H→L	H	H	H
H	H→L	H	H
L	X	L→H	H
X	L	L→H	H
L	X	H	L→H
X	L	H	L→H

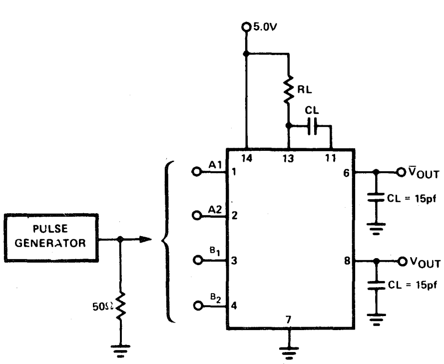
T_A = 25° C and V_{CC} = 5.0V

PARAMETER	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT
Propagation Delay					
Negative Trigger Input to True Output (t_{pd}+)	R_X = 5.0kΩ, C_X = 0; C_L = 15pf		25	40	ns
Negative Trigger Input to False Output (t_{pd}-)	R_X = 5.0kΩ, C_X = 0; C_L = 15pF		25	40	ns
Min. True Output Pulse Width	R_X = 5.0kΩ, C_X = 0; C_L = 15pF		45	65	ns
Pulse Width Variation	R_X = 10kΩ, C_X = 1000pF	3.08	3.42	3.76	μs
Timing Resistor		5.0		50	kΩ
C_{Stray} - Maximum allowable wiring capacitance	P13 to Ground			50	pF

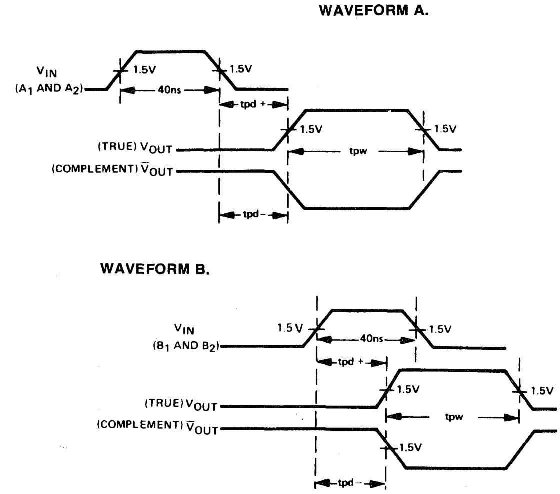
NOTES
1. Positive current is defined as into the pin referenced.
2. Unless otherwise noted, 10kΩ resistor placed between Pin 13 and V_{CC} (R_X).

AC TEST FIGURE AND WAVEFORMS

TRIGGER INPUT/OUTPUT AND PULSE WIDTH



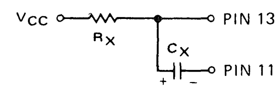
WAVEFORM A.

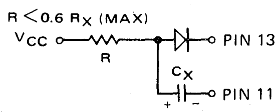


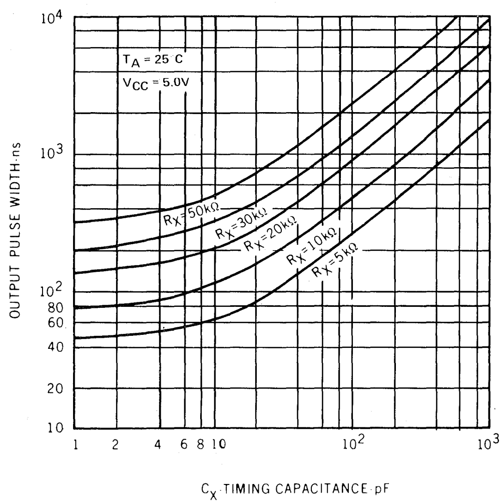
NOTES:
1. Pulse Generator has the following characteristics: t_r = t_f = 10ns (10% to 90%), AMP. = 3V.
2. C_L includes probe and jig capacitance.
3. For tpd+, tpd− and tpw (min.) RX = 5kΩ ± 1%, CX = OPEN, PRR = 1MHz.
4. For Δtpw: RX = 10kΩ ± 1%, C_X = 1000pF ± 1%, PRR = 200kHz.

8T22 A,F

OPERATION RULES







TYPICAL OUTPUT PULSE WIDTH VERSUS TIMING RESISTANCE AND CAPACITANCE FOR $C_X < 10^3$ pF IS SHOWN IN THE ABOVE GRAPH.

1. An external resistor (R_X) and external capacitor (C_X) are required as shown in the Logic Diagram.
2. The value of R_X may vary from 5.0 to 50 kΩ (0 to 75°).
3. C_X may vary from 0 to any necessary value available. If, however, the capacitor has leakages approaching 3.0 μA or if stray capacitance from either terminal to ground is more than 50 pF, the timing equations may not represent the pulse width obtained.
4. If electrolytic capacitors are to be used, the following configurations are recommended:
   - A. For use with low leakage electrolytic capacitors. The normal RC configuration can be used predicably only if the forward capacitor leakage at 5.0 volts is less than 3 μA, and the inverse capacitor leakage at 1.0 volt is less than 5 μA over the operational temperature range, and Rule 3 above is satisfied.
   - B. Use with high inverse leakage current electrolytic capacitors. The diode in this configuration prevents high inverse leakage currents through the capacitor by preventing an inverse voltage across the capacitor.

$t \approx 0.3\ RC_X$

The output pulse with (t) is defined as follows:

$$t = 0.32\ R_X C_X \left[1 + \frac{0.7}{R_X}\right]$$

Where R_X is in kΩ, C_X is in pF, t is in ns; for $C_X < 10^3$ pF.

DESCRIPTION

The 8T23 is a Dual Line Driver designed to meet all of the requirements of the IBM System/360, System/370 I/0 interface specifications (IBM Specification GA 22-6974-0).

The low impedance emitter follower output will drive terminated lines such as coaxial cable or twisted pair. The output is protected against accidental shorting by an internal clamping network which turns on once the output voltage drops below approximately 1.5 volts. The uncommited emitter output structure allows Dot-OR logic to be performed as in "Party-Line" operations.

Multiple emitter inputs allow the 8T23 to interface with standard TTL or DTL systems and the circuit operates from a single +5 volt power supply.

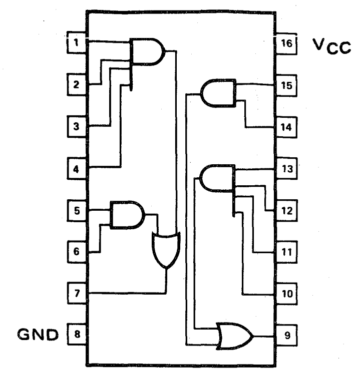
Additional logic incorporated in the 8T23 Dual Line Driver can be used during the power-up and power-down sequence to ensure that no spurious noise is generated on the line.

FEATURES

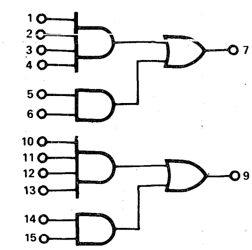
- **IOUT = 59.3mA AT 3.11 VOLTS**
- **UNCOMMITTED EMITTER OUTPUT STRUCTURE FOR PARTY-LINE OPERATION**
- **SHORT-CIRCUIT PROTECTION**
- **SINGLE 5 VOLT POWER SUPPLY.**
- **AND-OR LOGIC CONFIGURATION**

PIN CONFIGURATION

B,F,W PACKAGE



LOGIC DIAGRAM



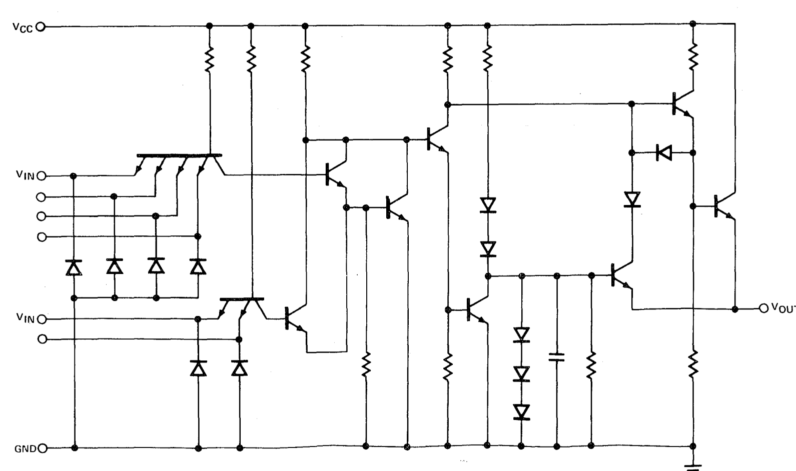
V_{CC} = (16)
GND = (8)
( ) = Denotes Pin Numbers

SWITCHING CHARACTERISTICS V_{CC} = 5.0V, T_A = 25° C[1,2]

PARAMETER	LIMITS			UNIT
	MIN	TYP	MAX	
t_{on}, Turn-On Delay		12 15	20 25	ns ns
t_{off}, Turn-Off Delay		12 20	20 35	ns ns

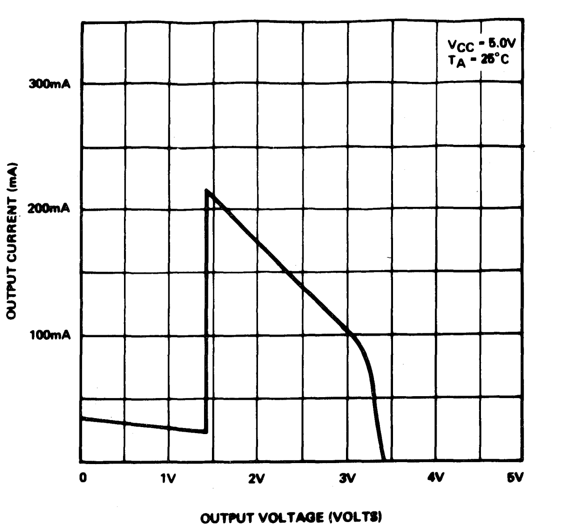
NOTES:
1. RL = 50Ω to ground.
2. Load is 50Ω in parallel with 100pF.
3. Reference AC Test Circuit and Pulse Requirements

CIRCUIT SCHEMATIC

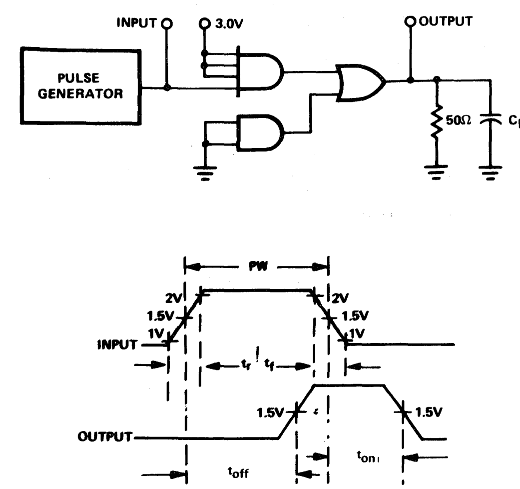


8T23 B,F,W

TYPICAL OUTPUT CHARACTERISTICS

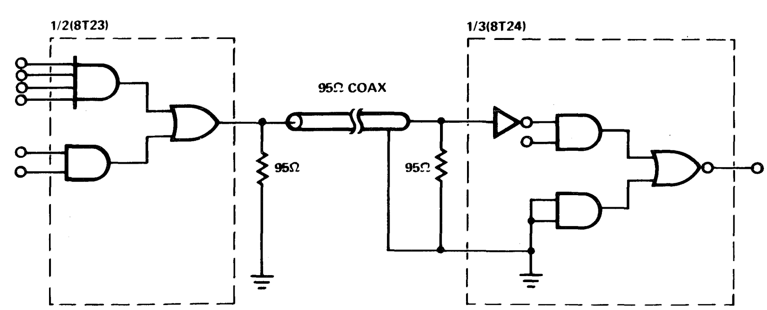


AC TEST FIGURE AND WAVEFORMS



INPUT PULSE:
AMPLITUDE = 3.0V
PW = 50ns (50% DUTY CYCLE)
$t_r = t_f \leq$ 5ns (10% AND 90% MEASUREMENT POINTS)

TYPICAL APPLICATIONS



8T24 B,F,W

DESCRIPTION

The 8T24 is a Triple Line Receiver designed specifically to meet the IBM System (360, System/370 I/O Interface Specification (IBM Specification GA 22-6974-0). Each receiver incorporates hysteresis to provide high noise immunity and high input impedance to minimize loading on the driver circuit.

An input voltage of 1.7 volts or more is interpreted as a logical one; an input of 0.70 volts or less is interpreted as a logical zero as is an open circuited input.

The receiver input (R) of the 8T24 will not be damaged by a DC input of +7.0 volts with power on or by a DC input of +6.0 volts with power off in the receiver. The 8T24 will also withstand an input of −0.15V with power on or off.

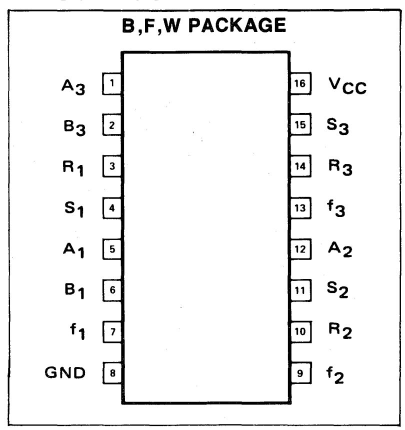
The 8T24 is fully compatible with TTL and DTL systems and operates from a single 5 volt power supply.

FEATURES

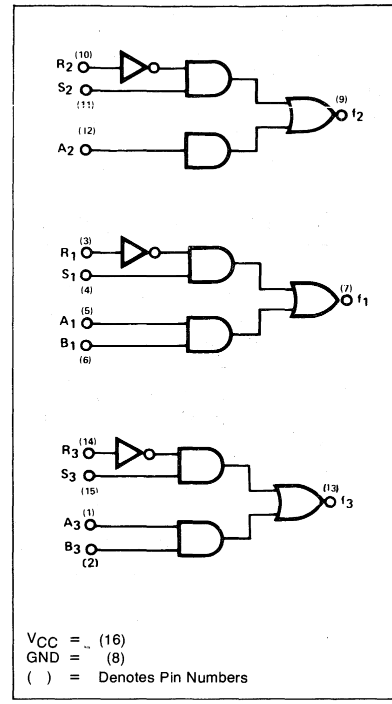
- BUILT-IN INPUT THRESHOLD HYSTERESIS*
- HIGH SPEED: $T_{ON} = T_{OFF} =$ 20ns (TYPICAL)
- EACH CHANNEL CAN BE STROBED INDEPENDENTLY
- FANOUT OF TEN (10) WITH STANDARD TTL INTEGRATED CIRCUITS
- INPUT GATING IS INCLUDED WITH EACH LINE RECEIVER FOR INCREASED APPLICATION FLEXIBILITY
- OPERATION FROM A SINGLE +5V POWER SUPPLY

* Hysteresis is defined as the difference between the input thresholds for the "1" and "0" output states. Hysteresis is specified at 0.4V typically and 0.2V minimum over the operating temperature range.

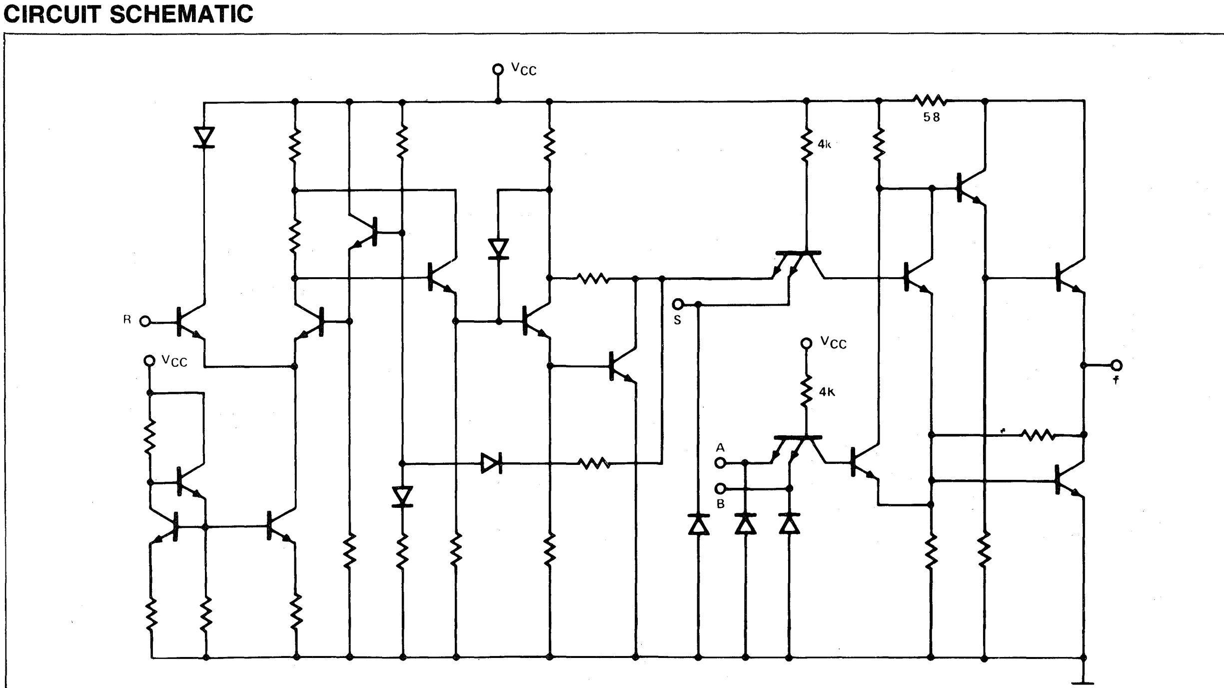
PIN CONFIGURATION



LOGICAL DIAGRAM WITH PIN LAYOUT



CIRCUIT SCHEMATIC

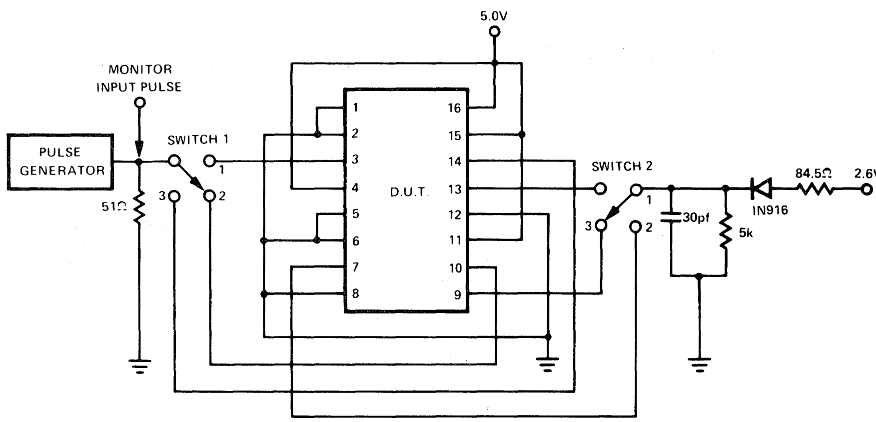


SWITCHING CHARACTERISTICS AT V_{CC} = 5.0v AND T_A = 25°C

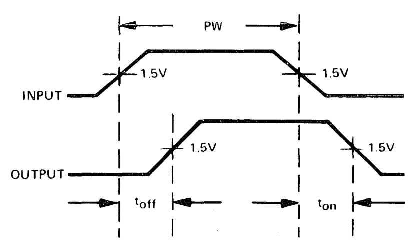
PARAMETER	TEST CONDITIONS R	S	A	B	LIMITS MIN	TYP	MAX	UNITS
t_{on}, Turn-On Delay						20	30	ns
t_{off}, Turn-Off Delay						20	30	ns
Hysteresis[1]		4.5V	0V	0V	0.2	0.4		V

1. Hysteresis is defined as the voltage difference between the R input level at which the output begins to go from "O" to "1" state and the level at which the output begins to go from "1" to "0".

AC TEST CIRCUIT AND WAVEFORMS



Input Pulse:
Amplitude = 2.6V
Pulse width = 200nS
(50% Duty Cycle)
tr = tf = 5nS (10% to 90%)

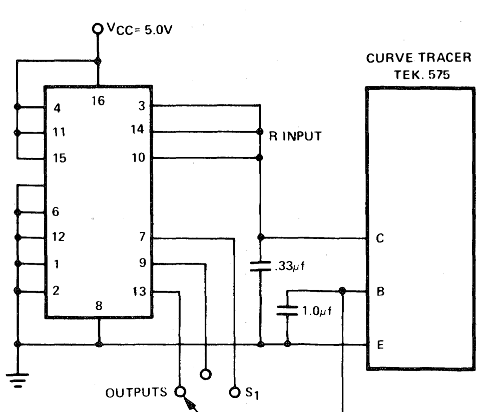


3 Receivers in the package.
Test each Receiver using switch positions as shown in Table 1.

TABLE 1

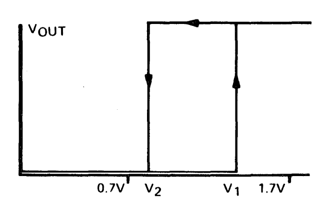
Receiver no.	POSITION Switch 1	Switch 2
Receiver 1	1	1
Receiver 2	2	2
Receiver 3	3	3

HYSTERESIS TEST CIRCUIT

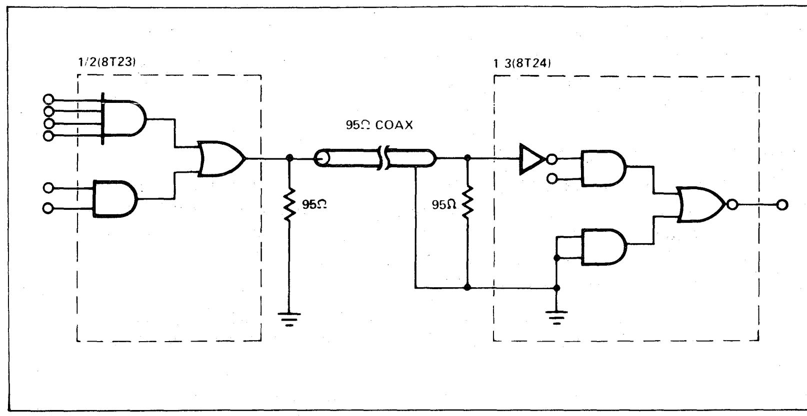


Verify in each of three (3) positions of S_1 (Figure 1) that the following occurs per Figure 2.

1. V_1 and V_2 must be between o.7V minimum and 1.7 maximum.
2. Hysteresis = $V_1 - V_2$



TYPICAL APPLICATION



DESCRIPTION

The 8T25 is a Dual MOS-to-TTL interface element. The Sense Amplifier is designed to accept low level MOS signals from the output of Random Access Memories and the information is stored in a latch in response to an external Strobe signal. A tristate output buffer presents the data to the output using conventional TTL logic levels. The 8T25 operates from a single +5 volt supply.

CIRCUIT OPERATION

A logic "1" level on the PRESET/DISABLE line will disconnect the outputs of the Sense Amplifier from a common bus by turning both totem-pole transistors off. When the Preset/Disable line returns to a logic "0" level, the outputs will be preset to a logic "1" state. A low-going Strobe pulse will then transfer the data at Inputs A and B to their respective outputs non-inverted.

Due to the internal latch, output data will remain stable regardless of any change in input levels until a Disable signal again forces both outputs to the high impedance state.

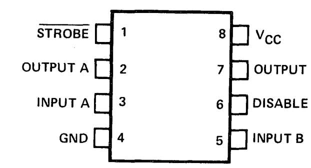
If the STROBE is not used (STROBE = 0) the effect of the Preset/Disable line is to first disconnect the data from the tri-state bus (PRESET/DISABLE HIGH) and then transfer the input data to the output.

FEATURES

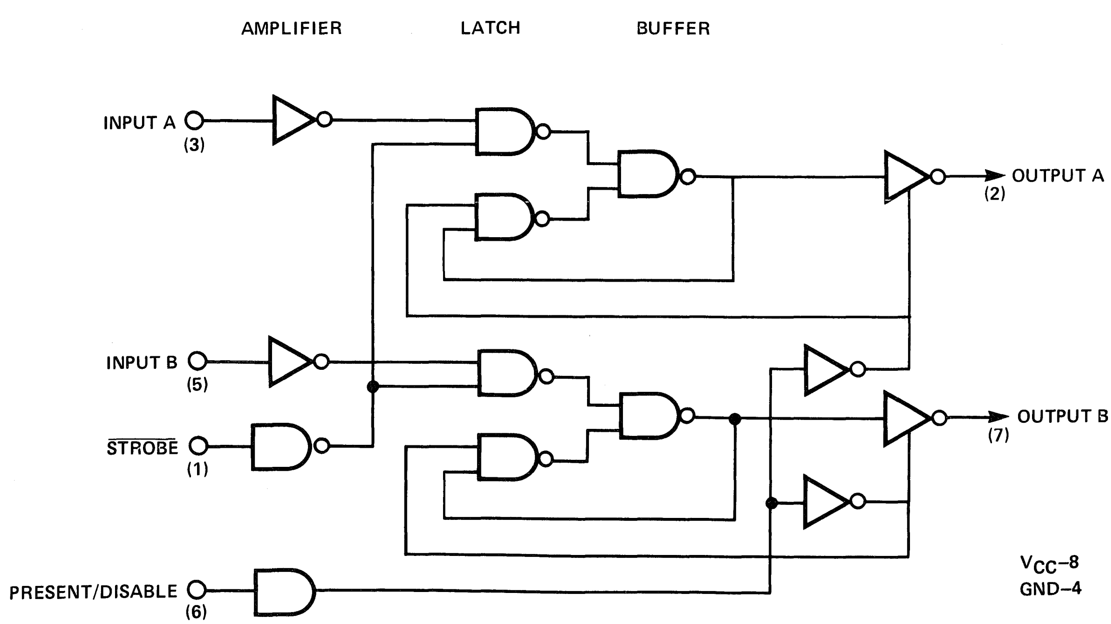
- MOS-TO-TTL CONVERTER
- INTERNAL LATCH
- TRISTATE OUTPUTS
- SINGLE +5V SUPPLY

PIN CONFIGURATION

V PACKAGE



LOGIC DIAGRAM



ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_{CC} = 5.0V$

PARAMETER	LIMITS MIN	TYP	MAX	UNIT
Propagation Delay Strobe to Output (t_{ds})		15	25	ns
Disable to "0" Output (t_{PZL})		15	25	ns
"0" Output to Disable (t_{PLZ})		8	15	ns
Disable to "1" Output (t_{PZH})		15	25	ns
"1" Output to Disable (t_{PHZ})		9	20	ns

AC TEST CIRCUITS AND WAVEFORMS

PROPAGATION DELAY (STROBE TO OUTPUT)

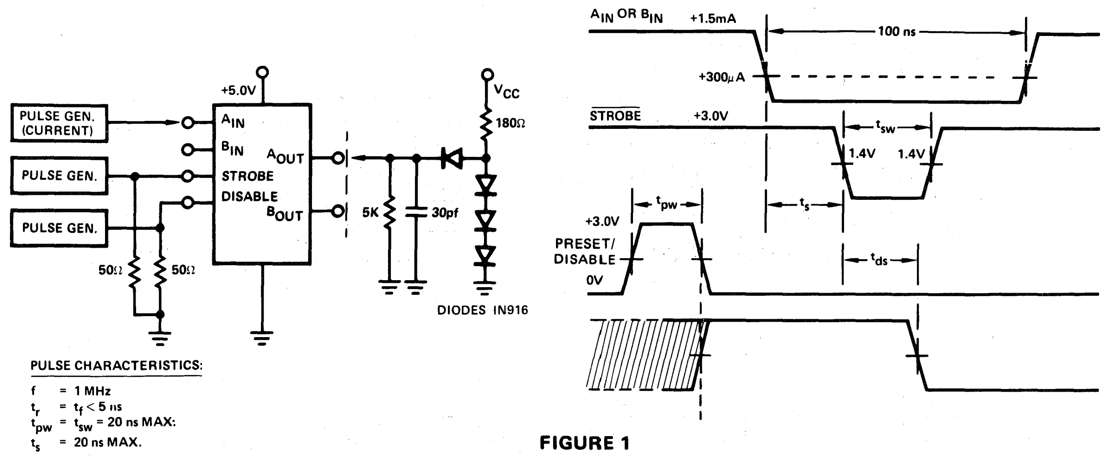
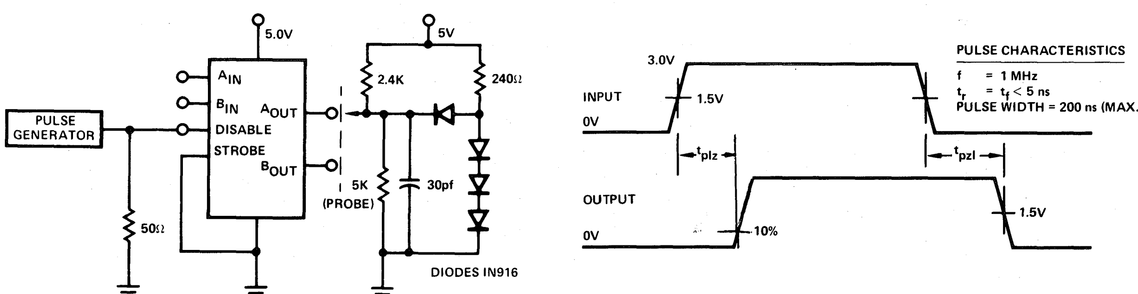


FIGURE 1

PROPAGATION DELAY (DISABLE TO OUTPUT)

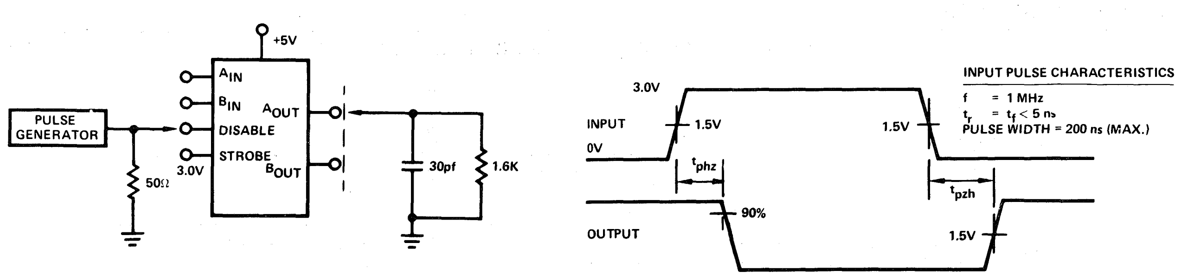


NOTE: t_{plz} = "0" OUTPUT TO HIGH–Z

t_{pzl} = HIGH–Z TO "0" OUTPUT

FIGURE 2

PROPAGATION DELAY (DISABLE TO OUTPUT)



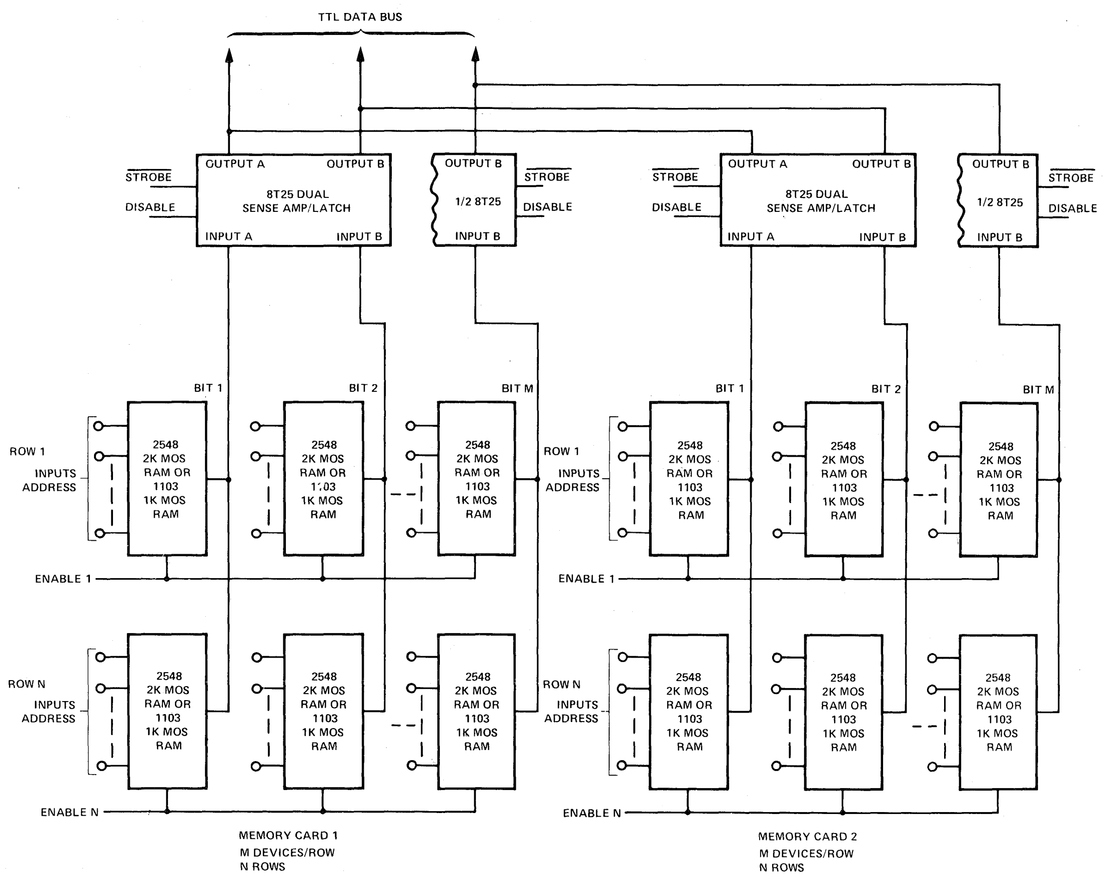
NOTE: t_{phz} = "1" OUTPUT TO HIGH–Z

t_{pzl} = HIGH–Z TO "0" OUTPUT

FIGURE 3

TYPICAL APPLICATION

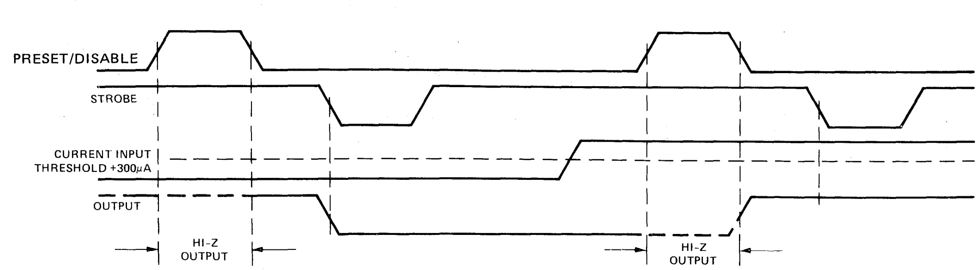
MOS MEMORY SYSTEM



NOTE: EACH MEMORY CARD IS AN
N (2K) XM MEMORY FOR 2548 2K MOS RAM
N(K) XM MEMORY FOR 1103 1K MOS RAM

TYPICAL WAVEFORMS

TYPICAL PRESET/DISABLE AND STROBE SEQUENCE*



* T .ese waveforms are easily obtained from the clock phases of the memory systems if desired.

DESCRIPTION

The 8T26A/28 consists of four pairs of Tri-State logic elements configured as Quad Bus Drivers/Receivers along with separate buffered receiver enable and driver enable lines. This single IC Quad Transceiver design distinguishes the 8T26A/28 from conventional multi-IC implementations. In addition, the 8T26/28's ultra high speed while driving heavy bus capacitance (300pF) makes these devices particularly suitable for memory systems and bidirectional data buses.

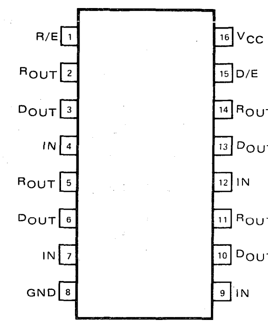
Both the Driver and Receiver gates have Tri-State outputs and low-current PNP inputs. Tri-State outputs provide the high switching speeds of totempole TTL circuits while offering the bus capability of open collector gates. PNP inputs reduce input loading to 200μA maximum.

APPLICATIONS

HALF-DUPLEX DATA TRANSMISSION
MEMORY INTERFACE BUFFERS
DATA ROUTING IN BUS ORIENTED SYSTEMS
HIGH CURRENT DRIVERS
MOS/CMOS-TO-TTL INTERFACE

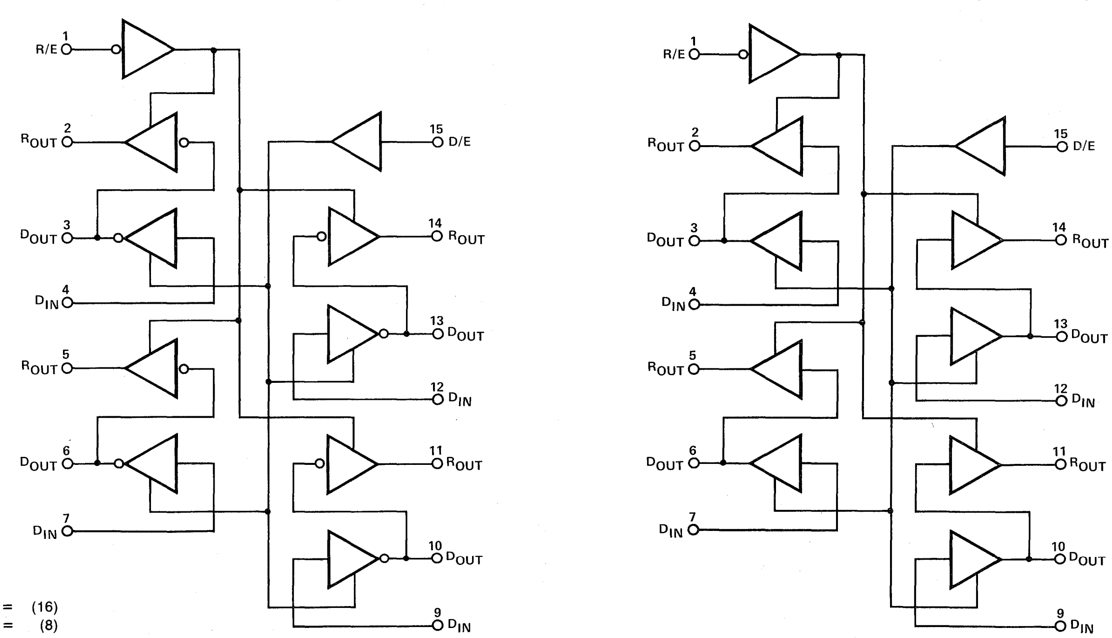
PIN CONFIGURATION

B,F PACKAGE



LOGIC DIAGRAM

8T26A — INVERTING OUTPUT (TRI-STATE) **8T28 — NON-INVERTING OUTPUT (TRI-STATE)**



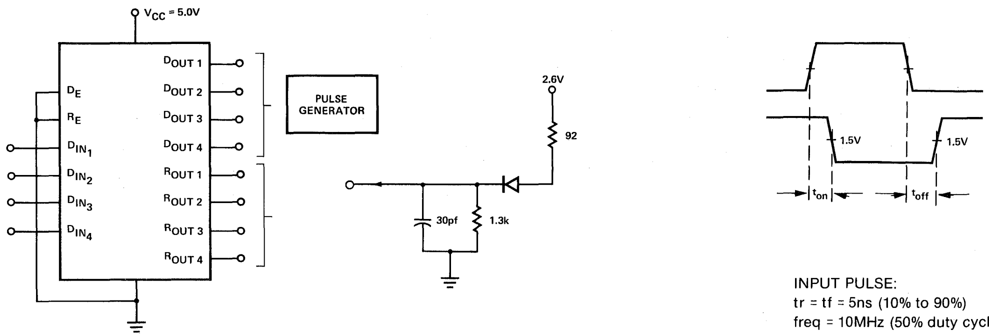
V_{CC} = (16)
GND = (8)
( ) = DENOTES PIN NUMBERS

SWITCHING CHARACTERISTICS

PARAMETER		TEST CONDITIONS	8T26A MAX	8T28 MAX	UNIT
Propagation Delay t_{ON}	D_{OUT} to R_{OUT}	C_L = 30pF, Note 9	14	17	ns
t_{OFF}	D_{OUT} to R_{OUT}		14	17	
t_{ON}	D_{IN} to D_{OUT}	C_L = 300pF, Note 9	14	17	ns
t_{OFF}	D_{IN} to D_{OUT}		14	17	
Data Enable to Data Output t_{PZL}	High Z to O	C_L = 300pF, Note 9	25	28	ns
t_{PLZ}	O to High Z		20	23	
Receiver Enable to Receiver Output t_{PZL}	High Z to O	C_L = 30pF, Note 9	20	23	ns
t_{PLZ}	O to High Z		15	18	

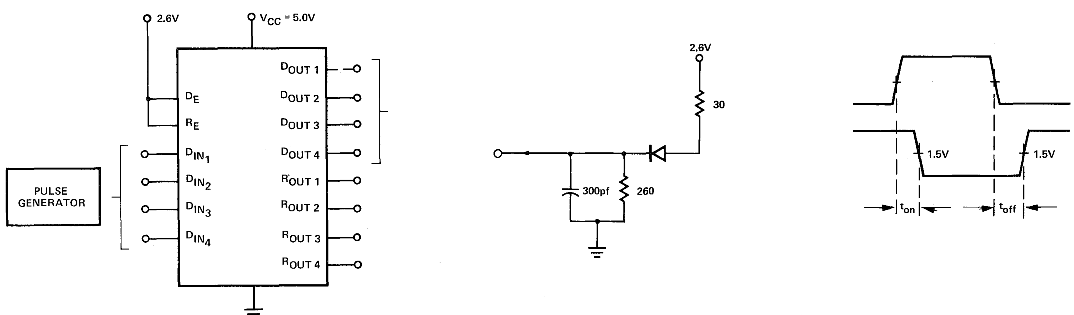
AC TEST CIRCUITS AND WAVEFORMS

PROPAGATION DELAY (DOUT TO ROUT)

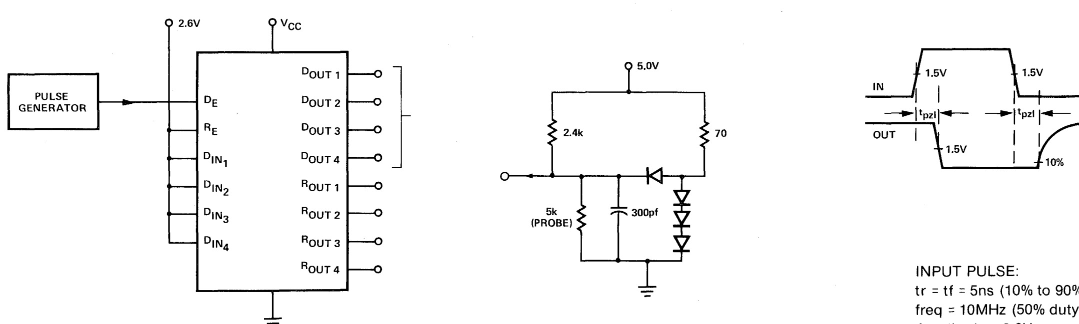


INPUT PULSE:
tr = tf = 5ns (10% to 90%)
freq = 10MHz (50% duty cycle)
Amplitude = 2.6V

PROPAGATION DELAY (DIN TO DOUT)



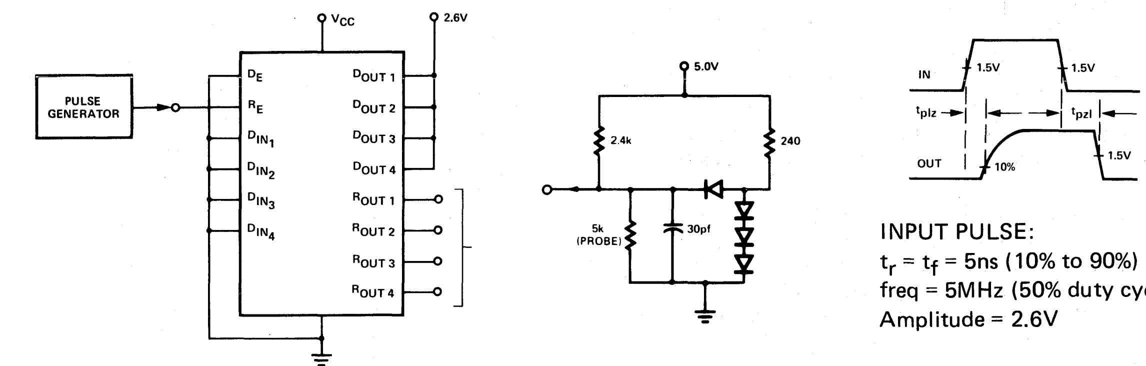
PROPAGATION DELAY (DATA ENABLE TO DATA OUTPUT)



INPUT PULSE:
tr = tf = 5ns (10% to 90%)
freq = 10MHz (50% duty cycle)
Amplitude = 2.6V

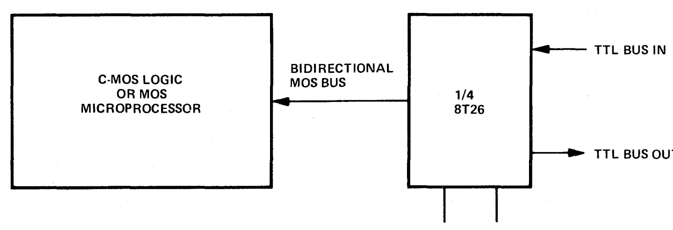
BLOCK DIAGRAM

PROPAGATION DELAY (RECEIVE ENABLE TO RECEIVE OUTPUT)



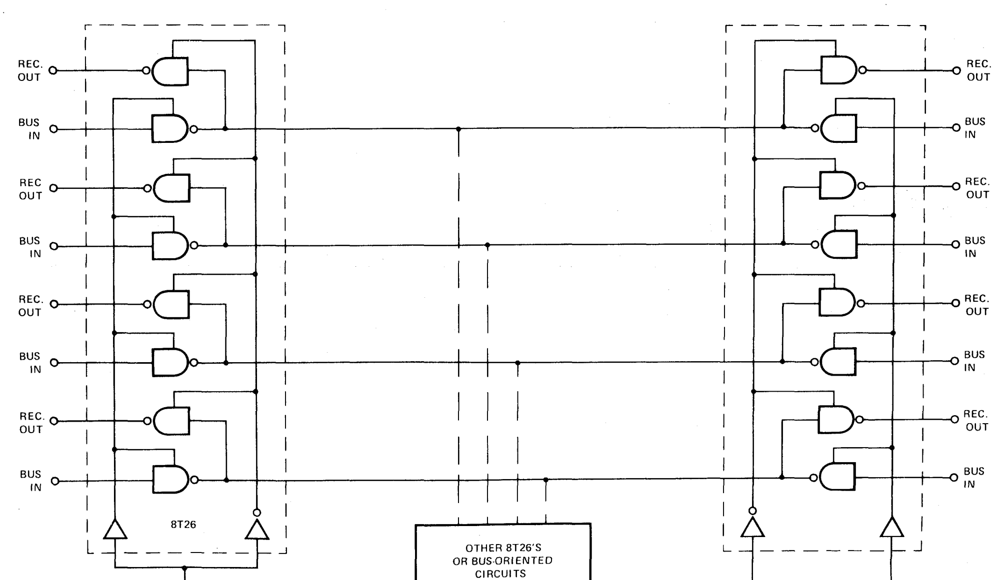
INPUT PULSE:
$t_r = t_f = 5ns$ (10% to 90%)
freq = 5MHz (50% duty cycle)
Amplitude = 2.6V

BIDIRECTIONAL MOS - CMOS TO TTL INTERFACE



TYPICAL APPLICATIONS

BIDIRECTIONAL DATA BUS



CONTROL LINES MAY BE TIED TOGETHER, SUCH THAT
LOGICAL '1' TRANSMIT, LOGICAL '0' RECEIVE

LOGICAL "0" = ACTIVE
LOGICAL "1" = HI-z

LOGICAL "1" = ACTIVE
LOGICAL "0" = HI-z

DESCRIPTION

The 8T30 is a dual bi-directional bus interchange element that interfaces MOS and TTL data busses. Data can be exchanged in a half-duplex transmission mode from a "party line" TTL/DTL bus to a MOS transceiver port and a TTL/DTL transceiver port. For maximum versatility the receive inputs and high current sink open collector transmit outputs are brought out separately.

Common receive and transmit enable controls condition each half of the 8T30 for six valid modes of operation as tabulated in Table 1.

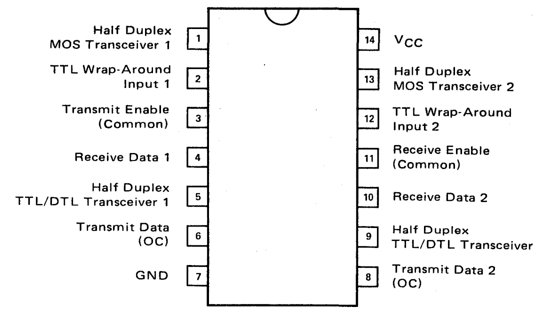
Pins 6 and 4 (8 and 10) are typically connected such that data from a common high performance "party line" bus can be routed to and from the TTL/DTL and MOS transceiver ports. In addition, wrap-around inputs are provided such that TTL/DTL data can be sent directly to the MOS transceiver port and the TTL/DTL "party line drivers" without using the TTL/DTL transceiver port.

A high performance emitter follower driver and a low current base input on the MOS transceiver port make the 8T30 a superior MOS bus interface element.

A power-down sequence (as V_{CC} is varied from 5.25V to 0V) of the 8T30 will have no effect on the transmit outputs i.e., the "party line" bus driving the port controller.

PIN CONFIGURATION

A,F PACKAGE



8T30 VALID OPERATING MODES

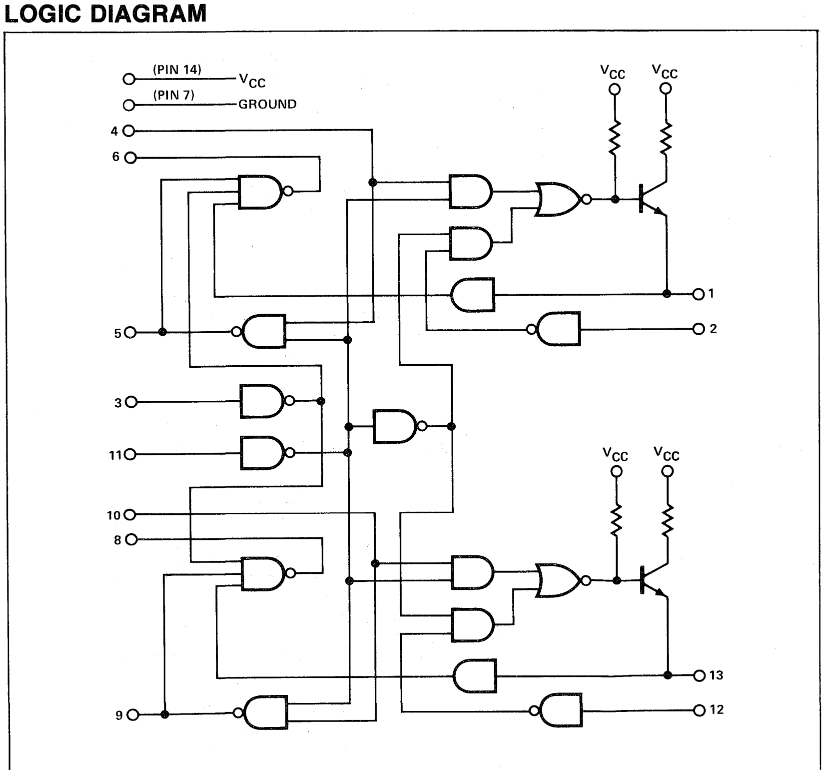
MODE OF OPERATION	PIN FUNCTIONS	PIN NUMBERS 6 & 4 (8 & 10)	2 (12)	5 (9)	3	11	1 (13)
Port Controller Receives Data From TTL/DTL System	Control		0		1	0	
	Data In	Data					
	Data Out			Data			Data
TTL/DTL Transceiver Sends Data to TTL/DTL System	Control		0		0	1	1
	Data In			Data			
	Data Out	Data					
MOS Transceiver Sends Data to TTL/DTL System	Control		0	1	0	1	
	Data In						Data
	Data Out	Data					
MOS Transceiver Receives Data from TTL/DTL Wrap-Around Input	Control	X		1	1	1	
	Data In		Data				
	Data Out						Data
TTL/DTL System Receives Data From TTL/DTL Wrap-Around Input	Control			1	0	1	
	Data In		Data				
	Data Out	Data					Data
Port Controller Idle (Random Activity on Pins 1(13), 2(12), and 5(9) Does Not Affect Bus on 6, 4 (8, 10)	Control		X	X	1	1	X
	Data In	X					
	Data Out	X					

(X = Don't Care, 1 = Logic "1", 0 = Logic "0")

AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_{CC} = 5.0V$

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
Propagation Delays						
TTL/DTL Transceiver Inputs to Transmit Outputs	t_{on}	Fig. 1, 2 $R_L = 220\Omega$, $C_L = 50pF$		14	25	ns
	t_{off}			14	20	ns
MOS Transceiver Inputs to Transmit Outputs	t_{on}	Fig. 2, 3 $R_L = 220\Omega$, $C_L = 50$ pF		23	70	ns
	t_{off}			23	50	ns
TTL Wraparound Inputs to Transmit Outputs	t_{on}	Fig. 2, 4 $R_L = 220\Omega$, $C_L = 50$ pF		120	175	ns
	t_{off}	$R_F = 11.2K$, $C_F = 30$ pF		36	75	ns
Receive Inputs to TTL/DTL Transceiver Outputs	t_{on}	Fig. 2, 5 $R_L = 100\Omega$, $C_L = 30$ pF		42	60	ns
	t_{off}	Fig. 2, 5 $R_L = 4K\Omega$, $C_L = 30$ pF		13	20	ns
Receive Inputs to MOS Transceiver Outputs	t_{on}	Fig. 6, 7 $R_F = 11.2K$, $C_F = 30$ pF		14	35	ns
	t_{off}			106	135	ns
Transmit Enable to Transmit Outputs	t_{on}	Fig. 8, 9 $R_L = 220\Omega$, $C_L = 50$ pF		19	40	ns
	t_{off}			19	40	ns
Receive Enable to TTL/DTL Transceiver Outputs	t_{on}	Fig. 9, 10 $R_L = 400\Omega$, $C_L = 30$ pF		46	60	ns
	t_{off}	Fig. 9, 10 $R_L = 4K\Omega$, $C_L = 30$ pF		19	35	ns
Receive Enable to MOS Transceiver Outputs	t_{on}	Fig. 11, 12 $R_F = 11.2K$, $C_F = 30$ pF		20	50	ns
	t_{off}			115	155	ns

LOGIC DIAGRAM



INTERFACE

AC TEST FIGURES AND WAVEFORMS

t_{on}, t_{off} TRANSCEIVER INPUTS TO TRANSMIT OUTPUTS

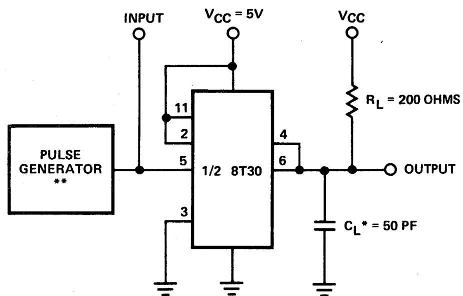
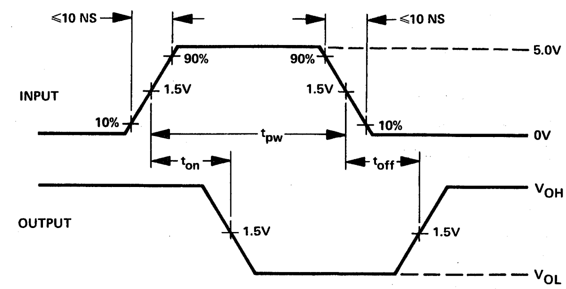


FIGURE 1

WAVEFORMS



*C_L INCLUDES STRAY AND PROBE CAPACITANCE
**$t_{PW} \cong 0.5\ \mu$SEC, PRR $\cong$ 1 MHz, $R_{out} \cong 50$ OHMS

FIGURE 2

t_{on}, t_{off} MOS TRANSCEIVER TO TRANSMIT OUTPUTS

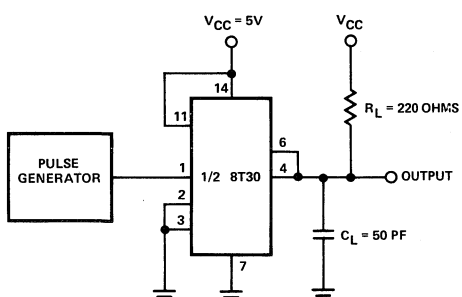
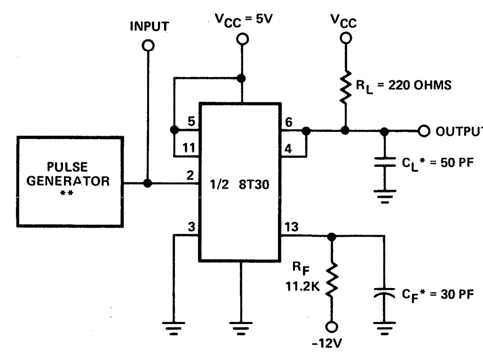


FIGURE 3

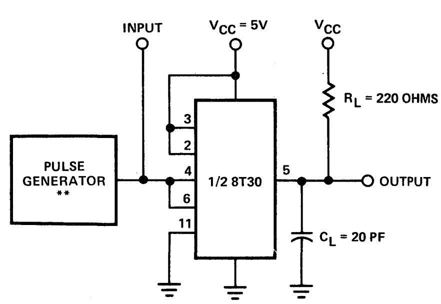
t_{on}, t_{off} TTL WRAPAROUND INPUTS TO TRANSMIT OUTPUTS



*C_F, C_L INCLUDES STRAY AND PROBE CAPACITANCE
**$t_{PW} \cong 0.5\ \mu$SEC, PRR $\cong$ 1 MHz, $R_{out} \cong 50$ OHMS
SEE FIGURE 2 FOR WAVEFORMS

FIGURE 4

t_{on}, t_{off} RECEIVE INPUTS TO TTL/DTL TRANSCEIVER OUTPUTS



*C_L INCLUDES STRAY AND PROBE CAPACITANCE
**$t_{PW} \cong 0.5\ \mu$SEC, PRR $\cong$ 1 MHz, $R_{out} \cong 50$ OHMS
SEE FIGURE 2 FOR WAVEFORMS

FIGURE 5

t_{on}, t_{off} RECEIVE INPUTS TO MOS TRANSCEIVER OUTPUTS

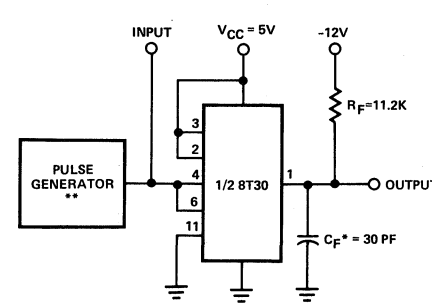
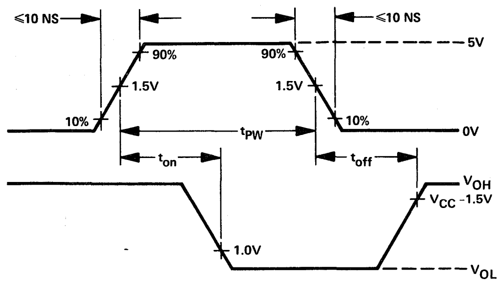


FIGURE 6

AC TEST FIGURES AND WAVEFORMS (Cont'd)

t_{on}, t_{off} WAVEFORMS



*C_L INCLUDES STRAY AND PROBE CAPACITANCE
**$t_{PW} \cong 0.5\ \mu SEC$, PRR ≅ 1 MHz, $R_{out} \cong 50$ OHMS

FIGURE 7

TRANSMIT ENABLE TO TRANSMIT OUTPUTS

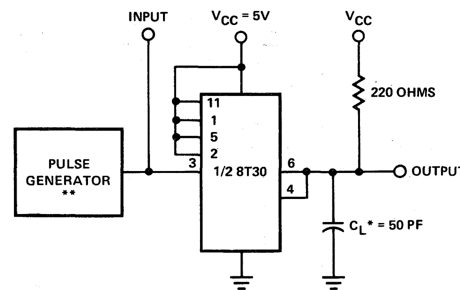
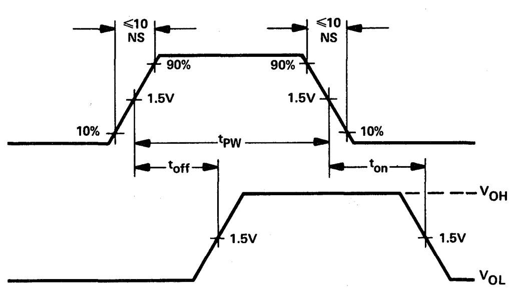


FIGURE 8

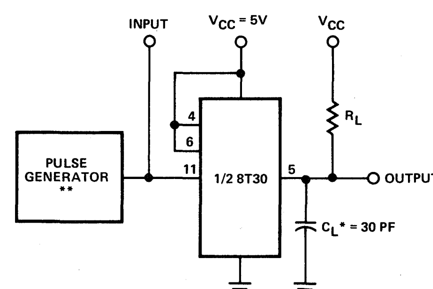
t_{on}, t_{off} WAVEFORMS



*C_F INCLUDES STRAY AND PROBE CAPACITANCE
**$t_{PW} \cong 0.5\ \mu SEC$, PRR ≅ 1 MHz, $R_{out} \cong 50$ OHMS

FIGURE 9

t_{on}, t_{off} RECEIVE ENABLE TO TTL/DTL TRANSCEIVER OUTPUTS



*C_F, C_L INCLUDES STRAY AND PROBE CAPACITANCE
**$t_{PW} \cong 0.5\ \mu SEC$, PRR ≅ 1 MHz, $R_{out} \cong 50$ OHMS
SEE FIGURE 2 FOR WAVEFORMS

FIGURE 10

t_{on}, t_{off} RECEIVE ENABLE TO MOS TRANSCEIVER OUTPUTS

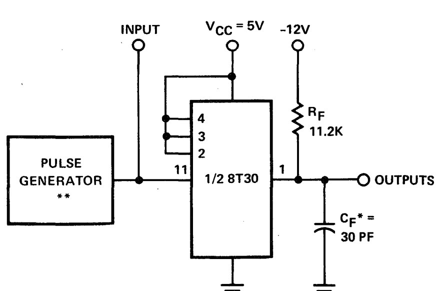
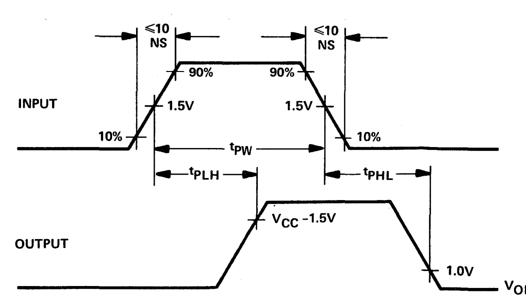


FIGURE 11

t_{on}, t_{off} WAVEFORMS

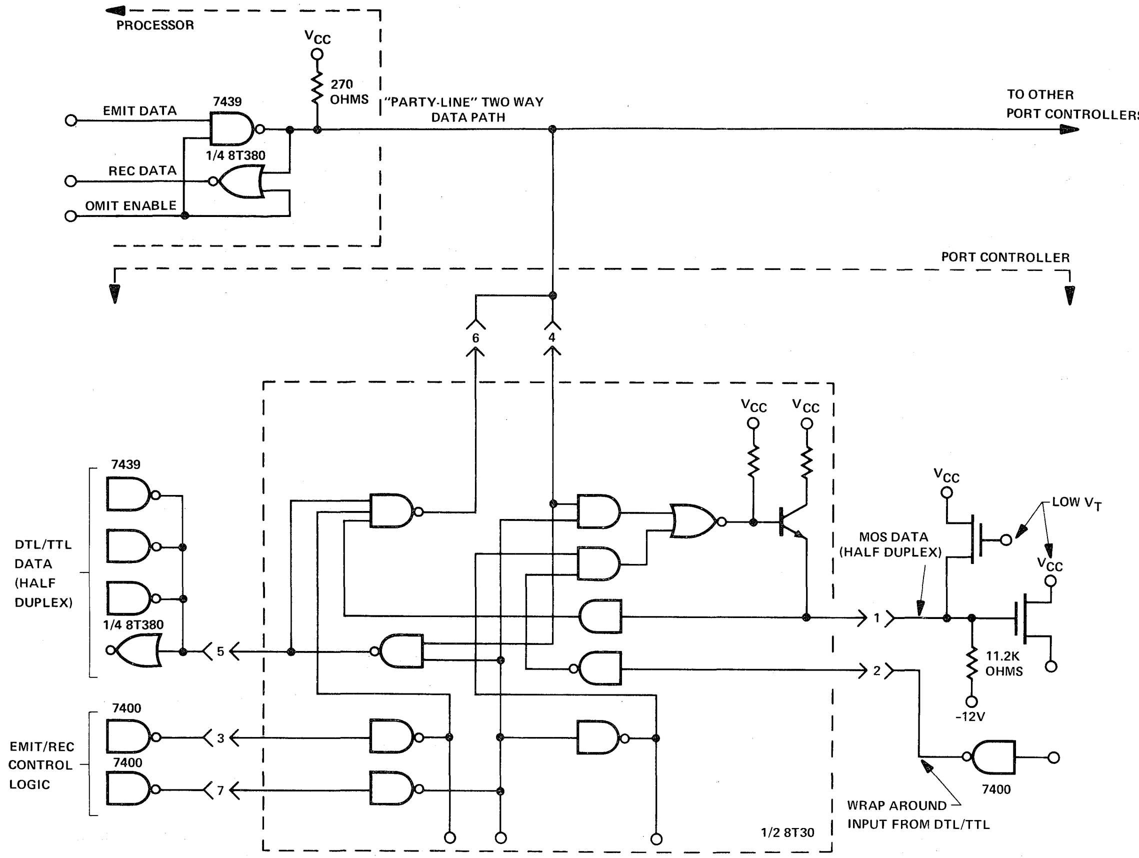


*C_F INCLUDES STRAY AND PROBE CAPACITANCE
**$t_{PW} \cong 0.5\ \mu SEC$, PRR ≅ 1 MHz, $R_{out} \cong 50$ OHMS

FIGURE 12

TYPICAL APPLICATION

PROCESSOR-PORT CONTROLLER INTERFACE FOR HALF-DUPLEX TTL/MOS DATA TRANSMISSION



VALID OPERATING MODES:

1. PROCESSOR TRANSMITTING TO PORT CONTROLLER
2. DTL/TTI HALF DUPLEX INPUT TRANSMITTING TO PROCESSOR
3. MOS HALF DUPLEX INPUT TRANSMITTING TO PROCESSOR
4. WRAP AROUND INPUT TRANSMITTING TO MOS OUTPUT
5. WRAP AROUND INPUT TRANSMITTING TO PROCESSOR
6. PORT CONTROLLER IDLE (NEITHER SENDING NOR RECEIVING) RANDOM ACTIVITY ON PINS 1, 2, 5 DOES NOT AFFECT TWO WAY "PARTY LINE" PATH

OBJECTIVE SPECIFICATION

8T31 N,F

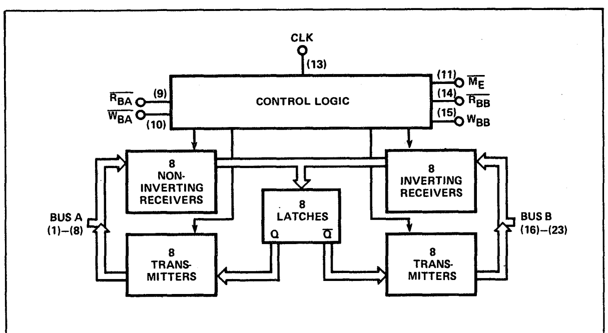
DESCRIPTION

The 8T31 8-bit Bidirectional I/O Port is designed to function as a general purpose I/O interface element in minicomputers, microcomputers and other bus oriented digital systems. It consists of 8 clocked latches with two sets of bidirectional inputs/outputs, Bus A (B_{A0}-B_{A7}) and Bus B (B_{B0}-B_{B7}). Each Bus has a write control line and a read control line. The two buses operate independently except for the case where the user is attempting to write data in from each bus simultaneously. In that case, the data on Bus A will be written into the latches while Bus B will be forced into a high impedance state. Data written into one Bus will appear inverted at the other Bus.

A master enable (M_E) is provided that enables or disables Bus B regardless of the state of the other inputs.

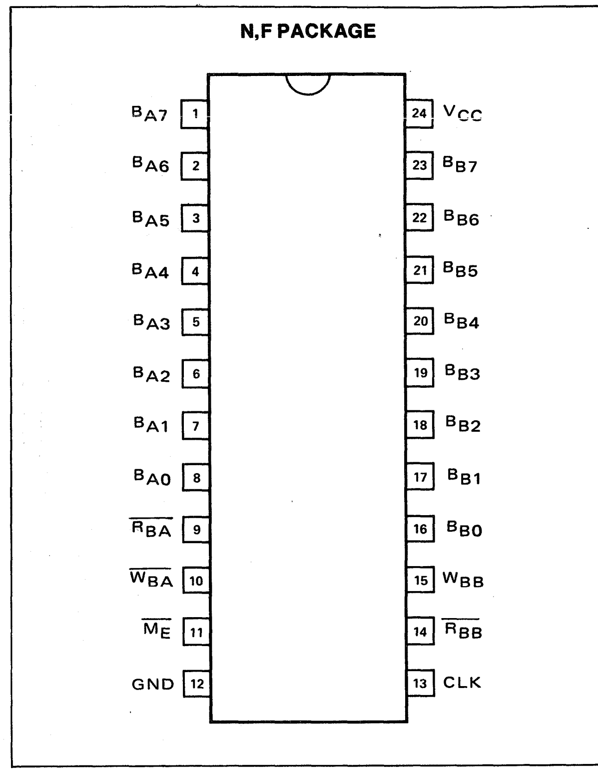
A unique feature of the 8T31 is its ability to start up in a predetermined state. If the clock is maintained at a voltage less than .8V until the power supply reaches 3.5V, Bus A will always be all logic 1 levels, while Bus B will be all logic 0 levels.

FUNCTIONAL BLOCK DIAGRAM



V_{CC} = (24)
GND = (12)
( ) DENOTES PIN NUMBERS

PIN CONFIGURATION



CONTROL FUNCTION TABLES

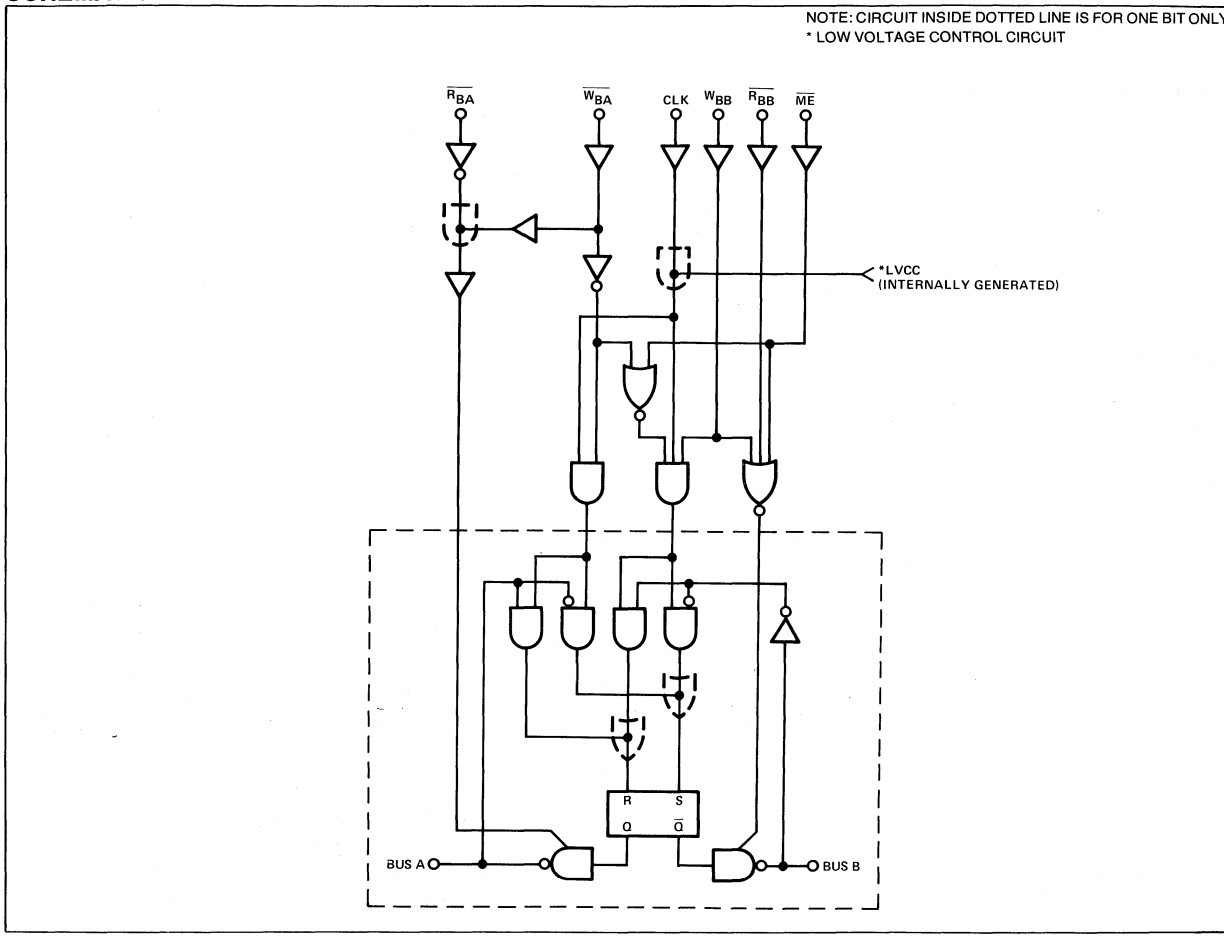
BUS A

$\overline{R_{BA}}$	$\overline{W_{BA}}$	CLK	BUS A
X	0	1	WRITE (INPUT)
0	1	X	READ (OUTPUT)
1	1	X	HI-Z

BUS B

$\overline{R_{BB}}$	W_{BB}	$\overline{W_{BA}}$	CLK	$\overline{ME}$	BUS B
X	X	X	X	1	HI-Z
1	0	X	X	0	HI-Z
X	1	0	X	0	HI-Z
0	0	X	X	0	READ (OUTPUT)
X	1	1	1	0	WRITE (INPUT)

SCHEMATIC

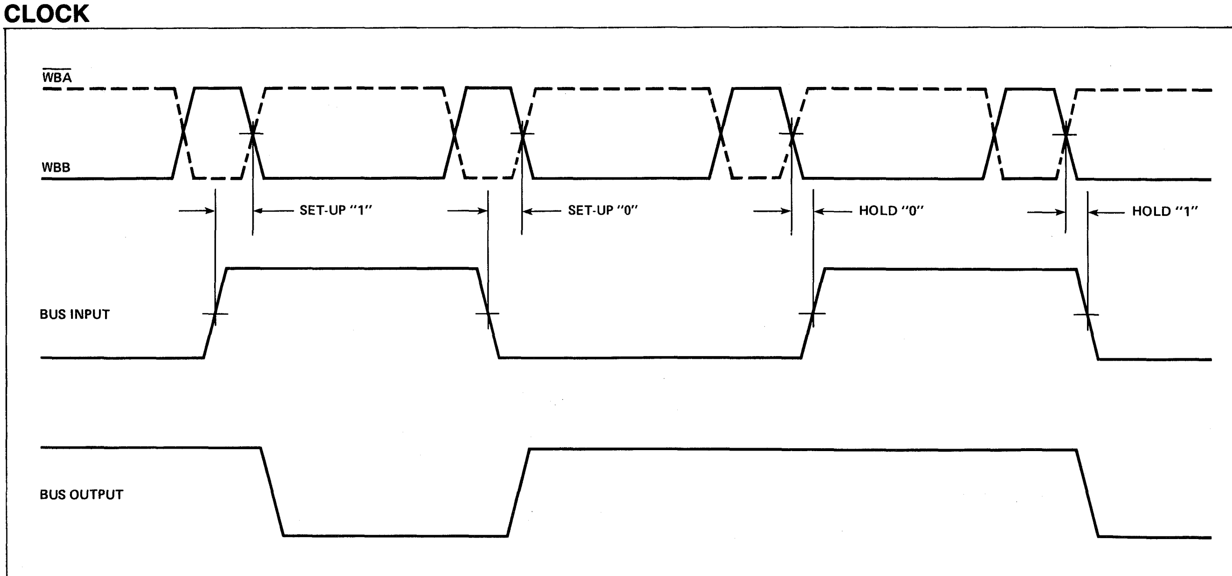

NOTE: CIRCUIT INSIDE DOTTED LINE IS FOR ONE BIT ONLY.
* LOW VOLTAGE CONTROL CIRCUIT
RBA
WBA
CLK
WBB
RBB
ME
*LVCC
(INTERNALLY GENERATED)
R
S
Q
Q
BUS A
BUS B

SWITCHING CHARACTERISTICS

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
t_{ZL}	Propagation Delay From Read (R_{BB}), Write (W_{BB}) and Master Enable (M_E) to Bus B	$C_L = 300pF$		27	45	ns
t_{ZH}		$C_L = 300pF$		29	50	ns
t_{ZL}		$C_L = 30pF$		17	30	ns
t_{ZH}		$C_L = 30pF$		14	25	ns
t_{LZ}		$C_L = 30pF$		13	20	ns
t_{HZ}		$C_L = 30pF$		17	30	ns
t_{SETUP}	Bus A Data Setup and Hold Times		0	−10		ns
t_{HOLD1}			10	4		ns
t_{HOLD0}			25	16		ns
t_{SETUP}	Bus A Write Setup and Hold Times		30	20		ns
t_{HOLD}			0	−30		ns
t_{SETUP}	Bus B Data Setup and Hold Times		*			ns
t_{HOLD}			0			ns
C_{IN}	Input Capacitances	$V_{IN} = 0V$			6	pF
	Control	$V_{IN} = 0V$			12	pF
	Data	$V_{IN} = 3V$			9	pF

* The Bus B Data Setup Time is equal to the clock pulse width.

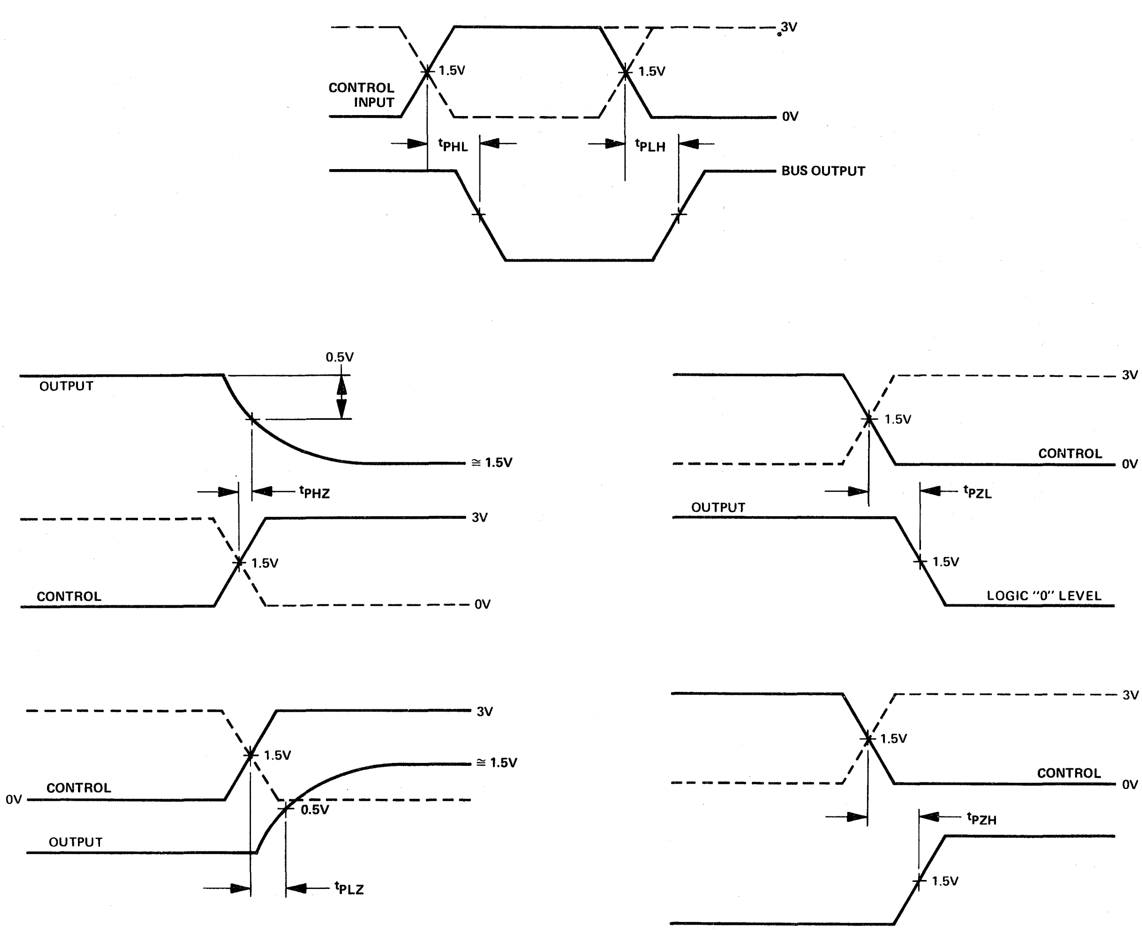
CLOCK



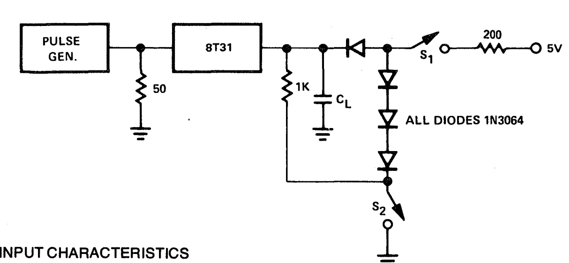
INTERFACE

AC WAVEFORMS

PROPAGATION DELAYS



AC TEST CIRCUIT



INPUT CHARACTERISTICS
PA = 3V, f = 1MHz $t_R = t_F$ = 2.5ns (10% to 90%)
C_L INCLUDES PROBE AND JIG CAPACITANCE

NOTE: ALL RESISTORS VALUES ARE TYPICAL AND IN OHMS.

TEST TABLE

	S_1	S_2
t_{PHL}	Closed	Closed
t_{PLH}	Closed	Closed
t_{PL}	Closed	Closed
t_{PHZ}	Closed	Closed
t_{PZL}	Closed	Open
t_{PZH}	Open	Closed

8T32-TM-STATE • 8T33-OPEN COLLECTOR

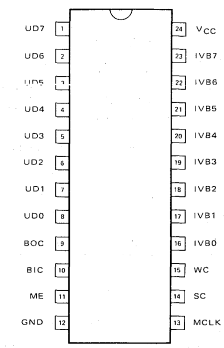
DESCRIPTION

The Interface Vector (IV) Byte is an 8-bit bi-directional data register designed to function as an I/O interface element in microprocessor systems. It contains eight clocked data latches accessible from either a microprocessor (IV) port or a user port. Separate I/O control is provided for each port. The two ports operate independently, except when both are attempting to input data into the IV Byte. In this case, the user port has priority.

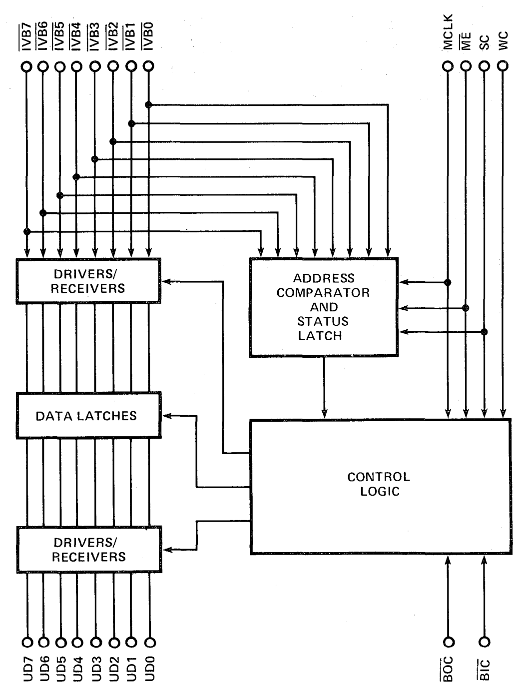
A unique feature of the IV Byte is the way in which it is addressed. Each IV Byte has an 8-bit, field programmable address, which is used to enable the microprocessor port. When the SC control signal is high, data at the microprocessor port is treated as an address. If the address matches the IV Byte's internally programmed address, the microprocessor port is enabled, allowing data transfer through it. The port remains enabled until an address which does not match is presented, at which time the port is disabled (data transfer is inhibited). A Master Enable input (ME) can serve as a ninth address bit, allowing 512 IV Bytes to be individually selected on a bus, without decoding. The user port is accessible at all times, independent of whether or not the microprocessor port is selected.

PIN CONFIGURATION

F,NA PACKAGE



BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION
USER DATA BUS CONTROL

The activity of the User Data Bus is controlled by the $\overline{\text{BIC}}$ and $\overline{\text{BOC}}$ inputs as shown in Table 1. (H represents high, L represents low.)

Table 1
BIC and BOC function Control

$\overline{\text{BIC}}$	$\overline{\text{BOC}}$	MCLK	USER DATA BUS
H	L	X	Output Data
L	X	H	Input Data
L	X	L	Inactive
H	H	X	Inactive

To avoid conflicts at the Data Latch, input from the microprocessor port is inhibited when $\overline{\text{BIC}}$ indicates user data is being input. Under all other conditions, the two ports operate independently.

INTERFACE VECTOR BUS CONTROL

As is shown in Table 2, the activity of the microprocessor port (IV Bus) is controlled by the $\overline{\text{ME}}$, SC, WC and $\overline{\text{BIC}}$ inputs, as well as the state of an internal status latch. $\overline{\text{BIC}}$ is included to show user port priority over the microprocessor port for data input.

TABLE 2
MICROPROCESSOR PORT FUNCTION CONTROL

$\overline{\text{ME}}$	SC	WC	MCLK	$\overline{\text{BIC}}$	Status Latch	IVBX Function
L	L	L	X	X	SET	Output Data
L	L	H	H	H	SET	Input Data
L	H	L	H	X	X	Input Address
L	H	H	H	L	X	Input Address
L	H	H	H	H	X	Input Data and Address
L	X	H	L	X	X	Inactive
L	H	X	L	X	X	Inactive
L	L	H	H	L	X	Inactive
L	L	X	X	X	not set	Inactive
H	X	X	X	X	X	Inactive

Each IV Byte's status latch stores the result of the most recent IV Byte select; it is set when the IV Byte's internal address matches the IV Bus. It is cleared when an address that differs from the internal address is presented on the IV Bus. In normal operation, the state of the status latch acts like a master enable; the microprocessor port can transfer data only when the status latch is set.

When SC and WC are both high, data on the IV Bus is accepted as data, whether or not the IV Byte was selected. The data is also interpreted as an address. The IV Byte sets its select status if its address matches the data read when SC and WC were both high; it resets its select status otherwise.

BUS OPERATION

Data written into the IV Byte from one port will appear inverted when read from the other port. Data written into the IV Byte from one port will not be inverted when read from the same port.

Figure 1 shows various ways to use the IV Byte in a system by controlling the states of the $\overline{\text{BIC}}$ and $\overline{\text{BOC}}$ lines. BYTE 1 is for input only, BYTE 2 is for output only, BYTE 3 is bidirectional under user control. BYTE 4 is output only (6 bits) with two bits reserved for system control of BYTE 5.

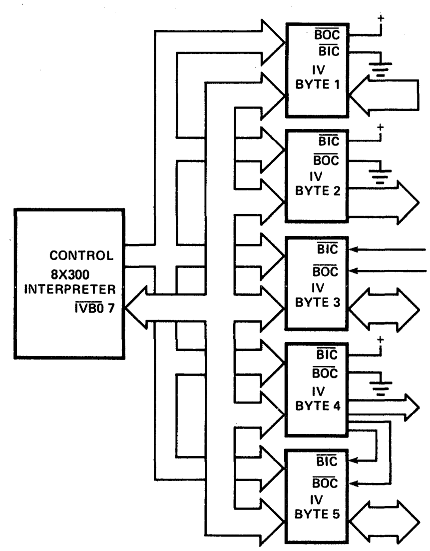
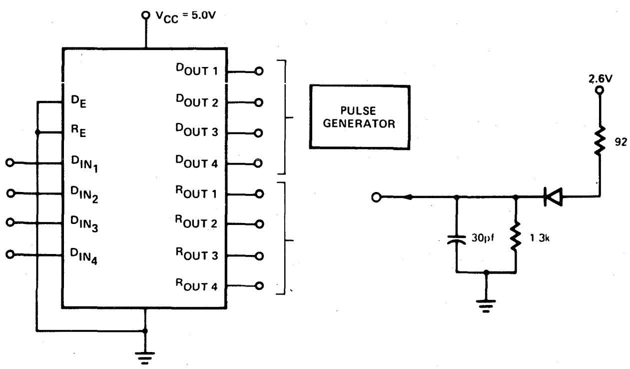
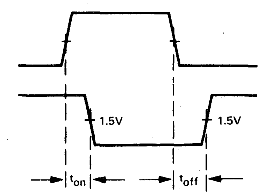


FIGURE 1
SOME IV BYTE CONFIGURATIONS

AC TEST CIRCUITS AND WAVEFORMS

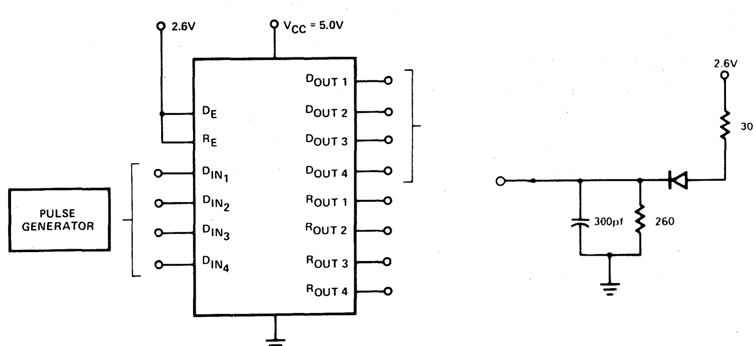
PROPAGATION DELAY (D_{OUT} TO R_{OUT})

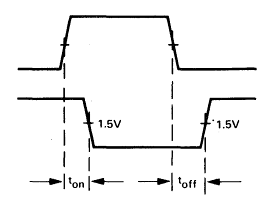




INPUT PULSE:
$t_r = t_f$ = 5ns (10% to 90%)
freq = 10MHz (50% duty cycle)
Amplitude = 2.6V

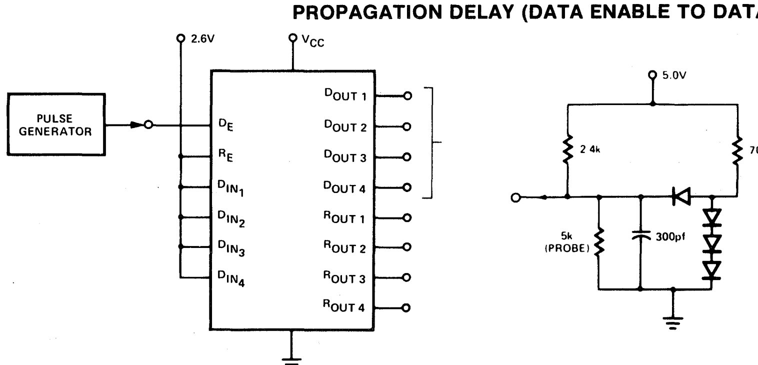
PROPAGATION DELAY (D_{IN} TO D_{OUT})

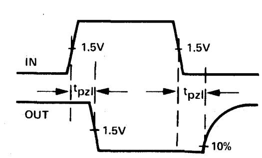




INPUT PULSE:
$t_r = t_f$ = 5ns (10% to 90%)
freq = 10MHz (50% duty cycle)
Amplitude = 2.6V

PROPAGATION DELAY (DATA ENABLE TO DATA OUTPUT)





INPUT PULSE:
$t_r = t_f$ = 5ns (10% to 90%)
freq = 5MHz (50% duty cycle)
Amplitude = 2.6V

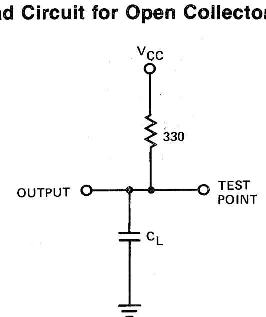
8T32-TM-STATE • 8T33-OPEN COLLECTOR

PIN DESCRIPTION

PIN	SYMBOL	NAME AND FUNCTION	TYPE
1-8	$\overline{UD0}$ — $\overline{UD7}$:	User Data I/O Lines. Bidirectional data lines to communicate with user's equipment. Either tri-state or open collector outputs are available.	ACTIVE HIGH
16-23	$\overline{IVB0}$ — IVB7:	Interface Vector Bus. Bidirectional tri-state data lines to communicate with controlling digital system (microprocessor).	ACTIVE LOW
10	$\overline{BIC}$:	Byte Input Control. User input to control writing into the IV Byte from the User Data Lines.	ACTIVE LOW
9	BOC:	Byte Output Control. User input to control reading from the IV Byte onto the User Data Lines.	ACTIVE LOW
14	SC:	Selected Command. When SC is high and WC is low, data on IVB0 — IVB7 is interpreted as an address. IV Byte selects itself if its address is identical to IV bus data; it de-selects itself otherwise.	ACTIVE HIGH
15	$\overline{WC}$:	Write Command. When WC is high and SC is low, IV Byte, if selected, stores contents of IVB0 — IVB7 as data.	ACTIVE HIGH
11	ME:	Master Enable. System input to enable or disable all other system inputs and outputs. It has no effect on user inputs and outputs.	ACTIVE LOW
13	MCLK:	Master Clock. Input to strobe data into the latches.	
24	VCC:	5 volt power connection.	
12	GND:	Ground.	

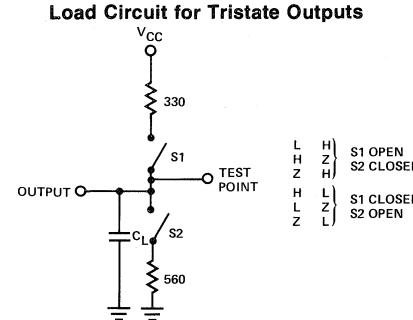
PARAMETER MEASUREMENT INFORMATION

Load Circuit for Open Collector Outputs



NOTE: ALL RESISTORS VALUES ARE TYPICAL AND IN OHMS.

Load Circuit for Tristate Outputs



NOTE: ALL RESISTORS VALUES ARE TYPICAL AND IN OHMS.

8T32-TM-STATE • 8T33-OPEN COLLECTOR

AC ELECTRICAL CHARACTERISTICS

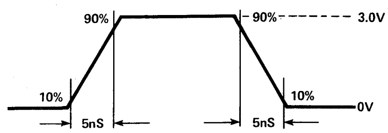
(Limits apply for V_{CC} = 5V ± 5% and 0° C ≤ T_A ≥ 70° C unless specified otherwise.)

Parameter	Symbol	Input	Output	Conditions	Limits Min.	Limits Typ.	Limits Max.	Units
User Data Delay (Note 1)	t_{PD}	UDX	$\overline{IVBX}$	C_L = 30pF		19		ns
		MCLK	$\overline{IVBX}$	C_L = 30pF		36		ns
User Output Enable	t_{OE}	$\overline{BIC}$	UDX	C_L= 30pF		26		ns
		$\overline{BOC}$	UDX	C_L = 30pF		28		ns
User Output Disable	t_{OD}	$\overline{BIC}$	UDX	C_L = 30pF		22		ns
		$\overline{BOC}$	UDX	C_L = 30pF		13		ns
IV Data Delay (Note 1)	t_{PD}	$\overline{IVBX}$	UDX	C_L = 30pF		32		ns
		MCLK	UDX	C_L = 30pF		40		ns
IV Output Enable	t_{OE}	$\overline{ME}$	$\overline{IVBX}$	C_L = 30pF		16		ns
		SC	$\overline{IVBX}$	C_L = 30pF		16		ns
		WC	$\overline{IVBX}$	C_L = 30pF		16		ns
IV Output Disable	t_{OD}	$\overline{ME}$	$\overline{IVBX}$	C_L = 30pF		15		ns
		SC	$\overline{IVBX}$	C_L = 30pF		15		ns
		WC	$\overline{IVBX}$	C_L = 30pF		15		ns
Clock Pulse Width	t_W	MCLK				20		ns
Setup Time (2)	t_{SETUP}	UDX				9		ns
		$\overline{BIC}$				22		ns
		$\overline{IVBX}$		(Note 5)		37		ns
		$\overline{ME}$		(Note 5)		23		ns
		SC		(Note 5)		23		ns
		WC		(Note 5)		12		ns
Hold Time (2)	t_{HOLD}	UDX		(Note 5)		16		ns
		$\overline{BIC}$		(Note 5)		3		ns
		$\overline{IVBX}$		(Note 5)		11		ns
		$\overline{ME}$		(Note 5)		0		ns
		SC		(Note 5)		0		ns
		WC		(Note 5)		4		ns

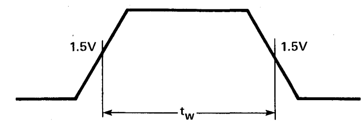
NOTES:
1. Data delays referenced to the clock are valid only if the input data is stable at the arrival of the clock and the hold time requirement is met.
2. Setup and hold times given are for "normal" operation. $\overline{BIC}$ setup and hold times are for a user write operation. SC setup and hold times are for an IV Byte select operation. WC setup and hold times are for an IV Bus write operation. ME setup and hold times are for both IV write and select operations.

8T32-TM-STATE • 8T33-OPEN COLLECTOR

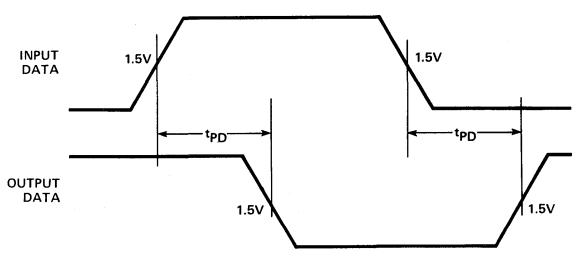
INPUT WAVEFORM



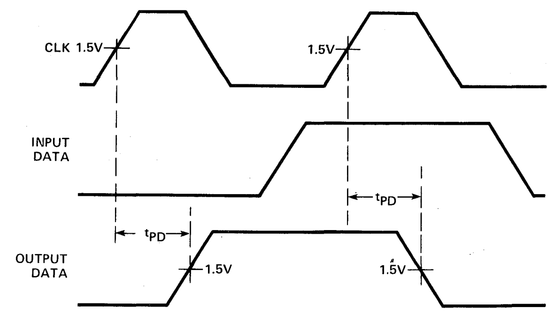
CLOCK PULSE WIDTH



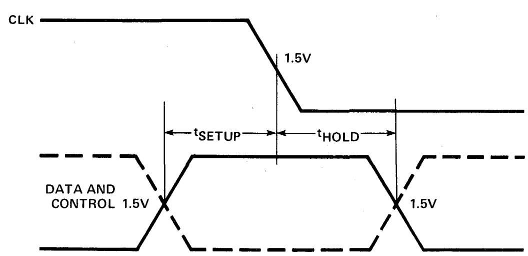
DATA DELAY TIMES
(INPUT DATA REFERENCED—CLK = '1')



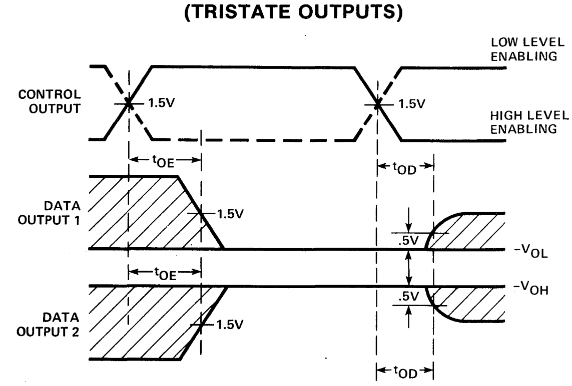
DATA DELAY TIMES
(CLOCK REFERENCED)



SETUP AND HOLD TIMES



OUTPUT ENABLE AND DISABLE TIMES
(TRISTATE OUTPUTS)



WAVEFORM #1 IS FOR AN OUTPUT WITH INTERNAL CONDITIONS SUCH THAT THE OUTPUT IS LOW WHEN THE TRI-STATE DRIVER IS ENABLED. WAVEFORM #2 IS FOR THE OPPOSITE CONDITION.

ADDRESS PROGRAMMING

The IV Byte is manufactured such that an address of all high-levels (> 2V) on the IV Data Bus inputs matches the Byte's internal address. To program a bit so a low-level input (< 0.8V) matches, the following procedure should be used:

1. Set all control inputs to their inactive state (BIC = BOC = ME = V_{CC}, SC = WC = MCLK = GND). Leave all IV Data Bus I/O pins open.
2. Raise V_{CC} to 7.75 V ± .25V.
3. After V_{CC} has stabilized, apply a programming pulse to the User Data Bus bit where a low-level match is desired. The voltage should be limited to 18V; the current should be limited to 75 mA. Apply the pulse as shown in Diagram 1.
4. Return V_{CC} to 0V (Note 6).

5. Repeat this procedure for each bit where a low-level match is desired.
6. Verify that the proper address is programmed by setting the Byte's status latch (IVB0 — IVB7 = desired address, ME = WC = L, SC = MCLK = H) and attempting to write through the IV Byte (BOC = SC = ME = L, BIC = WC = MCLK = H). If the proper address has been programmed, data presented at the IV Bus will appear inverted on the User Bus outputs. (Use normal V_{CC} and input voltages for verification.)

After the desired address has been programmed, a second procedure must be followed to isolate the address circuitry. The procedure is:

1. Set V_{CC} and all control inputs to 0V. (V_{CC} = BIC = BOC = ME = SC WC = MCLK = 0V). Leave all IV Data Bus I/O pins open.
2. Apply a protect programming pulse to every User Data Bus pin, one at a time. The voltage should be limited to 14V; the current should be limited to 150mA. Apply the pulse as shown in Diagram 2.
3. Verify that the address circuitry is isolated by applying 7V to each User Data Bus pin and measuring less than 1mA of input current. The conditions should be the same as in step 1 above. The rise time on the verification voltage must be slower than 100μs.

DIAGRAM 1
ADDRESS PROGRAMMING PULSE

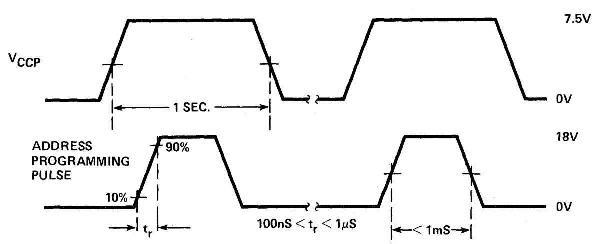
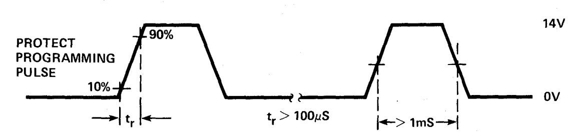


DIAGRAM 2
PROTECT PROGRAMMING PULSE



PROGRAMMING SPECIFICATIONS

Parameter	Symbol	Conditions	Limits Min.	Typ.	Max.	Units
Programming Supply Voltage	V_{CCP}					V
Address			7.5		8.0	V
Protect				0		V
Programming Supply Current	I_{CCP}	V_{CCP} = 8.0V			250	mA
MAX TIME $V_{CCP} > 5.25V$					1.0	sec.
Programming Voltage						
Address			17.5		18.0	V
Protect			13.5		14.0	V
Programming Current						
Address					75	mA
Protect					150	mA
Programming Pulse Rise Time						
Address			.1		1	μsec
Protect			100			μsec
Programming Pulse Width			.5		1	mS

NOTES:
6. If all programming can be done in less than 1 second, V_{CC} may remain at 7.75V for the entire programming cycle.

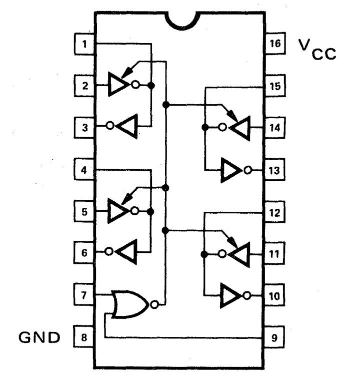
DESCRIPTION

The 8T34 is a quad transceiver with a common two input driver disable control. Tri-state driver outputs together with low input current requirements for the receivers offer extreme versatility in bus organized data transmission systems. The data busses may be terminated or unterminated.

Drivers in the third output state (Hi-Z) load the bus only with negligible current. The receiver input current is low, allowing at least 100 driver/receiver pairs to utilize a single bus. The receiver incorporates hysteresis to provide maximum noise immunity. In addition the receiver does not load the bus with V_{CC} = 0V as it may be the case when peripherals drive a common I/O bus and are shut off.

PIN CONFIGURATION

A PACKAGE



TRUTH TABLE

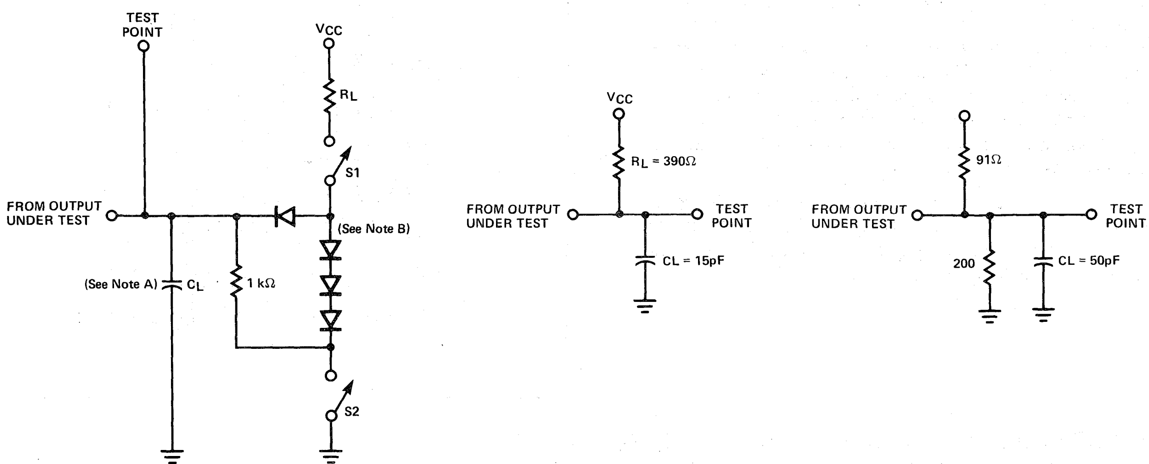
MODE	DISABLE	DISABLE	DRIVER	BUS	RECEIVER
	A	B	IN		OUT
RECEIVE	1	X	X	1	0
RECEIVE	X	1	X	0	1
DRIVE	0	0	1	0	1
DRIVE	0	0	0	1	0

ELECTRICAL CHARACTERISTICS (T_A = +25° C, V_{CC} = 5.0V)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{HZ}	Disable to Bus	Load 1, C_L = 15pF Waveform 4	8	15	30	ns
t_{LZ}	Disable to Bus	Load 1, C_L = 15pF Waveform 3	3	9	30	ns
t_{ZH}	Disable to Bus	Load 1, C_L = 50pF Waveform 3	5	10	30	ns
t_{ZL}	Disable to Bus	Load 1, C_L = 50pF Waveform 4	8	18	30	ns
t_{PHL}	Driver to Bus	Load 3	4	9	20	ns
t_{PLH}	Driver to Bus	Waveform 5	3	6	15	ns
t_{PHL}	Bus to Receiver	Load 2	5	14	25	ns
t_{PLH}	Bus to Receiver	Waveform 6	12	27	40	ns

SWITCHING PARAMETER MEASUREMENT INFORMATION

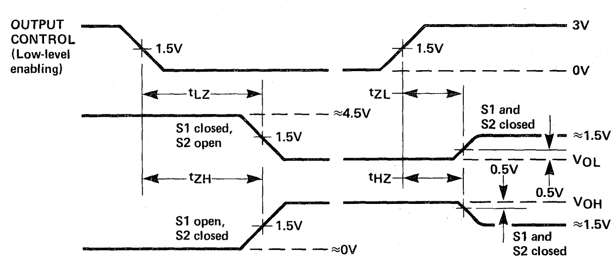
LOAD CIRCUIT FOR TRI-STATE OUTPUTS



LOAD 1 **LOAD 2** **LOAD 3**

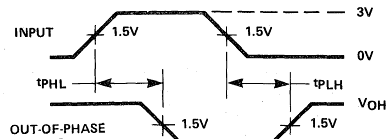
NOTES:
A. C_L includes probe and jig capacitance
B. Pin diodes are IN3064

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, TRI-STATE OUTPUTS

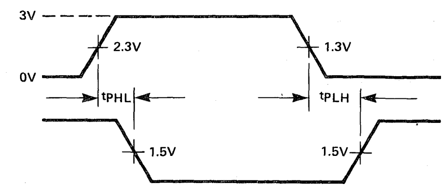


WAVEFORM 3 **WAVEFORM 4**

VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES



WAVEFORM 5



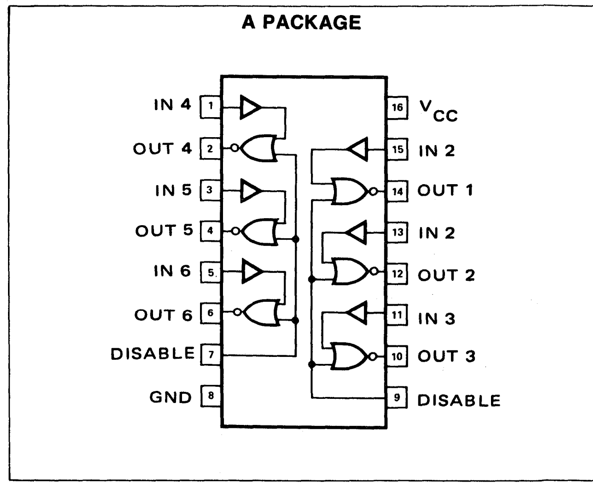
WAVEFORM 6

DESCRIPTION

The 8T37 is a hex bus receiver with hysteresis organized as two triple receivers with separate disable lines for each group. Typically the devices may be used in bus organized data transmission systems interconnected by terminated lines. The low input current requirement allows several drivers and receivers to communicate over a common bus in "party line" fashion. A power-up or power-down sequence of the receiver will not affect the bus. Built in hysteresis provides maximum noise immunity and makes the 8T37 also an ideal Schmitt trigger in those applications where the non-linear input characteristics of standard TTL are undesirable.

Low input current requirements make the hex-inverter inputs compatible with MOS/CMOS in addition to DTL/TTL. All inputs have clamping diodes to simplify systems design. The receiver outputs as well as the disable inputs are TTL/DTL compatible.

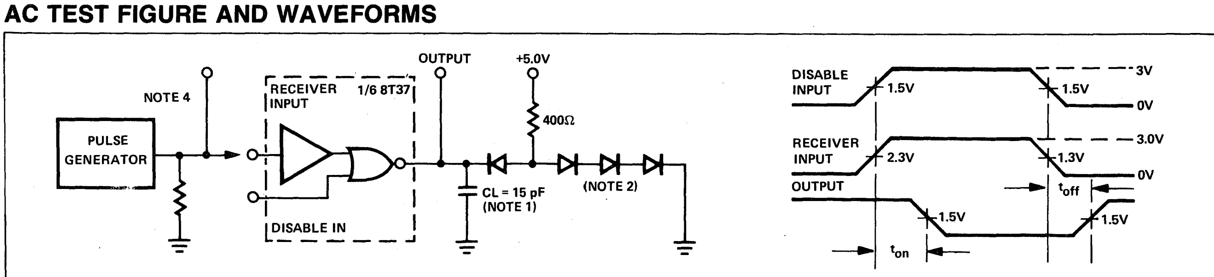
PIN CONFIGURATION



AC ELECTRICAL CHARACTERISTICS $T_A = 25°$ C, $V_{CC} = 5.0V$

PARAMETER	TEST CONDITIONS	LIMITS			UNIT
		MIN	TYP	MAX	
Propagation Delays (t_{on}, t_{off})					
Receiver t_{on}			10	30	ns
t_{off}	$R_L = 400\Omega$		20	30	ns
Disable t_{on}	$C_L = 15pF$		9	15	ns
t_{off}			11	15	ns

AC TEST FIGURE AND WAVEFORMS

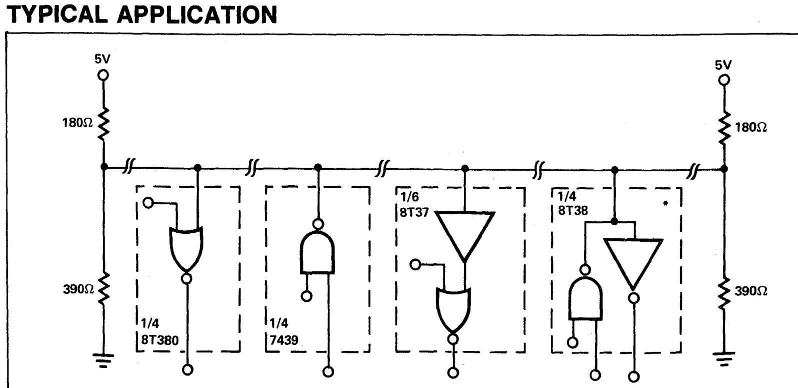


NOTES:
1. Including probe and jig capacitance
2. All diodes are 1N3064
3. Pulse generator characteristics P.A. = 3.5V
   $Z_{OUT} = 50\Omega$
   $P_{RR} = 1MH_z$
   $t_r = t_f \leq 10$ ns (10% to 90%)
   Duty Cycle = 50%
4. When testing receiver, Disable = 0; when testing disable, Receiver = 0.

* TO BE ANNOUNCED

EACH TERMINATOR IS 120 OHMS THE VENIN'S EQUIVALENT CIRCUIT. USING FLAT RIBBON A MAXIMUM REASONABLE LENGTH IS 50 FT. THE COMBINED LENGTH OF ALL TAPS OR STUBS SHOULD BE SUBTRACT. ED.

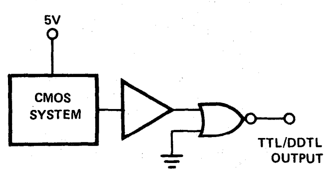
TYPICAL APPLICATION



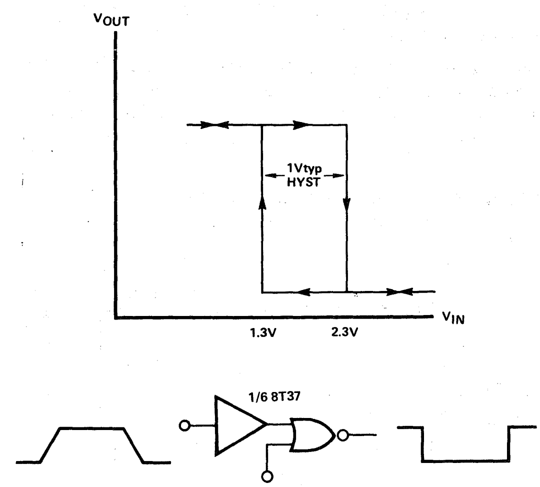
SCHMITT TRIGGER

The receiver transfer curve shown makes the 8T37 ideal in a variety of Schmitt Trigger and waveshaping applications.

C-MOS TO TTL INTERFACE



TRANSFER CURVE



OBJECTIVE SPECIFICATION 8T38A

OBJECTIVE SPECIFICATION DESCRIPTION

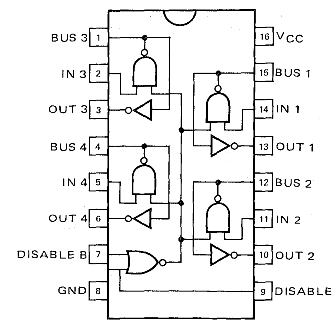
The 8T38 is a quad bus transceiver with a common two input disable control for the drivers. Open collector driver outputs together with low input requirements for the receivers offer extreme versatility in low cost bus organized systems.

Busses may be terminated at both ends such that up to 100 driver/receiver pairs can utilize a common data bus. The receiver incorporates hysteresis to provide maximum noise immunity. In addition the receiver does not load the bus when $V_{CC} = 0$.

In those applications where only bus receiver are required the 8T380 quad bus receiver should be considered.

PIN CONFIGURATION

A PACKAGE



TRUTH TABLE

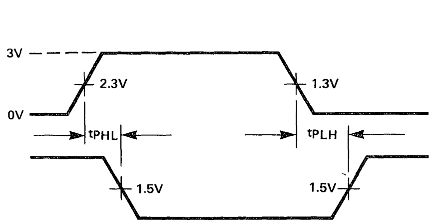
MODE	DISABLE	DISABLE	DRIVER	BUS	RECEIVER
	A	B	IN		OUT
RECEIVE	1	X	X	1	0
RECEIVE	X	1	X	0	1
DRIVE	0	0	1	0	1
DRIVE	0	0	0	1	0

AC ELECTRICAL CHARACTERISTICS ($T_A = +25°C$, $V_{CC} = 5.0V$)

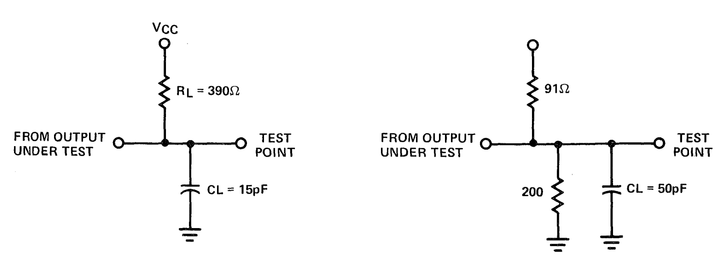
PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
t_{PHL}	Disable to Bus	Load 2 V_{in} = 0V to 3V	11	19	30	ns
t_{PLH}	Disable to Bus	Measured from V_{in} = 1.5V to Vbus = 1.5V	15	23	35	ns
t_{PHL}	Driver to Bus		5	12	20	ns
t_{PLH}	Driver to Bus		5	12	25	ns
t_{PHL}	Bus to Receiver		5	14	25	ns
		Load 1 Waveform 1				
t_{PLH}	Bus to Receiver		12	27	40	ns

SWITCHING PARAMETER MEASUREMENT INFORMATION

WAVEFORM 1



LOAD CIRCUITS



LOAD 1 LOAD 2

8T80 A,F,W

DESCRIPTION

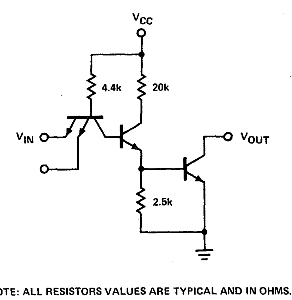
The 8T80 quad 2-input NAND interface gate and the 8T90 Hex inverter interface buffer are level translators that adapt standard 5V DTL/TTL logic to voltage levels of up to 30V.

The 8T80 performs the NAND function for positive logic (high level = logic "1") and the 8T90 performs the inverting function.

The output structure of the 8T80/90 is a high voltage transistor with uncommitted collector which allows logic swings up to 30 volts. The "bare" collector is useful for collector logic or wired-and connections.

Applications include TTL to MOS interface, lamp and relay driving as well as high level logic interfaces.

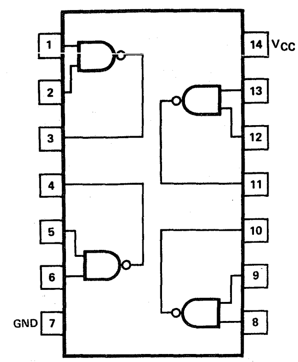
CIRCUIT SCHEMATIC



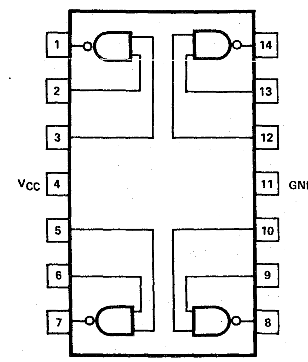
NOTE: COMPONENT VALUES ARE TYPICAL.

PIN CONFIGURATIONS

A,F PACKAGE



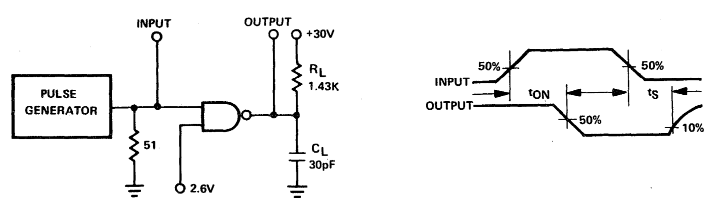
W PACKAGE



AC CHARACTERISTICS $T_A = 25° C$, $V_{CC} = 5.0V$

PARAMETER	TEST CONDITIONS	LIMITS			UNIT
		MIN	TYP	MAX	
Turn-on Delay	$R_L = 1.43K$		35	55	ns
Storage Time	$C_L = 30pF$		40	95	ns

AC TEST AND WAVEFORMS



INPUT PULSE: AMPLITUDE = 3.6V, P.W. = 1μsec, $t_r = t_f = 10nsec$.

QUAD 2-INPUT NAND INTERFACE GATE
HEX INVERTER INTERFACE ELEMENT

8T90

8T90 A,F,W

DESCRIPTION

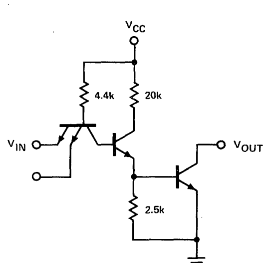
The 8T80 quad 2-input NAND interface gate and the 8T90 Hex inverter interface buffer are level translators that adapt standard 5V DTL/TTL logic to voltage levels of up to 30V.

The 8T80 performs the NAND function for positive logic (high level = logic "1" and the 8T90 performs the inverting function.

The output structure of the 8T80/90 is a high voltage transistor with uncommitted collector which allows logic swings up to 30 volts. The "bare" collector is useful for collector logic or wired-and connections.

Applications include TTL to MOS interface, lamp and relay driving as well as high level logic interfaces.

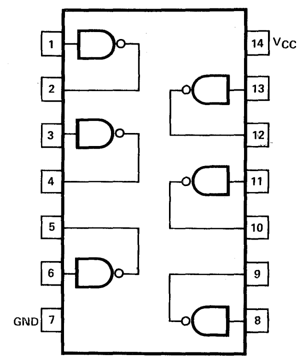
CIRCUIT SCHEMATIC



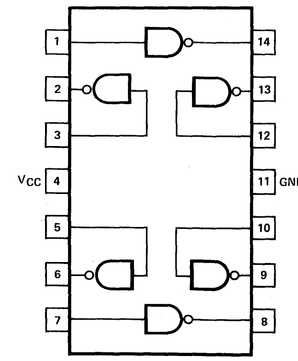
NOTE: COMPONENT VALUES ARE TYPICAL.

PIN CONFIGURATIONS

A,F PACKAGE



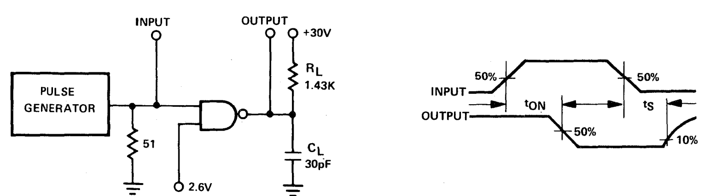
W PACKAGE



AC CHARACTERISTICS $T_A = 25°$ C, $V_{CC} = 5.0V$

CHARACTERISTIC	LIMITS MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
Turn-on Delay		35	55	ns	$R_L = 1.43K$
Storage Time		40	95	ns	$C_L = 30pF$

AC TEST FIGURE AND WAVEFORMS

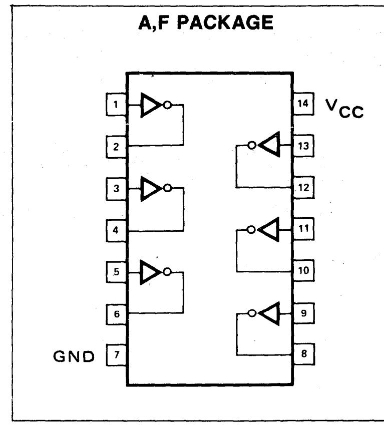


INPUT PULSE: AMPLITUDE = 3.6V, P.W. = 1μsec, $t_f = t_f$ = 10nsec.

OBJECTIVE SPECIFICATION DESCRIPTION

The 8T93 Hex Inverter interface elements have been designed with Schottky TTL technology. This makes it possible to combine ultra-high speed with a low current PNP input structure. Because of its low input current requirements the 8T93 is ideal in applications such as bus receivers, low power TTL interfaces as well as MOS and C-MOS to TTL buffers. The 8T93 has active pullups.

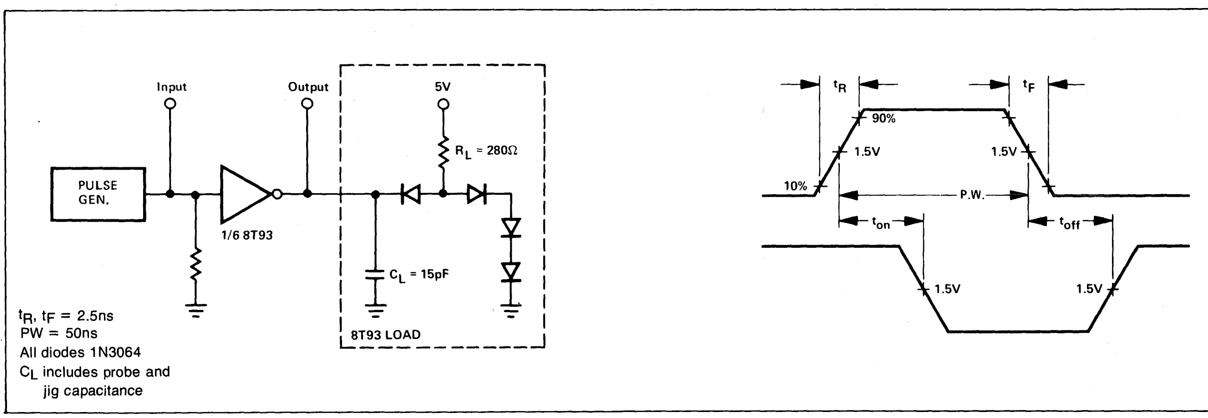
PIN CONFIGURATION



AC ELECTRICAL CHARACTERISTICS $T_A = 25° C$, $V_{CC} = 5V$

PARAMETER	TEST CONDITIONS	LIMITS			UNIT
		MIN	TYP	MAX	
Propagation Delay t_{on}, t_{off}	$R_L = 280$ $C_L = 15$ pF		5		ns

AC TEST FIGURE AND WAVEFORMS

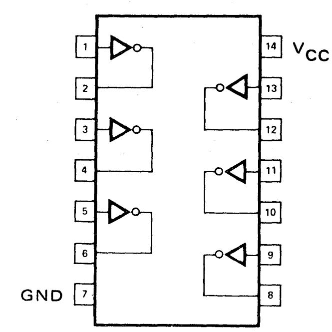


8T94 A,F

OBJECTIVE SPECIFICATION DESCRIPTION

The 8T94 Hex Inverter interface elements have been designed with Schottky TTL technology. This makes it possible to combine ultra-high speed with a low current PNP input structure. Because of its low input current requirements the 8T94 is ideal in applications such as bus receivers, low power TTL interfaces as well as MOS and C-MOS to TTL buffers.

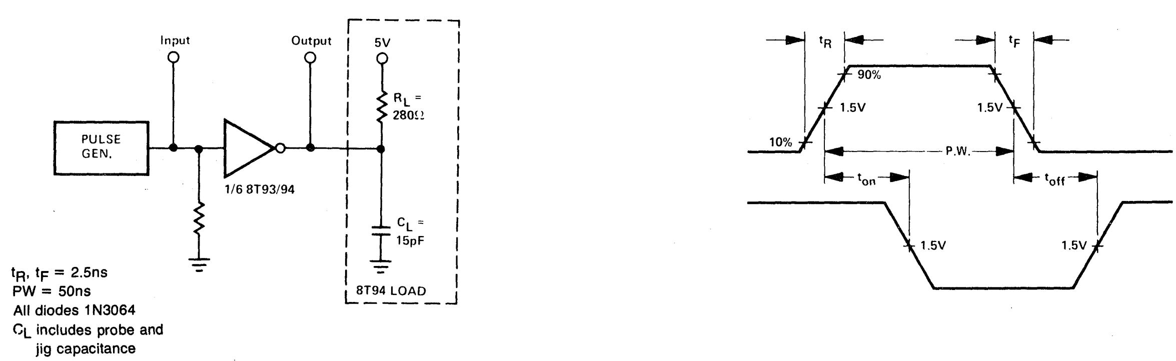
PIN CONFIGURATION



AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_{CC} = 5V$

PARAMETER	TEST CONDITIONS	LIMITS			UNITS
		MIN	TYP	MAX	
Propagation Delay t_{on}, t_{off}	$R_L = 280$ $C_L = 15$ pF		6		ns

AC TEST FIGURE AND WAVEFORMS



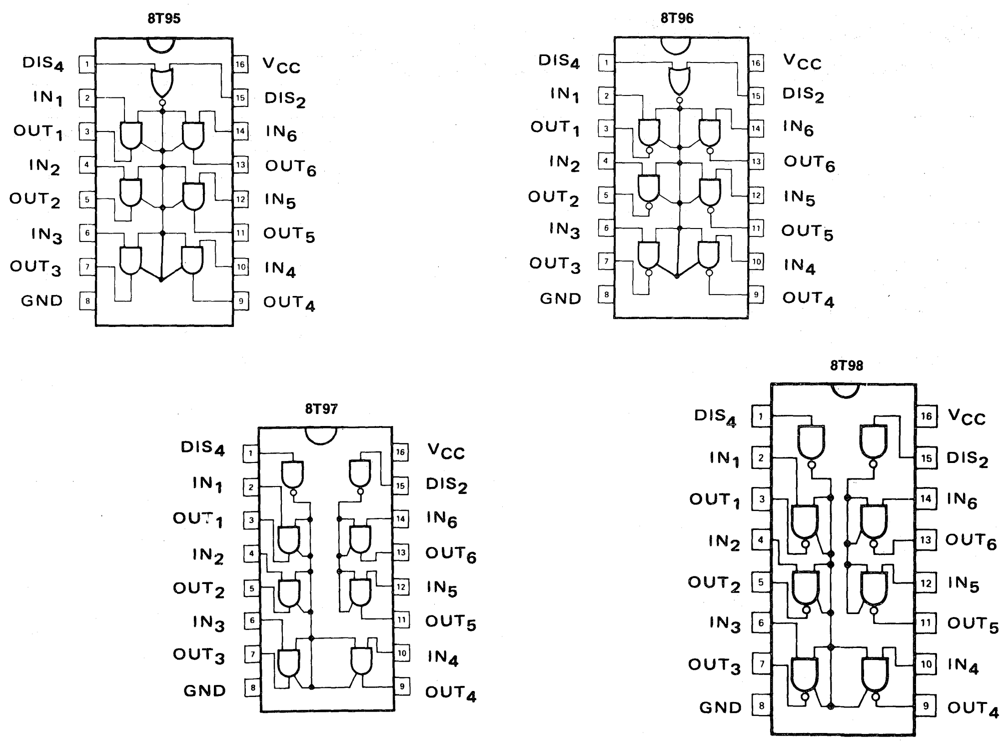
8T95 B,F • 8T96 B,F • 8T97 B,F • 8T98 B,F

DESCRIPTION

Each of the Tri-State Bus Interface Elements described herein has low current PNP inputs and is designed with Schottky TTL technology for ultra high speed. The devices are used to convert TTL/DTL or MOS/CMOS to tri-state TTL Bus levels. For maximum systems flexibility the 8T95 and 8T97 do so without logic inversion, whereas, the 8T96 and 8T98 provide the logical complement of the input. The 8T95 and 8T96 feature a common control line for all six devices, whereas, the 8T97 and 8T98 have control lines for four devices from one input and two from another input.

PIN CONFIGURATIONS

B,F PACKAGE



TRUTH TABLES

8T95			
DISABLE DIS1	INPUT DIS2	INPUT	OUTPUT
0	0	0	0
0	0	1	1
0	1	x	H-z
1	0	x	H-z
1	1	x	H-z

8T96			
DISABLE DIS1	INPUT DIS2	INPUT	OUTPUT
0	0	0	1
0	0	1	0
0	1	x	H-z
1	0	x	H-z
1	1	x	H-z

TRUTH TABLES (Cont'd)

8T97

DISABLE DIS_4	INPUT DIS_2	INPUT	OUTPUT
0	0	0	0
0	0	1	1
x	1	x	H-z*
1	x	x	H-z**

8T98

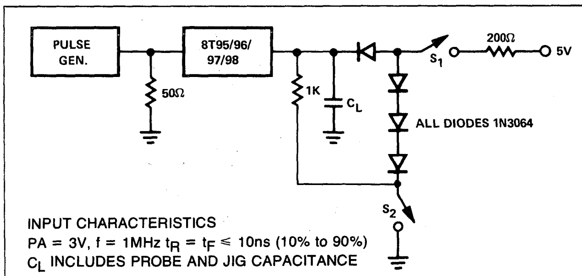
DISABLE DIS_4	INPUT DIS_2	INPUT	OUTPUT
0	0	0	1
0	0	1	0
x	1	x	H-z*
1	x	x	H-z**

* Output 5-6 only ** Output 1-4 only x = Irrelevant

AC ELECTRICAL CHARACTERISTICS T_A = 25° C and V_{CC} = 5.0V

	PARAMETER	TEST CONDITIONS	MIN 95/97	MIN 96/98	TYP 95/97	TYP 96/98	MAX 95/97	MAX 96/98	UNITS
	Propagation Delays (All Devices)								
t_{on}	Data Inputs to	See AC Test Figures	3	3	9	6	13	10	ns
t_{off}	Data Outputs		3	4	7	7	12	11	ns
	Disable to Outputs								
t_{PIH}	Logic "1" to High Z		3	3	5	6	10	10	ns
t_{POH}	Logic "0" to High Z		3	5	6	10	12	16	ns
t_{PHI}	High Z to Logic "1"		8	7	19	15	25	22	ns
t_{PHO}	High Z to Logic "0"		12	11	14	18	25	24	ns

AC TEST CIRCUIT

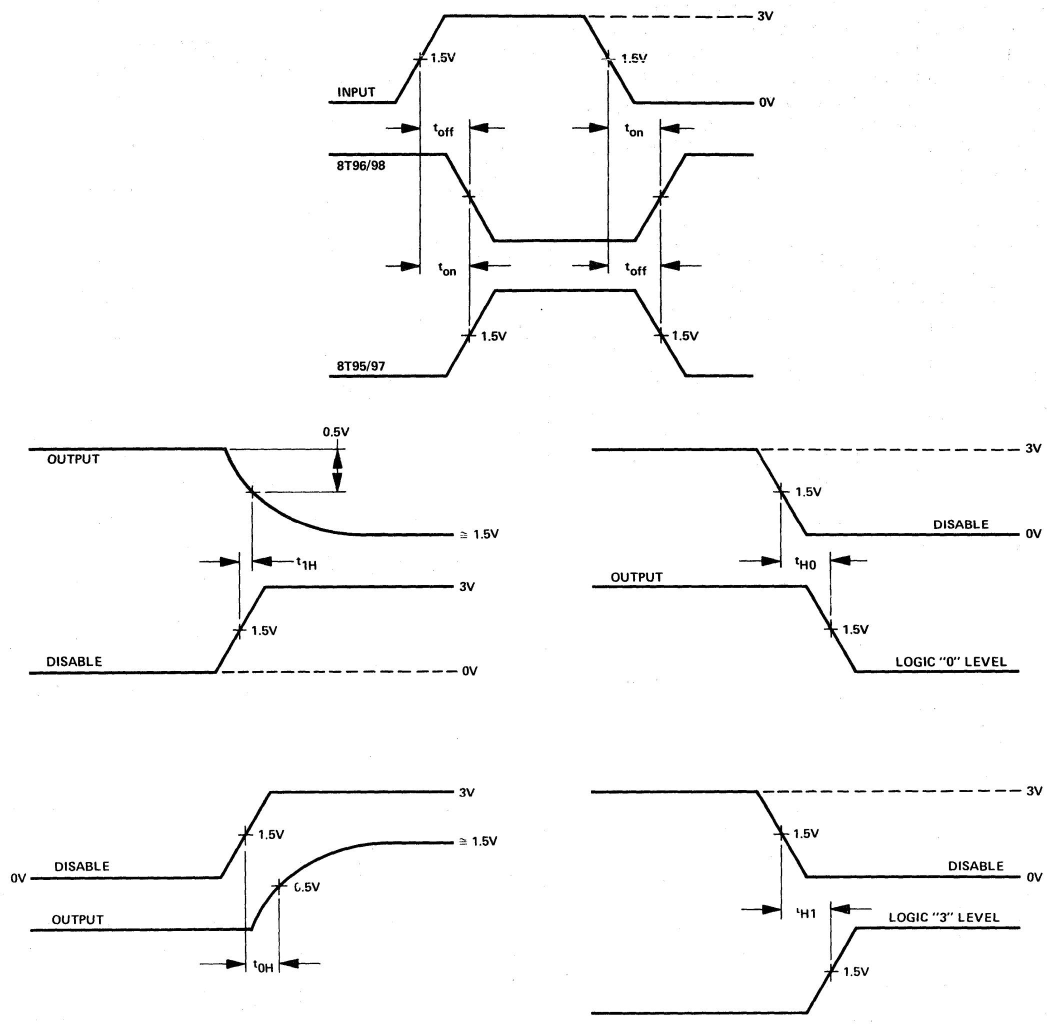


INPUT CHARACTERISTICS
PA = 3V, f = 1MHz $t_R = t_F \leq$ 10ns (10% to 90%)
C_L INCLUDES PROBE AND JIG CAPACITANCE

TRUTH TABLE

	S_1	S_2	C_L
t_{on}	Closed	Closed	50pF
t_{off}	Closed	Closed	50pF
t_{0H}	Closed	Closed	5pF
t_{1H}	Closed	Closed	5pF
t_{H0}	Closed	Open	50pF
t_{H1}	Open	Closed	50pF

PROPAGATION DELAYS



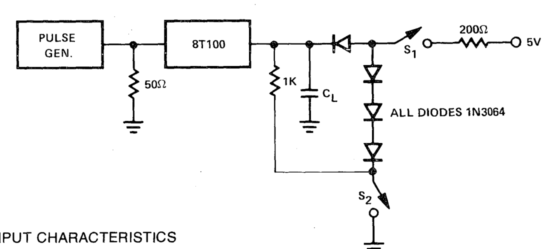
DESCRIPTION

The 8T100/101 are universal differential line drivers with tri-state outputs. The various operating modes of the drivers are controlled by 2 control lines. By proper controlling these control lines, the driver can be made to operate in single ended or multiplexed configuration. The tri-state capability allows disabled drivers to stay on the line in a multiplexed system without loading the line. The differential feature, when used with suitable line receiver eliminates troublesome ground loops and common mode noise associated with single wire transmission. 8T101 provides clamp diodes from output to V_{CC} on all drivers.

TRUTH TABLE

Operating Mode	A	B	Data In	Q Out	Q Out
Driver On	0	0	0	1 (Source) 0 (Sink)	0 (Sink) 1 (Source)
Driver Off (3-4-State)	1	1	0 1	Hi-Z Hi-Z	Hi-Z Hi-Z
Party-Line	0	1	0 1	Hi-Z 0 (Sink)	Hi-Z 1 (Source)
Party-Line	1	0	0 1	1 (Source) Hi-Z	0 (Sink) Hi-Z

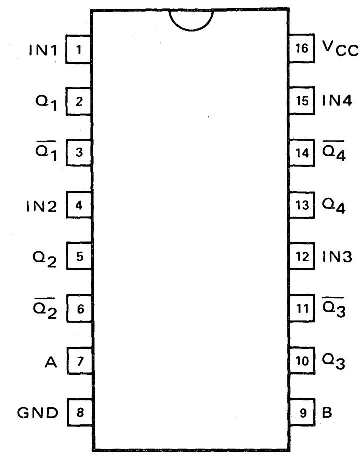
AC TEST CIRCUIT



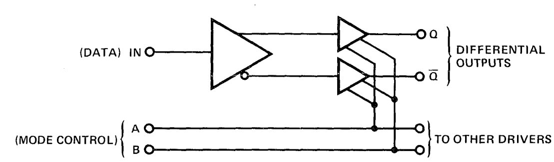
INPUT CHARACTERISTICS
PA = 3V, f = 1MHz $t_R = t_F \leq$ 10ns (10% to 90%)
C_L INCLUDES PROBE AND JIG CAPACITANCE

PIN CONFIGURATION

PACKAGE

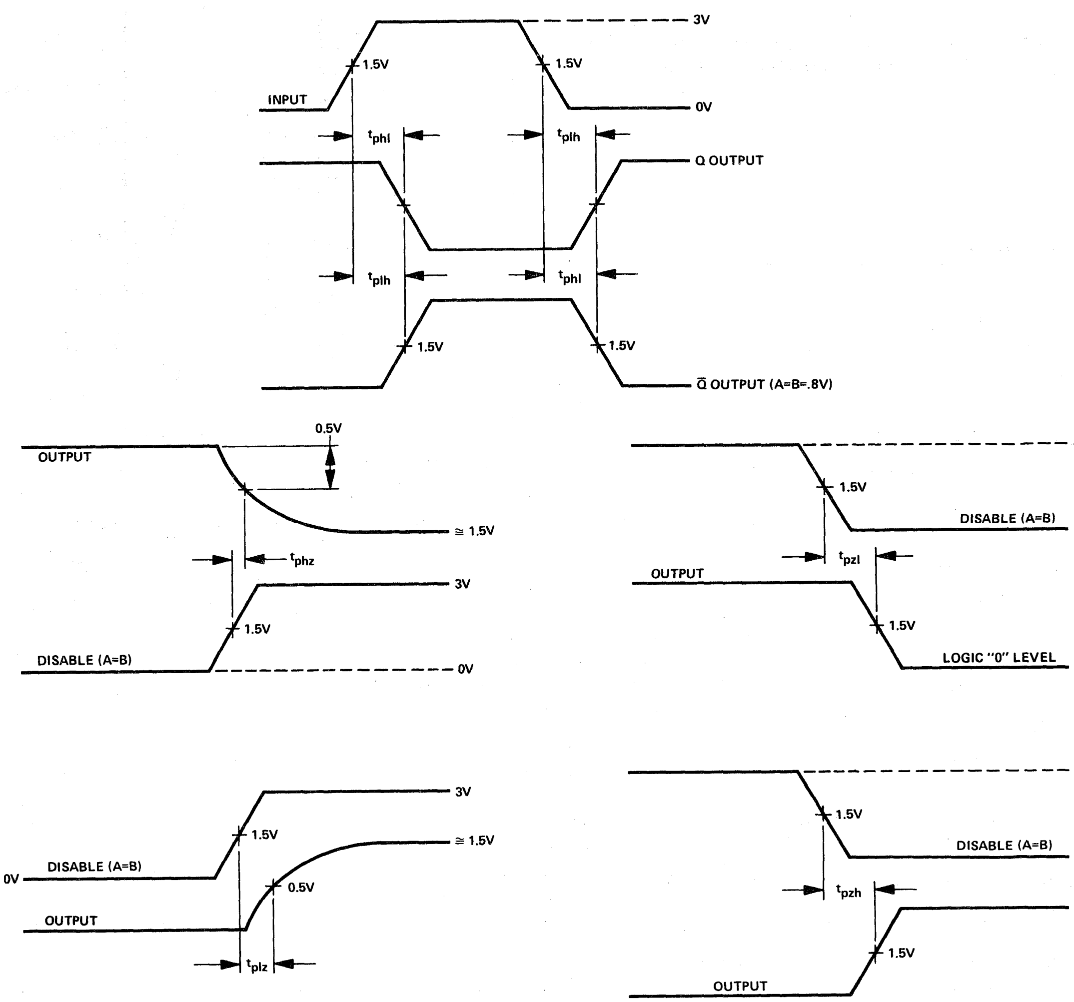


LOGIC DIAGRAM



AC TEST TABLE

	S_1	S_2	C_L
t_{PHL}	Closed	Closed	300pF
t_{PLH}	Closed	Closed	300pF
t_{PLZ}	Closed	Closed	5pF
t_{PHZ}	Closed	Closed	5pF
t_{PZL}	Closed	Open	300pF
t_{PZH}	Open	Closed	300pF


3V
1.5V
1.5V
INPUT
0V
t_{phl}
t_{plh}
Q OUTPUT
t_{plh}
t_{phl}
1.5V
1.5V
$\bar{Q}$ OUTPUT (A=B=.8V)
0.5V
OUTPUT
≅ 1.5V
t_{phz}
3V
1.5V
DISABLE (A=B)
0V
3V
1.5V
DISABLE (A=B)
0V
t_{pzl}
OUTPUT
1.5V
LOGIC "0" LEVEL
3V
1.5V
≅ 1.5V
0V
DISABLE (A=B)
0.5V
OUTPUT
t_{plz}
3V
1.5V
DISABLE (A=B)
0V
t_{pzh}
1.5V
OUTPUT

INTERFACE

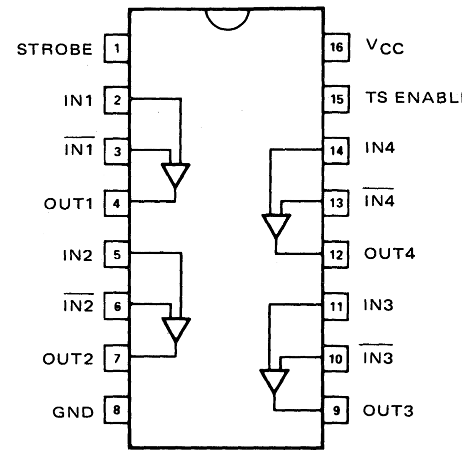
8T110 F • 8T111 F

DESCRIPTION

These devices are intended to receive differential input signals and convert them to TTL levels. A common strobe and a common output enable lines are provided for all receivers. Common mode rejection range of ±15V is provided to assure that the ground shift or ground noise between the transmitter and receiver will not affect the data. 8T111 also provides termination resistors.

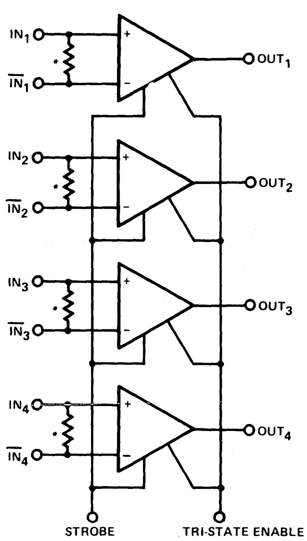
PIN CONFIGURATION

F PACKAGE*



* Output non-inverting.

LOGIC DIAGRAM



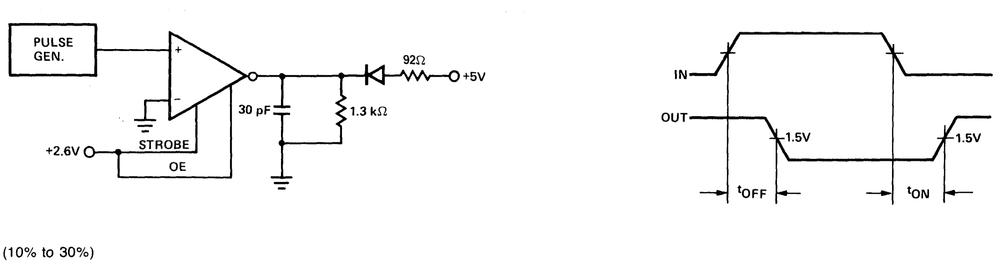
* 8T111 OPTION INTERNALLY CONNECTED $130\Omega \leq R_{IN} \leq 170\Omega$

SWITCHING CHARACTERISTICS $V_{CC} = 5.0V$, $T_A = 25°C$

PARAMETER UNIT	TEST CONDITIONS	LIMITS MIN	TYP	MAX	UNIT
Differential Input to Low Level Output	$V_{CC} = 5V$			30	ns
Differential Input to High Level Output				24	ns
Strobe Input to Low Level Output				16	ns
Strobe Input to High Level Output				18	ns
Output Enable to Outputs:					
High Level to Hi-Z				16	ns
Low Level to Hi-Z				18	ns
Hi-Z to Low Level				23	ns
Hi-Z to High Level				21	ns
Inverting Input Resistance		10.5		15	KΩ
Non-Inverting Input Resistance		5.5		7.75	KΩ

AC TEST CIRCUITS AND WAVEFORMS

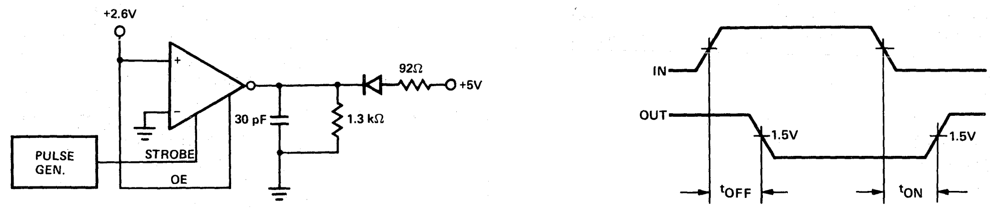
PROPAGATION DELAY (INPUT TO OUTPUT)



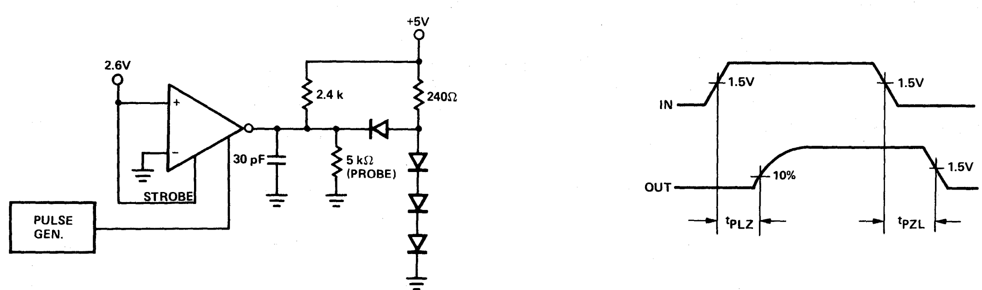
$t_r = t_f$ = 2.5ns (10% to 30%)
Frequency = 10 MHz (50% duty cycle)
Amplitude = 2.6V

AC TEST CIRCUIT AND WAVEFORMS (Cont'd)

PROPAGATION DELAY (STROBE TO OUTPUT)



OUTPUT ENABLE TO OUTPUT



INTERFACE

DESCRIPTION

The 8T363 Dual Zero Crossing Detector is an interface circuit incorporating a differential amplifier input and logic gate output. The input amplifier is referenced to zero volts and employs temperature compensation to ensure stable thresholds. The output structure of the 8T363 is compatible with DTL and TTL circuits.

APPLICATIONS

Zero-Crossing Detector
High Stability One-Shot
Bi-Directional One-Shot
Frequency Doubler
Stable-Low Frequency Oscillator
Linear Amplifier
Frequency to Voltage Converter

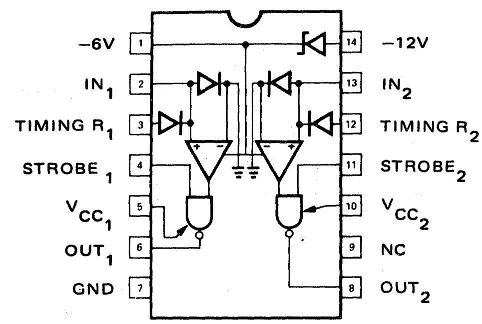
ABSOLUTE MAXIMUM RATINGS

Input Voltage	+7.0V
Output Voltage	+6.0V
V_{CC}	+6.0V
Input Current	± 10mA
Output Current	+30, −10mA
Storage Temperature	−65° C to +175° C
Operating Temperature	0° C to +75° C
V —	−7V or −13.5V

Maximum ratings are limiting values above which serviceability may be impaired.

PIN CONFIGURATION

A PACKAGE

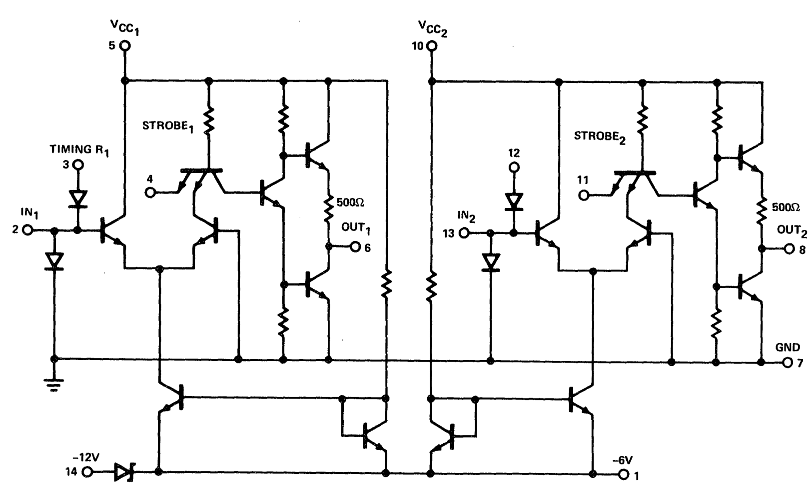


NC = no connection

AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_{CC} = 5.0V$, $V^- = -6V$

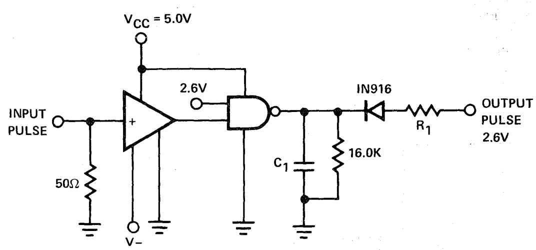
PARAMETER	TEST CONDITIONS	MAX	UNITS
Turn on Delay Detector Strobe to Output	See Test Figure 1, T_A = 25°C See Test Figure 2, V signal = V_{CC} through 10KΩ resistor, T_A = 25°C	85 50	ns ns
Turn off Delay Detector Strobe to Output	See Test Figure 1, T_A = 25°C See Test Figure 2, V signal = V_{CC} through 10KΩ resistor, T_A = 25°C	65 50	ns ns
Input Voltage (Timing R V_F Diode) Uncertainty Region-Signal Icc/Detector I_{EE}	$V_7 = V_2 = V_{13}$, I_3 = 1mA, I_{12} = 1mA $V_7 = V_3 = V_{12}$, Note 9, T_A = 25°C	1 ±30 6.5 −13.0	V mV mA mA

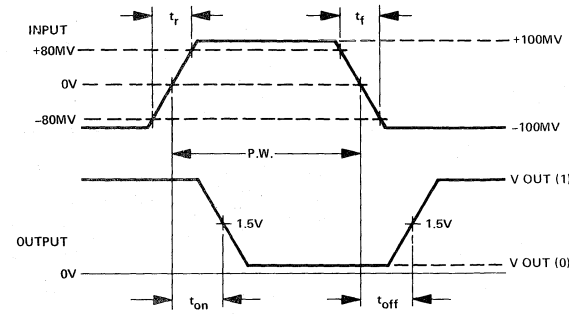
CIRCUIT SCHEMATIC



NOTE
Pins 5, 6, 8, and 10 are tied to pin 14 through isolation diodes.

FIGURE 1 — t_{on}, t_{off} DETECTOR INPUTS

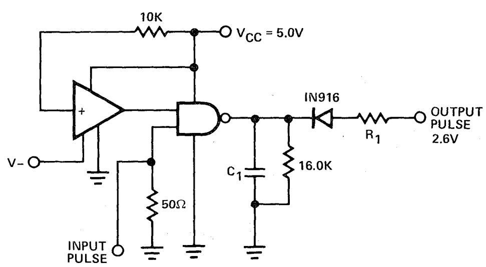


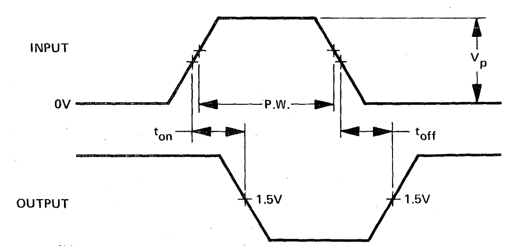


t_{on}	t_{off}
C_1 = 27pF	18pF
R_1 = 210Ω	1.91kΩ

Input Pulse: Vin
Pulse Width = 350ns at 50% Points
tr = tf = 10ns
Amplitude = ±100mV

FIGURE 2 — t_{on}, t_{off} STROBE TO OUTPUT



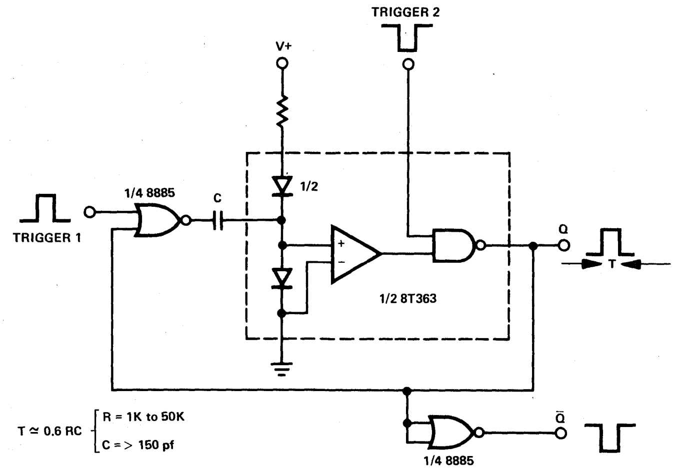


t_{on}	t_{off}
C_1 = 27pF	18pF
R_1 = 210Ω	1.91kΩ

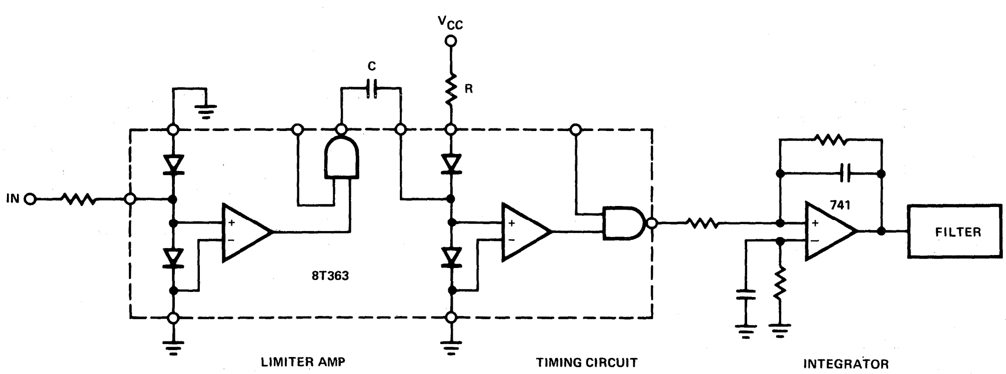
Input Pulse: Vin
Pulse width = 200ns at 50% Points
tr = tf (10%-90%) = 10ns
Amplitude Vp = 4.0V

TYPICAL APPLICATIONS

MONOSTABLE MULTIVIBRATOR



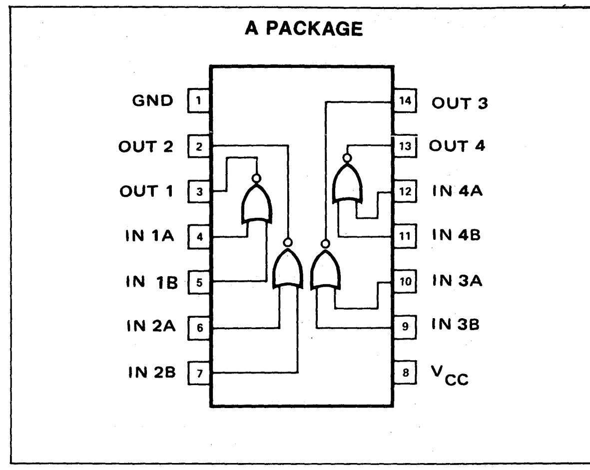
FREQUENCY TO VOLTAGE CONVERTER



Sine wave inputs up to approximately 500 kHz are limited, amplified and used to trigger the timing circuit. The timing circuit output is a constant pulse width (pw≈0.6RC). The constant width pulses are integrated and then filtered to attenuate the remaining high frequency carrier components.

DESCRIPTION

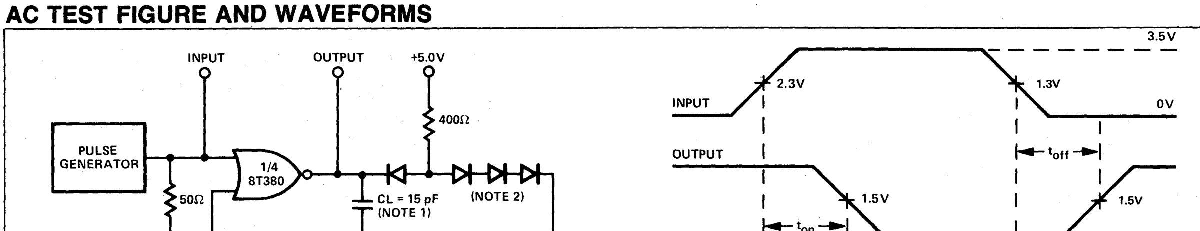
The 8T380 is a quad 2-input bus receiver with hysteresis for use in I/O, data, and memory busses. Built in hysteresis provides maximum noise immunity and a power-up or power-down sequence on the receiver will not affect the bus. Low input current allows several drivers and receivers to communicate over a common bus in "Party Line" fashion. The receiver has been designed to be pincompatible with the Signetics Utilogic II SP 380 gate and provides increased noise immunity as well as lower input current. The 8T 380 is ideal as a Schmitt Trigger in analog interfaces that cannot tolerate the non-linear input impedance characteristics of standard TTL. Further, the low input requirements allow the 8T380 to be used as a CMOS to TTL interface. All inputs have clamping diodes to simplify systems design.



AC ELECTRICAL CHARACTERISTICS
T_A = 25°C, V_{CC} = 5.0V

PARAMETER	LIMITS			UNITS
	MIN.	TYP.	MAX.	
t_{on}, Turn-on Delay		16	35	ns
t_{off}, Turn-off Delay		20	35	ns

AC TEST FIGURE AND WAVEFORMS



NOTES
1. Including probe and jig capacitance
2. All diodes are 1N3064
3. Pulse generator characteristics

TYPICAL APPLICATIONS

A generalized "Party Line" bus interface is shown in Figure 1. Each driver/receiver combination can communicate with any other pair or all. Open collector Nand Gates such as the Signetics 7439 have adequate drive capability for the bus terminations as well as 20 driver/receiver pairs. In addition the bussing scheme is non-inverting as shown and bus drivers are activated by a logic "1" whereas bus receivers are activated by a Logic "0".

Each terminator consisting of a 180 ohm resistor to ground is a 120 ohm. Thevenin's equivalent circuit. The maximum length of cable that can be driven is a complex relationship involving the type of cable used as well as the distribution of drivers and receivers on the buss. Using flat ribbon cable, a maximum reasonable length is 50 ft. minus the combined length of all taps or stubs.

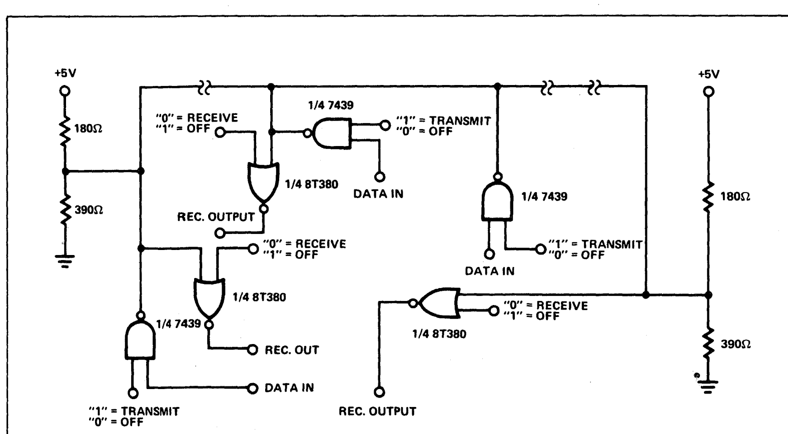


FIGURE 1

SCHMITT TRIGGER

The receiver transfer curve shown in Figure 2a makes the 8T380 ideal in a variety of Schmitt Trigger and waveshaping applications such as Figure 2b.

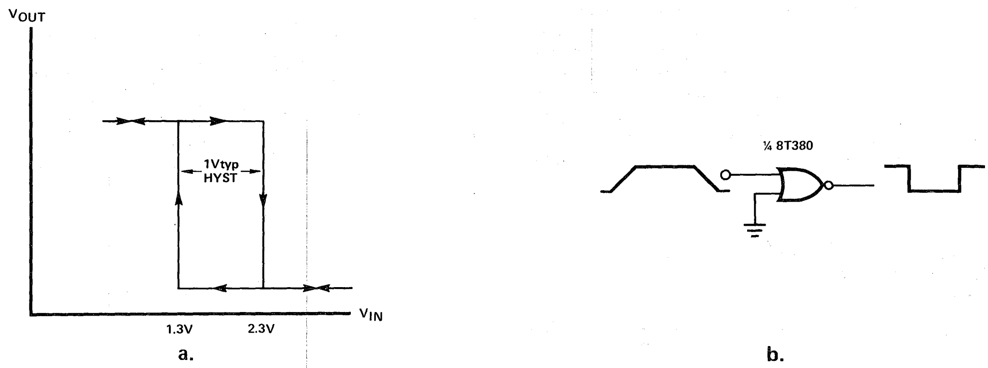


FIGURE 2

MOS/C-MOS INTERFACE

The low input current which is only 50μA max. in the logical "1" state and no current in the logical "0" state marks the 8T380 an ideal MOS/C-MOS interface element.

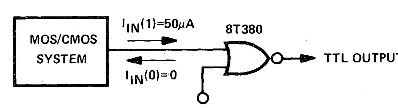


FIGURE 3

FEATURES

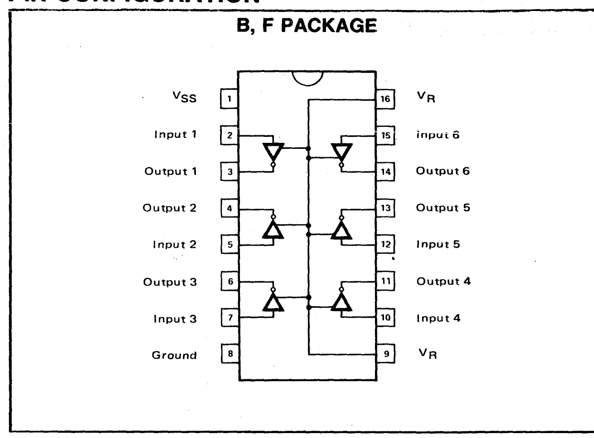
- LOW SATURATION VOLTAGE (TYPICALLY 0.5V) FOR MINIMUM POWER DISSIPATION
- HIGH OUTPUT SINK CURRENT CAPABILITY — 400mA
- LOW INPUT CURRENT LOADING FOR MOS COMPATIBILITY
- LOW STANDBY POWER CONSUMPTION
- SUITABLE FOR 3 VOLT BATTERY OPERATION
- INPUTS/OUTPUTS ARE COMPATIBLE WITH 75494

ABSOLUTE MAXIMUM RATINGS

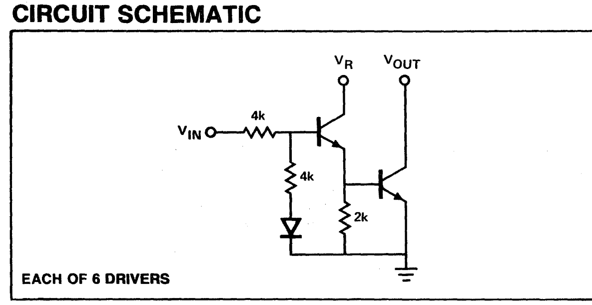
Input Voltage Range[1] .... −12 to VSS volts
Output Voltage[2] .... 10 volts
Output to Input Voltage Differential .... 10 volts
Voltage at VSS (Pin 1) .... 10 volts
Output Current — each output 400mA
Output Current — all outputs 1200mA
Continuous Total Power Dissipation
at or Below 25°C3 .... 800mW
Current in VR (Pin 9 or 16) 25mA
Operating Free-Air Temperature Range .... 0 to 70°C
Storage Temperature Range .... −65 to 150°C
Lead Temperature 1/16 inch from
Case for 10 Seconds .... 260°C

NOTES:
1. The inputs are the only pins which may be negative with respect to ground.
2. Voltage values are with respect to ground.
3. Above 25°C, derate power dissipation at 6.25mW/°C.

PIN CONFIGURATION



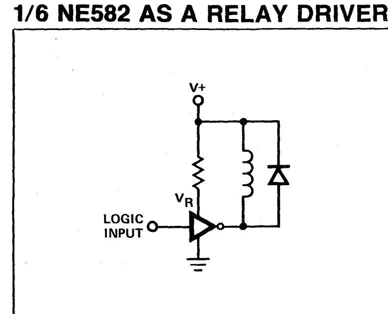
CIRCUIT SCHEMATIC



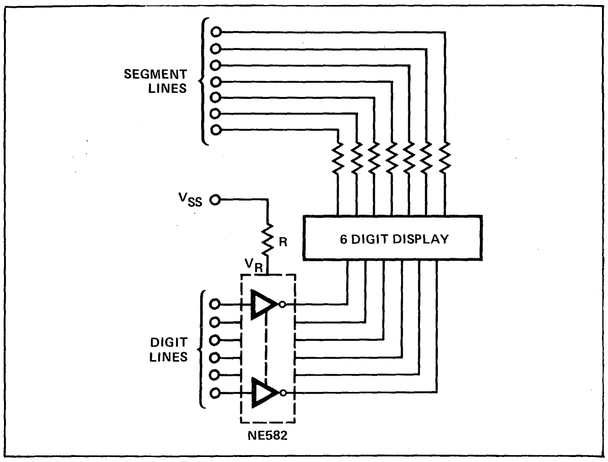
SWITCHING CHARACTERISTICS (T_A = 25°C)

PARAMETER	TEST CONDITIONS	LIMITS			UNIT
		MIN	TYP	MAX	
T_{PLH} Propagation Delay, Low to High Level Output	R_R = 680Ω, R_L = 39Ω, C_L = 15pF	—	80	—	ns
T_{PHL} Propagation Delay, High to Low Level Output	V_{IH} = 7.5V, V_{IL} = 0V, $t_r = t_f \leq 10$ns, $t_W = 1\mu$s, PRR = 100kHz	—	10	—	ns
V_R	V_1 = 6.5V, I_R = 6mA, I_{OL} = 80mA	0.9		1.5	V
I_{SS} Current into Pin 1	V_{SS} = 10V			100	μA

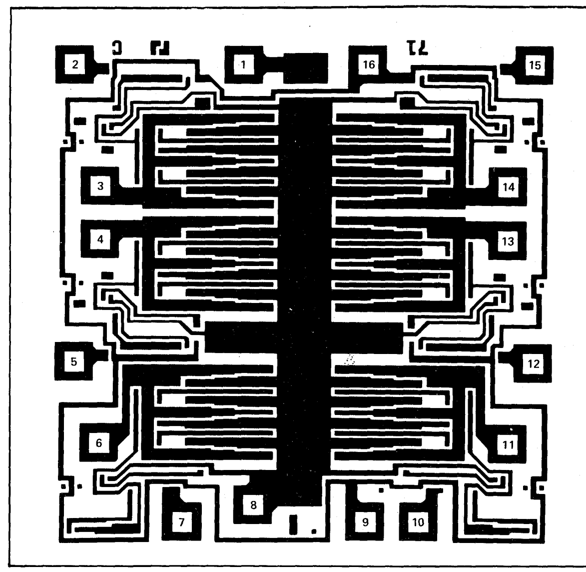
1/6 NE582 AS A RELAY DRIVER



TYPICAL APPLICATION FOR DIGIT DRIVING OF AN LED DISPLAY

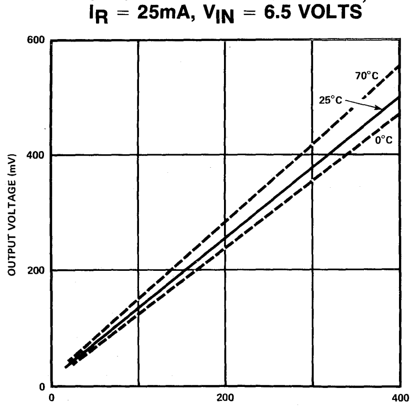


CHIP LAYOUT

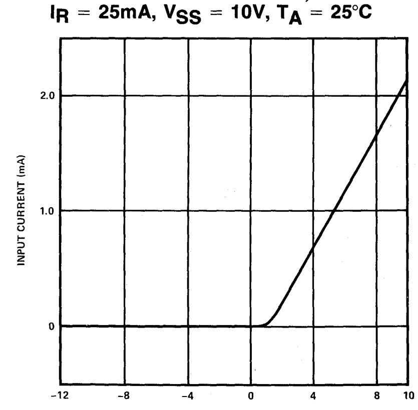


TYPICAL CHARACTERISTIC CURVES

OUTPUT SATURATION VOLTAGE AS A FUNCTION OF OUTPUT LOAD CURRENT, I_R = 25mA, V_{IN} = 6.5 VOLTS



INPUT CURRENT AS A FUNCTION OF INPUT VOLTAGE, I_R = 25mA, V_{SS} = 10V, T_A = 25°C



OBJECTIVE SPECIFICATION

DESCRIPTION

The NE584 and NE585 are respectively cathode and anode drivers for multiplexed gas discharge displays.

The NE584 cathode driver is capable of driving up to 9 display segments, eg., 7 digit segments, decimal point and comma. The NE585 anode drivers can drive up to 9 digits, adequate for most calculators and seven segment display applications. More digits may be driven by using 2 or more anode drivers.

The display segments are driven by floating current sources maintaining uniform brightness across the panel and a minimum of system components. A current feedback circuit is included to hold the anode voltage steady under all load conditions — maximum voltage ripple being typically held to less than 1 volt.

An external resistor on the NE584 circuit provides for external programming of segment current.

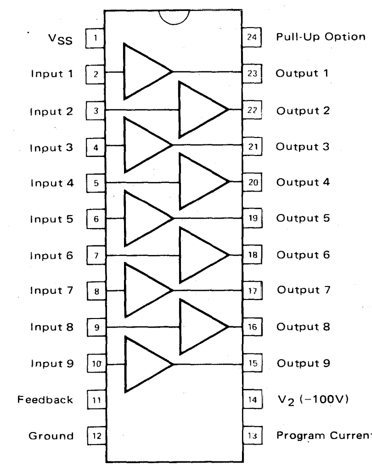
The total driver system component count for a 9 digit display is only 4 components (see figure 1) comprising 2 integrated circuits (NE584 and NE585), 1 resistor and 1 small value capacitor. Power supply requirements are −100V, +100V and the V_{SS} supply. A single 200 V supply may be used with additional external components.

FEATURES

- INTERNAL FEEDBACK NETWORK ENSURES OPTIMUM OPERATING CONDITIONS
- MINIMUM COMPONENT COUNT FOR SYSTEM COST EFFECTIVENESS
- HIGH SYSTEM RELIABILITY
- INTERNAL CURRENT LIMITING PROTECTION
- SEGMENT CURRENT PROGRAMMABILITY FOR OPTIMUM OPERATION OF ALL CHARACTER SIZES.

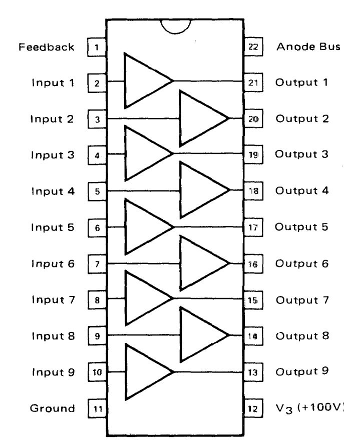
PIN CONFIGURATION

PACKAGE



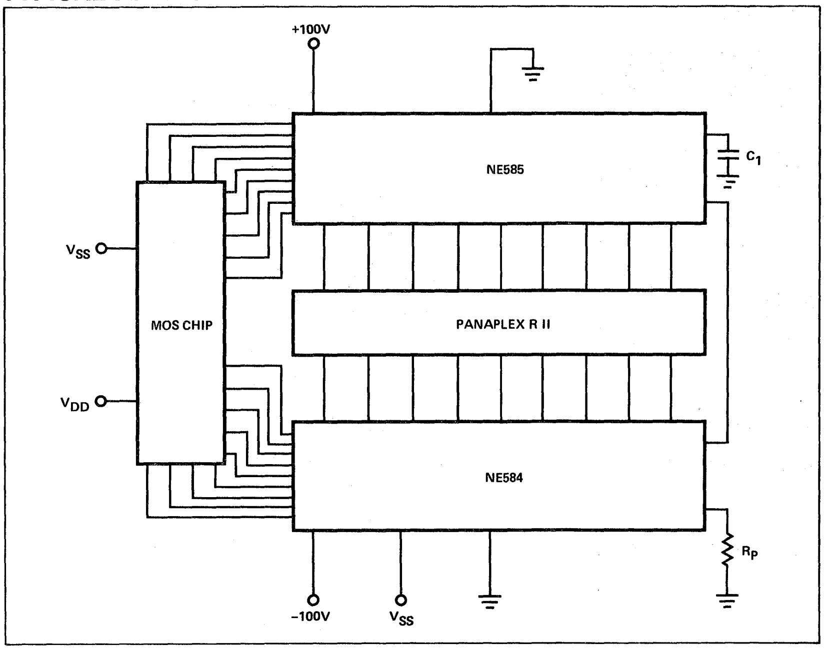
NE 584

PACKAGE



NE 585

TYPICAL APPLICATIONS

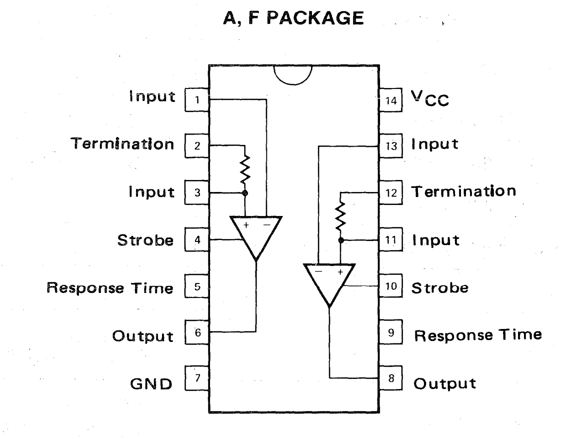


FEATURES
- OPERATION FROM A SINGLE +5V LOGIC SUPPLY
- INPUT VOLTAGE RANGE OF ±15V
- INDEPENDENT CHANNEL STROBING
- HIGH INPUT RESISTANCE
- FANOUT OF TWO WITH DTL OR TTL
- OUTPUT CAN BE WIRE OR'ED

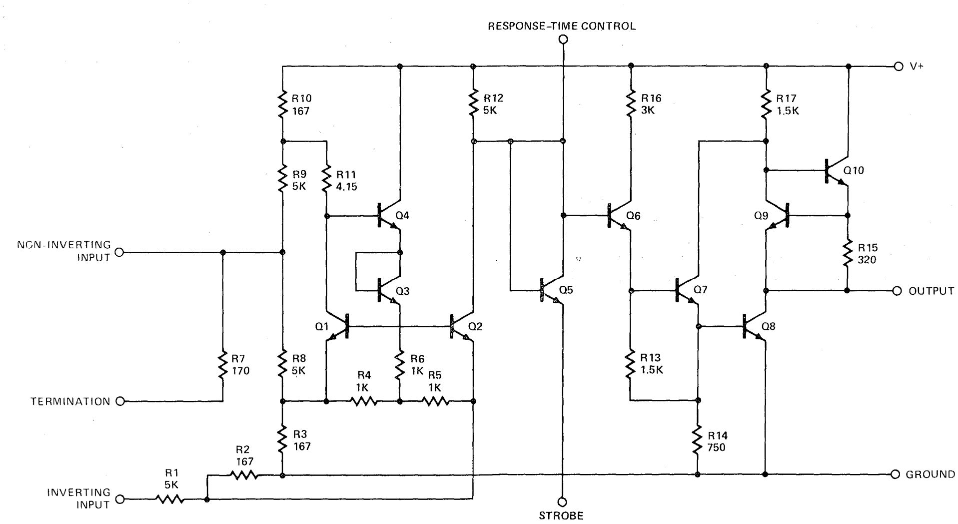
ABSOLUTE MAXIMUM RATINGS

Supply Voltage	8.0V
Input Voltage	±20V
Differential Input Voltage	±20V
Strobe Voltage	8.0V
Output Sink Current	25mA
Power Dissipation	600mW
Operating Temperature Range (DM7820)	−55°C to 125°C
Operating Temperature Range (DM8820)	0°C to 70°C
Lead Temperature (Soldering, 10 sec)	300°C

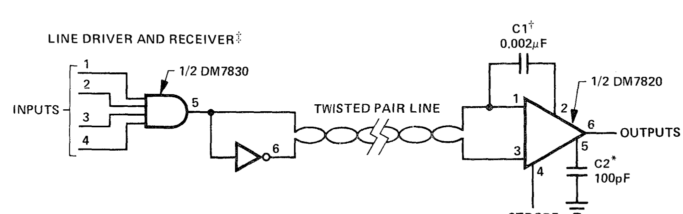
PIN CONFIGURATION



DM7820-DM8820 CIRCUIT SCHEMATIC



DM7820-DM8820 TYPICAL APPLICATION



†EXACT VALUE DEPENDS ON LINE LENGTH
‡V_{CC} IS 4.5V to 5.5V FOR BOTH THE DM7820 and DM7830
*OPTIONAL TO CONTROL RESPONSE TIME

ELECTRICAL CHARACTERISTICS (Notes 1 and 2)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Threshold Voltage	$V_{IN} = 0$ $-15V \quad V_{IN} \quad 15V$	-0.5 -1.0	0 0	0.5 1.0	V V
High Output Level	I_{OUT} 0.2mA	2.5		5.5	V
Low Output Level	I_{SINK} 3.5mA	0		0.4	V
Inverting Input Resistance		3.6	5.0		kΩ
Non-inverting Input Resistance		1.8	2.5		kΩ
Line Termination Resistance	$T_A = 25°C$	120	170	250	Ω
Response Time	$C_{DELAY} = 0$ $C_{DELAY} = 100pF$		40 150		ns ns
Strobe Current	$V_{STROBE} = 0.4V$ $V_{STROBE} = 5.5V$		1.0	1.4 -5.0	mA μA
Power Supply Current	$V_{IN} = 15V$ $V_{IN} = 0$ $V_{IN} = -15V$		3.2 5.8 8.3	6.0 10.2 15.0	mA mA mA
Non-inverting Input Current	$V_{IN} = 15V$ $V_{IN} = 0$ $V_{IN} = -15V$	 -1.6 -9.8	5.0 -1.0 -7.0	7.0	mA mA mA
Inverting Input Current	$V_{IN} = 15V$ $V_{IN} = 0$ $V_{IN} = -15V$	 -4.2	3.0 0 -3.0	4.2 0.5	mA mA mA

NOTES:

1. These specifications apply for $4.5V \leq V_{CC} \leq 5.5V$, $-15V \leq V_{CM} \leq 15V$ and $-55°C \leq T_A \leq 125°C$ for the DM7820 or 0°C TA 70°C for the DM8820 unless otherwise specified: typical values given are for $V_{CC} = 5.0V$, $T_A = 25°C$ and $V_{CM} = 0$ unless stated differently.
2. The specifications and curves given are for one side only. Therefore, the total package dissipation and supply currents will be double the values given when both receivers are operated under identical conditions.

DM7830 A,F
DM8830 A,F

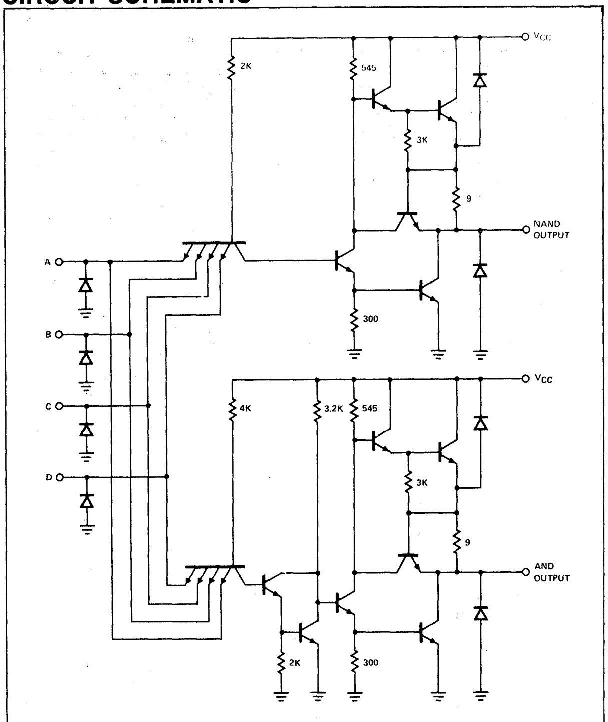
FEATURES

- SINGLE 5 VOLT POWER SUPPLY
- HIGH SPEED
- DIODE PROTECTED OUTPUTS FOR TERMINATION OF POSITIVE AND NEGATIVE VOLTAGE TRANSIENTS
- DIODE PROTECTED INPUTS TO PREVENT LINE RINGING
- SHORT CIRCUIT PROTECTION

ABSOLUTE MAXIMUM RATINGS

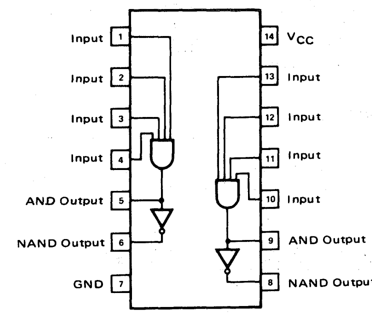
V_{CC}	7.0V
Input Voltage	5.5V
Operating Temperature	
DM7830	−55°C to +125°C
DM8830	0°C to 70°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C
Output Short Circuit Duration (125°C)	1 second

CIRCUIT SCHEMATIC

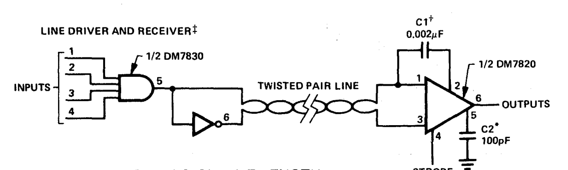


PIN CONFIGURATION

A,F PACKAGE

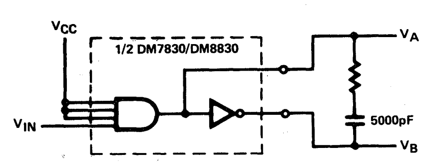


TYPICAL APPLICATION



†EXACT VALUE DEPENDS ON LINE LENGTH
‡V_{CC} IS 4.5V to 5.5V FOR BOTH THE DM7820 AND DM7830
*OPTIONAL TO CONTROL RESPONSE TIME

AC TEST CIRCUIT



†EXACT VALUE DEPENDS ON TRANSMISSION RATE
‡V_{CC} IS 4.5V to 5.5V FOR BOTH THE DM7820 AND DM7830
*OPTIONAL TO CONTROL RESPONSE TIME

SWITCHING CHARACTERISTICS

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
Propagation Delay	t_{pd} 1	T_A=25°C		8	12	ns
AND Gate	t_{pd} 0	V_{CC}=5.0V		11	18	ns
Propagation Delay	t_{pd} 1	C_L=15pF		8	12	ns
NAND Gate	t_{pd} 0	See Figure 1		5	8	ns
Differential Delay t1		Load, 100Ω and 5000pF		12	16	ns
Differential Delay t2		See Figure 2		12	16	ns

NOTES
1. Specifications apply for DM7830 −55°C ≤T_A≤+125°C, V_{CC} = +5V ±10%, DM8830 0°C≤T_A≤70°C, V_{CC} = +5V ±5% unless otherwise stated. Typical values given are for T_A = 25°C, V_{CC} = 5.0V.

SWITCHING TIME WAVEFORMS

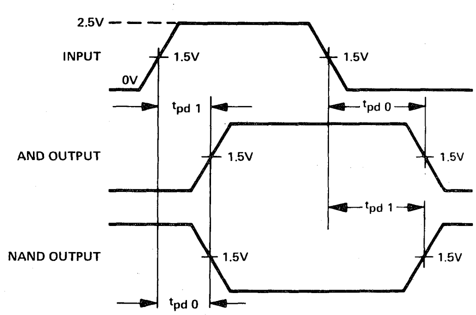


FIGURE 1

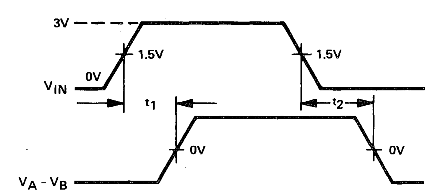


FIGURE 2

FEATURES

- CURRENT SOURCE OUTPUTS
- ADJUSTABLE OUTPUT CURRENT — 0.2 TO 1.5 mA
- HIGH OUTPUT BREAKDOWN VOLTAGE — 110V TYP
- SUITABLE FOR MULTIPLEX OPERATION
- BLANKING AND RIPPLE BLANKING PROVISIONS
- LOW FAN-IN AND LOW POWER

PIN CONFIGURATION

B PACKAGE

Pin	Function	Pin	Function
1	B Input	16	V_{CC}
2	C Input	15	f Output
3	Program	14	g Output
4	BI/RBO	13	a Output
5	RBI	12	b Output
6	D Input	11	c Output
7	A Input	10	d Output
8	GND	9	e Output

TRUTH TABLE

SEGMENT IDENTIFICATION

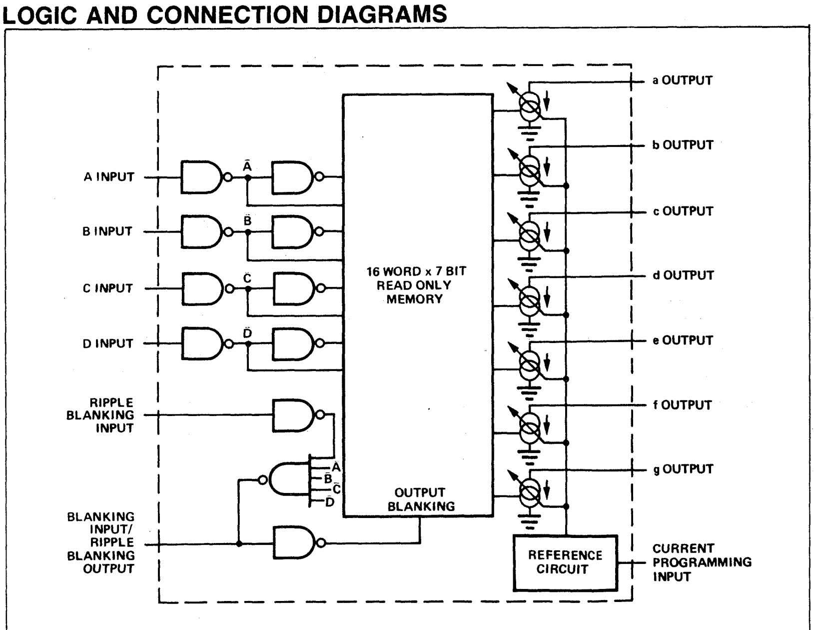
DECIMAL OR FUNCTION	RBI	D	C	B	A	BI/ RBO	a	b	c	d	e	f	g	DISPLAY
0	1	0	0	0	0	1	0	0	0	0	0	0	1	
1	X	0	0	0	1	1	1	0	0	1	1	1	1	
2	X	0	0	1	0	1	0	0	1	0	0	1	0	
3	X	0	0	1	1	1	0	0	0	0	1	1	0	
4	X	0	1	0	0	1	1	0	0	1	1	0	0	
5	X	0	1	0	1	1	0	1	0	0	1	0	0	
6	X	0	1	1	0	1	0	1	0	0	0	0	0	
7	X	0	1	1	1	1	0	0	0	1	1	1	1	
8	X	1	0	0	0	1	0	0	0	0	0	0	0	
9	X	1	0	0	1	1	0	0	0	0	1	0	0	
10	X	1	0	1	0	1	0	0	0	1	0	0	0	
11	X	1	0	1	1	1	1	1	0	0	0	0	0	
12	X	1	1	0	0	1	0	1	1	0	0	0	1	
13	X	1	1	0	1	1	1	0	0	0	0	1	0	
14	X	1	1	1	0	1	0	1	1	0	0	0	0	
15	X	1	1	1	1	1	0	1	1	1	0	0	0	
B1	X	X	X	X	X	0	1	1	1	1	1	1	1	
RBI	0	0	0	0	0	0	1	1	1	1	1	1	1	

ABSOLUTE MAXIMUM RATINGS

VCC	7V
Input Voltage (Except B1)	6V
Input Voltage (B1)	VCC
Power Dissipation (Note 1)	600mW
Operating Temperature Range	0°C to 70°C
Storage Temperature Range	−65°C to 150°C
Lead Temperature (Soldering, 10 sec)	300°C

Note 1: Min/max limits apply across the guaranteed operating temperature range of 0°C to 70°C unless otherwise specified. Typicals are for V_{CC} = 5V, T_A = 25°C. Positive current is defined as current into the referenced pin.

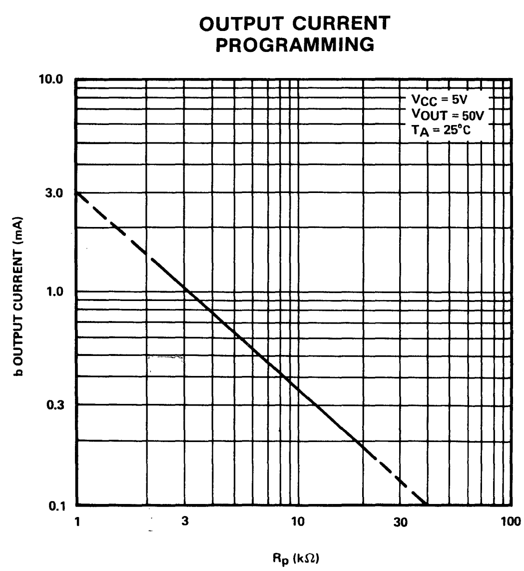
LOGIC AND CONNECTION DIAGRAMS

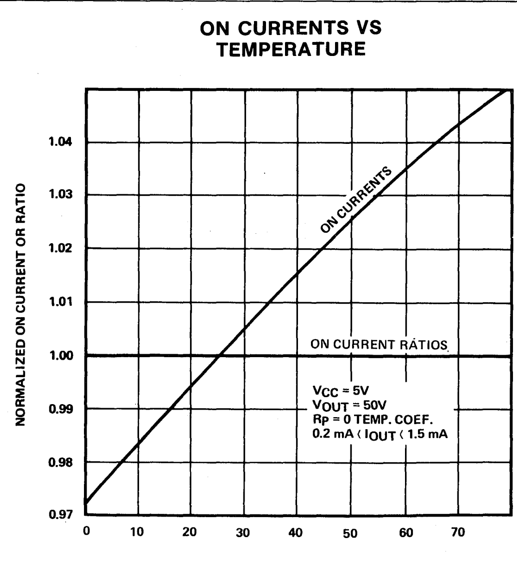


SWITCHING CHARACTERISTICS

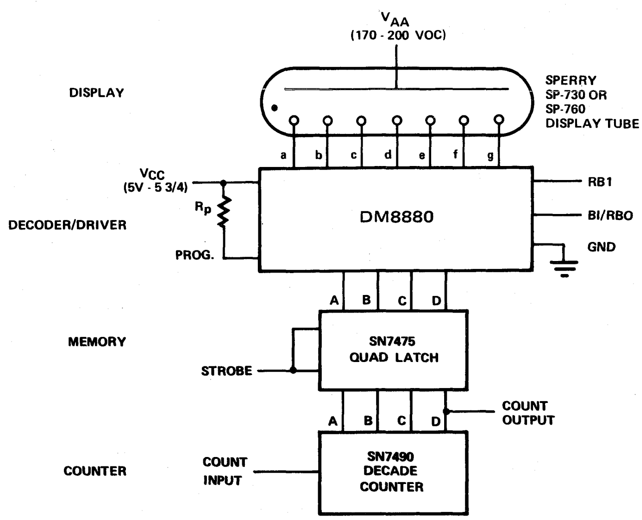
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Segment Outputs:					
Outputs a, f, g On Current Ratio	All Outputs = 50V, Output b Curr. = Ref.	0.88	0.93	0.98	
Output c On Current Ratio	All Outputs = 50V, Output b Curr. = Ref.	1.19	1.25	1.31	
Output d On Current Ratio	All Outputs = 50V, Output b Curr. = Ref.	0.95	1.00	1.05	
Output e On Current Ratio	All Outputs = 50V, Output b Curr. = Ref.	1.04	1.10	1.16	
Output b On Current	VCC = 5V, VOUT b= 50V, TA = 25°C, RP = 18.1k	0.18	0.20	0.22	mA
	VCC = 5V, VOUT b = 50V, TA = 25°C, RP = 7.03k	0.45	0.50	0.55	mA
	VCC = 5V, VOUT b = 50V, TA = 25°C, RP = 3.40k	0.90	1.00	1.10	mA
	VCC = 5V, VOUT b = 50V, TA = 25°C, RP = 2.20k	1.45	1.50	1.65	mA
Output Saturation Voltage	VCC = 4.75V, IOUT = 2mA, RP = 1k ±5%		0.8	2.5	V
Output Leakage Current	VOUT = 75V, BI = 0V		.003	3	μA
Output Breakdown Voltage	IOUT = 250μA, BI = 0V	80	110		V
Propagation Delays:					
BCD Input to Segment Output	VCC = 5V, TA = 25°C		0.4	10	μs
BI to Segment Output	VCC = 5V, TA = 25°C		0.4	10	μs
RBI to Segment Output	VCC = 5V, TA = 25°C		0.7	10	μs
RBI to RBO	VCC = 5V, TA = 25°C		0.4	10	μs

TYPICAL APPLICATION





TYPICAL APPLICATION (Continued)



INTERFACE

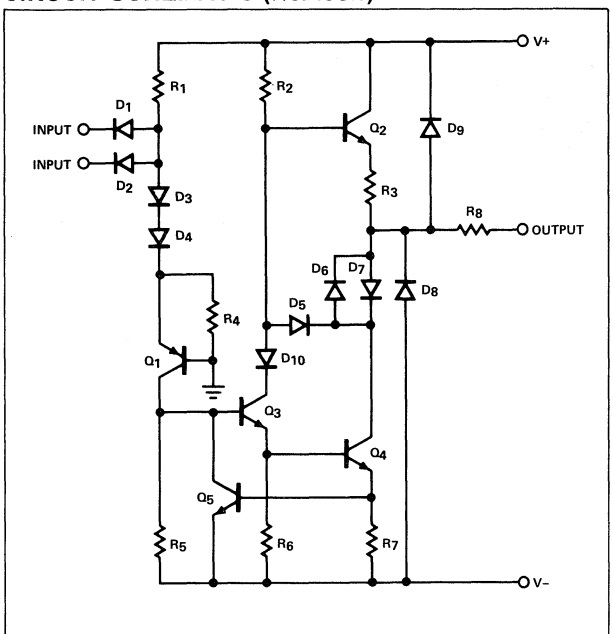
FEATURES

- CURRENT LIMITED OUTPUT: ±10mA TYP
- POWER-OFF SOURCE IMPEDANCE: 300Ω MIN
- SIMPLE SLEW RATE CONTROL WITH EXTERNAL CAPACITOR
- FLEXIBLE OPERATING SUPPLY RANGE
- INPUTS ARE DTL/TTL COMPATIBLE

ABSOLUTE MAXIMUM RATINGS (Note 1)

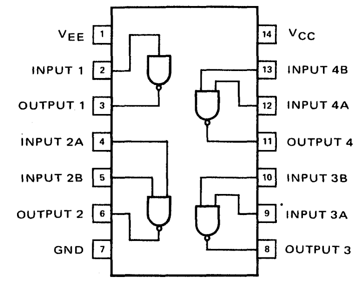
Supply Voltage V+	+15V
V−	−15V
Input Voltage (VIN)	−15V ≤VIN ≤7.0V
Output Voltage	±15V
Power Dissipation	1000mW
Operating Temperature Range	0°C to +75°C
Storage Temperature Range	−65°C to +175°C
Lead Temperature (Soldering, 10 sec)	300°C

CIRCUIT SCHEMATIC (¼CIRCUIT)

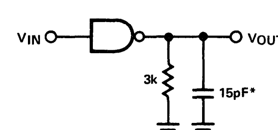


PIN CONFIGURATION

F PACKAGE

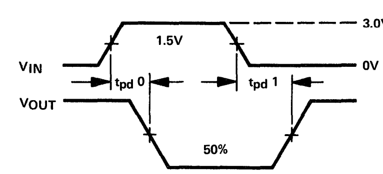


AC LOAD CIRCUIT



*CL INCLUDES PROBE AND JIG CAPACITANCE

SWITCHING WAVEFORMS



tr and tf ARE MEASURED BETWEEN 10% AND 90% OF THE OUTPUT WAVEFORM

SWITCHING CHARACTERISTICS (Note 2)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Propagation Delay to "1" (tpd1)	RL = 3.0kΩ, CL = 15pF, TA = 25°C		230	300	ns
Propagation Delay to "0" (tpd0)	RL = 3.0kΩ, CL = 15pF, TA = 25°C		70	175	ns
Rise Time (tr)	RL = 3.0kΩ, CL = 15pF, TA = 25°C		75	100	ns
Fall Time (tf)	RL = 3.0kΩ, CL = 15pF, TA = 25°C		40	75	ns

NOTES
1. Voltage values shown are with respect to network ground terminal. Positive current is defined as current into the referenced pin.
2. These specifications apply for V+ = +9.0V± 1%, V− = −9.0V± 1%, TA = 0°C to +75°C unless otherwise noted. All typicals are for V+ = 9.0V, V− = −9.0V, and TA = 25°C.

APPLICATIONS

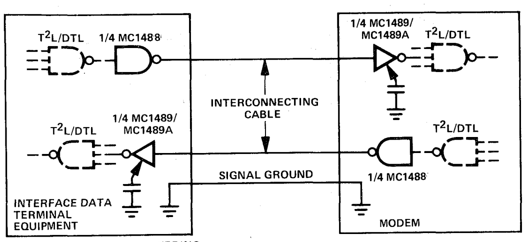
By connecting a capacitor to each driver output the slew rate can be controlled utilizing the output current limiting characteristics of the MC1488. For a set slew rate the appropriate capacitor value may be calculated using the following relationship

$$C = I_{SC}\ (\Delta T/\Delta V)$$

where C is the required capacitor, I_{SC} is the short circuit current value, and $\Delta V/\Delta T$ is the slew rate.

RS232C specifies that the output slew rate must not exceed 30V per microsecond. Using the worst case output short circuit current of 12mA in the above equation, calculations result in a required capacitor of 400pF connected to each output.

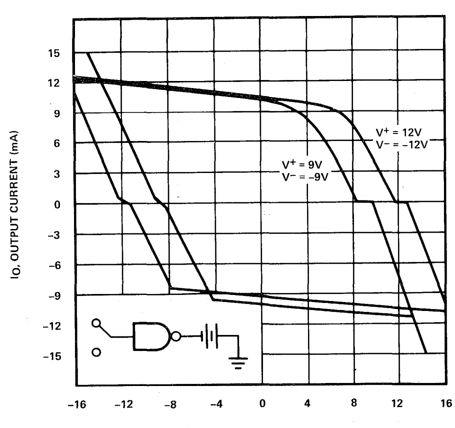
RS232C DATA TRANSMISSION



* OPTIONAL FOR NOISE FILTERING

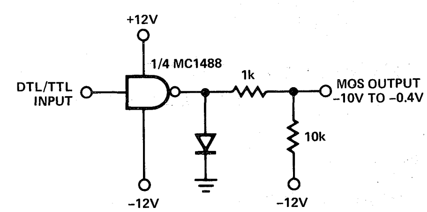
CHARACTERISTIC CURVES

OUTPUT VOLTAGE AND CURRENT-LIMITING CHARACTERISTICS

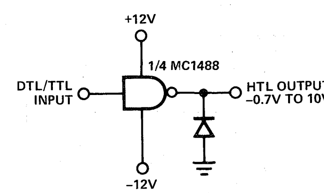


TYPICAL APPLICATIONS

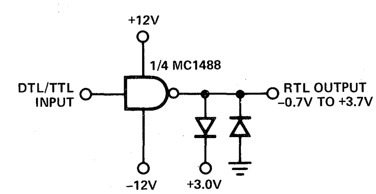
DTL/TTL-TO-MOS TRANSLATOR



DTL/TTL-TO-HTL TRANSLATOR



DTL/TTL-TO-RTL TRANSLATOR



INTERFACE

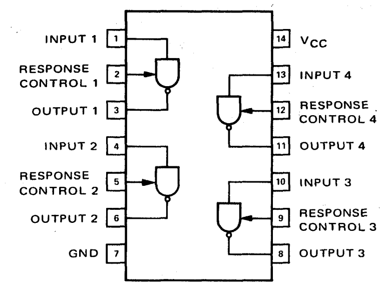
MC1489F MC1489A-F

FEATURES
- FOUR TOTALLY SEPARATE RECEIVERS PER PACKAGE
- PROGRAMMABLE THRESHOLD
- BUILT-IN INPUT THRESHOLD HYSTERESIS
- "FAIL SAFE" OPERATING MODE
- INPUTS WITHSTAND ±30V

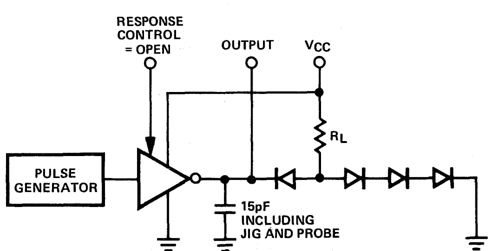
ABSOLUTE MAXIMUM RATINGS
The following apply for TA = 25°C unless otherwise specified.

Power Supply Voltage	10V
Input Voltage Range	±30V
Output Load Current	20mA
Power Dissipation	1W
Operating Temperature Range	0°C to +75°C
Storage Temperature Range	−65°C to +175°C

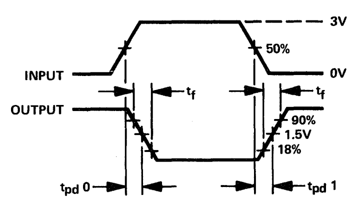
PIN CONFIGURATION
F PACKAGE



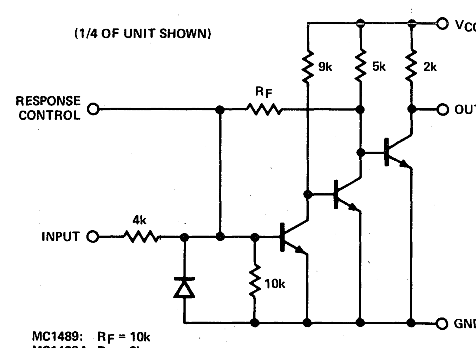
AC TEST CIRCUIT



VOLTAGE WAVEFORMS



CIRCUIT SCHEMATIC

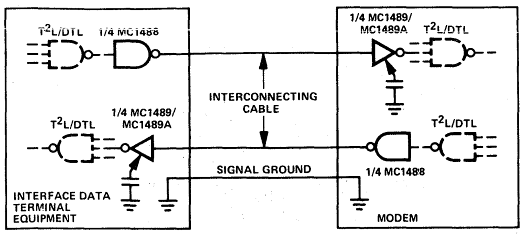


SWITCHING CHARACTERISTICS MC1489/MC1489A V_{CC} = 5.0V ±1%, T_A = 25°C

PARAMETER	CONDITIONS	MC1489			MC1489A			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Input to Output "High" Propagation Delay (t_{pd1})	R_L = 3.9k (AC Test Circuit)		25	85		25	85	ns
Input to Output "Low" Propagation Delay (t_{pd0})	R_L = 390Ω (AC Test Circuit)		20	50		20	50	ns
Output Rise time	R_L = 3.9k (AC Test Circuit)		110	175		110	175	ns
Output Fall Time	R_L = 390Ω (AC Test Circuit)		9	20		9	20	ns

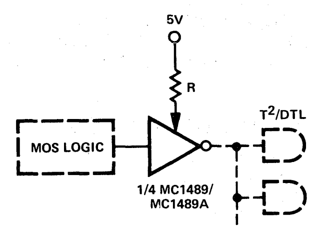
TYPICAL APPLICATIONS

RS232C DATA TRANSMISSION



• OPTIONAL FOR NOISE FILTERING

MOS TO T²L/DTL TRANSLATOR



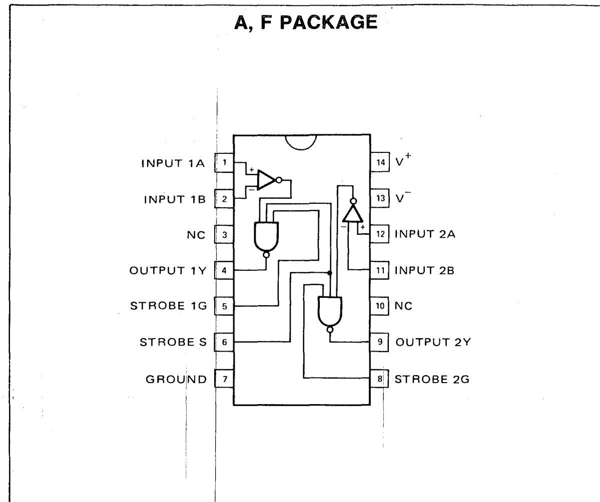
FEATURES

- FUNCTIONALLY EQUIVALENT AND PIN COMPATIBLE TO SN75107A/207A
- 17ns MAXIMUM GUARANTEED PROPAGATION DELAY
- 20 μA MAXIMUM INPUT BIAS CURRENT
- STTL COMPATIBLE STROBES AND OUTPUTS
- LARGE COMMON MODE INPUT VOLTAGE RANGES
- OPERATES FROM STANDARD SUPPLY VOLTAGES

ABSOLUTE MAXIMUM RATINGS

Positive Supply Voltage (V+)	+7V
Negative Supply Voltage (V−)	−7V
Differential input voltage	±6V
Common mode input voltage	±5V
Strobe/Gate input voltage	+5.5V
Power Dissipation	600mw
Operating Temperature Range	0°C to 70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering 60 seconds)	+300°C

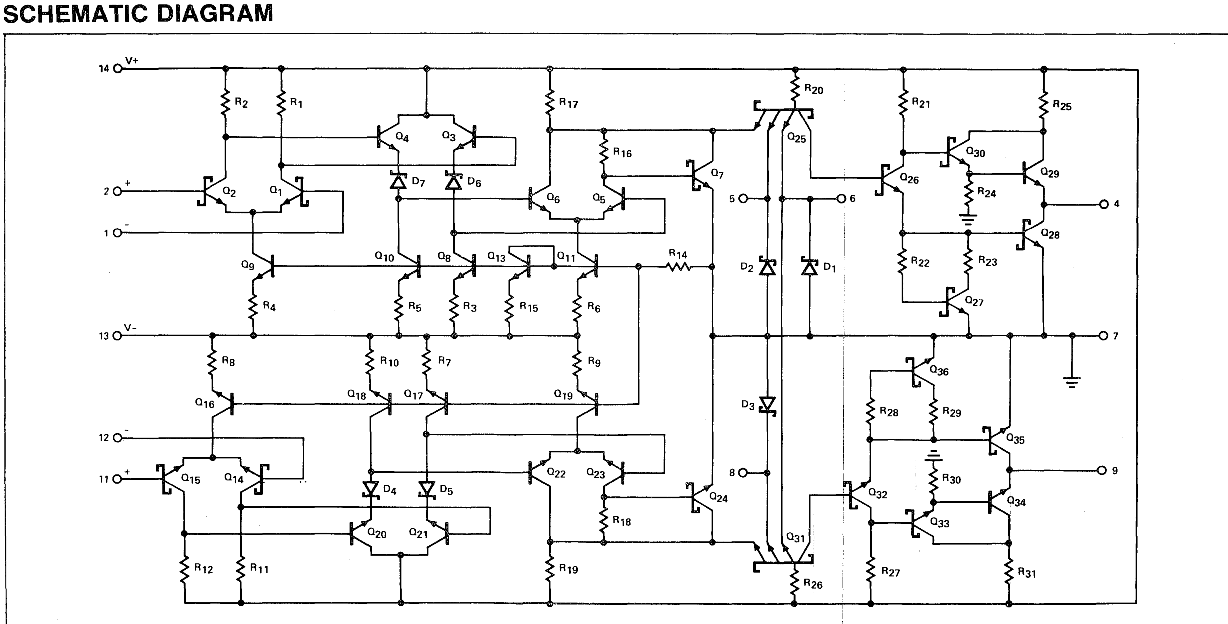
PIN CONFIGURATION



APPLICATIONS

MOS MEMORY SENSE AMP
A/D CONVERSION
HIGH SPEED LINE RECEIVER

SCHEMATIC DIAGRAM



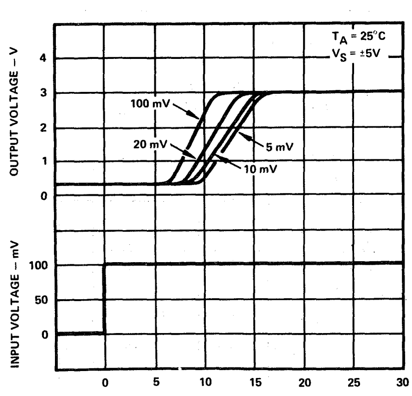
SWITCHING CHARACTERISTICS $V+ = +5.00$, $V- = -5.00$, $T_A = 0$ to 70°C (Unless Otherwise Noted).

PARAMETER	TEST CONDITIONS	75S107/207			UNIT
		MIN	TYP	MAX	
Amplifier Input					
Input offset voltage 75S107	$V+ = 4.75$, $V- = -4.75$			25	mV
75S207				10	mV
Input Bias Current 25°C	$V+ = 5.25$, $V- = -5.25$		7.5	20	µV
Over temp range	$V+ = 5.25$, $V- = -5.25$			40	µA
Input offset current 25°C	$V+ = 5.25$, $V- = -5.25$		1.0	5	µA
Over temp range	$V+ = 5.25$, $V- = -5.25$			12	µA
Input common mode voltage range	$V+ = 4.75$, $V- = -4.75$	±3			V
Input resistance			4		kΩ
Input capacitance			3	6	pF
Voltage gain			5		V/mV
Power Supply Requirements					
Supply Voltage					
V+		4.75	5.00	5.25	V
V−		−4.75	−5.00	−5.25	V
Large Signal Switching Speed					
T_PLH (D) low to high propagation delay from amp inputs to output	$R_L = 280\Omega$ $C_L = 15$ pF, $T_A = 25°C$ Note 1		12	17	ns
T_PHL (D) high to low propagation delay from amp inputs to output	$R_L = 280\Omega$ $C_L = 15$ pF, $T_A = 25°C$ Note 1		9	13	ns
T_PLH (S) low to high propagation delay from strobes input to output	$R_L = 280\Omega$ $C_L = 15$ pF, $T_A = 25°C$ Note 2		4.5	6	ns
T_PHL (S) high to low propagation delay strobe input to output	$R_L = 280\Omega$ $C_L = 15$ pF, $T_A = 25°C$ Note 2		3.0	4.5	ns
Maximum Operating Frequency	$R_L = 280\Omega$ $C_L = 15$ pF, $T_A = 25°C$	40	55		MHz

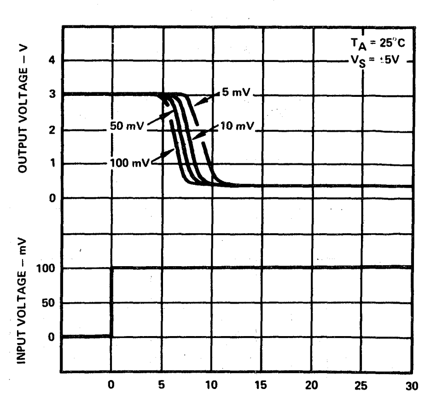
NOTES:
1. Response time measured from 0 V point of ±100 mV P-P 10 MHz square wave to the 1.5 point of the output.
2. Response time measured from 1.5 V point of input to 1.5 V point of output.
3. Response time measured from the start of a 100 mV input step with 5 mV overdrive to the 1.5 V point of the output.

TYPICAL PERFORMANCE CHARACTERISTICS

RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES

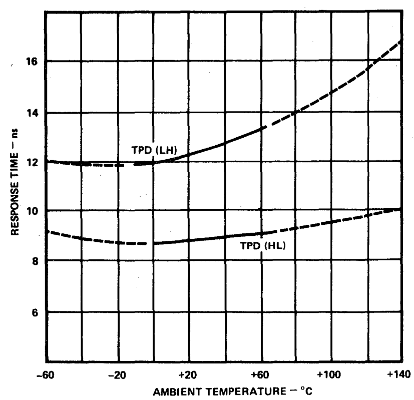


RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES

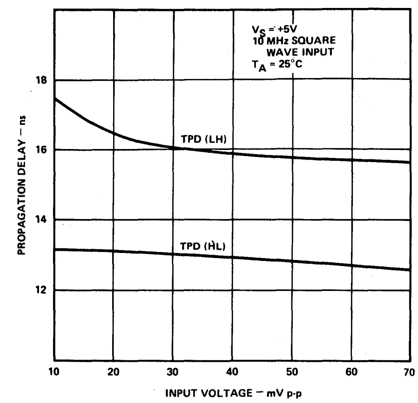


TYPICAL PERFORMANCE CHARACTERISTICS (CONT'D)

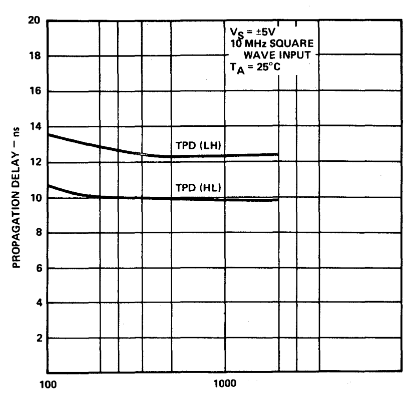
RESPONSE TIME VS. TEMPERATURE



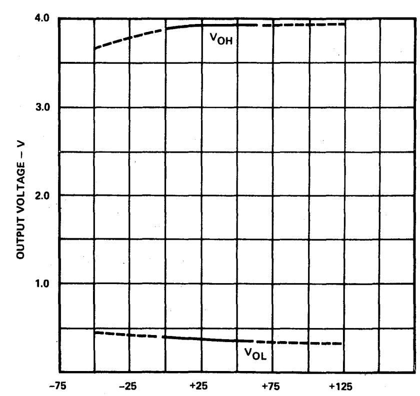
PROPAGATION DELAY FOR VARIOUS INPUT VOLTAGE



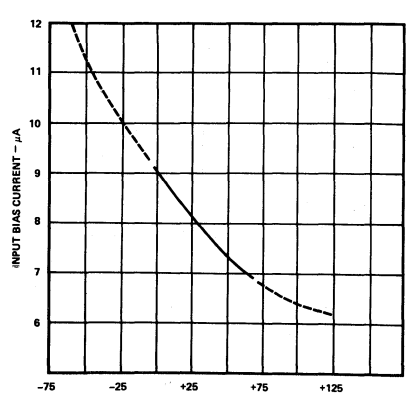
PROPAGATION DELAY FOR VARIOUS INPUT VOLTAGE



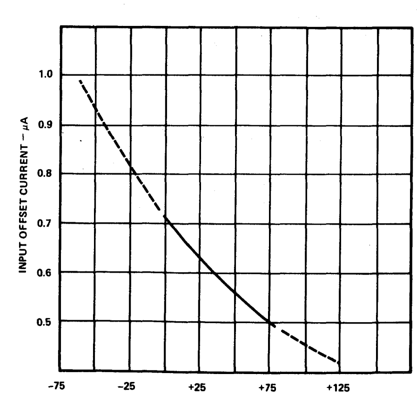
OUTPUT VOLTAGE VS. AMBIENT TEMPERATURE



INPUT BIAS CURRENT VS. AMBIENT TEMPERATURE



INPUT OFFSET CURRENT VS. AMBIENT TEMPERATURE



FEATURES

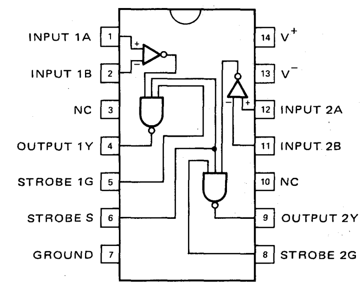
- FUNCTIONALLY EQUIVALENT AND PIN COMPATIBLE TO SN75108A/208A
- 17ns MAXIMUM GUARANTEED PROPAGATION DELAY
- 20μA MAXIMUM INPUT BIAS CURRENT
- TTL COMPATIBLE STROBES AND OUTPUTS
- OPEN COLLECTOR OUTPUTS
- LARGE COMMON MODE INPUT VOLTAGE RANGE
- OPERATES FROM STANDARD SUPPLY VOLTAGES

ABSOLUTE MAXIMUM RATINGS

Positive Supply Voltage (V+)	+7V
Negative Supply Voltage (V−)	−7V
Differential input voltage	±6V
Common mode input voltage	±5V
Strobe/Gate input voltage	+5.5V
Power Dissipation	600mw
Operating Temperature Range	0°C to 70°C
Storage temperature range	−65°C to +150°C
Lead temperature (Soldering 60 seconds)	+300°C

PIN CONFIGURATION

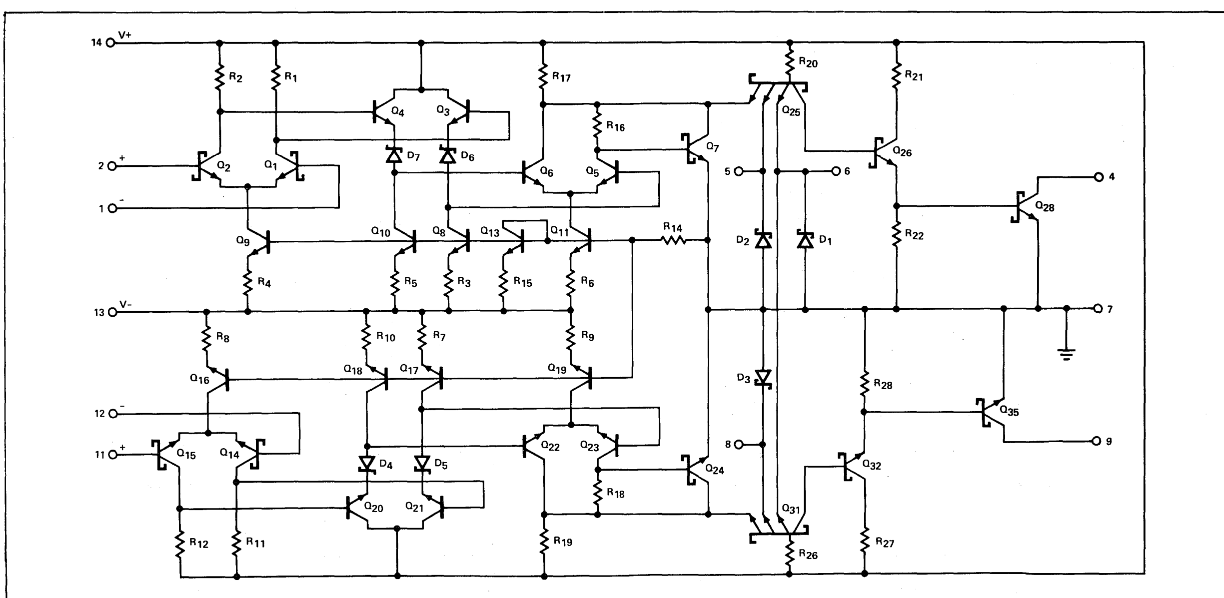
A, F PACKAGE



APPLICATIONS

HIGH SPEED LINE RECEIVER
MOS MEMORY SENSE AMP
A/D CONVERSION

SCHEMATIC DIAGRAM

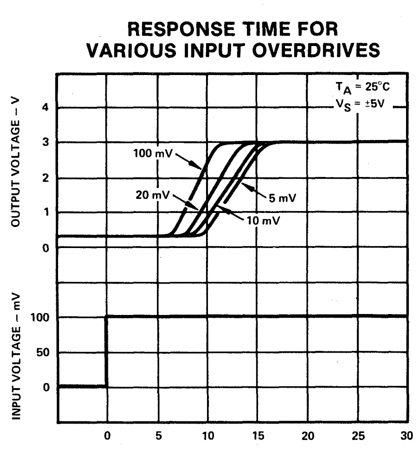


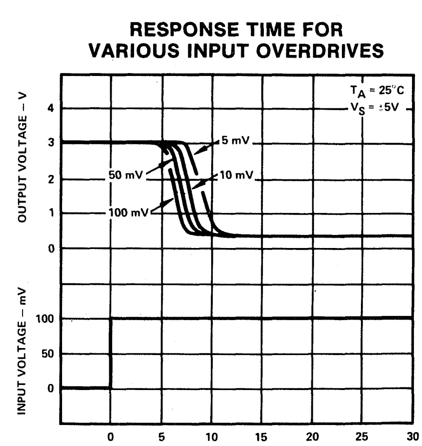
SWITCHING CHARACTERISTICS V+ = +5.00, V− = −5.00, T_A = 0 to 70°C (Unless Otherwise Noted).

PARAMETER	TEST CONDITIONS	75S108/208			UNIT
		MIN	TYP	MAX	
Amplifier Input					
Input offset voltage 75S108	V+ = 4.75, V− = −4.75			25	mV
75S208				10	
Input Bias Current a 25°C	V+ = 5.25, V− = −5.25		7.5	20	μA
over temp range	V+ = 5.25, V− = −5.25			40	μA
Input offset current a 25°C	V+ = 5.25, V− = −5.25		1.0	5	μA
over temp range	V+ = 5.25, V− = −5.25			12	μA
Input common mode voltage range	V+ = 4.75, V− = −4.75	±3		+3	V
Input resistance			4		kΩ
Input capacitance			3	6	pF
Voltage gain			5		V/mV
Power Supply Requirements					
Supply Voltage					
V+		4.75	5.00	5.25	V
V−		−4.75	−5.00	−5.25	V
Large Signal Switching Speed					
T_pLH (D) low to high propagation delay from amp inputs to output	R_L = 280ΩC_L = 15 pF T_A = 25°C Note 1		12	17	ns
T_pHL (D) high to low propagation delay from amp inputs to output	R_L = 280Ω C_L = 15 pF T_A = 25°C Note 1		9	13	ns
T_pLH (S) low to high propagation delay from strobes input to output	R_L = 280Ω C_L = 15 pF T_A = 25°C Note 2		6	10	ns
T_pHL (S) high to low propagation delay strobe input to output	R_L = 280Ω C_L = 15 pF T_A = 25°C Note 2		5	8	ns
Maximum Operating Frequency	R_L = 280Ω C_L = 15 pF T_A = 25°C	25	35		MHz

NOTES:
1. Response time measured from 0V point of ±100 mV P-P 10MHz square wave to the 1.5 point of the output.
2. Response time measured from 1.5V point of input to 1.5V point of output.
3. Response time measured from the start of a 100mV input step with 5mV overdrive to the 1.5V point of the output.

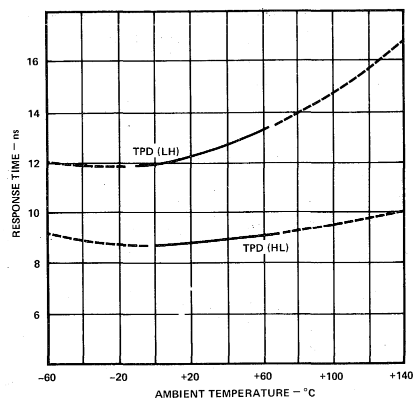
TYPICAL PERFORMANCE CHARACTERISTICS



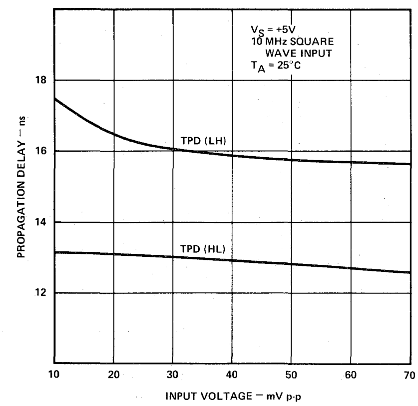


TYPICAL PERFORMANCE (Cont'd)

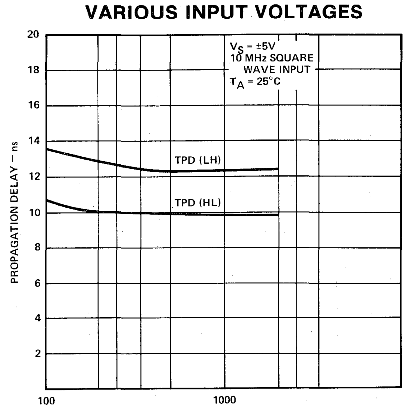
RESPONSE TIME VS TEMPERATURE



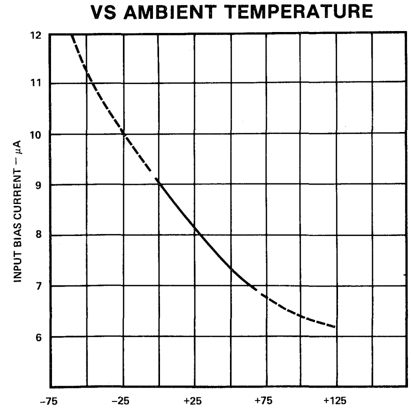
PROPAGATION DELAY FOR VARIOUS INPUT VOLTAGES



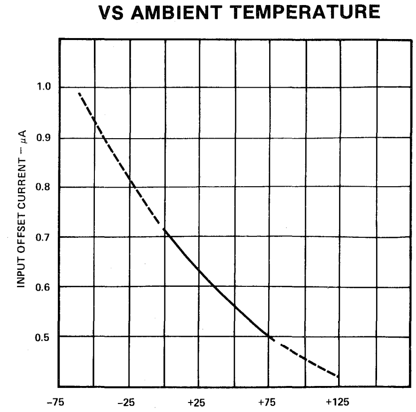
PROPAGATION DELAY FOR VARIOUS INPUT VOLTAGES



INPUT BIAS CURRENT VS AMBIENT TEMPERATURE

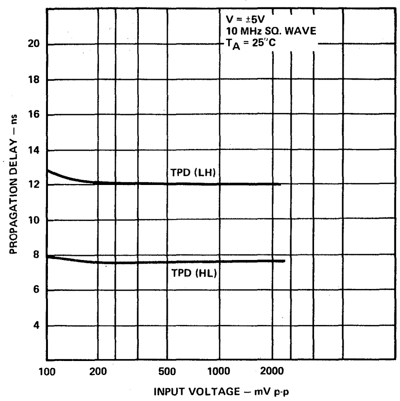


INPUT OFFSET CURRENT VS AMBIENT TEMPERATURE

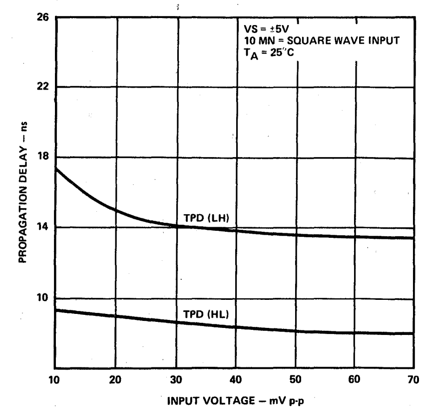


TYPICAL PERFORMANCE (Continued)

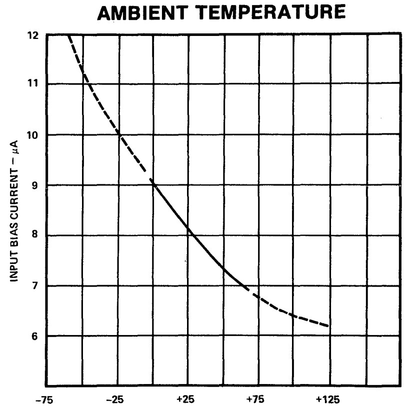
PROPAGATION DELAY FOR VARIOUS INPUT VOLTAGES



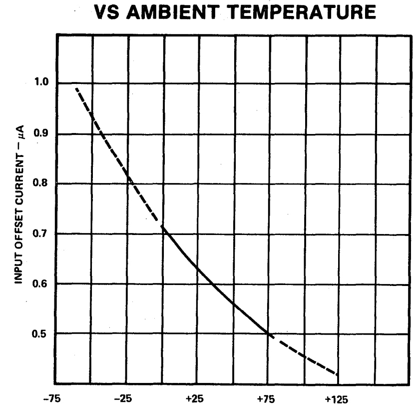
PROPAGATION DELAY FOR VARIOUS INPUT VOLTAGE



INPUT BIAS CURRENT VS AMBIENT TEMPERATURE



INPUT OFFSET CURRENT VS AMBIENT TEMPERATURE

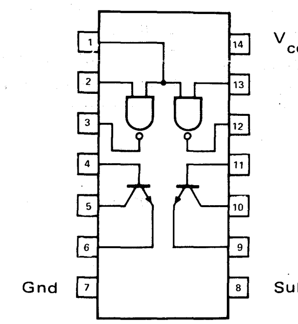


FEATURES

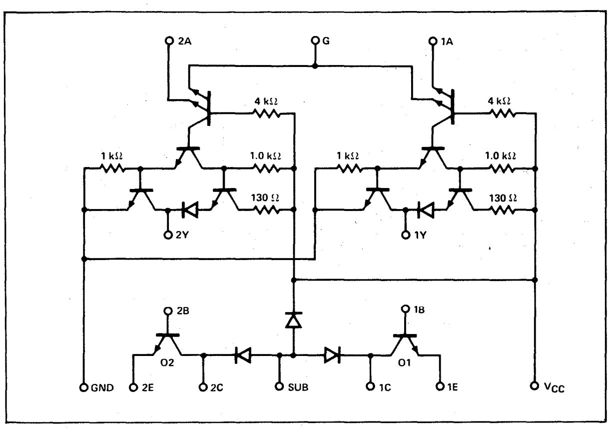
- 300mA OUTPUT CURRENT CAPABILITY
- HIGH VOLTAGE OUTPUTS
- NO OUTPUT LATCH-UP AT 20V
- HIGH SPEED SWITCHING
- CIRCUIT FLEXIBILITY FOR VARIED APPLICATIONS
- TTL OR DTL COMPATIBLE DIODE-CLAMPED INPUTS
- STANDARD SUPPLY VOLTAGES

PIN CONFIGURATION

A, F PACKAGE



EQUIVALENT CIRCUIT



ABSOLUTE MAXIMUM RATINGS

	55450B	75450B	UNIT
Supply voltage, V_{CC} (see Note 1).	7	7	V
Input voltage	5.5	5.5	V
Interemitter voltage (see Note 2)	5.5	5.5	V
V_{CC}-to-substrate voltage	35	35	V
Collector-to-substrate voltage	35	35	V
Collector-base voltage	35	35	V
Collector-emitter voltage (see Note 3)	30	30	V
Emitter-base voltage	5	5	V
Output voltage (see Note 4)			V
Collector current (see Note 5)	300	300	mA
Output current (see Note 5)			mA
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 6)	800	800	mW
Operating free-air temperature range	−55 to 125	0 to 70	°C
Storage temperature range	−65 to 150	−65 to 150	°C
Lead Temperature 1/16 inch from case for 60 seconds	300	300	°C
Lead temperature 1/16 inch from case for 10 seconds	260	260	°C

1. Voltage values are with respect to network ground terminal unless otherwise specified.
2. This is the voltage between two emitters of a multiple-emitter transitor.
3. This value applies when the base-emitter resistance (R_{BE}) is equal to or less than 500 Ω
4. This is the maximum voltage which should be applied to any output when it is in the off state.
5. Both halves of these dual circuits may conduct rated current simultaneously; however, power dissipation averaged over a short time interval must fall within the continuous dissipation rating.
6. For operation above 25°C free-air temperature, refer to Dissipation Derating Curve, Figure 20. This rating for the T package requires a heat sink that provides a thermal resistance from case to free-air, $R_{\theta CA}$, of not more than 95°C/W.

ELECTRICAL CHARACTERISTICS—OUTPUT TRANSISTORS

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
$V_{(BR)CBO}$	Collector-Base Breakdown Voltage	$I_C = 100\mu A$,	$I_E = 0$	35			V
$V_{(BR)CER}$	Collector-Emitter Breakdown Voltage	$I_C = 100\mu A$,	$R_{BE} = 500\ \Omega$	30			V
$V_{(BR)EBO}$	Emitter-Base Breakdown Voltage	$I_E = 100\mu A$,	$I_C = 0$	5			V
h_{FE}	Static Forward Current Transfer Ratio	$V_{CE} = 3\ V$, $T_A = 25°C$	$I_C = 100mA$,	25			
		$V_{CE} = 3V$, $T_A = 25°C$	$I_C = 300mA$,	30			
		$V_{CE} = 3\ V$, $T_A = -55°C$	$I_C = 100\ mA$,	10			
		$VCE = 3\ V$, $TA = -55°C$	$I_C = 300mA$,	15			
V_{BE}[1]	Base-Emitter Voltage	$I_B = 10\ mA$,	$I_C = 100\ mA$		0.85	1.2	V
		$I_B = 30\ mA$,	$I_C = 300\ mA$		1.05	1.4	
$V_{CE(sat)}$[1]	Collector-Emitter Saturation Voltage	$I_B = 10\ mA$,	$I_C = 100\ mA$		0.25	0.5	V
		$I_B = 30\ mA$,	$I_C = 300\ mA$		0.5	0.8	

†All typical values are at $V_{CC} = 5\ V$, $T_A = 25°C$ 1. These parameters must be measured using pulse techniques. $t_w = 300\ \mu s$, duty cycle $\leq 2\%$.

SWITCHING CHARACTERISTICS,–TTL GATES $V_{CC} = 5\ V$, $T_A = 25°C$

PARAMETER		TEST FIGURE	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	1	$C_L = 15\ pF$,	$R_L = 400\ \Omega$		12	22	ns
t_{PHL}	Propagation delay time, high-to-low-level output					8	15	na

OUTPUT TRANSISTORS

PARAMETER		TEST FIGURE	TEST CONDITIONS‡		MIN	TYP	MAX	UNIT
t_d	Delay time	2	$I_C = 200\ mA$,	$I_{B(1)} = 20\ mA$,		8	15	ns
t_r	Rise time		$I_{B(2)} = -40\ mA$,	$V_{BE(off)} = -1\ V$,		12	20	ns
t_s	Storage time		$C_L = 15\ pF$,	$R_L = 50\ \Omega$		7	15	ns
t_f	Fall time					6	15	ns

Voltage and current values shown are nominal; exact values vary slightly with transistor parameters.

PARAMETER MEASUREMENT INFORMATION

TEST CIRCUIT **VOLTAGE WAVEFORMS**

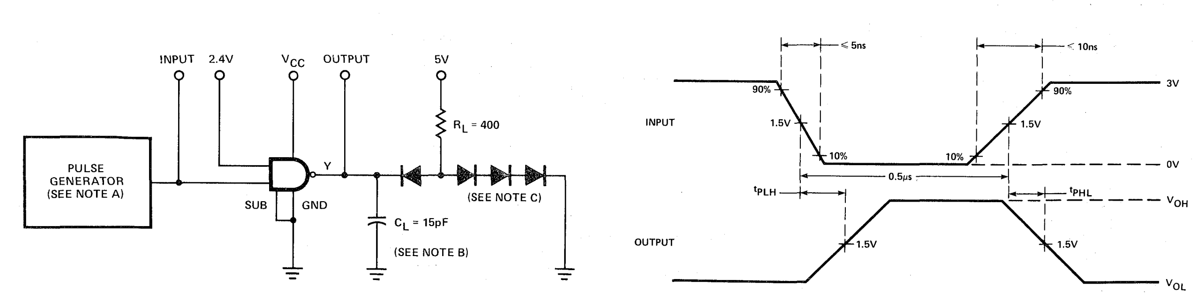
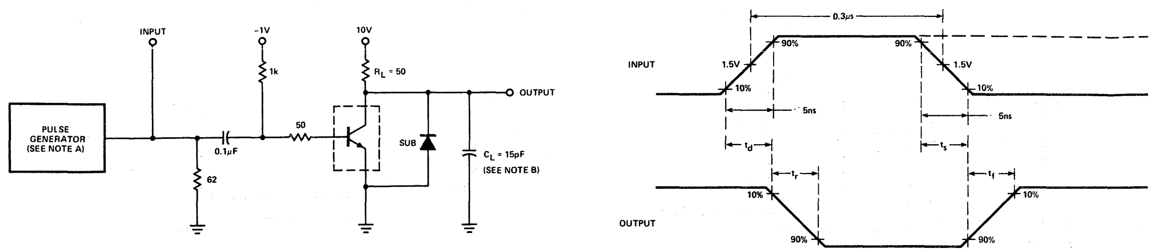


FIGURE 1

NOTE: All resistor values are typical and in ohms.

PARAMETER MEASUREMENT INFORMATION (CONT'D)



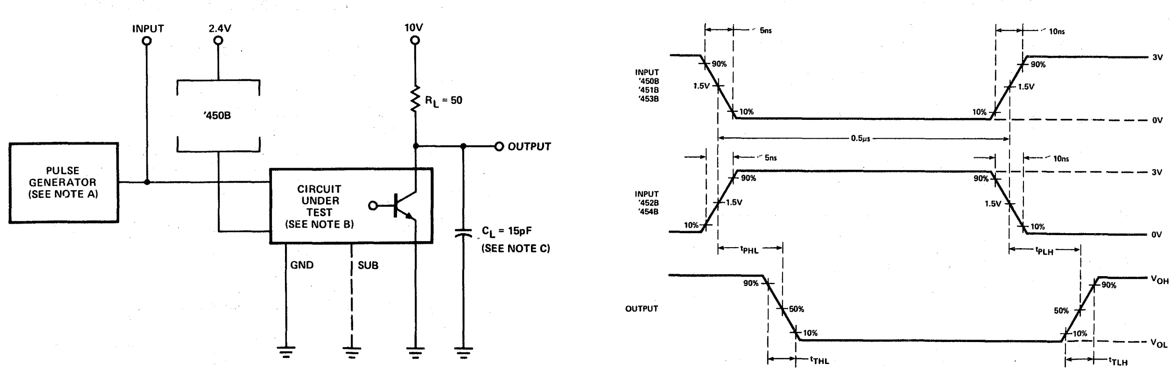
NOTE: All resistor values are typical and in ohms.

FIGURE 2—SWITCHING TIMES, EACH TRANSISTOR

GATES AND TRANSISTORS COMBINED

PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
tPLH Propagation delay time, low-to-high-level output	3	$I_C \approx$ 200mA, C_L = 15 pF, R_L = 50 Ω		20	30	ns
tPHL Propagation delay time, high-to-low-level output				20	30	ns
tTLH Transition time, low-to-high-level output				7	12	ns
tTHL Transition time, high-to-low-level output				9	15	ns
VOH High-level output voltage after switching	4	V_S = 20 V, $I_C \approx$ 300 mA, R_{BF} = 500 Ω	VS–6.5			mV

PARAMETER MEASUREMENT INFORMATION (CONT'D)



NOTE: All resistor values are typical and in ohms.

FIGURE 3—SWITCHING TIMES OF COMPLETE DRIVERS

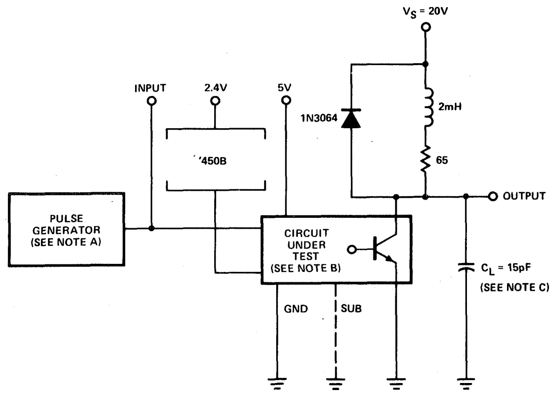
NOTES: A. The pulse generator has the following characteristics: PRR = 1 MHz, Zout ≈ 50 Ω

B. When testing 55450B or 75450B, connect output Y to transistor base and ground the substrate terminal.

C. CL includes probe and jig capacitance.

PARAMETER MEASUREMENT INFORMATION (cont'd)

TEST CIRCUIT



NOTE: ALL RESISTORS VALUES ARE TYPICAL AND IN OHMS.

VOLTAGE WAVEFORMS

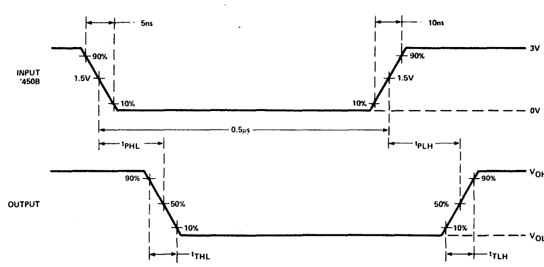


FIGURE 4 — LATCH-UP TEST OF COMPLETE DRIVERS

NOTES:
A. The pulse generator has the following characteristics: PRR = 12.5 kHz, Z_{out} = 50Ω.
B. When testing 55450B or 75450B, connect output Y to transistor base with a 500- Ω resistor from there to ground, and ground to substrate terminal.
C. C_L includes probe and jig capacitance.

TYPICAL CHARACTERISTICS CURVES

TTL GATE HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT

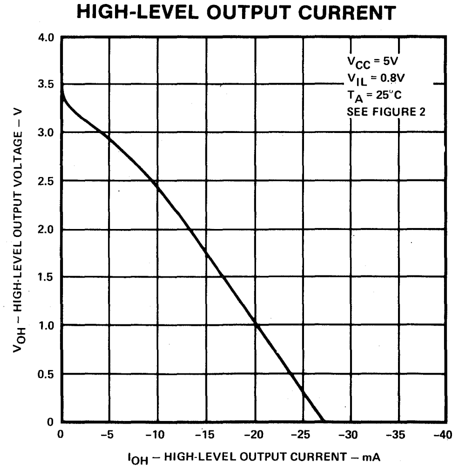


FIGURE 5

TRANSISTOR STATIC FORWARD CURRENT TRANSFER RATIO vs COLLECTOR CURRENT

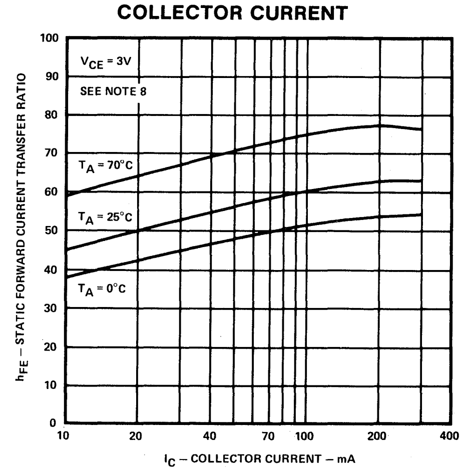


FIGURE 6

TYPICAL CHARACTERISTICS CURVES (cont'd)

TRANSISTOR BASE-EMITTER VOLTAGE vs COLLECTOR CURRENT

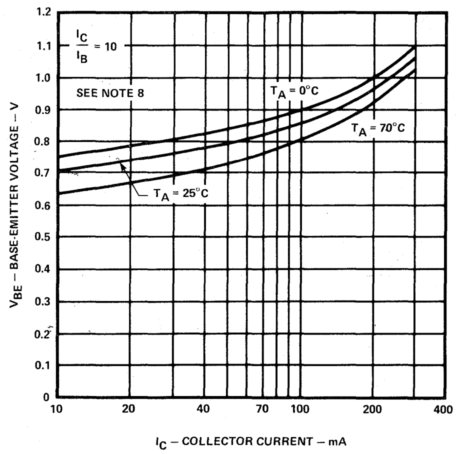


FIGURE 7

TRANSISTOR COLLECTOR-EMITTER SATURATION VOLTAGE vs COLLECTOR CURRENT

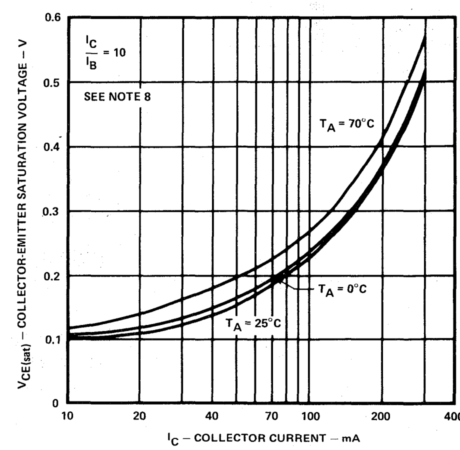


FIGURE 8

NOTE 8: These parameters must be measured using pulse techniques, tw = 300 μs, duty cycle ≤ 2%.

DISSIPATION DERATING CURVE

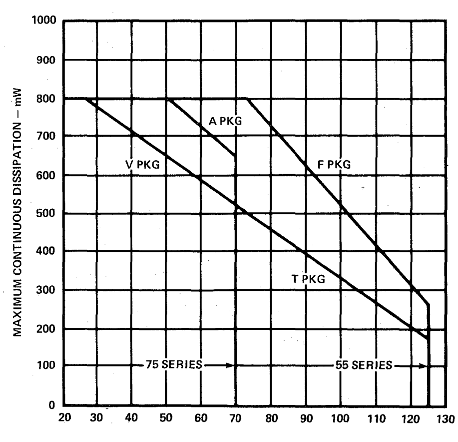


FIGURE 9

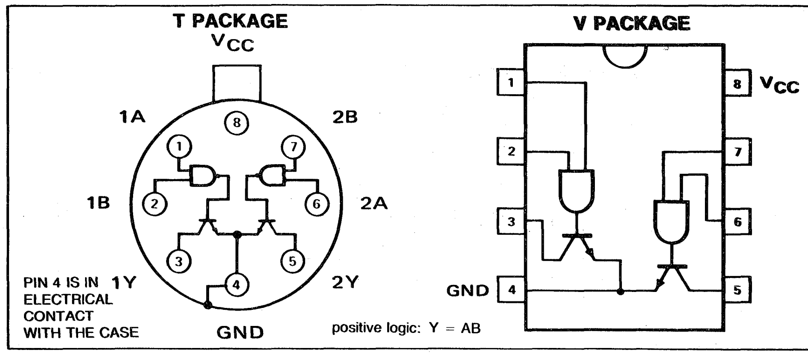
NOTE 9. THIS RATING FOR THE T PACKAGE REQUIRES A HEAT SINK THAT PROVIDES A THERMAL RESISTANCE FROM CASE TO FREE-AIR, $R_{\theta CA}$, OF NOT MORE THAN 95°C/WATT.

INTERFACE

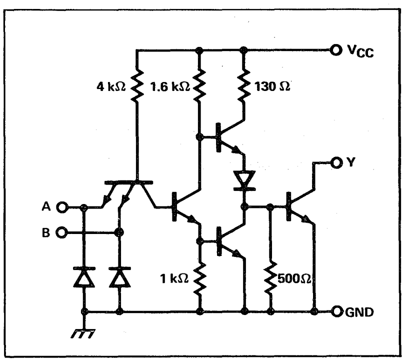
FEATURES

- 300mA OUTPUT CURRENT CAPABILITY
- HIGH VOLTAGE OUTPUTS
- NO OUTPUT LATCH-UP AT 20V
- HIGH SPEED SWITCHING
- CIRCUIT FLEXIBILITY FOR VARIED APPLICATIONS
- TTL OR DTL COMPATIBLE DIODE CLAMPED INPUTS
- STANDARD SUPPLY VOLTAGES

PIN CONFIGURATION



EQUIVALENT CIRCUIT (Each driver)



TRUTH TABLE

A	B	Y
L	L	L (on state)
L	H	L (on state)
H	L	L (on state)
H	H	H (off state)

ABSOLUTE MAXIMUM RATINGS

		55451B	75451B	UNIT
Supply voltage, V_{CC} (see Note 1)		7	7	V
Input voltage		5.5	5.5	V
Interemitter voltage (see Note 2)		5.5	5.5	V
V_{CC}-to-substrate voltage				V
Collector-to-substrate voltage				V
Collector base voltage				V
Collector-emitter voltage (see Note 3)				V
Emitter-base voltage				V
Output voltage (see Note 4)		30	30	V
Collector current (see Note 5)				mA
Output current (see Note 5)		300	300	mA
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 6)		800	800	mW
Operating free-air temperature range		55 to 125	0 to 70	°C
Storage temperature range		65 to 150	−65 to 150	°C
Lead temperature 1/16 inch from case for 60 seconds	F or T package	300	300	°C
Lead temperature 1/16 inch from case for 10 seconds	A or V package	260	260	°C

NOTES:
1. Voltage values are with respect to network ground terminal unless otherwise specified.
2. This is the voltage between two emitters of a multiple-emitter transistor.
3. This value applies when the base-emitter resistance (R_{BE}) is equal to or less than 500 Ω.
4. This is the maximum voltage which should be applied to any output when it is in the off state.
5. Both halves of these dual circuits may conduct rated current simultaneously; however, power dissipation averaged over a short time interval must fall within the continuous dissipation rating.
6. For operation above 25°C free-air temperature, refer to Dissipation Derating Curve, Figure 20. This rating for the T package requires a heat sink that provides a thermal resistance from case to free-air, $R_{\theta CA}$, of not more than 95°C/W.

SWITCHING CHARACTERISTICS, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	3	$I_O \approx 200$ mA, $C_L = 15$ pF, $R_L = 50\Omega$		18	25	ns
t_{PHL}	Propagation delay time, high-to-low-level output				18	25	ns
t_{TLH}	Transition time, low-to-high-level output				5	8	ns
t_{THL}	Transition time, high-to-low-level output				7	12	ns
V_{OH}	High-level output voltage after switching	4	$V_S = 20$ V, $I_O \approx 300$ mA	V_S−6.5			mV

PARAMETER MEASUREMENT INFORMATION

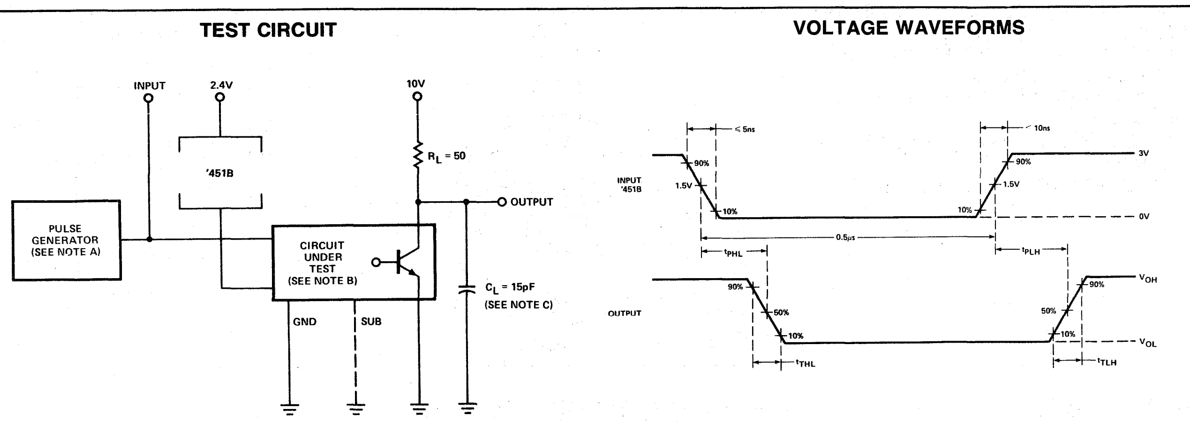


FIGURE 3 — SWITCHING TIMES OF COMPLETE DRIVERS

NOTES: A. The pulse generator has the following characteristics: PRR = 1 MHz, $Z_{out} \approx 50\ \Omega$

B. When testing 55450B or 75450B, connect output Y to translator base and ground the substrate terminal.

C. C_L includes probe and jig capacitance.

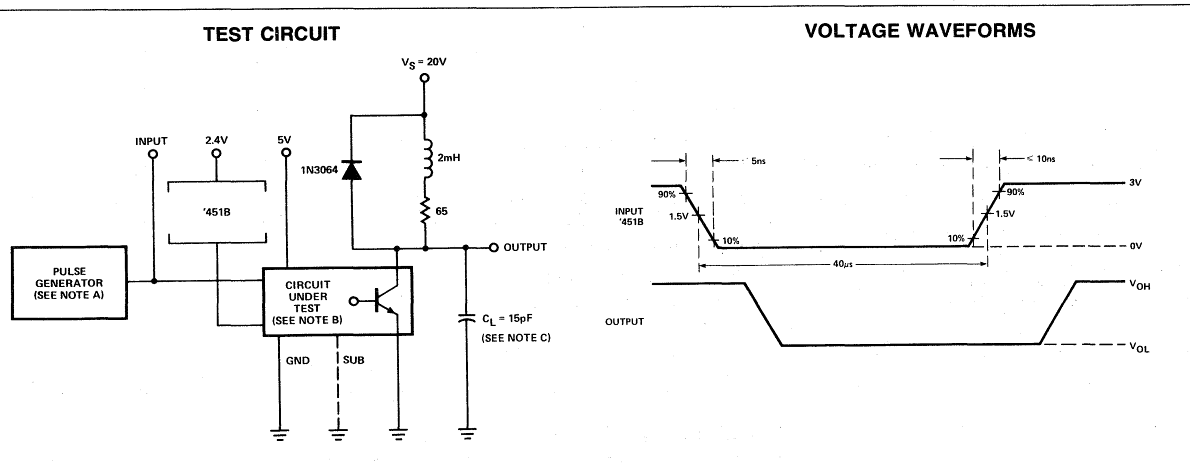


FIGURE 4 — LATCH-UP TEST OF COMPLETE DRIVERS

NOTES: A. The pulse generator has the following characteristics: PRR = 12.5 kHz, $Z_{out} = 50\Omega$.

When testing 55450B or 75450B, connect output Y to transistor base with a 500-Ω resistor from there to ground, and ground the substrate terminal.

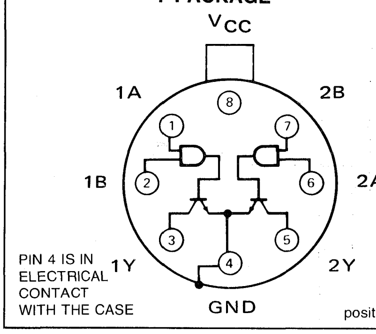
C. C_L includes probe and jig capacitance.

FEATURES

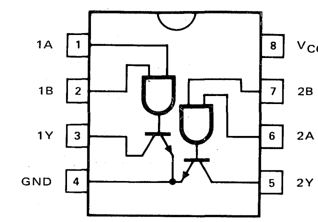
- 300 mA OUTPUT CURRENT CAPABILITY
- HIGH VOLTAGE OUTPUTS
- NO OUTPUT LATCH UP AT 20V
- HIGH SPEED SWITCHING
- CIRCUIT FLEXIBILITY FOR VARIED APPLICATIONS
- TTL OR DTL COMPATIBLE DIODE — CLAMPED INPUTS
- STANDARD SUPPLY VOLTAGES

PIN CONFIGURATION

T PACKAGE



V PACKAGE



positive logic: Y = AB

TRUTH TABLE

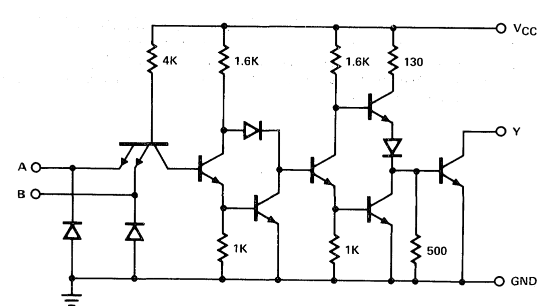
A	B	Y
L	L	H (off state)
L	H	H (off state)
H	L	H (off state)
H	H	L (on state)

NOTES:
1. Voltage values are with respect to network ground terminal unless otherwise specified.
2. This is the voltage between two emitters of a multiple emitter transistor.
3. This value applies when the base-emitter resistance (R_{BB}) is equal to or less than 500Ω.
4. This is the maximum voltage which should be applied to any output when it is in the off state.
5. Both halves of these dual circuits may conduct rated current simultaneously; however, power dissipation averaged over a short time interval must fall within the continuous dissipation rating.
6. For operation above 25°C free-air temperature, refer to Dissipation Derating Curve, Figure 20. This rating for the T package requires a heat sink that provides a thermal resistance from case to free-air, $R_{\theta CA}$, of not more than 95°C/W.

ABSOLUTE MAXIMUM RATINGS

		55452B	75452B	UNIT
Supply voltage, V_{CC} (see Note 1)		7	7	V
Input voltage		5.5	5.5	V
Interemitter voltage (see Note 2)		5.5	5.5	V
V_{CC}-to-substrate voltage				V
Collector-to-substrate voltage				V
Collector-base voltage				V
Collector-emitter voltage (see Note 3)				V
Emitter-base voltage				V
Output voltage (see Note 4)		30	30	V
Collector current (see Note 5)				mA
Output current (see Note 5)		300	300	mA
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 6)		800	800	mW
Operating free-air temperature range		55 to 125	0 to 70	°C
Storage temperature range		65 to 150	−65 to 150	°C
Lead temperature 1/16 inch from case for 60 seconds	F or T package	300	300	°C
Lead temperature 1/16 inch from case for 10 seconds	A or V package	260	260	°C

EQUIVALENT CIRCUIT (Each Driver)



SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	$I_O \approx$ 200 mA, C_L = 15 pF, R_L = 50Ω		26	35	ns
t_{PHL}	Propagation delay time, high-to-low-level output			24	35	ns
t_{TLH}	Transition time, low-to-high-level output			5	8	ns
t_{THL}	Transition time, high-to-low-level output			7	12	ns
V_{OH}	High-level output voltage after switching	V_S = 20V, $I_O \approx$ 300 mA	V_S −6.5			mV

PARAMETER MEASUREMENT INFORMATION

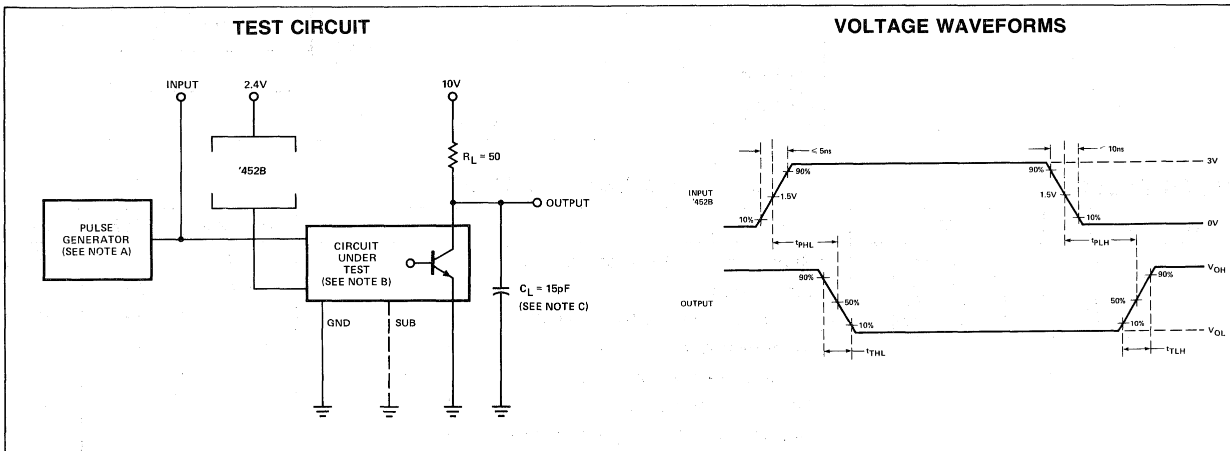


FIGURE 3 - SWITCHING TIMES OF COMPLETE DRIVERS

NOTES: A. The pulse generator has the following characteristics: PRR = 1 MHz, Zout ≈ 50Ω
B. When testing 55450B or 75450B, connect output Y to transistor base and ground the substrate terminal.
C. CL includes probe and jig capacitance.

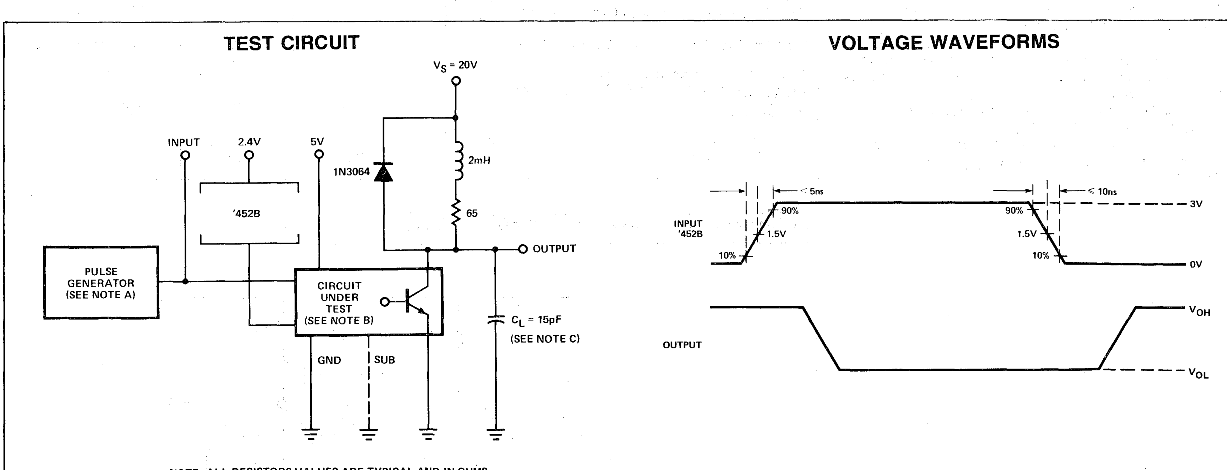


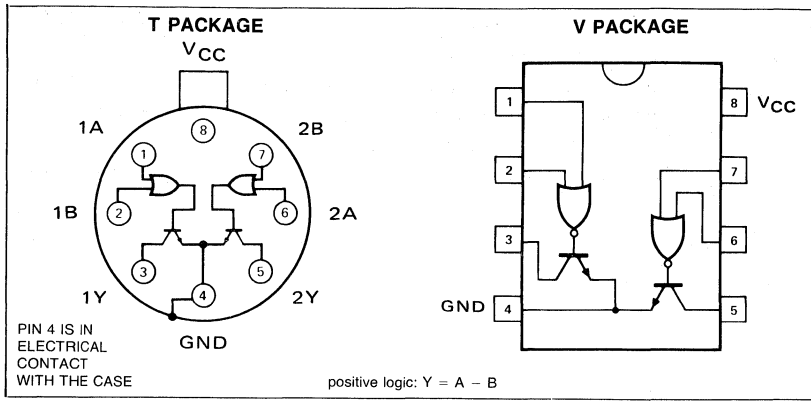
FIGURE 4 - LATCH-UP TEST OF COMPLETE DRIVERS

NOTES: A. The pulse generator has the following characteristics: PRR = 12.5 kHz, Zout = 50Ω
B. When testing 55450B or 75450B, connect output Y to transistor base with a 500-Ω resistor from there to ground, and ground the substrate terminal
C. CL includes probe and jig capacitance.

FEATURES

- 300 mA WITH CURRENT CAPABILITY
- HIGH VOLTAGE OUTPUTS
- NO OUTPUT LATCH UP AT 20V
- HIGH SPEED SWITCHING
- CIRCUIT FLEXIBILITY FOR VARIED APPLICATIONS
- TTL OR DTL COMPATIBLE DIODE — CLAMPED INPUTS

PIN CONFIGURATION



TRUTH TABLE

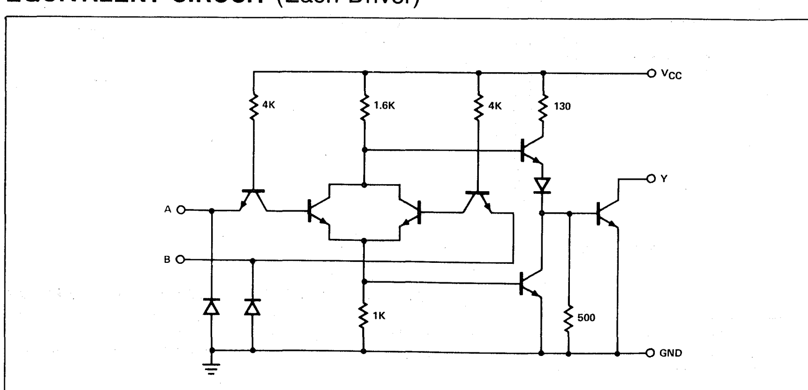
A	B	Y
L	L	L (off state)
L	H	H (off state)
H	L	H (off state)
H	H	H (on state)

ABSOLUTE MAXIMUM RATINGS

		55452B	75452B	UNIT
Supply voltage, V_{CC} (see Note 1)		7	7	V
Input voltage		5.5	5.5	V
Interemitter voltage (see Note 2)		5.5	5.5	V
V_{CC}-to-substrate voltage				V
Collector-to-substrate voltage				V
Collector-base voltage				V
Collector-emitter voltage (see Note 3)				V
Emitter-base voltage				V
Output voltage (see Note 4)		30	30	V
Collector current (see Note 5)				mA
Output current (see Note 5)		300	300	mA
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 6)		800	800	mW
Operating free-air temperature range		−55 to 125	0 to 70	°C
Storage temperature range		−65 to 150	−65 to 150	°C
Lead temperature 1/16 inch from case for 60 seconds	F or T package	300	300	°C
Lead temperature 1/16 inch from case for 10 seconds	A or V package	260	260	°C

NOTES:
1. Voltage values are with respect to network ground terminal unless otherwise specified.
2. This is the voltage between two emmitters of a multiple emitter transistor.
3. This value applies when the base-emitter resistance (R_{BB}) is eaual to or less than 500Ω.
4. This is the maximum voltage which should be applied to any output when it is in the off state.
5. Both halves of these d d circuits may conduct rated current simultaneously; however, power dissipation averaged over a short time interval must fall within the continuous dissipation rating.
6. For operation above 25°C free-air temperature, refer to Dissipation Derating Curve, Figure 20. This rating for the T package requires a heat sink that provides a thermal resistance from case to free-air, $R_{\theta CA}$, of not more than 95°C/W.

EQUIVALENT CIRCUIT (Each Driver)



SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

SYMBOL	PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	3	$I_O \approx$ 200 mA, C_L = 15 pF, R_L = 50Ω		26	25	ns
t_{PHL}	Propagation delay time, high-to-low-level output				24	25	ns
t_{TLH}	Transition time, low-to-high-level output				5	8	ns
t_{THL}	Transition time, high-to-low-level output				7	12	ns
V_{OH}	High-level output voltage after switching	4	V_S = 20V, $I_O \approx$ 300 mA	V_S −6.5			mV

PARAMETER MEASUREMENT INFORMATION

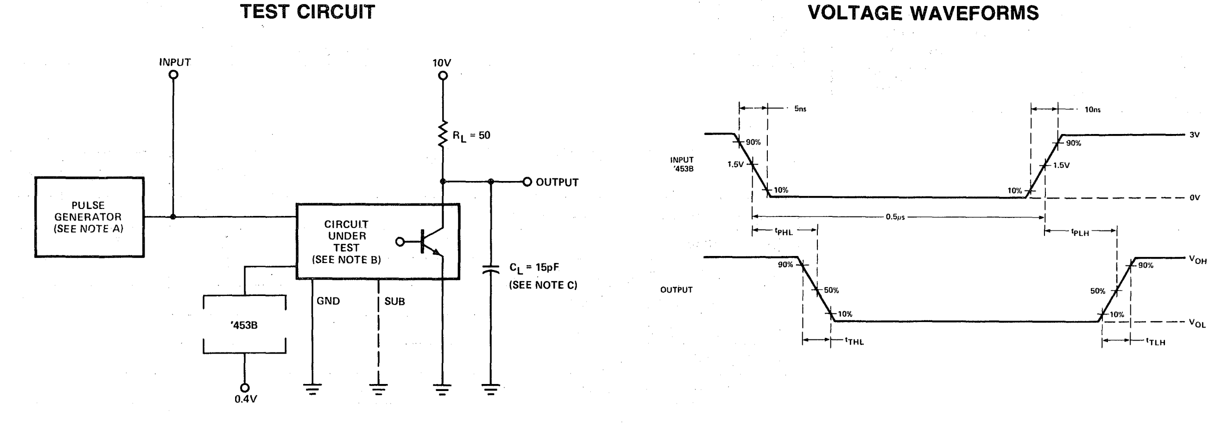


FIGURE 3 - SWITCHING TIMES OF COMPLETE DRIVERS

NOTES: A. The pulse generator has the following characteristics: PRR = 1 MHz, $Z_{out} \approx$ 50Ω

B. When testing 65460B or 75450B, connect output Y to transistor base and ground the substrate terminal.

C. C_L includes probe and jig capacitance.

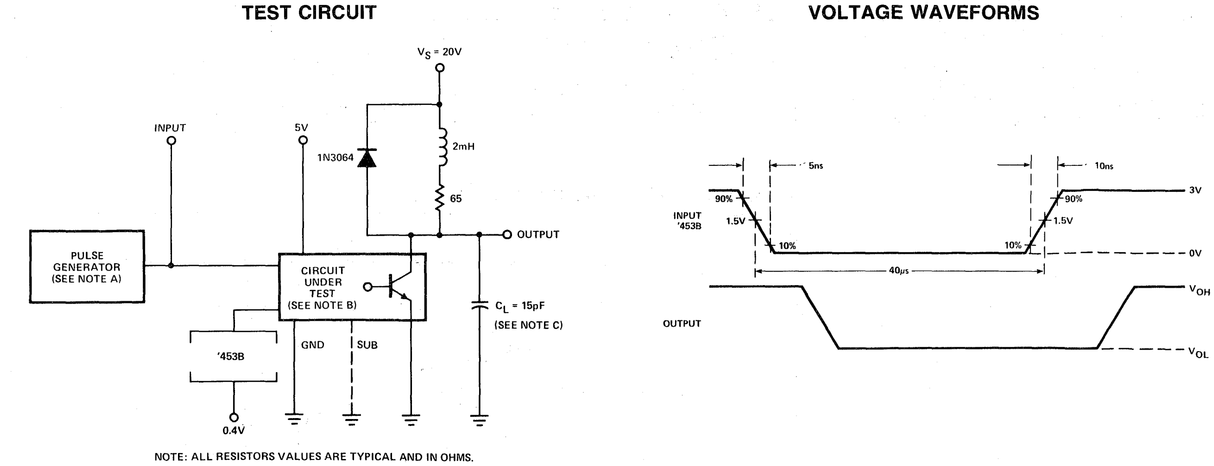


FIGURE 4 - LATCH-UP TEST OF COMPLETE DRIVERS

NOTES: A. The pulse generator has the following characteristics: PRR = 12.5 kHz, Z_{out} = 50Ω

B. When testing 55450B or 75450B, connect output Y to transistor base with a 500-Ω resistor from there to ground, and ground the substrate terminal.

C. C_L includes probe and jig capacitance.

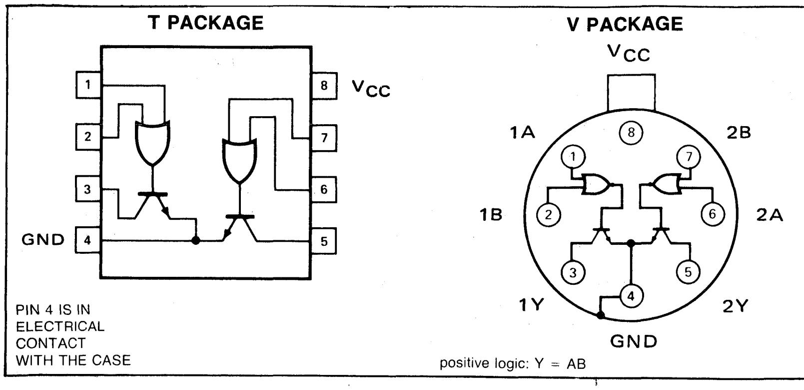
FEATURES

- 300 mA OUTPUT CURRENT CAPABILITY
- HIGH VOLTAGE OUTPUTS
- NO OUTPUT LATCH UP AT 20V
- HIGH SPEED SWITCHING
- CIRCUIT FLEXIBILITY FOR VARIED APPLICATIONS
- TTL OR DTL COMPATIBLE DIODE — CLAMPED INPUTS
- STANDARD SUPPLY VOLTAGES

TRUTH TABLE

A	B	Y
L	L	H (off state)
L	H	H (on state)
H	L	H (on state)
H	H	L (on state)

PIN CONFIGURATION

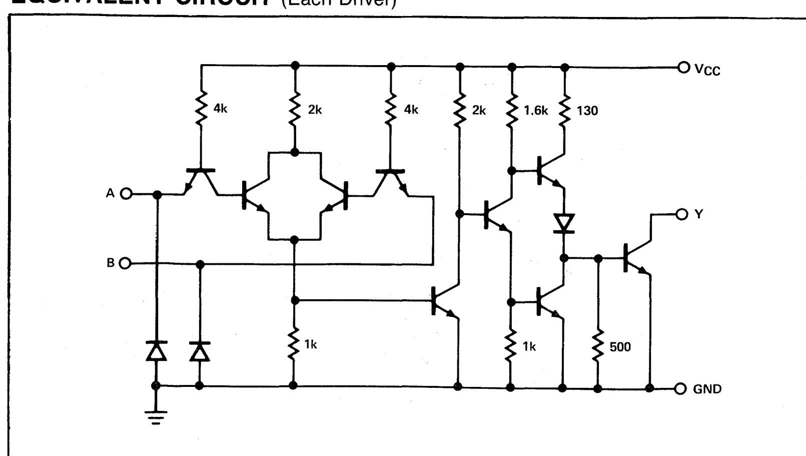


ABSOLUTE MAXIMUM RATINGS

		55452B	75452B	UNIT
Supply voltage, V_{CC} (see Note 1)		7	7	V
Input voltage		5.5	5.5	V
Interemitter voltage (see Note 2)		5.5	5.5	V
V_{CC}-to-substrate voltage				V
Collector-to-substrate voltage				V
Collector-base voltage				V
Collector-emitter voltage (see Note 3)				V
Emitter-base voltage				V
Output voltage (see Note 4)		30	30	V
Collector current (see Note 5)				mA
Output current (see Note 5)		300	300	mA
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 6)		800	800	mW
Operating free-air temperature range		−55 to 125	0 to 70	°C
Storage temperature range		−65 to 150	−65 to 150	°C
Lead temperature 1/16 inch from case for 60 seconds	F or T package	300	300	°C
Lead temperature 1/16 inch from case for 10 seconds	A or V package	260	260	°C

NOTES:
1. Voltage values are with respect to network ground terminal unless otherwise specified.
2. This is the voltage between two emitters of a multiple emitter transistor.
3. This value applies when the base-emitter resistance (R_{BB}) is equal to or less than 500Ω.
4. This is the maximum voltage which should be applied to any output when it is in the off state.
5. Both halves of these dual circuits may conduct rated current simultaneously; however, power dissipation averaged over a short time interval must fall within the continuous dissipation rating.
6. For operation above 25°C free-air temperature, refer to Dissipation Derating Curve, Figure 20. This rating for the T package requires a heat sink that provides a thermal resistance from case to free-air, $R_{\theta CA}$, of not more than 95°C/W.

EQUIVALENT CIRCUIT (Each Driver)



SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C

SYMBOL	PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output				27	35	ns
t_{PHL}	Propagation delay time, high-to-low-level output		I_O 200mA, C_L = 15 pF,		24	35	ns
t_{TLH}	Transition time, low-to-high-level output	3	R_L = 50		5	8	ns
t_{THL}	Transition time, high-to-low-level output				7	12	ns
V_{OH}	High-level output voltage after switching	4	V_S = 20 V, I_O 300 mA	V_S-6.5			mV

PARAMETER MEASUREMENT INFORMATION

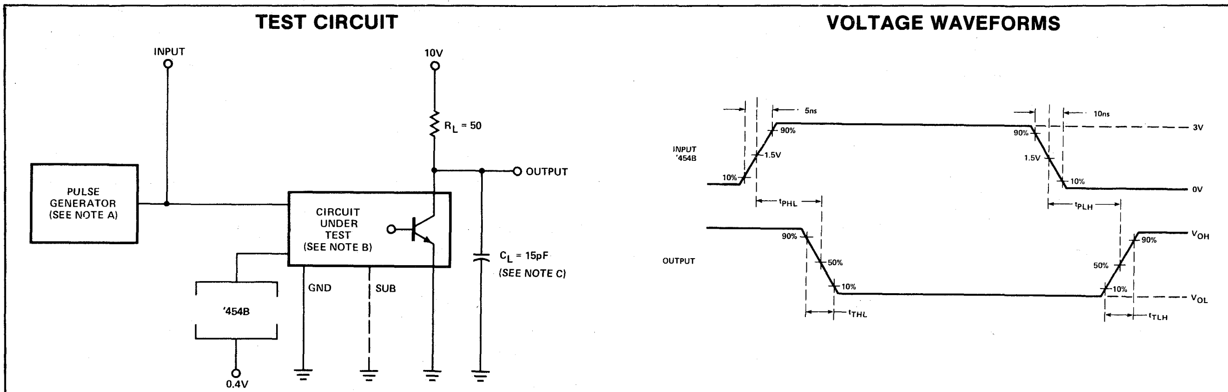
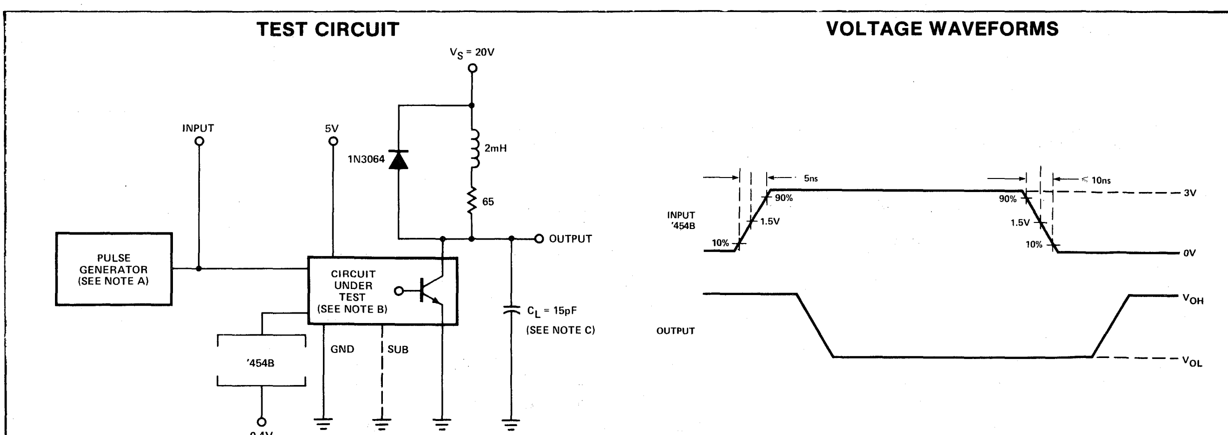


FIGURE 3 — SWITCHING TIMES OF COMPLETE DRIVERS

NOTES:
A. The pulse generator has the following characteristics: PRR = 1 MHz, $Z_{out} \approx 50\Omega$
B. When testing 55450B or 75450B, connect output Y to transistor base and ground the substrate terminal.
C. CL includes probe and jig capacitance.



NOTE: ALL RESISTORS VALUES ARE TYPICAL AND IN OHMS.

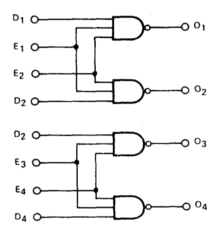
FIGURE 4 — LATCH-UP TEST OF COMPLETE DRIVERS

NOTES:
A. The pulse generator has the following characteristics: PRR = 12.5 kHz, Z_{out} = 50Ω
B. When testing 55450B or 75450B, connect output Y to transistor base with a 500-Ω resistor from there to ground, and ground to substrate terminal.
C. CL includes probe and jig capacitance.

FEATURES

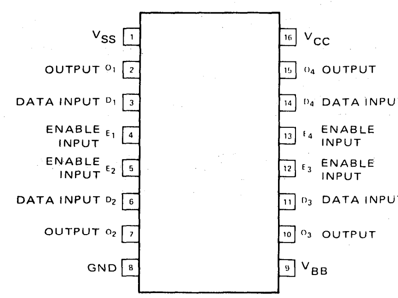
- DTL/TTL COMPATIBLE INPUTS
- 1103 AND 1103A RAM COMPATIBLE OUTPUTS
- HIGH OUTPUT SOURCE/SINK CURRENT CAPABILITY — 100mA
- HIGH SPEED — 45ns MAX. tD WITH 200 pFd LOAD
- INPUT AND OUTPUT DIODE CLAMPING TO MINIMIZE LINE REFLECTION
- HIGH INPUT BREAKDOWN VOLTAGE — 19 VOLTS

LOGIC DIAGRAM



PIN CONFIGURATION

F PACKAGE



ABSOLUTE MAXIMUM RATINGS

Operating Temperature Range	0° to 70°C
Storage Temperature	−65° to +150°C
Input Voltage Ranges	−0.5 to +21VDC
V_{CC} Supply Voltage Range	−0.5 to +7.0VDC
Output Voltage Range (with respect to ground)	−0.5 to +25VDC
V_{SS} Voltage Range (with respect to ground)	−0.5 to +25VDC
V_{BB} Voltage Range	−0.5 to +25VDC

A.C. CHARACTERISTICS T_A = 0°C to 70°C, V_{CC} = 5V ±5%, V_{BB} = V_{SS} +3 to 4V, f = 2MHz, 50% Duty Cycle

	PARAMETERS	DELAY DIFFERENTIAL (1) C_L = 200 pF max.	C_L=100 pF MIN	C_L=100 pF MAX	C_L=200 pF MIN	C_L=200 pF MAX
t_{+-}	INPUT TO OUTPUT DELAY	5	5	15	5	15
t_{-+}	INPUT TO OUTPUT DELAY	10	5	25	5	25
t_r	OUTPUT RISE TIME	10	5	20	5	30
t_f	OUTPUT FALL TIME	10	5	20	10	30
t_D	DELAY + RISE OR FALL TIME	10	10	35	20	45

(1) This is defined as the maximum skew between any output in the same package, e.g., all the input to output delays for the t−+ parameter are within a maximum of 10nsec of each other in the same package.

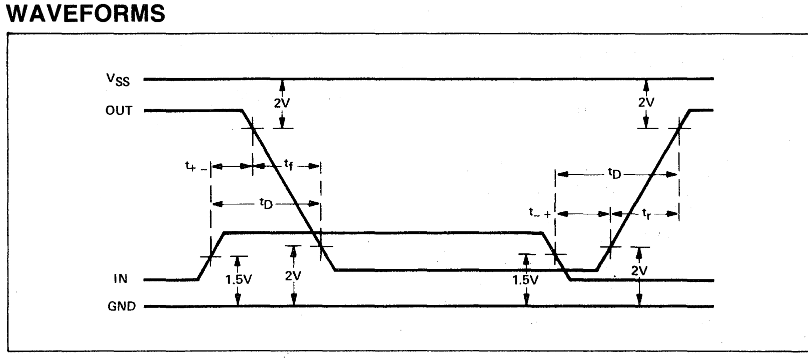
D.C. CHARACTERISTICS T_A = 0°C to 70°C, V_{CC} = 5V ±5%, V_{SS} = 16V ±5%, V_{BB} = V_{SS} +3.0V to 4.0V

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNITS
I_{FD}	Data Input Load Current	V_D = 0.45V, V_{CC} = 5.25V, All Other Inputs at 5.25V, V_{SS} = 16V, V_{BB} = 19V		−0.25	mA
I_{FE}	Enable Input Load Current	V_E = 0.45V, V_{CC} = 5.25V, All Other Inputs at 5.25V, V_{SS} = 16V, V_{BB} = 19V		−0.50	mA
I_{RD}	Data Input Leakage Current	V_D = 19V, V_{CC} = 5.0V, All Other Inputs Grounded, V_{SS} = 16V, V_{BB} = 19V		20	μA
I_{RE}	Enable Input Leakage Current	V_D = 19V, V_{CC} = 5.0V, All Other Inputs Grounded, V_{SS} = 16V, V_{BB} = 19V		20	μA

D.C. CHARACTERISTICS (Cont'd) T_A = 0°C to 70°C, V_{CC} = 5V ±5%, V_{SS} = 16V ±5%, V_{BB} = V_{SS} +3.0V to 4.0V

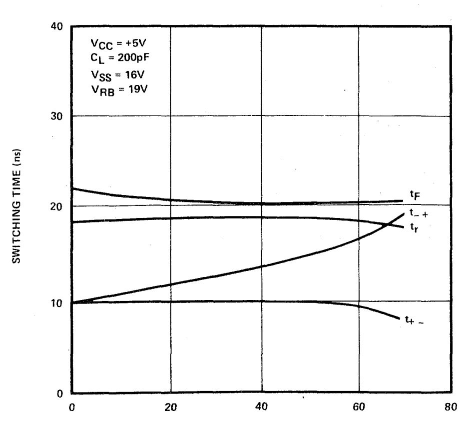
SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNITS
POWER SUPPLY CURRENT DRAIN: All Outputs "Low"					
I_{CC}	Current from V_{CC}	V_{CC} = 5.25V, V_{SS} = 16.8V		83	mA
I_{SS}	Current from V_{SS}			250	μA
I_{BB}	Current from V_{BB}	V_{BB} = 20.8V All Inputs High		21	mA
P_{TOTAL}	Total Power Dissipation			900	mW
All Outputs "High"					
I_{CC}	Current from V_{CC}	V_{CC} = 5.25V, V_{SS} = 16.8V		33	mA
I_{SS}	Current from V_{SS}	V_{BB} = 20.8V		250	μA
I_{BB}	Current from V_{BB}	All Inputs High		3	mA
P_{TOTAL}	Total Power Dissipation			250	mW
STANDBY CONDITION WITH V_{CC} = 0V, V_{SS} = V_{BB}					
I_{CC}	Current from V_{CC}	V_{CC} = 0V, V_{SS} = 16.8V V_{BB} = 16.8V		0	mA
I_{SS}	Current from V_{SS}			250	μA
I_{BB}	Current from V_{BB}			250	μA
P_{TOTAL}	Total Power Dissipation			10	mW

WAVEFORMS

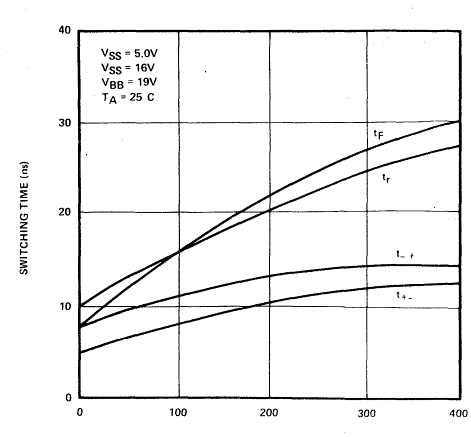


TYPICAL CHARACTERISTICS

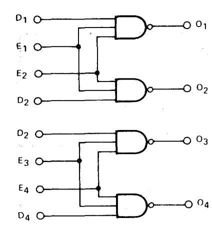
SWITCHING TIME VS. AMBIENT TEMPERATURE



SWITCHING TIME VS. LOAD CAPACITANCE

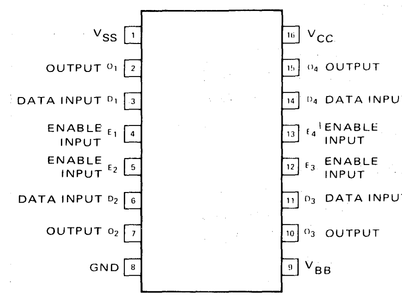


LOGIC DIAGRAM



PIN CONFIGURATION

F PACKAGE



ABSOLUTE MAXIMUM RATINGS

Operating Temperature Range	0° to 70°C
Storage Temperature	−65° to +150°C
Input Voltage Ranges	−0.5 to +21VDC
V_{CC} Supply Voltage Range	−0.5 to +7.0VDC
Output Voltage Range (with respect to ground)	−0.5 to +25VDC
V_{SS} Voltage Range (with respect to ground)	−0.5 to +25VDC
V_{BB} Voltage Range	−0.5 to +25VDC

A.C. CHARACTERISTICS T_A = 0°C to 55°C, V_{CC} = 5V ±5%, V_{SS} = 19V ±5%, V_{BB} = V_{SS} +3 to 4V, f = 2MHz, 50% Duty Cycle

PARAMETERS		DELAY DIFFERENTIAL (1) C_L = 200 pF max.	C_L=100 pF MIN	C_L=100 pF MAX	C_L=200 pF MIN	C_L=200 pF MAX
t_{+-}	INPUT TO OUTPUT DELAY	5	5	15	5	15
t_{-+}	INPUT TO OUTPUT DELAY	10	5	25	5	25
t_r	OUTPUT RISE TIME	10	5	20	5	30
t_f	OUTPUT FALL TIME	10	5	20	10	30
t_D	DELAY + RISE OR FALL TIME	10	10	35	20	45

(1) This is defined as the maximum skew between any output in the same package, e.g., all the input to output delays for the t−+ parameter are within a maximum of 10nsec of each other in the same package.

D.C. CHARACTERISTICS T_A = 0°C to 55°C, V_{CC} = 5V ±5%, V_{SS} = 19V ±5%, V_{BB} −V_{SS} = 3.0V to 4.0V

PARAMETER		CONDITIONS	MIN	MAX	UNITS
I_{FD}	Data Input Load Current	V_D = 0.45V, V_{CC} = 5.25V, All Other Inputs at 5.25V, V_{SS} = 16V, V_{BB} =19V		−0.25	mA
I_{FE}	Enable Input Load Current	V_E = 0.45V, V_{CC} = 5.25V, All Other Inputs at 5.25V, V_{SS} = 16V, V_{BB} =19V		−0.50	mA
I_{RD}	Data Input Leakage Current	V_D = 19V, V_{CC} = 5.0V, All Other Inputs Grounded, V_{SS} = 16V, V_{BB} =19V		20	μA
I_{RE}	Enable Input Leakage Current	V_D = 19V, V_{CC} = 5.0V, All Other Inputs Grounded, V_{SS} = 16V, V_{BB} =19V		20	μA
C_{IN}	INPUT CAPACITANCE	V_{BIAS} =2.0V, V_{CC} = 0V		8 (Typical)	pF

D.C. CHARACTERISTICS (Cont'd) T_A = 0°C to 55°C, V_{CC} = 5V ±5%, V_{SS} = 19V ±5%, $V_{BB} - V_{SS}$ = 3.0V to 4.0V

PARAMETER		CONDITIONS	MIN	MAX	UNITS
POWER SUPPLY CURRENT DRAIN:					
All Outputs "Low"					
I_{CC}	Current from V_{CC}	V_{CC} = 5.25V, V_{SS} = 20V		83	mA
I_{SS}	Current from V_{SS}			250	μA
I_{BB}	Current from V_{BB}	V_{BB} = 24V All Inputs Open		25	mA
P_{TOTAL}	Total Power Dissipation			1040	mW
All Outputs "High"					
I_{CC}	Current from V_{CC}	V_{CC} = 5.25V, V_{SS} = 20V		33	mA
I_{SS}	Current from V_{SS}	V_{BB} = 24V		250	μA
I_{BB}	Current from V_{BB}	All Inputs Grounded		5	mA
P_{TOTAL}	Total Power Dissipation			297	mW
STANDBY CONDITION WITH V_{CC} = OV, V_{SS} = V_{BB}					
I_{CC}	Current from V_{CC}	V_{CC} = 0V, V_{SS} = 20V		0	mA
I_{SS}	Current from V_{SS}	V_{BB} = 20V		500	μA
I_{BB}	Current from V_{BB}			500	μA
P_{TOTAL}	Total Power Dissipation			15	mW

FEATURES

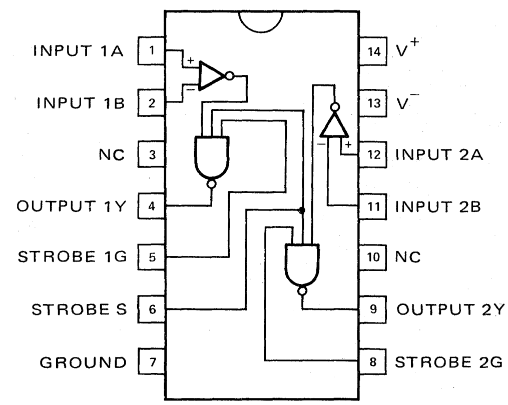
- FUNCTIONALLY EQUIVALENT AND PIN COMPATIBLE TO SN75207
- 17ns MAXIMUM GUARANTEED PROPAGATION DELAY
- 20μA MAXIMUM INPUT BIAS CURRENT
- STTL COMPATIBLE STROBES AND OUTPUTS
- LARGE COMMON MODE INPUT VOLTAGE RANGE
- OPERATES FROM STANDARD SUPPLY VOLTAGES

ABSOLUTE MAXIMUM RATINGS

Positive Supply Voltage (V+)	+7V
Negative Supply Voltage (V−)	−7V
Differential input voltage	±6V
Common mode input voltage	±5V
Strobe/Gate input voltage	+5.5V
Power Dissipation	600mw
Operating Temperature Range	0°C to 70°C
Storage temperature range	−65°C to +150°C
Lead temperature (Soldering 60 seconds)	+300°C

PIN CONFIGURATION

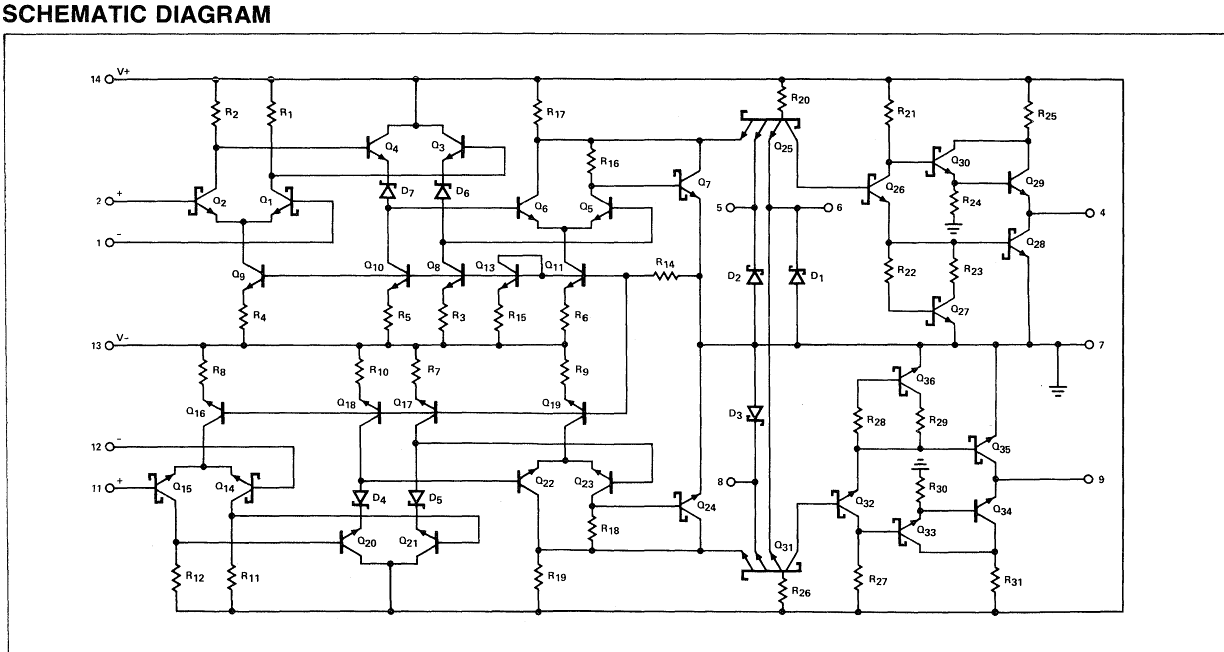
A, F PACKAGE



APPLICATIONS

HIGH SPEED LINE RECEIVER
MOS MEMORY SENSE AMP
A/D CONVERSION

SCHEMATIC DIAGRAM



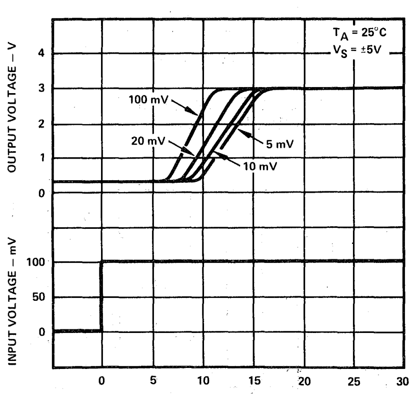
ELECTRICAL CHARACTERISTICS V+ = +5.00, V− = −5.00, T_A = 0 to 70°C (Unless Otherwise Noted).

PARAMETER	TEST CONDITIONS	75S207 MIN	TYP	MAX	UNIT
Amplifier Input					
Input offset voltage	V+ = 4.75, V− = −4.75			10	mV
Input Bias Current a 25°C	V+ = 5.25, V− = −5.25		7.5	20	μA
over temp range	V+ = 5.25, V− = −5.25			40	μA
Input offset current a 25°C	V+ = 5.25, V− = −5.25		1.0	5	μA
over temp range	V+ = 5.25, V− = −5.25			12	μA
Input common mode voltage range	V+ = 4.75, V− = −4.75	±3			V
Input resistance			4		kΩ
Input capacitance			3	6	pF
Voltage gain			5		V/mV
Power Supply Requirements					
Supply Voltage					
V+		4.75	5.00	5.25	V
V−		−4.75	−5.00	−5.25	V
Large Signal Switching Speed					
TpLH (D) low to high propagation delay from amp inputs to output	R_L = 280ΩC_L = 15 pF T_A = 25°C Note 1		12	17	ns
TpHL (D) high to low propagation delay from amp inputs to output	R_L = 280Ω C_L = 15 pF T_A = 25°C Note 1		9	13	ns
TpLH (S) low to high propagation delay from strobes input to output	R_L = 280Ω C_L = 15 pF T_A = 25°C Note 2		4.5	6	ns
TpHL (S) high to low propagation delay strobe input to output	R_L = 280Ω C_L = 15 pF T_A = 25°C Note 2		3.0	4.5	ns
Maximum Operating Frequency	R_L = 280Ω C_L = 15 pF T_A = 25°C	40	55		MHz

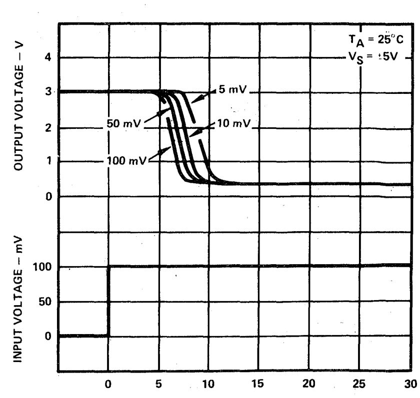
NOTES:
1. Response time measured from 0V point of ±100 mV P-P 10MHz square wave to the 1.5 point of the output.
2. Response time measured from 1.5V point of input to 1.5V point of the output.
3. Response time measured from the start of a 100mV input step with 5mV overdrive to the 1.5V point of the output.

TYPICAL PERFORMANCE CHARACTERISTICS

RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



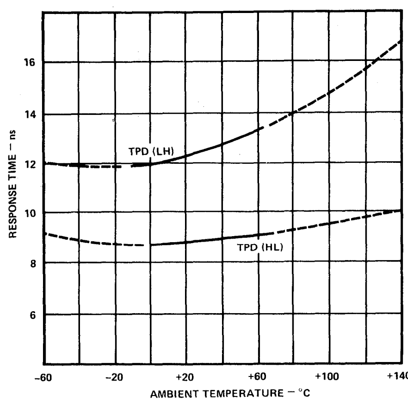
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



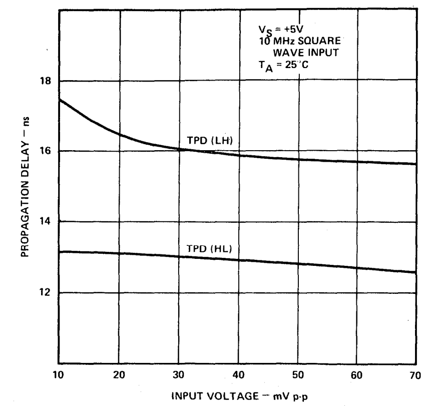
INTERFACE

TYPICAL PERFORMANCE CHARACTERISTICS

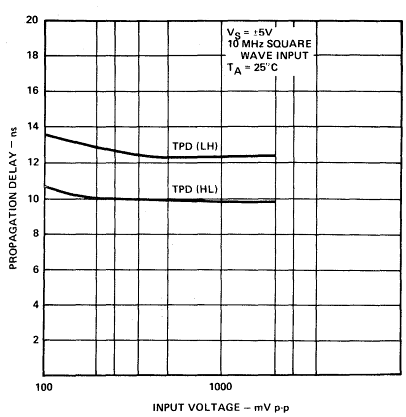
RESPONSE TIME VS. TEMPERATURE



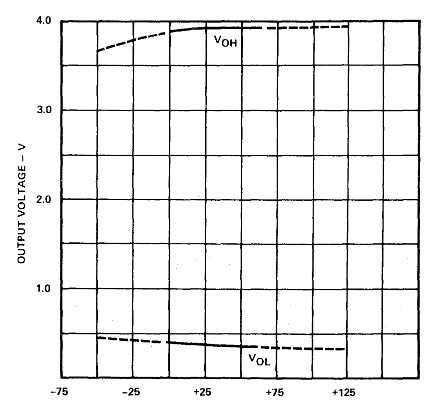
PROPAGATION DELAY FOR VARIOUS INPUT VOLTAGE



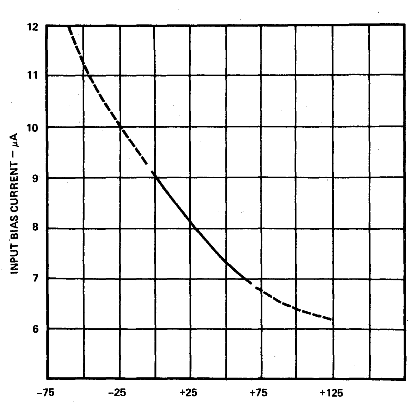
PROPAGATION DELAY FOR VARIOUS INPUT VOLTAGE



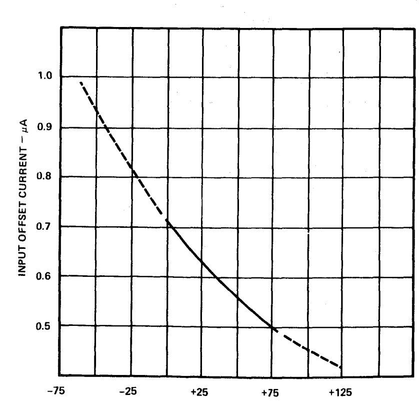
OUTPUT VOLTAGE VS. AMBIENT TEMPERATURE



INPUT BIAS CURRENT VS. AMBIENT TEMPERATURE



INPUT OFFSET CURRENT VS. AMBIENT TEMPERATURE



FEATURES

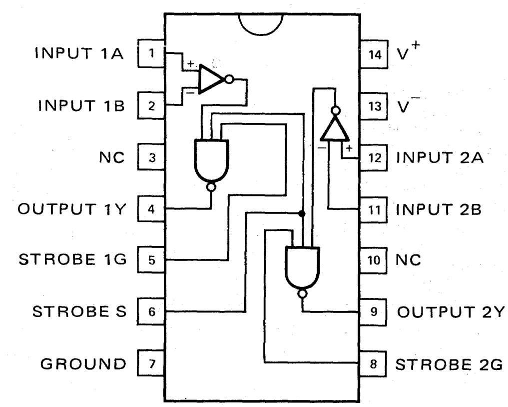
- FUNCTIONALLY EQUIVALENT AND PIN COMPATIBLE TO SN75208
- 17ns MAXIMUM GUARANTEED PROPAGATION DELAY
- 20 μA MAXIMUM INPUT BIAS CURRENT
- STTL COMPATIBLE STROBES AND OUTPUTS
- OPEN COLLECTOR OUTPUTS
- LARGE COMMON MODE INPUT VOLTAGE RANGE
- OPERATES FROM STANDARD SUPPLY VOLTAGES

ABSOLUTE MAXIMUM RATINGS

Positive Supply Voltage (V+)	+7V
Negative Supply Voltage (V−)	−7V
Differential input voltage	±6V
Common mode input voltage	±5V
Strobe/Gate input voltage	+5.5V
Power Dissipation	600mw
Operating Temperature Range	0°C to 70°C
Storage temperature range	−65°C to +150°C
Lead temperature (Soldering 60 seconds)	+300°C

PIN CONFIGURATION

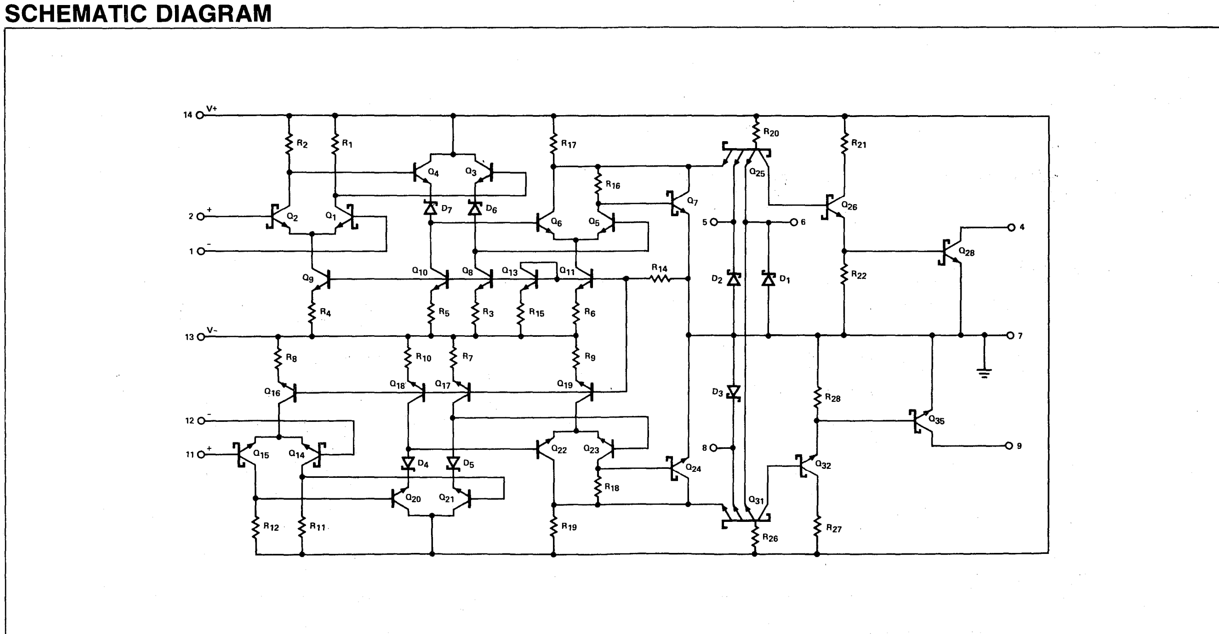
A, F PACKAGE



APPLICATIONS

MOS MEMORY SENSE AMP
A/D CONVERSION
HIGH SPEED LINE RECEIVER

SCHEMATIC DIAGRAM



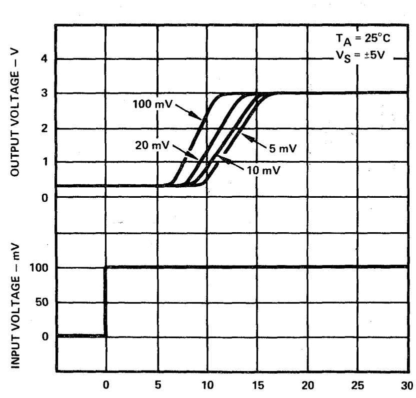
ELECTRICAL CHARACTERISTICS $V+ = +5.00$, $V- = -5.00$, $T_A = 0$ to 70°C (Unless Otherwise Noted).

PARAMETER	TEST CONDITIONS	75S208 MIN	75S208 TYP	75S208 MAX	UNIT
Amplifier Input					
Input offset voltage	V+ = 4.75, V− = −4.75			10	mV
Input Bias Current *w* 25°C	V+ = 5.25, V− = −5.25		7.5	20	μA
over temp range	V+ = 5.25, V− = −5.25			40	μA
Input offset current *w* 25°C	V+ = 5.25, V− = −5.25		1.0	5	μA
over temp range	V+ = 5.25, V− = −5.25			12	μA
Input common mode voltage range	V+ = 4.75, V− = −4.75	±3			V
Input resistance			4		kΩ
Input capacitance			3	6	pF
Voltage gain			5		V/mV
Power Supply Requirements					
Supply Voltage					
V+		4.75	5.00	5.25	V
V−		−4.75	−5.00	−5.25	V
Large Signal Switching Speed					
T_{pLH} (D) low to high propagation delay from amp inputs to output	$R_L = 280\Omega C_L = 15$ pF $T_A = 25°C$ Note 1		12	17	ns
T_{pHL} (D) high to low propagation delay from amp inputs to output	$R_L = 280\Omega C_L = 15$ pF $T_A = 25°C$ Note 1		9	13	ns
T_{pLH} (S) low to high propagation delay from strobes input to output	$R_L = 280\Omega C_L = 15$ pF $T_A = 25°C$ Note 2		6	10	ns
T_{pHL} (S) high to low propagation delay strobe input to output	$R_L = 280\Omega C_L = 15$ pF $T_A = 25°C$ Note 2		5	8	ns
Maximum Operating Frequency	$R_L = 280\Omega$ $C_L = 15$ pF $T_A = 25°C$	25	35		MHz

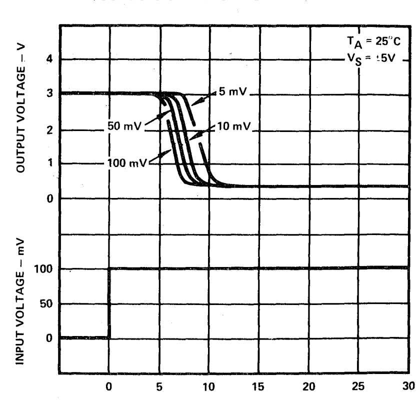
NOTES:
1. Response time measured from 0V point of ±100 MHz square wave to the 1.5 point of the output.
2. Response time measured from 1.5V point of input to 1.5V point of the output.
3. Response time measured from the start of a 100mV input step with 5mV overdrive to the 1.5V point of the output.

TYPICAL PERFORMANCE CHARACTERISTICS

RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES

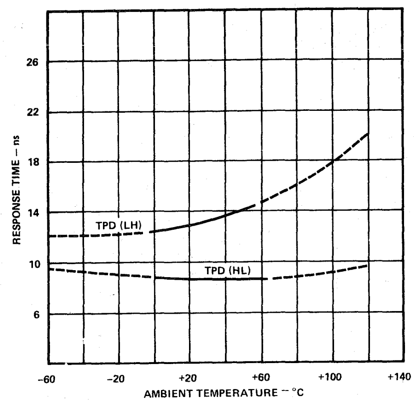


RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES

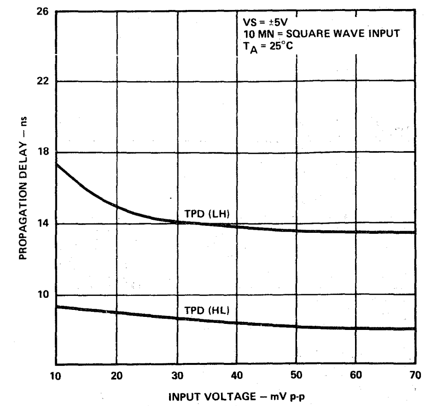


TYPICAL PERFORMANCE CHARACTERISTICS

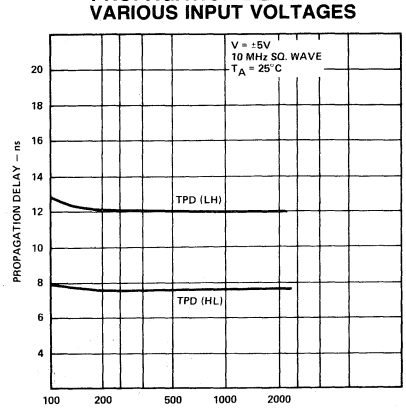
RESPONSE TIME VS. TEMPERATURE



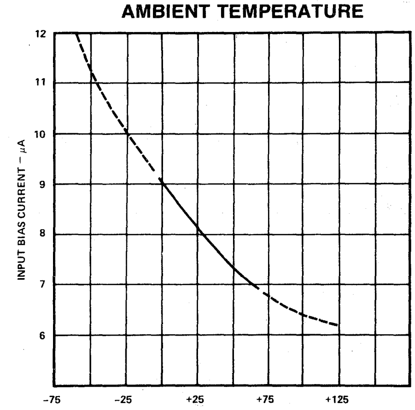
PROPAGATION DELAY FOR VARIOUS INPUT VOLTAGES



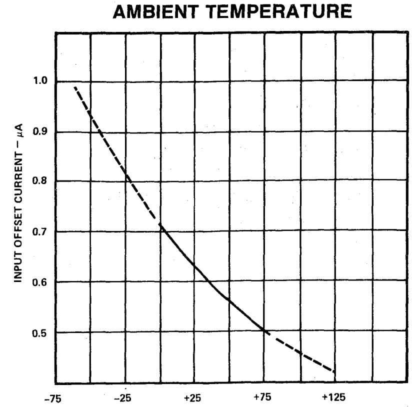
PROPAGATION DELAY FOR VARIOUS INPUT VOLTAGES



INPUT BIAS CURRENT VS. AMBIENT TEMPERATURE



INPUT OFFSET CURRENT VS. AMBIENT TEMPERATURE



FEATURES

- DUAL SENSE AMPS
- ±4mV THRESHOLD UNCERTAINTY
- DESIGN VERSATILITY
- 25ns PROPAGATION DELAY

ABSOLUTE MAXIMUM RATINGS

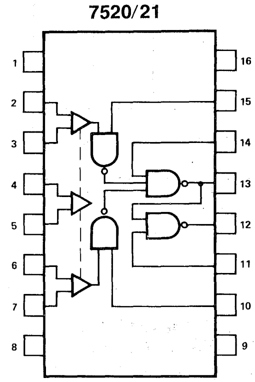
Differential Input Voltage	±5V
V_{CC}	±7V
Strobe & Gain Input Voltages	+5.5V
Storage Temperature	−65°C to +150°C
Operating Temperature	0°C to +70°C
Power Dissipation	500mW

PIN CONFIGURATIONS

B PACKAGE

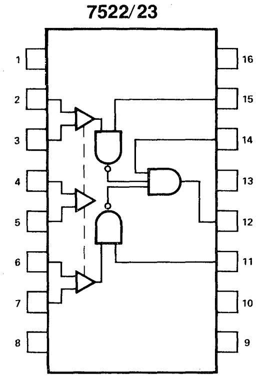
7520/21

ORDER PART NOS. SN7520N/ SN7521N



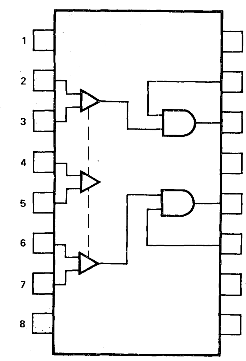
7522/23

ORDER PART NOS. SN7522N/ SN7523N



7524/25

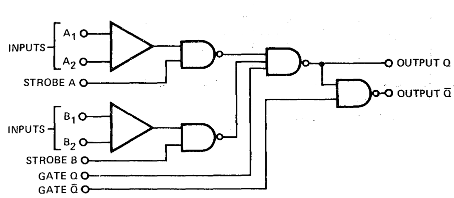
ORDER PART NOS. SN7524N/ SN7525N



*The 7520/21/22/23/24/25 does not require an external capacitor (C_{ext}) to stabilize the pre-amplifier. Pin 1 may be used as a test point, giving access to the pre-amplifier output. No degradation of performance will result if a 100pF capacitor is connected from Pin 1 to GND.

LOGIC DIAGRAMS

7520/21



Output Q = $\overline{G_Q} + \overline{(S_A\ IN_A + S_B\ IN_B)\ G_Q}$

$\overline{\text{Output } \overline{Q}} = G_{\overline{Q}}\ (\overline{G_Q} + S_A\ IN_A + S_B\ IN_B)$

where:

G_Q = Gate Q≥2V

S_A = Strobe A≥2V

IN_A = (V_{inD} at Inputs A_1 and A_2)>V_T

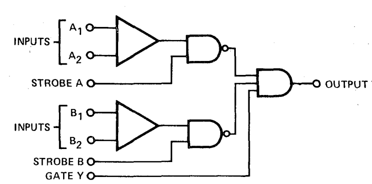
S_B = Strobe B≥2V

IN_B = (V_{inD} at Inputs B_1 and B_2)>V_T

$\overline{G_Q}$ = Gate Q≤0.8V

$G_{\overline{Q}}$ = Gate $\overline{Q}$≥2V

7522/23



$\overline{\text{Output Y}}$ = G($S_A\ IN_A + S_B + IN_B$) + $\overline{G}$

where:

G = Gate≥2V

S_A = Strobe A≥2V

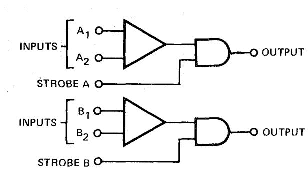
IN_A = (V_{inD} at Inputs A_1 and A_2)>V_T

S_B = Strobe B≥2V

IN_B =(V_{inD} at Inputs B_1 and B_2)>V_T

G = Gate≤0.4V

7524/25



Output A = $S_A\ IN_A$

Output B = $S_B\ IN_B$

where:

S_A = Strobe A≥2V

IN_A = (V_{inD} at Inputs A_1 and A_2)>V_T

S_B = Strobe B≥2V

IN_B = (V_{inD} at Inputs B_1 and B_2)>V_T

AC CHARACTERISTICS 7520/21

PROPAGATION DELAY TIMES			MIN	TYP	MAX	UNIT
SYMBOL	FROM INPUT	TO OUTPUT				
$t_{pd}(1)DQ$, $t_{pd}(0)DQ$	A_1-A_2-or B_1-B_2	Q		20 30	40 	ns ns
$t_{pd}(1)D\overline{Q}$, $t_{pd}(0)D\overline{Q}$	A_1-A_2 or B_1-B_2	$\overline{Q}$		25 35	 55	ns ns
$t_{pd}(1)SQ$, $t_{pd}(0)SQ$	Strobe A or B	Q		15 25	30 	ns ns
$t_{pd}(1)S\overline{Q}$, $t_{pd}(0)S\overline{Q}$	Strobe A or B	$\overline{Q}$		15 35	 55	ns ns
$t_{pd}(1)G_QQ$, $t_{pd}(0)G_QQ$	Gate Q	Q		10 15	20 	ns ns
$t_{pd}(1)G_Q\overline{Q}$, $t_{pd}(0)G_Q\overline{Q}$	Gate Q	$\overline{Q}$		15 20	 30	ns ns
$t_{pd}(1)G_{\overline{Q}}\overline{Q}$, $t_{pd}(0)G_{\overline{Q}}\overline{Q}$	Gate $\overline{Q}$	$\overline{Q}$		15 10	 20	ns ns

AC CHARACTERISTICS 7522/23

PROPAGATION DELAY TIMES			MIN	TYP	MAX	UNIT
SYMBOL	FROM INPUT	TO OUTPUT				
$t_{pd}(1)D$	A_1-A_2 or B_1-B_2	Y		20		ns
$t_{pd}(0)D$				30	45	ns
$t_{pd}(1)S$	Strobe A or B	Y		15		ns
$t_{pd}(0)S$				25	40	ns
$t_{pd}(1)G$	Gate	Y		10		ns
$t_{pd}(0)G$				15	25	ns

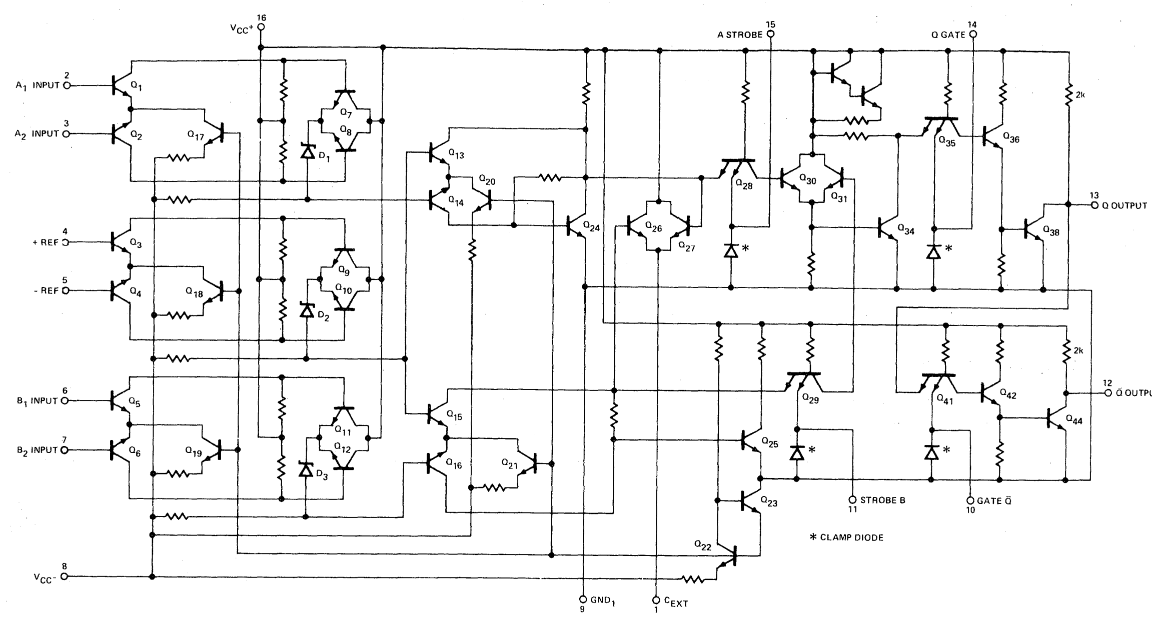
AC CHARACTERISTICS 7524/25

PROPAGATION DELAY TIMES			MIN	TYP	MAX	UNIT
SYMBOL	FROM INPUT	TO OUTPUT				
$t_{pd}(1)D$	A_1-A_2 or B_1-B_2	A or B		25	40	ns
$t_{pd}(0)D$				20		ns
$t_{pd}(1)S$	Strobe A or B	A or B		15	30	ns
$t_{pd}(0)S$				20		ns

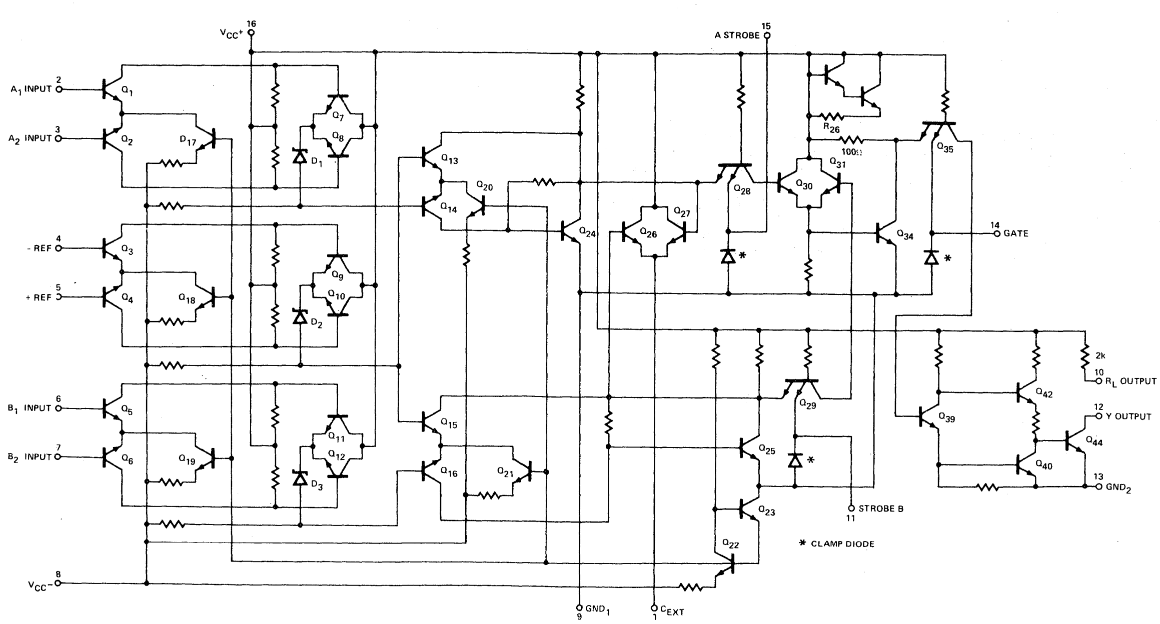
NOTES:
1. The differential input threshold voltage (V_T) is defined as the DC input voltage (V_{in}) required to force the output of the sense amplifier to the logic gate threshold voltage level.
2. Common mode input firing voltage is the common mode voltage that will exceed the dynamic range of the input at the specified conditions and cause the logic output to switch. The specified common mode input signal is applied with a strobe enable signal present.
3. Differential input overload recovery time is the time necessary for the device to recover from the specified differential input overload signal prior to the strobe enable signal.
4. Common mode input overload recovery time is the time necessary for the device to recover from the specified common mode input overload signal prior to the strobe enable signal.

SCHEMATIC DIAGRAMS

7520/21

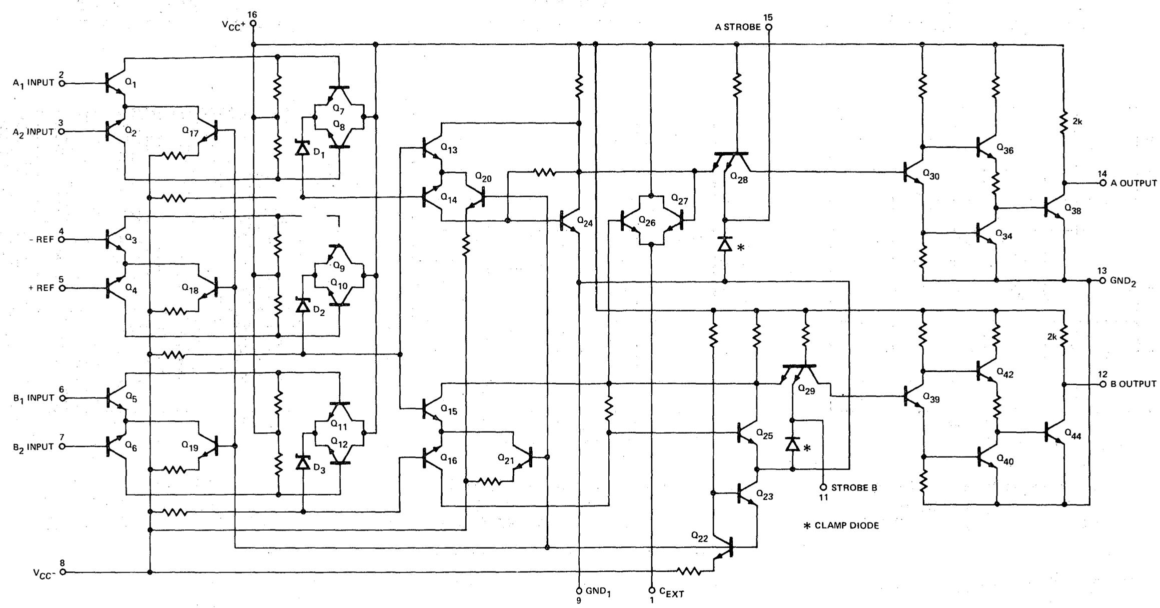


7522/23



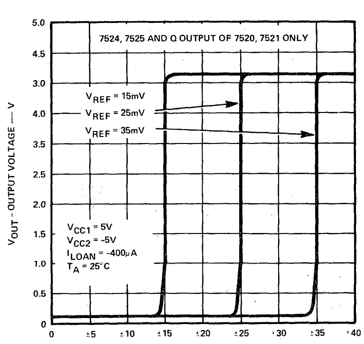
SCHEMATIC DIAGRAMS (CONT'D)

7524/25

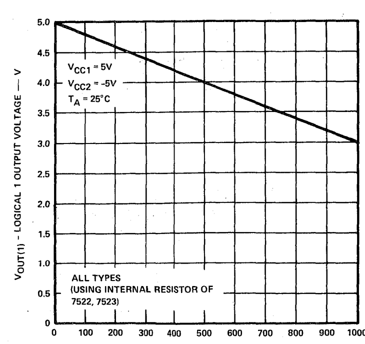


TYPICAL CHARACTERISTIC CURVES

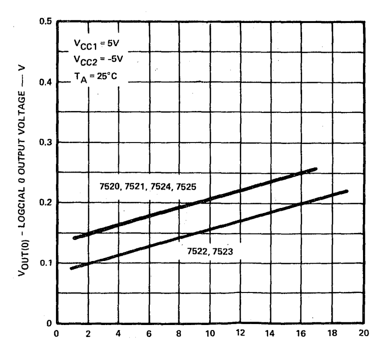
OUTPUT VOLTAGE VERSUS DIFFERENTIAL-INPUT VOLTAGE



LOGICAL 1 OUTPUT VOLTAGE VERSUS LOAD CURRENT



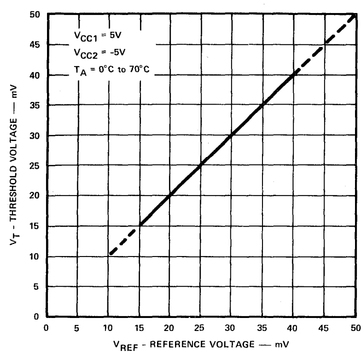
LOGICAL 0 OUTPUT VOLTAGE VERSUS SINK CURRENT



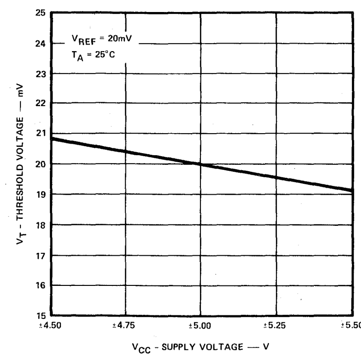
INTERFACE

TYPICAL CHARACTERISTIC CURVES (CONT'D)

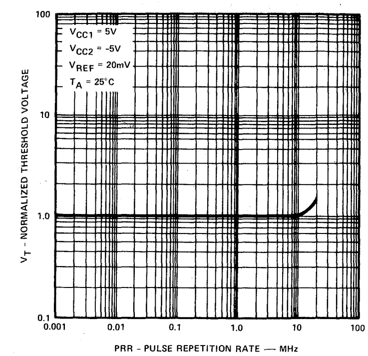
THRESHOLD VOLTAGE VERSUS REFERENCE VOLTAGE



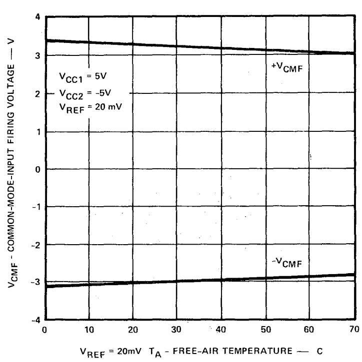
THRESHOLD VOLTAGE VERSUS SUPPLY VOLTAGE



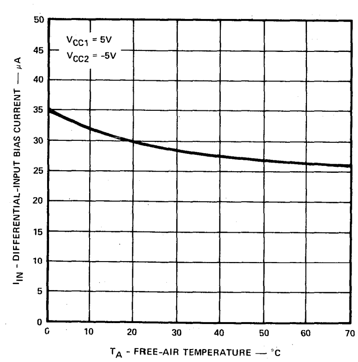
NORMALIZED THRESHOLD VOLTAGE VERSUS PULSE REPETITION RATE



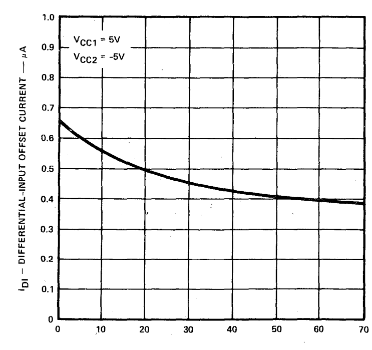
COMMON MODE FIRING VOLTAGE VERSUS FREE-AIR TEMPERATURE



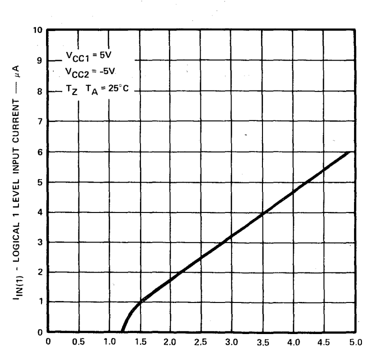
DIFFERENTIAL-INPUT BIAS CURRENT VERSUS FREE-AIR TEMPERATURE



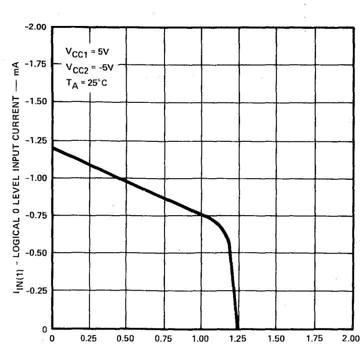
DIFFERENTIAL-INPUT OFFSET CURRENT VS FREE-AIR TEMPERATURE



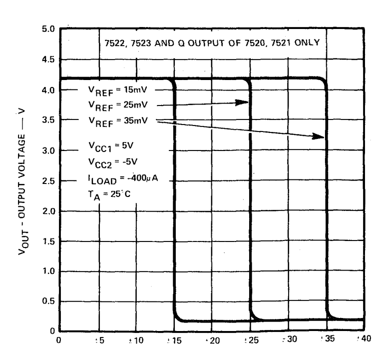
LOGICAL 1 LEVEL INPUT CURRENT VS INPUT VOLTAGE



LOGICAL 0 LEVEL INPUT CURRENT VS INPUT VOLTAGE



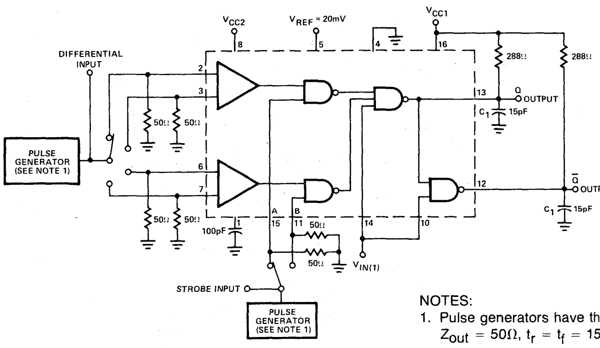
OUTPUT VOLTAGE VERSUS DIFFERENTIAL INPUT VOLTAGE



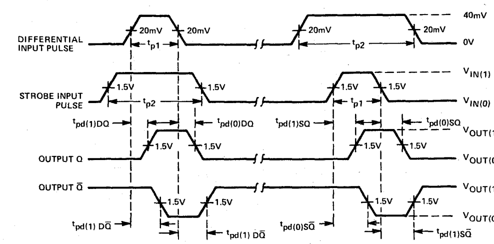
SWITCHING CHARACTERISTICS (Propagation Delay Times)

7520/21

TEST CIRCUIT—DIFFERENTIAL AND STROBE INPUTS TO OUTPUTS



VOLTAGE WAVEFORMS—DIFFERENTIAL AND STROBE INPUTS TO OUTPUTS



NOTES:
1. Pulse generators have the following characteristics: Z_{out} = 50Ω, $t_r = t_f$ = 15(±5)ns, t_{p1} = 100 ns, t_{p2} = 300ns, and PRR = 1 MHz.
2. C_1 includes probe and jig capacitance.

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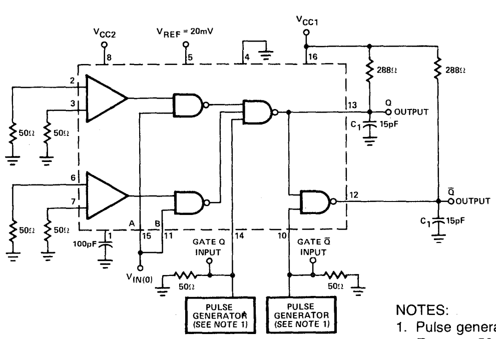
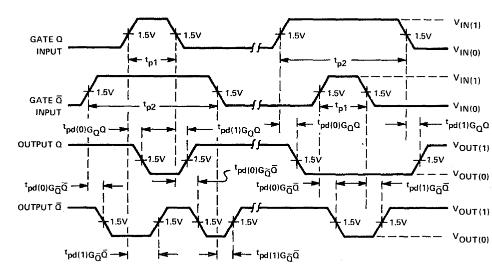
TEST CIRCUIT



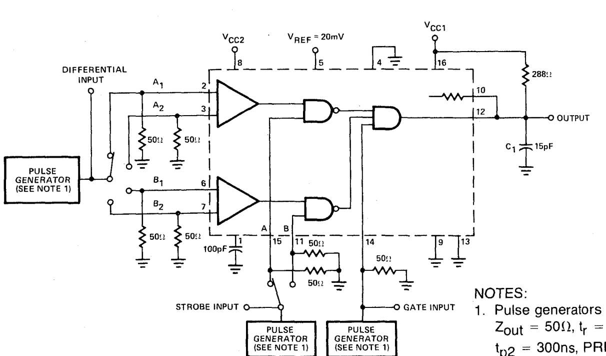
VOLTAGE WAVEFORMS



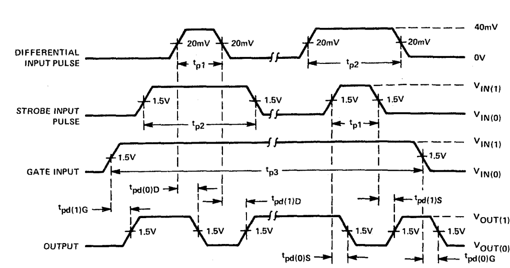
NOTES:
1. Pulse generators have the following characteristics: Z_{OUT} = 50Ω, $t_r = t_f$ = 15(±5)ns, t_{p1} = 100 ns, t_{p2} = 300ns, and PRR = 1 MHz.
2. C_1 includes probe and jig capacitance.

7522/23

TEST CIRCUIT



VOLTAGE WAVEFORMS



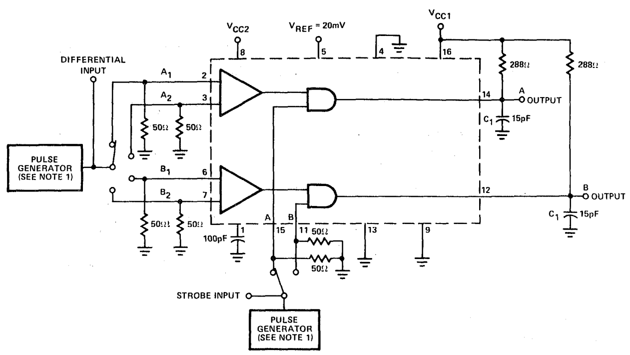
NOTES:
1. Pulse generators have the following characteristics: Z_{out} = 50Ω, $t_r = t_f$ = 15(±5)ns, t_{p1} = 100 ns, t_{p2} = 300ns, PRR = 1 MHz.
2. Strobe input pulse is applied to Strobe A when inputs A_1-A_2 are being tested and to Strobe B when inputs B_1-B_2 are being tested.
3. C_1 includes probe and jig capacitance.

INTERFACE

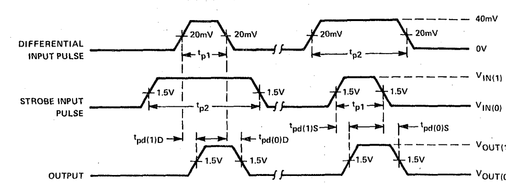
SWITCHING CHARACTERISTICS (Propagation Delay Times) (Cont'd)

TEST CIRCUIT

7524/25



VOLTAGE WAVEFORMS



NOTES:
1. Pulse generators have the following characteristics: Z_{out} = 50Ω, $t_r = t_f = 15(\pm 5)$ns, t_{p1} = 100ns, t_{p2} = 300ns, PRR = 1 MHz.
2. Strobe input pulse is applied to Strobe A when inputs A_1-A_2 are being tested and to Strobe B when inputs B_1-B_2 are being tested.
3. C_1 includes probe and jig capacitance.

FEATURES
- 400mA OUTPUT CAPABILITY
- HIGH VOLTAGE OUTPUTS
- DUAL SINK/SOURCE OUTPUTS
- INTERNAL DECODING AND TIMING CIRCUITRY
- FAST SWITCHING TIMES
- OUTPUT SHORT-CIRCUIT PROTECTION

ABSOLUTE MAXIMUM RATINGS
Over Operating Case Temperature Range (Unless Otherwise Noted).

Supply voltage V_{CC} (See Note 1)	17 V
Input voltage (See Note 2)	5.5 V
Operating case temperature range	0°C to 70°C
Continuous total power dissipation at (or below) 70°C case temperature	800 mW
Storage temperature range	−65°C to 150°C

NOTES:
1. Voltage values are with respect to network ground terminal.
2. Input signals must be zero or positive with respect to network ground terminal.

FUNCTION TABLE

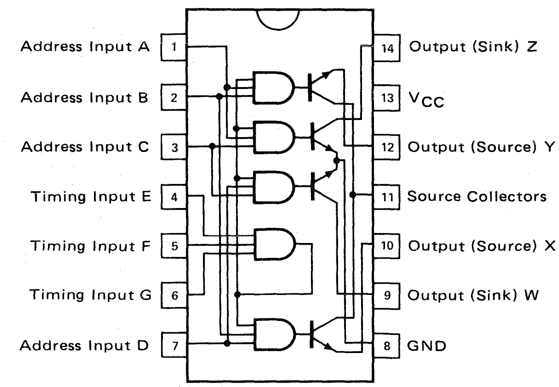
INPUTS							OUTPUTS			
ADDRESS				TIMING			SINK	SOURCES		SINK
A	B	C	D	E	F	G	W	X	Y	Z
L	L	H	H	H	H	H	ON	OFF	OFF	OFF
L	H	L	H	H	H	H	OFF	ON	OFF	OFF
H	H	L	L	H	H	H	OFF	OFF	ON	OFF
H	L	H	L	H	H	H	OFF	OFF	OFF	ON
X	X	X	X	L	X	X	OFF	OFF	OFF	OFF
X	X	X	X	X	L	X	OFF	OFF	OFF	OFF
X	X	X	X	X	X	L	OFF	OFF	OFF	OFF

H = high level, L = low level, X = irrelevant

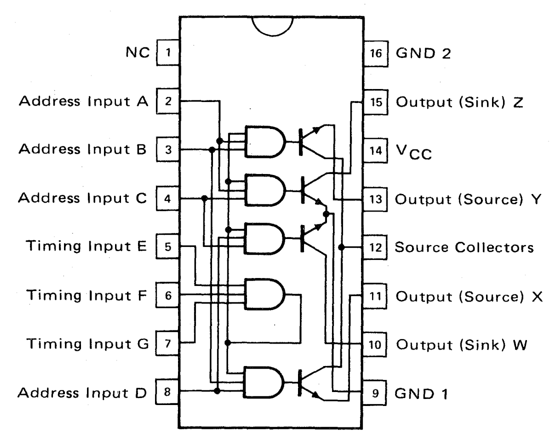
NOTE: Not more than one output is to be on at one time: When all timing inputs are high, two of the address inputs must be low.

PIN CONFIGURATION

A PACKAGE



F PACKAGE

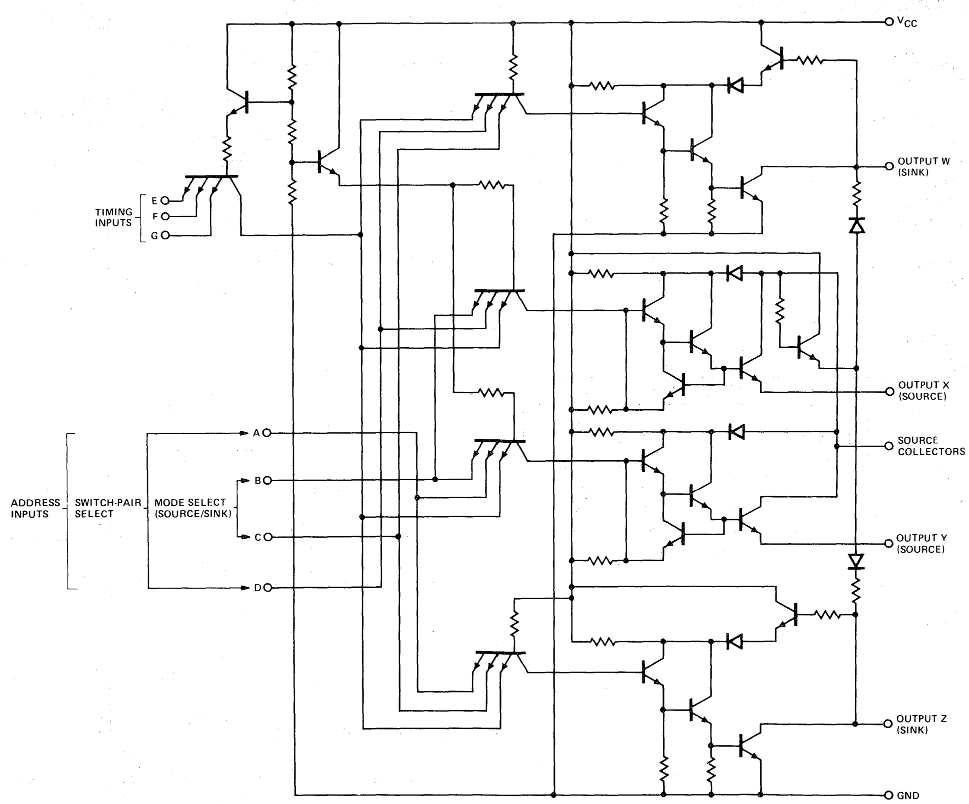


ELECTRICAL CHARACTERISTICS V_{CC} = 14V, T_C = 0°C to 70°C (Unless Otherwise Noted).

PARAMETER		TEST FIGURE	TEST CONDITIONS		LIMITS			UNIT
					MIN	TYP[1]	MAX	
$V_{(sat)}$	Sink saturation voltage	2	$I_{sink} \cong$ 420mA,	RL = 53		0.75	0.85	V
$V_{(sat)}$	Source saturation voltage	2	$I_{source} \cong$ −420mA,	RL = 47.5		0.75	0.85	V
I_{off}	Output off-state current	1	V_I = OV			125	200	μA

NOTE:
1. All typical values are at T_C = 25°C

SCHEMATIC DIAGRAM

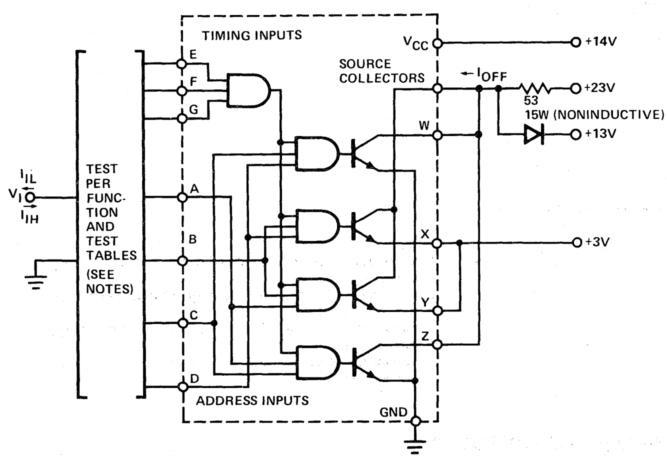


SWITCHING CHARACTERISTICS V_{CC} = 14V, T_C = 25°C

PARAMETER		TEST FIGURE	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT
t_{PLH}	Propagation Delay Time Low-to-High-Level Source Output	5	R_{L1} = 53			90	ns
t_{PHL}	Propagation Delay Time High-to-Low-Level Source Output	5	R_{L2} = 500, C_L = 20pF			50	ns
t_{PLH}	Propagation Delay Time Low-to-High-Level Sink Output	6				110	ns
t_{PHL}	Propagation Delay Time High-to-Low-Level Sink Output	6	R_L = 53, C_L = 20pF			40	ns
t_s	Sink storage time	6				70	ns

PARAMETER MEASUREMENT INFORMATION

D.C. TEST CIRCUITS†

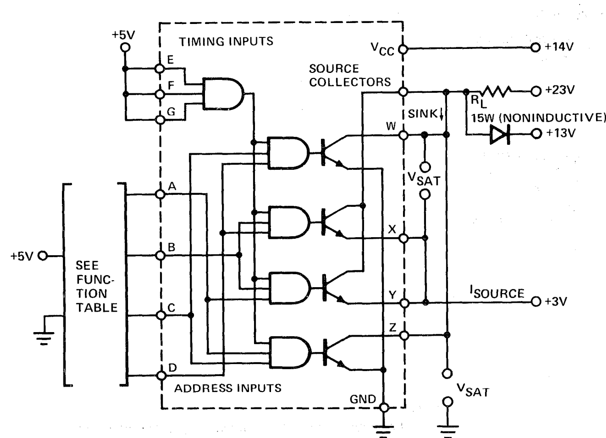


TEST TABLE FOR I_{IL}

APPLY 3.5V	GROUND	TEST I_{IL}
B, C, E, F, and G	A and D	A
B, C, E, F, and G	A and D	D
A, D, E, F, and G	B and C	B
A, D, E, F, and G	B and C	C
A, B, C, D, F, and G	E	E
A, B, C, D, E, and G	F	F
A, B, C, D, E, and F	G	G

NOTES:
1. Check V_{IH} and V_{IL} per Function Table.
2. Measure I_{IL} per Test Table.
3. When measuring I_{IH}, all other inputs are at ground. Each input is tested separately.

FIGURE 1—V_{IL}, V_{IH}, I_{IL}, I_{IH}, and Ioff



NOTE: This parameter must be using pulse techniques, t_W = 500ns, duty cycle ≤ 1%.

FIGURE 2—$V_{(sat)}$

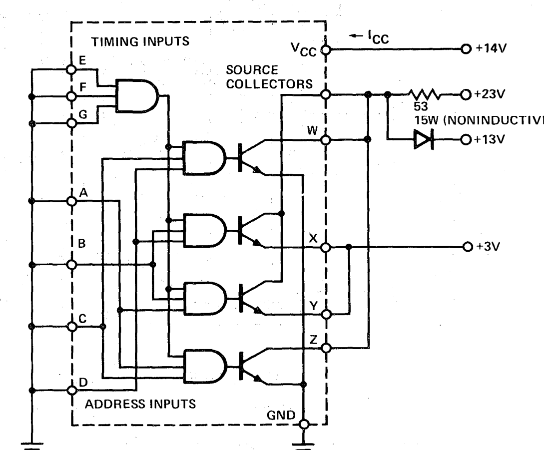
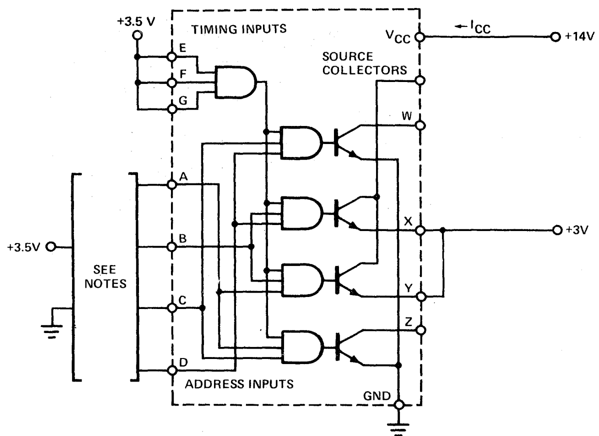


FIGURE 3—I_{CC} (ALL OUTPUTS OFF)

†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

PARAMETER MEASUREMENT INFORMATION

D.C. TEST CIRCUITS† (Continued)



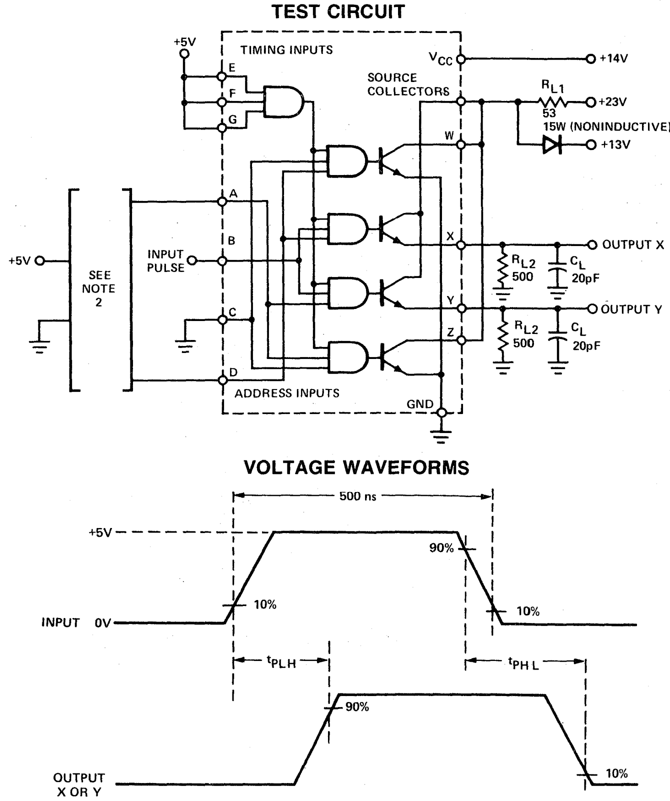
NOTES:
1. Ground A and B, apply 3.5V to C and D, and measure I_{CC} (output W is on).
2. Ground B and D, apply 3.5V to A and C, and measure I_{CC} (output Z is on).
3. Ground A and C, apply 3.5V to B and D, and measure I_{CC} (output X is on).
4. Ground C and D, apply 3.5V to A and B, and measure I_{CC} (output Y is on).

FIGURE 4—I_{CC} (ONE OUTPUT ON)

†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

SWITCHING CHARACTERISTICS

TEST CIRCUIT

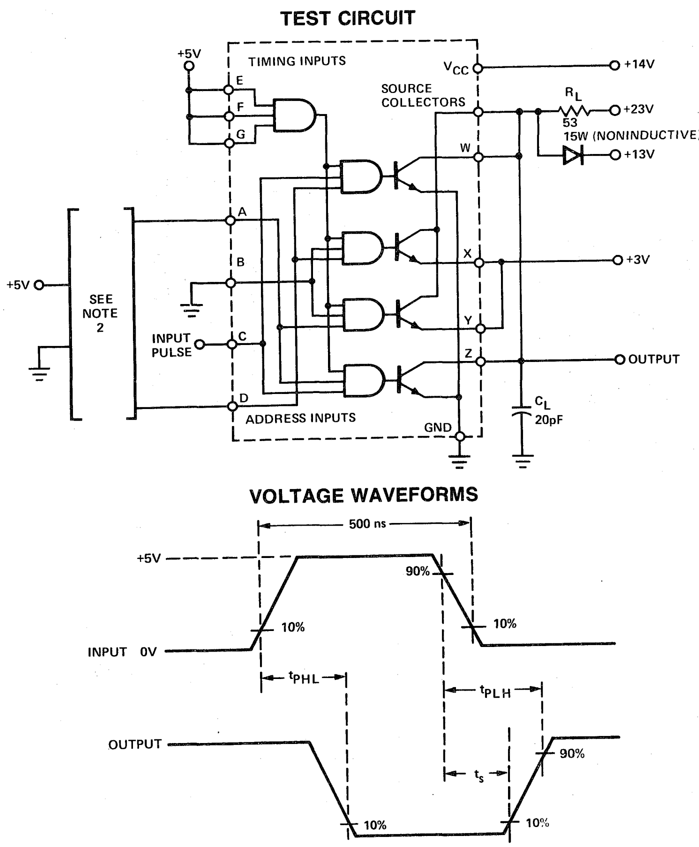


NOTES:
1. The input waveform is supplied by a generator with the following characteristics: $t_r = t_f = 10$ ns, duty cycle $\leq 1\%$, and $Z_{out} \approx 50\Omega$.
2. When measuring delay times at output X, apply +5V to Input D, and ground A. When measuring delay times at output Y, apply +5V to Input A, and ground D.
3. C_L includes probe and jig capacitance.
4. Unless otherwise noted all resistors are 0.5W.

FIGURE 5—SOURCE-OUTPUT SWITCHING TIMES

PARAMETER MEASUREMENT INFORMATION

SWITCHING CHARACTERISTICS (Continued)



NOTES:
1. The input waveform is supplied by a generator with the following characteristics: $t_r = t_f = 10$ ns, duty cycle ≤ 1%, and $Z_{out} \approx 50$.
2. When measuring delay times at output W, apply +5V to Input D, and ground A. When measuring delay times at output Z, apply +5V to Input A, and ground D.
3. C_L includes probe and jig capacitance.

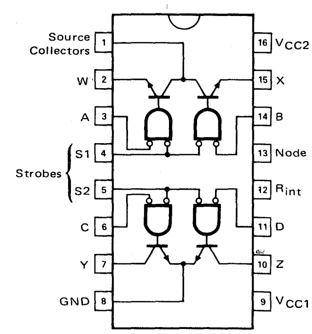
FIGURE 6—SINK-OUTPUT SWITCHING TIMES

FEATURES

- 600mA OUTPUT CAPABILITY
- FAST SWITCHING TIMES
- OUTPUT SHORT-CIRCUIT PROTECTION
- DUAL SINK AND DUAL SOURCE OUTPUTS
- MINIMUM TIME SKEW BETWEEN ADDRESS AND OUTPUT CURRENT RISE
- 24 VOLT OUTPUT CAPABILITY
- SOURCE BASE DRIVE EXTERNALLY ADJUSTABLE
- TTL OR DTL COMPATIBILITY
- INPUT CLAMPING DIODES

PIN CONFIGURATION

BA, F PACKAGE



TRUTH TABLE

ADDRESS INPUTS		STROBE INPUTS		OUTPUTS	
SOURCE A B	SINK C D	SOURCE S1	SINK S2	SOURCE W X	SINK Y Z
L H	X X	L	H	ON OFF	OFF OFF
H L	X X	L	H	OFF ON	OFF OFF
X X	L H	H	L	OFF OFF	ON OFF
X X	H L	H	L	OFF OFF	OFF ON
X X	X X	H	H	OFF OFF	OFF OFF
H H	H H	X	X	OFF OFF	OFF OFF

H = high level, L = low level, X = irrelevant

NOTE:
Not more than one output is to be on at any one time.

ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING 55325	RATING 75325	UNIT
Supply voltage V_{CC1} (see Note 1)		7	7	V
Supply voltage V_{CC2} (see Note 2)		25	25	V
Input voltage (any address or strobe input)		5.5	5.5	V
Continuous total dissipation at (or below) 100°C case temperature (see Note 2)		1	1	W
Operating free-air temperature range		−55 to 125	0 to 70	°C
Storage temperature range		−65 to 150	−65 to 150	°C
Lead temperature 1/16 inch from case for 60 seconds	F Package	300	300	°C
Lead temperature 1/16 inch from case for 10 seconds	BA Package	260	260	°C

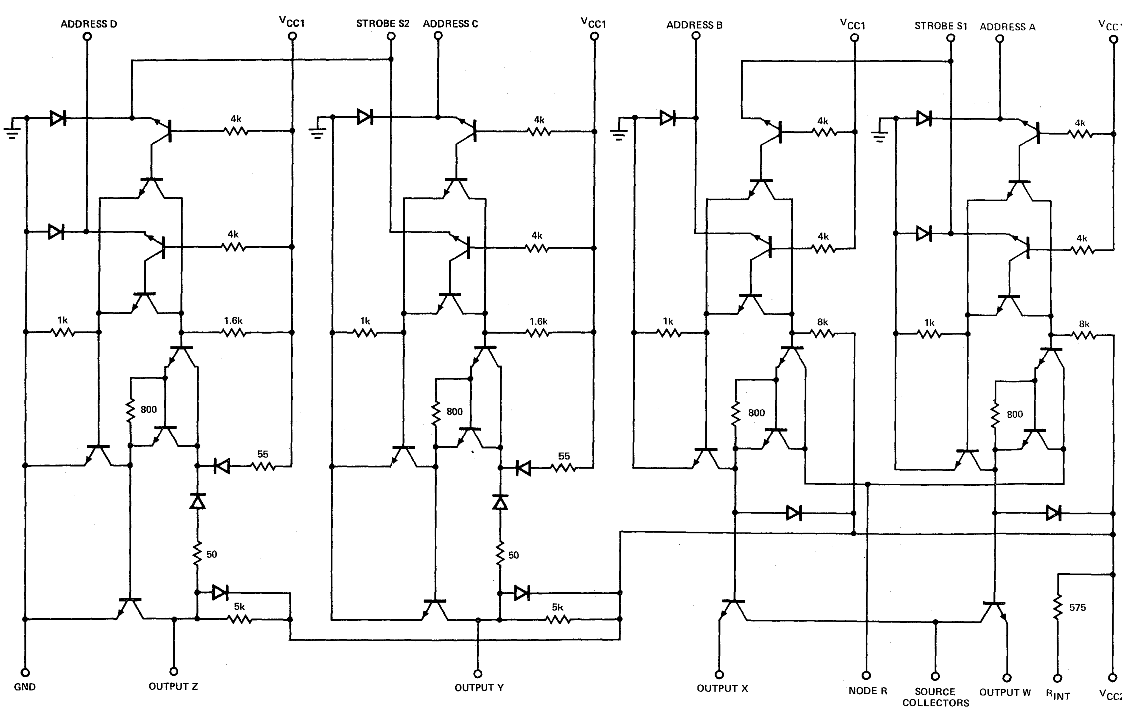
NOTES: 1. Voltage values are with respect to network ground terminal. 2. For operation above 100°C case temperature, refer to Dissipation Derating Curve, Figure 20. For dissipation ratings in free-air, see Figure 21.

SWITCHING CHARACTERISTICS V_{CC1} = 5V, T_A = 25°C

PARAMETER[1]	TO (OUTPUT)	TEST FIGURE	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT
t_{PLH}	Source collectors	9	V_{CC2} = 15V, R_L = 24Ω, C_L = 25pF		25	50	ns
t_{PHL}					25	50	
t_{TLH}	Source outputs	10	V_{CC2} = 20V, R_L = 1kΩ, C_L = 25pF		55		ns
t_{THL}					7		
t_{PLH}	Sink outputs	9	V_{CC2} = 15V, R_L = 24Ω, C_L = 25pF		20	45	ns
t_{PHL}					20	45	
t_{TLH}	Sink outputs	9	V_{CC2} = 15V, R_L = 24Ω, C_L = 25pF		7	15	ns
t_{THL}					9	20	
t_s	Sink outputs	9	V_{CC2} = 15V, R_L = 24Ω, C_L = 25pF		15	30	ns

NOTE:
1. t_{PLH} = propagation delay time, low-to-high-level output
t_{PHL} = propagation delay time, high-to-low-level output
t_{TLH} = transition time, low-to-high-level output
t_{THL} = transition time, high-to-low-level output
t_s = storage time

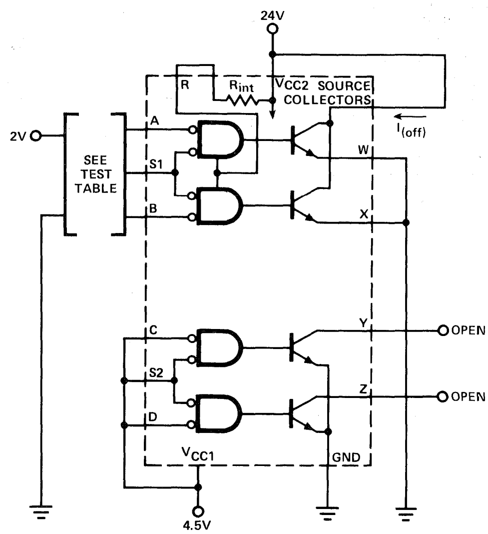
CIRCUIT SCHEMATIC



NOTE: ALL RESISTORS VALUES ARE TYPICAL AND IN OHMS.

PARAMETER MEASUREMENT INFORMATION (Cont'd)

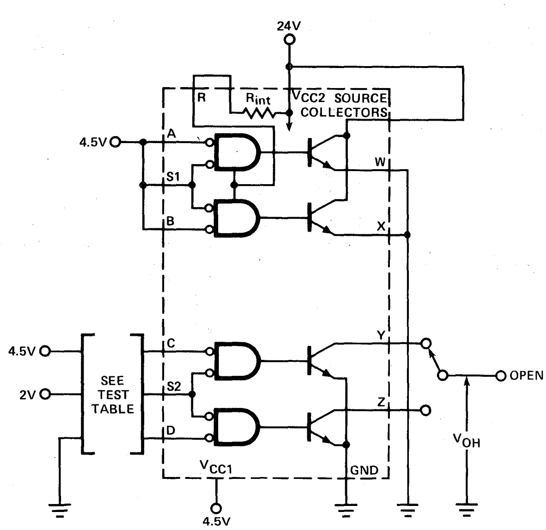
DC TEST CIRCUITS*



TEST TABLE

A	B	S1
GND	GND	2V
2V	2V	GND

FIGURE 1 – V_{IH} AND $I_{(off)}$



TEST TABLE

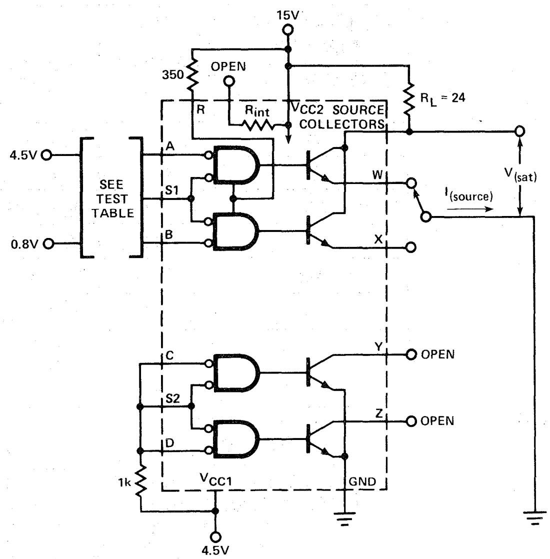
C	D	S2	Y	Z
2V	4.5V	GND	V_{OH}	OPEN
GND	4.5V	2V	V_{OH}	OPEN
4.5V	2V	GND	OPEN	V_{OH}
4.5V	GND	2V	OPEN	V_{OH}

*ARROWS INDICATE ACTUAL DIRECTION OF CURRENT FLOW

FIGURE 2 – V_{IH} AND V_{OH}

PARAMETER MEASUREMENT INFORMATION (Cont'd)

DC TEST CIRCUITS* (Continued)

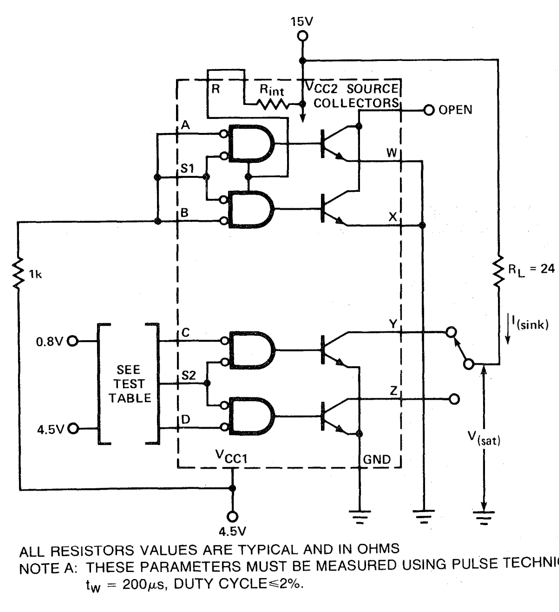


TEST TABLE

A	B	S1	W	X
0.8V	4.5V	0.8V	GND	OPEN
4.5V	0.8V	0.8V	OPEN	GND

ALL RESISTORS VALUES ARE TYPICAL AND IN OHMS
NOTE A: THESE PARAMETERS MUST BE MEASURED USING PULSE TECHNIQUES.
t_W = 200μs, DUTY CYCLE≤2%.

FIGURE 3 – V_{IL} AND SOURCE $V_{(sat)}$



TEST TABLE

C	D	S2	Y	Z
0.8V	4.5V	0.8V	RL	OPEN
4.5V	0.8V	0.8V	OPEN	RL

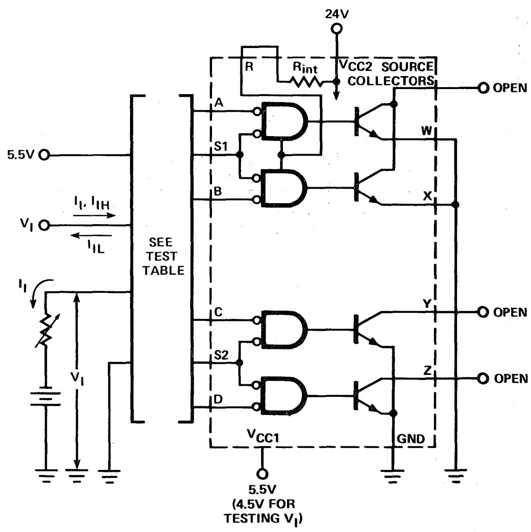
ALL RESISTORS VALUES ARE TYPICAL AND IN OHMS
NOTE A: THESE PARAMETERS MUST BE MEASURED USING PULSE TECHNIQUES.
t_W = 200μs, DUTY CYCLE≤2%.

*ARROWS INDICATE ACTUAL DIRECTION OF CURRENT FLOW.

FIGURE 4 – V_{IL} AND SINK $V_{(sat)}$

PARAMETER MEASUREMENT INFORMATION (Cont'd)

DC TEST CIRCUITS* (Continued)



TEST TABLES

I_I, I_{IH}

APPLY V_I = 5.5V. MEASURE I_I / APPLY V_I = 2.4V. MEASURE I_{IH}	GROUND	APPLY 5.5V
A	S1	B, C, S2, D
S1	A, B	C, S2, D
B	S1	A, C, S2, D
C	S2	A, S1, B, D
S2	C, D	A, S1, B
D	S2	A, S1, B, C

V_I, I_{IL}

APPLY V_I = 0.4V, MEASURE I_{IL} / APPLY I_I = − 10mA, MEASUREMENT V_I	APPLY 5.5V
A	S1, B, C, S2, D
S1	A, B, C, S2, D
B	A, S1, C, S2, D
C	A, S1, B, S2, D
S2	A, S1, B, C, D
D	A, S1, B, C, S2

FIGURE 5 – V_I, I_I, I_{IH}, AND I_{IL}

*ARROWS INDICATE ACTUAL DIRECTION OF CURRENT FLOW.

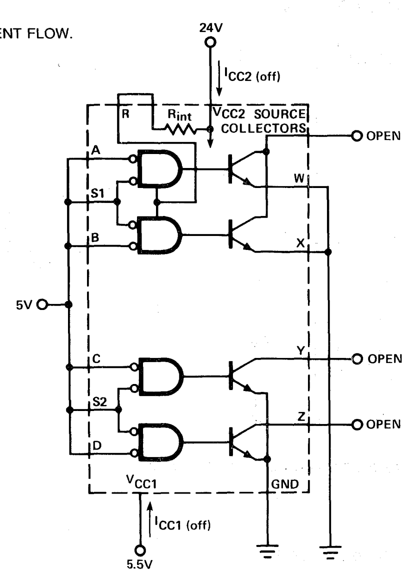
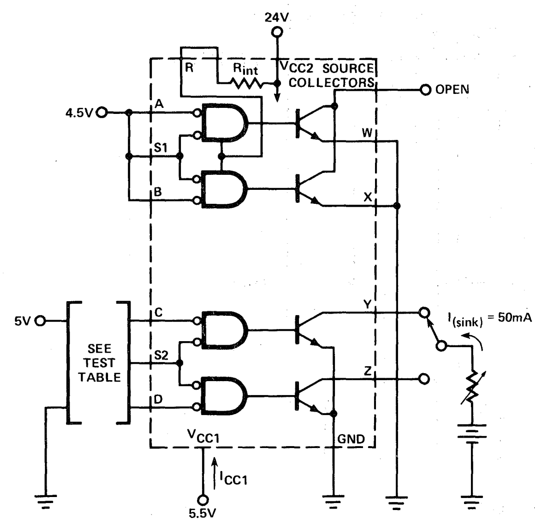


FIGURE 6 – $I_{CC1(off)}$ AND $I_{CC2(off)}$

PARAMETER MEASUREMENT INFORMATION (Cont'd)

DC TEST CIRCUITS* (Continued)

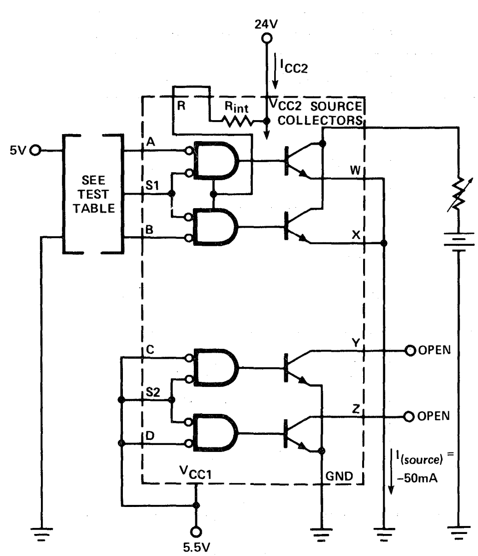


TEST TABLE

C	D	S2	Y	Z
GND	5V	GND	I(sink)	OPEN
5V	GND	GND	OPEN	I(sink)

FIGURE 7 – I_{CC1}, EITHER SINK ON

*ARROWS INDICATE ACTUAL DIRECTION OF CURRENT FLOW.



TEST TABLE

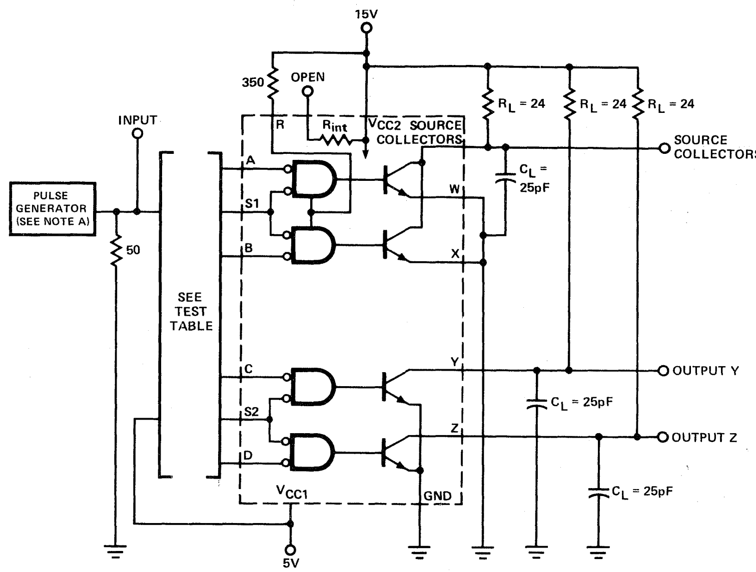
A	B	S1
GND	5V	GND
5V	GND	GND

FIGURE 8 – I_{CC2}, EITHER SOURCE ON

INTERFACE

PARAMETER MEASUREMENT INFORMATION (Cont'd.)

SWITCHING CHARACTERISTICS

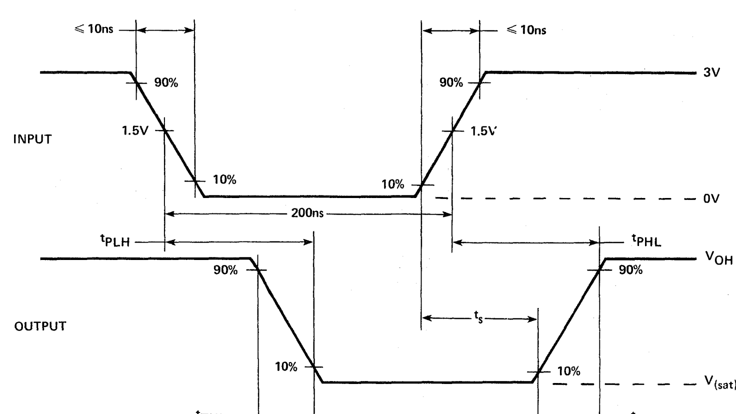


TEST CIRCUIT

NOTES:
ALL RESISTORS VALUES ARE TYPICAL AND IN OHMS.
A. THE PULSE GENERATOR HAS THE FOLLOWING CHARACTERISTICS:
Z_{out} = 50Ω, DUTY CYCLE ≤1%.
B. C_L INCLUDES PROBE AND JIG CAPACITANCE.

TEST TABLE

PARAMETER	OUTPUT UNDER TEST	INPUT	CONNECT TO 5V
t_{PLH} and t_{PHL}	Source collectors	A and S1	B, C, D and S2
		B an S1	A, C, D and S2
t_{PLH}, t_{PHL}, t_{TLH}, t_{THL}, and t_s	Sink output Y	C and S2	A, B, D and S1
	Sink output Z	D and S2	A, B, C and S1

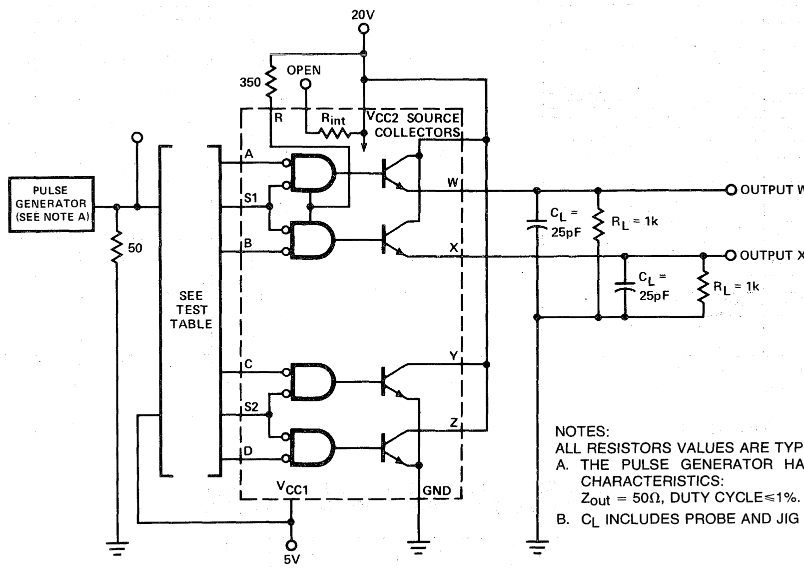


VOLTAGE WAVEFORMS

FIGURE 9 – SWITCHING TIMES

PARAMETER MEASUREMENT INFORMATION (Cont'd.)

SWITCHING CHARACTERISTICS Continued

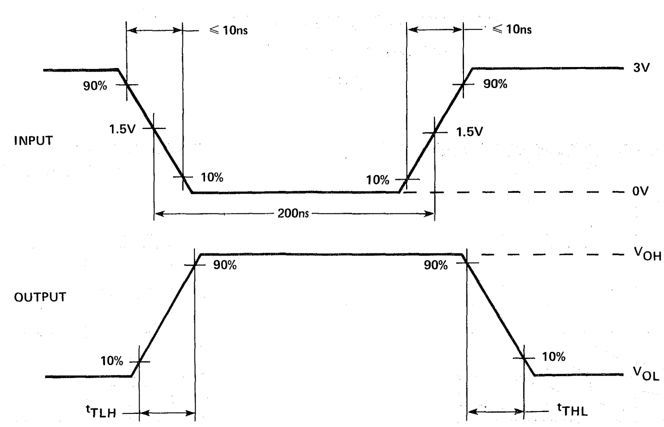


NOTES:
ALL RESISTORS VALUES ARE TYPICAL AND IN OHMS.
A. THE PULSE GENERATOR HAS THE FOLLOWING CHARACTERISTICS: Z_{out} = 50Ω, DUTY CYCLE≤1%.
B. C_L INCLUDES PROBE AND JIG CAPACITANCE.

TEST CIRCUIT

TEST TABLE

PARAMETER	OUTPUT UNDER TEST	INPUT	CONNECT TO 5V
t_{TLH} and t_{THL}	Source output W	A and S1	B, C, D and S2
	Source output X	B and S1	A, C, D and S2



VOLTAGE WAVEFORMS

FIGURE 10 – TRANSITION TIMES OF SOURCE OUTPUTS

INTERFACE

TYPICAL CHARACTERISTICS

OFF-STATE CURRENT INTO SOURCE COLLECTORS vs FREE-AIR TEMPERATURE

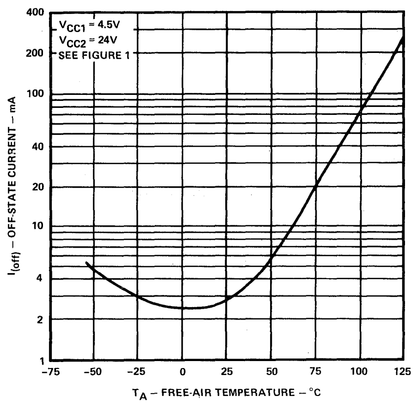


FIGURE 11

HIGH-LEVEL SINK OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE

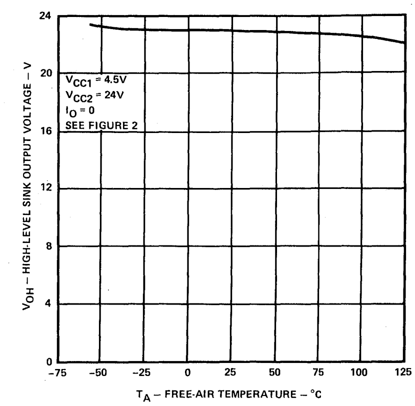


FIGURE 12

SOURCE OR SINK SATURATION VOLTAGE vs SOURCE CURRENT OR SINK CURRENT

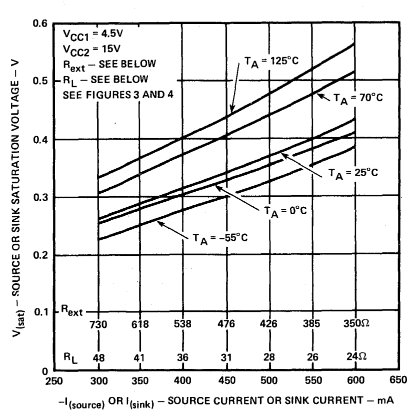


FIGURE 13

SOURCE OR SINK SATURATION VOLTAGE vs FREE-AIR TEMPERATURE

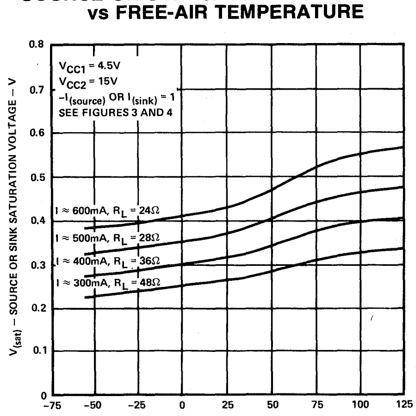


FIGURE 14

SUPPLY CURRENT, ALL SOURCES AND SINKS OFF vs FREE-AIR TEMPERATURE

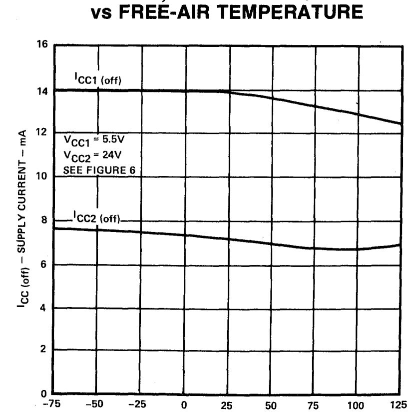
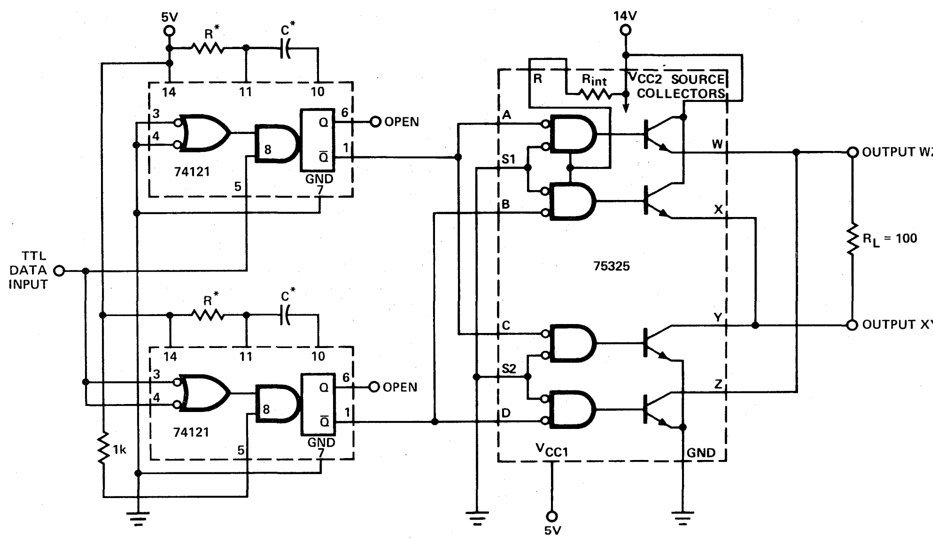


FIGURE 15

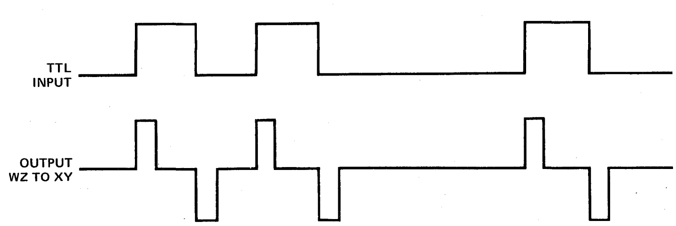
TYPICAL APPLICATION DATA

BALANCED BIPOLAR LOGIC-LINE DRIVER

The circuit shown in Figure 16 converts standard TTL logic to bipolar logic. Bipolar logic is primarily used in transmitting data or clock pulses over long lines. This line-driver may be operated from a single 5-volt supply; however, the output drive may be increased by raising the supply voltage to the source collectors. The circuit features a tri-state output which is off during the absence of data, thus not dissipating high power. It provides a balanced drive circuit giving maximum noise immunity when used with the proper line receiver. Large drive levels can be used to further increase noise immunity. The circuit is capable of driving twisted-pair lines of several miles in length of low-impedance coaxial lines.



TEST CIRCUIT



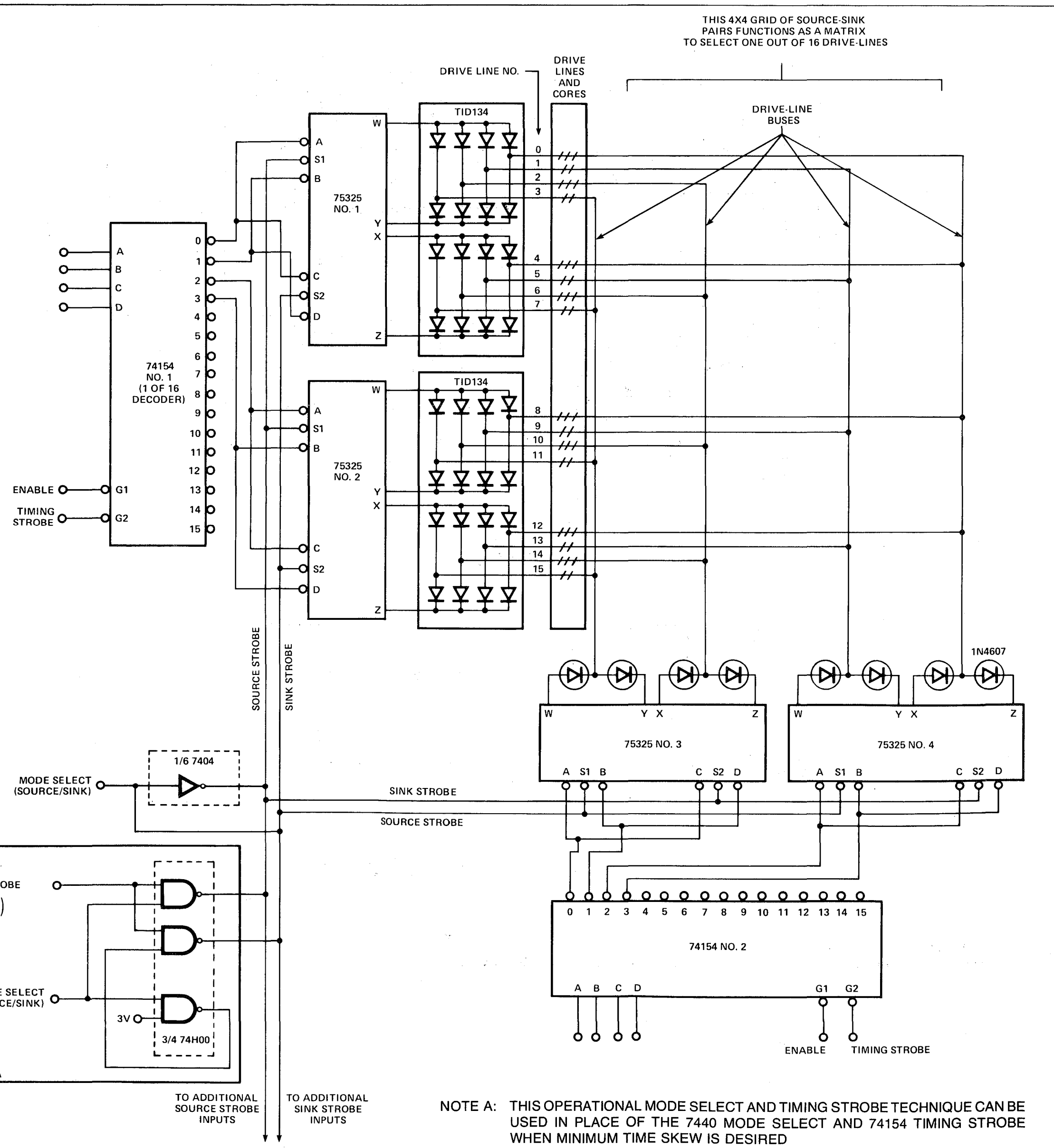
VOLTAGE WAVEFORMS

ALL RESISTORS VALUES ARE TYPICAL AND IN OHMS.
*R AND C ARE ADJUSTED TO GIVE THE DESIRED BIPOLAR OUTPUT PULSE WIDTH.

FIGURE 16 – BALANCED BIPOLAR LOGIC – LINE DRIVER

TYPICAL APPLICATION DATA (Continued)

In memory-drive applications the 75325 (or for full-temperature operation, the 55325) can be connected in any of several ways. Typically, however, sources and sinks are arranged in pairs from which many drive-lines branch off as shown in Figure 17. Here each drive-line is served by a unique combination of two source/sink pairs so that a selection matrix is formed. To select drive-line 13, 75154 No. 1 must be set to 3 (with mode select high), enabling source X of 75325 No. 2 to drive lines 12 through 15, and 74154 No. 2 must be set to 2, providing a sink at Y of 75325 No. 4 for drive-line 13 only. Alternatively, to drive current in drive-line 13 in the opposite direction, only the mode-select voltage would be changed from high to low. The size of such a matrix is limited only by the number of drive-lines that a source/sink pair can serve. This number in turn depends on the capacitive and inductive load that each drive-line of the particular system imposes on the driver. A 256-drive-line selection matrix is shown in Figure 18. These 256 drive-lines are sufficient to serve (256/2)2 = 16,384 individual cores.



NOTE A: THIS OPERATIONAL MODE SELECT AND TIMING STROBE TECHNIQUE CAN BE USED IN PLACE OF THE 7440 MODE SELECT AND 74154 TIMING STROBE WHEN MINIMUM TIME SKEW IS DESIRED

FIGURE 17 – 75325 USED AS A MEMORY DRIVER TO SELECT ONE OF SIXTEEN DRIVE LINES

TYPICAL APPLICATION DATA (Continued)

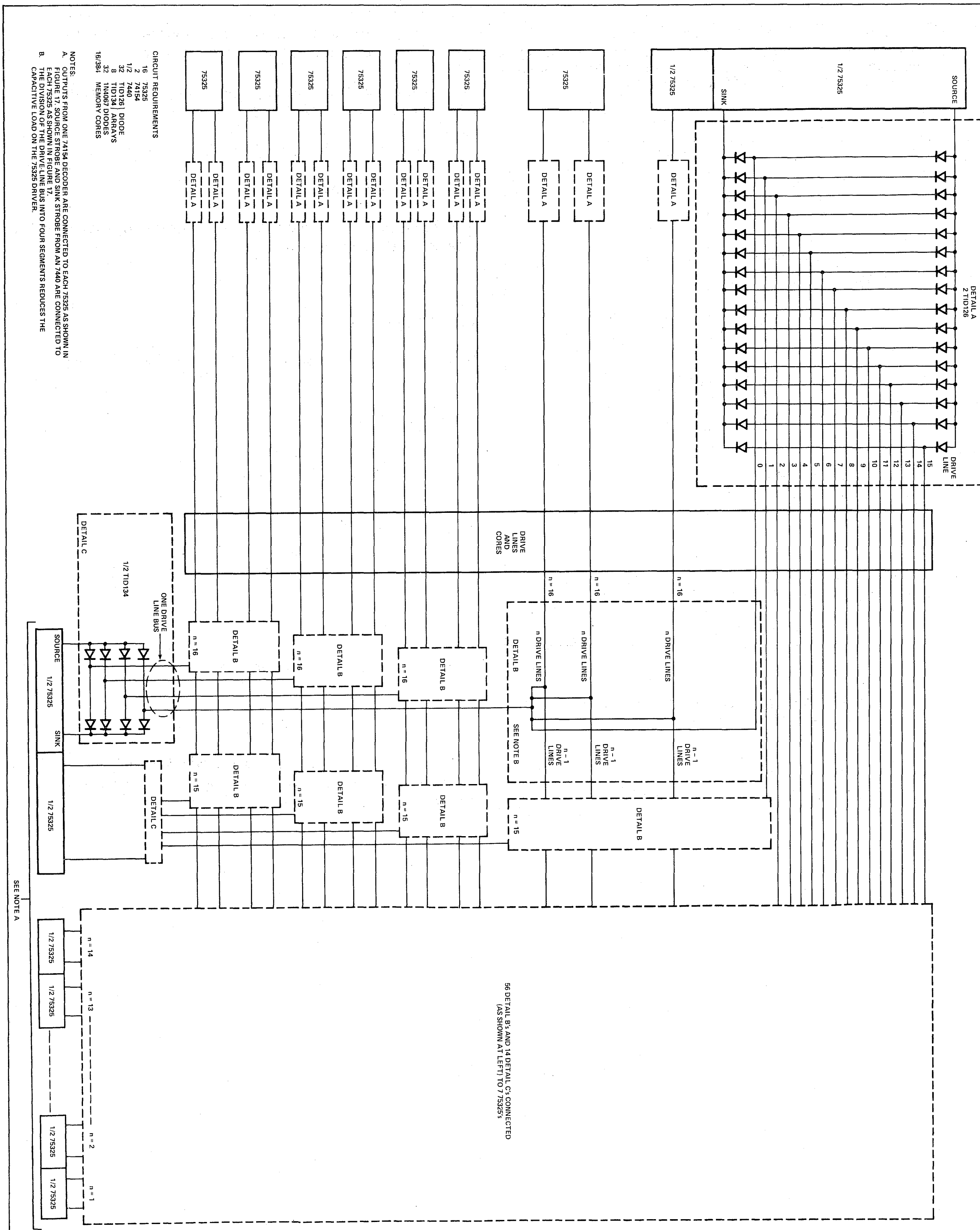
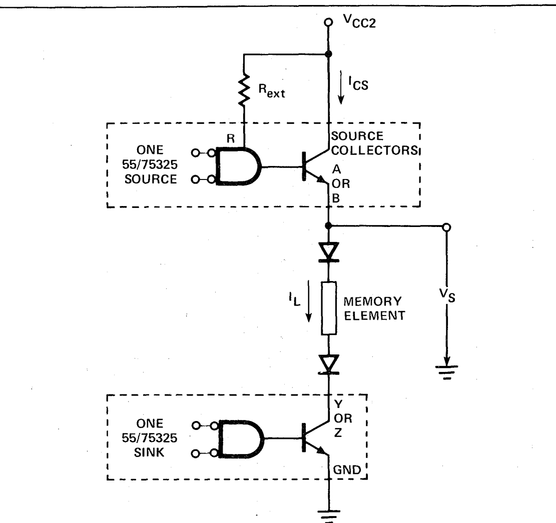


FIGURE 18 – 75325 SERVING 256 DRIVE LINES IN A MAGNETIC MEMORY

TYPICAL APPLICATION DATA (Continued)

EXTERNAL RESISTOR CALCULATION

A typical magnetic-memory word-drive requirement is shown in Figure 19. A source-output transistor of one 75325 delivers load current (I_L). The sink-output transistor of another 75325 sinks this current.



NOTES:
A. FOR CLARITY, PARTIAL LOGIC DIAGRAMS OF TWO 75325's ARE SHOWN.
B. SOURCE AND SINK SHOWN ARE IN DIFFERENT PACKAGES.

FIGURE 19

The value of the external pull-up resistor (Rext) for a particular memory application may be determined using the following equation:

$$R_{ext} = \frac{16\left[V_{CC2(min)} - V_S - 2.2\right]}{I_L - 1.6\left[V_{CC2(min)} - V_S - 2.9\right]} \quad \text{(Equation 1)}$$

where: R_{ext} is in kΩ
$V_{CC2(min)}$ is the lowest expected value of VCC2 in volts,
V_S is the source output voltage in volts with respect to ground,
I_L is in mA.

The power dissipated in resistor R_{ext} during the load current pulse duration is calculated using Equation 2,

$$P_{Rext} \approx \frac{I_L}{16}\left[V_{CC2(min)} - V_S - 2\right] \quad \text{(Equation 2)}$$

where: P_{Rext} is in mW.

After solving for R_{ext}, the magnitude of the source collector current (I_{CS}) is determined from Equation 3,

$$I_{CS} \approx 0.94\ I_L \quad \text{(Equation 3)}$$

where: I_{CS} is in mA.

As an example, let $V_{CC2(min)} = 20V$ and $V_L = 3V$ while I_L of 500mA flows.

Using Equation 1,

$$Rext = \frac{16\ (20 - 3 - 2.2)}{500 - 1.6\ (20 - 3 - 2.9)} = 0.5k\Omega$$

and from Equation 2,

$$P_{Rext} \approx \frac{500}{16}\left[20 - 3 - 2\right] \approx 470mW$$

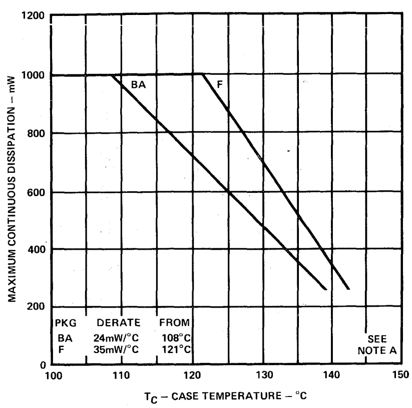
The amount of the memory system current source (ICS) from Equation 3 is:

$$I_{CS} \approx 0.94\ (500) \approx 470mA$$

In this example the regulated source-output transistor base current through the external pull-up resistor (R_{ext}) and the source gate is approximately 30mA. This current and I_{CS} comprise I_L.

THERMAL INFORMATION

CASE TEMPERATURE DISSIPATION DERATING CURVE



NOTE A: RATED OPERATING FREE-AIR TEMPERATURE RANGES MUST BE OBSERVED REGARDLESS OF HEAT SINKING.

FIGURE 20

FREE-AIR TEMPERATURE DISSIPATION DERATING CURVE

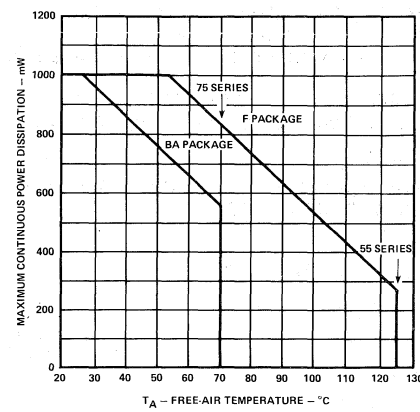


FIGURE 21

FEATURES

- DUAL POSITIVE-LOGIC NAND TTL-TO-MOS DRIVER
- VERSATILE INTERFACE CIRCUIT FOR USE BETWEEN TTL AND HIGH-CURRENT, HIGH-VOLTAGE SYSTEMS
- CAPABLE OF DRIVING HIGH-CAPACITANCE LOADS
- COMPATIBLE WITH MANY POPULAR MOS RAMs
- V_{CC2} SUPPLY VOLTAGE VARIABLE OVER WIDE RANGE TO 24 VOLTS MAXIMUM
- TTL AND DTL COMPATIBLE DIODE-CLAMPED INPUTS
- OPERATES FROM STANDARD BIPOLAR AND MOS SUPPLY VOLTAGES
- HIGH-SPEED SWITCHING
- TRANSIENT OVERDRIVE MINIMIZES POWER DISSIPATION
- LOW STANDBY POWER DISSIPATION

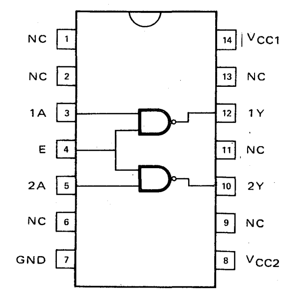
ABSOLUTE MAXIMUM RATINGS

Supply voltage range of V_{CC1} (Note 1)	−0.5V to 7V
Supply voltage range of V_{CC2}	−0.5V to 25V
Input voltage	5.5V
Inter-input voltage (Note 2)	5.5V
Continuous total dissipation at (or below) 25°C free-air temperature (Note 3):	
F package	1300mW
V package	1000mW
Operating free-air terperature range	0°C to 70°C
Storage temperature range	−65°C to 150°C
Lead temperature 1/16 inch from case for 60 seconds: F package	300°C
Lead temperature 1/16 inch from case for 10 seconds: V package	260°C

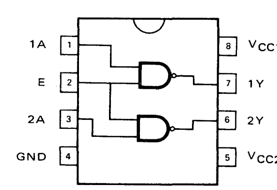
NOTES:
1. Voltage values are with respect to network ground terminal.
2. This rating applies between the A input of either driver and the common E input.
3. For operation above 25°C free-air temperature, refer to Dissipation Derating Curve, Figure 17.

PIN CONFIGURATION

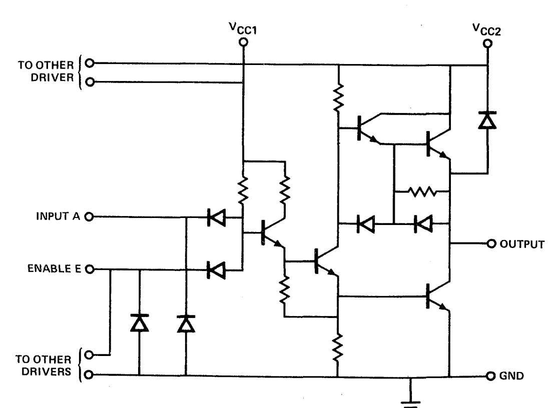
F PACKAGE



V PACKAGE



SCHEMATIC (EACH DRIVER)

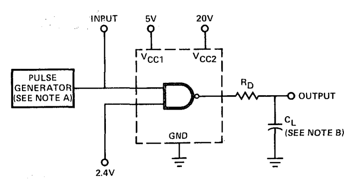


SWITCHING CHARACTERISTICS, V_{CC1} = 5V, V_{CC2} = 20V, TA = 25°C

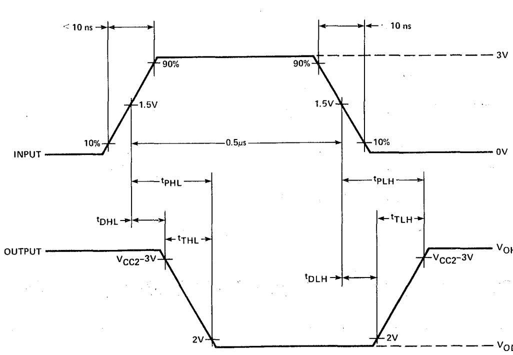
PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
t_{DLH}	Delay time, low-to-high-level output	C_L = 390pF, R_D = 10Ω, See Figure 1, Unused gate input grounded		11	20	ns
t_{DHL}	Delay time, high-to-low-level output			10	18	ns
t_{TLH}	Transition time, low-to-high-level output			25	40	ns
t_{THL}	Transition time, high-to-low-level output			21	35	ns
t_{PLH}	Propagation delay time, low-to-high-level output		10	36	55	ns
t_{PHL}	Propagation delay time, high-to-low-level output		10	31	47	ns

PARAMETER MEASUREMENT INFORMATION

TEST CIRCUIT



VOLTAGE WAVEFORM



NOTES:

A. THE PULSE GENERATOR HAS THE FOLLOWING CHARACTERISTICS: PRR = 1MHz, Z_{OUT} < 50Ω.

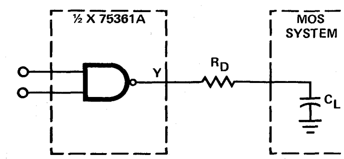
B. C_L INCLUDES PROBE AND JIG CAPACITANCE.

FIGURE 1—SWITCHING TIMES, EACH DRIVER

DESIGN PRECAUTIONS

– USE OF DAMPING RESISTOR TO REDUCE OR ELIMINATE OUTPUT TRANSIENT OVERSHOOT IN CERTAIN 75361A APPLICATIONS

The fast switching speeds of this device may produce undesirable output transient overshoot because of load or wiring inductance. A small series damping resistor may be used to reduce or eliminate this output transient overshoot. The optimum value of the damping resistor to use depends on the specific load characteristics and switching speed. A typical value would be between 10Ω and 30Ω. See Figure 13.



NOTE: $R_D \approx 10\Omega$ TO 30Ω (OPTIONAL).

FIGURE 13

POWER DISSIPATION PRECAUTIONS

Significant power may be dissipated in the 75361A driver when charging and discharging high-capacitance loads over a wide voltage range at high frequencies. Figure 5 shows the power dissipated in a typical 75361A as a function of load capacitance and frequency. Average power dissipated by this driver can be broken into three components:

$$P_{T\,(AV)} = P_{DC(AV)} + P_{C(AV)} + P_{S(AV)}$$

where $P_{DC(AV)}$ is the steady-state power dissipation with the output high or low, $P_{C(AV)}$ is the power level during charging or discharging of the load capacitance, and $P_{S(AV)}$ is the power dissipation during switching between the low and high levels. None of these include energy transferred to the load and all are averaged over a full cycle.

The power components per driver channel are:

$$P_{DC(AV)} = \frac{PL\ t_L + PH\ t_H}{T}$$

$$P_{C(AV)} \approx C\ V_C^2\ f$$

$$P_{S(AV)} = \frac{PLH\ t_{LH} + PHL\ t_{HL}}{T}$$

where the times are as defined in Figure 14.

PL, PH, PLH, and PHL are the respective instantaneous levels of power dissipation and C is load capacitance.

The 75361A is so designed that P_S is a negligible portion of P_T in most applications. Except at very high frequencies, $t_L + t_H \gg t_{LH} + t_{HL}$ so that P_S can be neglected. Figure 5 for no load demonstrates this point. The power dissipation contributions from both channels are then added together to obtain total device power.

The following example illustrates this power calculation technique. Assume both channels are operating identically with C = 200pF, f = 2MHz, V_{CC1} = 5V, V_{CC2} = 20V, and duty cycle = 60% outputs high (t_H/T = 0.6). Also, assume V_{OH} = 19.3V, V_{OL} = 0.1V, PS is negligible, and that the current from V_{CC2} is negligible when the output is high.

On a per-channel basis using data sheet values:

$$P_{DC(AV)} = \left[(5V)\left(\frac{2mA}{2}\right) + (20V)\left(\frac{0mA}{2}\right)\right](0.6) + \left[(5V)\left(\frac{16mA}{2}\right) + (20V)\left(\frac{7mA}{2}\right)\right](0.4)$$

$P_{DC(AV)}$ = 47mW per channel

$P_{C(AV)} \approx (200pF)\ (19.2V)^2\ (2MHz)$

$P_{C(AV)} \approx$ 148mW per channel.

For the total device dissipation of the two channels:

$P_{T(AV)} \approx 2\ (47 + 148)$

$P_{T(AV)} \approx$ 390mW typical for total package.

VOLTAGE WAVEFORM

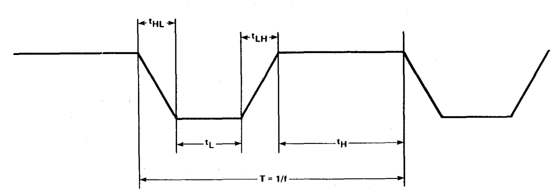


FIGURE 14—OUTPUT VOLTAGE WAVEFORM

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Analog

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AVERAGE INPUT OFFSET CURRENT t° COEFF — The change in input offset current divided by the change in ambient temperature producing it.

AVERAGE INPUT OFFSET VOLTAGE t° COEFF — The change in input offset voltage divided by the change in ambient temperature producing it.

COMMON MODE INPUT RESISTANCE — The resistance hooking into both inputs, with inputs tied together.

COMMON MODE REJECTION RATIO (CMRR) — The ratio of the change of input offset voltage to the input common mode voltage change producing it.

FULL POWER BANDWIDTH — The maximum frequency at which the full sinewave output might be obtained.

INPUT BIAS CURRENT — The average of the two input currents at zero output voltage. In some cases, the input current is measured for either input independently.

INPUT CAPACITANCE — The capacitance looking into either input terminal with the other grounded.

INPUT CURRENT — The current into an input terminal.

INPUT NOISE VOLTAGE — The square root of the mean square narrow-band noise voltage referred to the input.

INPUT OFFSET CURRENT — The difference in the currents into the two input terminals with the output at zero volts.

INPUT OFFSET VOLTAGE — That voltage which must be applied between the input terminals to obtain zero output voltage. The input offset voltage may also be defined for the case where two equal resistances are inserted in series with the input leads.

INPUT RESISTANCE — The resistance looking into either input terminal with the other grounded.

INPUT VOLTAGE RANGE — The range of voltages on the input terminals for which the amplifier operates within specifications. In some cases, the input offset specifications apply over the input voltage range.

LARGE-SIGNAL VOLTAGE GAIN — The ratio of the maximum output voltage swing to the change in input voltage required to drive the output to this voltage.

OUTPUT RESISTANCE — The resistance seen looking into the output terminal with the output at null. This parameter is defined only under small signal conditions at frequencies above a few hundred cycles to eliminate the influence of drift and thermal feedback.

OUTPUT SHORT-CIRCUIT CURRENT — The maximum output current available from the amplifier with the output shorted to ground or to either supply.

OUTPUT VOLTAGE SWING — The peak output swing, referred to zero, that can be obtained.

POWER CONSUMPTION — The DC power required to operate the amplifier with the output at zero and with no load current.

POWER SUPPLY REJECTION RATIO — The ratio of the change in input offset voltage to the change in supply voltages producing it.

RISE TIME — The time required for an output voltage step to change from 10% to 90% of its final value.

SLEW RATE — The maximum rate of change of output voltage under large signal condition.

SUPPLY CURRENT — The current required from the power supply to operate the amplifier with no load and the output at zero.

TEMPERATURE STABILITY OF VOLTAGE GAIN — The maximum variation of the voltage gain over the specified temperature range.

REGULATORS

DROPOUT VOLTAGE — The input-output voltage differential at which the circuit ceases to regulate against further reductions in input voltage.

INPUT-OUTPUT VOLTAGE DIFFERENTIAL — The range of voltage difference between the supply voltage and the regulated output voltage over which the regulator will operate.

LINE REGULATION — The percentage change in output voltage for a specified change in input voltage.

LOAD REGULATION — The percentage change in output voltage for a specified change in load current.

MAXIMUM POWER DISSIPATION — The maximum total device dissipation for which the regulator will operate within specifications.

OUTPUT NOISE VOLTAGE — The rms output noise voltage with constant load and no input ripple.

OUTPUT VOLTAGE RANGE — The range of output voltage over which the regulator will operate.

QUIESCENT CURRENT — That part of input current to the regulator that is not delivered to the load.

REFERENCE VOLTAGE — The output of the reference amplifier measured with respect to the negative supply.

RIPPLE REJECTION — The ratio of the peak-to-peak input ripple voltage to the peak-to-peak output ripple voltage.

SENSE VOLTAGE — The voltage between current sense and current limit terminals necessary to cause current limiting.

SHORT CIRCUIT CURRENT LIMIT — The output current of the regulator with the output shorted to the negative supply.

STANDBY CURRENT DRAIN — The supply current drawn by the regulator with no output load and no reference voltage load.

COMPARATORS/SENSE AMPLIFIERS

COMMON MODE FIRING VOLTAGE — The CM input voltage that exceeds the dynamic range of the inputs with strobe enabled resulting in the output switching states.

COMMON MODE RECOVERY TIME — The time from the turn off of the CM signal to the analog input threshold of the earliest sense line pulse signal that can be processed normally. Processed normally refers to bi-polar signals greater than or less than the input threshold with a corresponding proper output.

EQUIVALENT INPUT COMMON MODE NOISE VOLTAGE — The change in input offset voltage due to common mode input noise.

LOGIC INPUT HIGH VOLTAGE — The minimum voltage allowed at a bit control gate to hold the bit off.

LOGIC INPUT LOW VOLTAGE — The maximum voltage allowed at a bit control gate to hold the bit on.

OUTPUT SINK CURRENT — The maximum negative current that can be delivered by the comparator.

PEAK OUTPUT CURRENT — The maximum current that may flow into the output load without causing damage to the comparator.

PROPAGATION DELAY — The interval between the application of an input voltage step and its arrival at either output, measured at 50% of the final value.

RESPONSE TIME — The interval between the application of an input step function and the time when the output crosses the logic threshold voltage. The input step drives the comparator from some initial, saturated input voltage to an input level just barely in excess of that required to bring the output from saturation to the logic threshold voltage overdrive.

STROBE CURRENT — The maximum current drawn by the strobe terminals when it is at the zero logic level.

STROBE DELAY — The time delay measured from strobe to output threshold with a signal present exceeding the input threshold.

STROBE RELEASE TIME — The time required for the output to rise to the logic threshold voltage after the strobe terminal has been driven from the zero to the one logic level. Appropriate input conditions are assumed.

STROBED OUTPUT LEVEL — The DC output voltage, independent of input voltage, with the voltage on the strobe terminal equal to or less than a minimum specified amount.

SWITCHING SPEED — The time required to turn on the least significant bit.

THRESHOLD UNCERTAINTY — With all sense amps sharing the same input threshold less the uncertainty as a "0". This includes unit to unit, power supply and temperature variations.

THRESHOLD VOLTAGE — The typical referred to input voltage which determines whether an input is a "1" or a "0". A signal whose magnitude is greater than the threshold level is sensed as a logic "1" and a signal whose magnitude is less as a "0".

ZERO SCALE OUTPUT CURRENT — The output current for all bits turned off.

COMMUNICATIONS CIRCUITS

AGC DETECTOR SENSITIVITY — The ratio of the incremental differential DC voltage change at the AGC detector output terminals to the incremental change in peak-to-peak voltage at the AGC detector input terminal for a specified burst input level, with the local oscillator locked.

APC DETECTOR SENSITIVITY — The ratio of the incremental differential DC voltage change at the APC detector output terminals to the incremental change in relative phase at the APC detector input terminal for a specified burst input level.

AVERAGE TEMPERATURE COEFFICIENT OF OUTPUT VOLTAGE — The percentage change in output voltage for a specified change in ambient temperature.

BANDWIDTH — The frequency at which the differential gain is 3dB below its low frequency value.

DIFFERENTIAL OUTPUT VOLTAGE SWING — The peak differential output swing that can be obtained without clipping.

DIFFERENTIAL VOLTAGE GAIN — The ratio of the change in differential output voltage to the change in differential input voltage producing it.

OSCILLATOR CONTROL SENSITIVITY — The ratio of the incremental change in oscillator free running frequency to the incremental change in the differential DC voltage at the APC detector output terminals.

OUTPUT COMMON MODE VOLTAGE — The average of the voltages at the two output terminals.

OUTPUT OFFSET VOLTAGE — The difference between the voltages at the two output terminals with the inputs grounded.

TOTAL HARMONIC DISTORTION — The ratio of the sum of the amplitudes of all signals harmonically related to the fundamental, and the amplitude of the fundamental signal.

ANALOG-OPERATIONAL AMPLIFIERS
ELECTRICAL CHARACTERISTICS TABLE (Cont'd) V_S = + 15V unless otherwise specified

PARAMETER / DEVICE	TEST CONDITIONS	V_{OS} (mV) Offset Voltage $R_S \leq 10K\Omega$			V_{OS} DRIFT ($\mu V/°C$) $R_S = 0\Omega$			I_{OS} (mA) Offset Current			I_{OS} DRIFT pA/°C			I_{BIAS} (nA) Input Current		
	TEMPERATURE	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
NE531[1]	$T_A = 25°C$		2.0	6		N/A			50	200		N/A			400	1500
	$0°C \leq T_A \leq +70°C$			7.5		N/A			$T_A = +70°C$	200		N/A			$T_A = +70°C$	1500
									$T_A = 0°C$	300					$T_A = 0°C$	2000
SE531[1]	$T_A = 25°C$		2.0	5.0		N/A			30	200		N/A			300	500
	$-55°C \leq T_A +125°C$			6		N/A			$T_A = +125°C$	200		N/A			$T_A = +125°C$	500
									$T_A = -55°C$	500					$T_A = -55°C$	1500
NE532	$T_A = 25°C$		±2	±6[3]		N/A			±5	±50		N/A			I_{IN+} or I_{IN-}[4] 45	250
	$V^+ = 5V$ $0°C \leq T_A \leq +70°C$			±7.5[3]		7				±150		10				500
SA532	$T_A = 25°C$		±2	±6[3]		N/A			±5	±50		N/A			I_{IN+} or I_{IN-}[4] 45	250
	$V^+ = 5V$ $-40°C \leq T_A \leq 85°C$			±7.5[3]		7				±150		10				500
SE532	$T_A = 25°C$		±2	±5[3]		N/A			±3	±30		N/A			I_{IN+} or I_{IN-}[4] 45	150
	$V^+ = 5V$ $-55°C \leq T_A \leq 125°C$			±7[3]		7				±100		10				300
SA534	$T_A = 25°C$		±2	±7[3]		N/A			±5	±50		N/A			I_{IN+} or I_{IN-}[4] 45	250
	$-40 \leq T_A \leq 85°C$			±9[3]		7				±150						500
NE535	$T_A = 25°C$		2.0	5.0		N/A			15	40		N/A			65	150
	$0°C \leq T_A +70°C$		2.0	6.0		6.0				80		N/A				200

ANALOG-OPERATIONAL AMPLIFIERS

ELECTRICAL CHARACTERISTICS TABLE (Cont'd) V_S = + 15V unless otherwise specified

PARAMETER DEVICE	TEST CONDITIONS	V_{CM} (V) Common Mode Voltage Range			CMRR (dB) Common Mode Rejection Ratio $R_S \leq \pm 10K\Omega$			R_{IN} (MΩ) INPUT RESISTANCE			A_{VOL} (V/MV) LARGE SIGNAL VOLTAGE GAIN $R_L \geq 2K\Omega$ $V_{OUT} \pm 10V$ $V_S = \pm 15V$		
	TEMPERATURE	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
NE531[1]	T_A = 25°C	±10			70	100			20		20,000	60,000	
	0°C ≤ T_A ≤ +70°C		N/A			N/A			N/A		15,000		
SE531[1]	T_A = 25°C	±10				N/A			20		50,000	100,000	
	−55°C ≤ T_A +125°C		N/A		70	90			N/A		25,000		
NE532	T_A = 25°C		V^+ = 30V[5]		70	85			N/A		V^+ = 15V		
	V^+ = 5V	0		V^+−1.5							25	100	
	0°C ≤ T_A ≤ +70°C	0		V^+−2		N/A			N/A		15		
SA532	T_A = 25°C		V^+ = 30V[5]		70	85			N/A		V^+ = 15V		
	V^+ = 5V	0		V^+−1.5							25	100	
	−40°C ≤ T_A ≤ 85°C	0		V^+−2		N/A			N/A		15		
SE532	T_A = 25°C		V^+ = 30V[5]		70	85			N/A		V^+ = 15V		
	V^+ = 5V	0		V^+−1.5							50	100	
	−55°C ≤ T_A ≤ 125°C	0		V^+−2		N/A			N/A		25		
SA534	T_A = 25°C		V^+ = 30V[5]		70	85			N/A		V^+ = 15V		
		0		V^+−1.5							25	100	
	−40 ≤ T_A ≤ 85°C	0		V^+−2		N/A			N/A		15		
NE535	T_A = 25°C	±12	±13			N/A		1.0	6.0		50	500	
	0°C ≤ T_A +70°C		N/A		70	90			N/A		75		

ANALOG-OPERATIONAL AMPLIFIERS

ELECTRICAL CHARACTERISTICS TABLE (Cont'd) V_S = + 15V unless otherwise specified

PARAMETER DEVICE	TEST CONDITIONS	V_{OUT} OUTPUT VOLTAGE SWING (V) $R_L \geqslant 2K\Omega$			I_{CC} SUPPLY CURRENT (MA)			POWER CONSUMPTION			P_{SRR} SUPPLY VOLTAGE REJECTION RATION (μV/V) $R_S \leqslant 10K\Omega$		
	TEMPERATURE	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
NE531[1]	T_A = 25°C		N/A			5.5	10		165	300		10	150
	0°C $\leqslant T_A \leqslant$ +70°C	±10	±13			N/A			N/A			N/A	
SE531[1]	T_A = 25°C		N/A			5.5	7.0		165	210		N/A	
	-55°C $\leqslant T_A$ +125°C	±10	±13			N/A			N/A			10	150
NE532	T_A = 25°C V^+ = 5V		N/A			N/A			N/A		65	100	
	0°C $\leqslant T_A \leqslant$ +70°C	V_{OH} V^+ = 30V			$R_L = \infty$ On All Op Amps				N/A			N/A	
		26				0.5	1.2						
			$R_L \geqslant 10K\Omega$										
		27	28										
		V_{OL} V^+ = 5V											
			$R_L \leqslant 10K\Omega$										
			5mV	20mV									
SA532	T_A = 25°C V^+ = 5V		N/A			N/A			N/A		65	100	
	-40°C $\leqslant T_A \leqslant$ 85°C	V_{OH} V^+ = 30V			$R_L = \infty$ On All Op Amps				N/A			N/A	
		26				0.5	1.2						
			$R_L \geqslant 10K\Omega$										
		27	28										
		V_{OL} V^+ = 5V											
			$R_L \leqslant 10K\Omega$										
			5mV	20mV									
SE532	T_A = 25°C V^+ = 5V		N/A			N/A			N/A		65	100	
	-55°C $\leqslant T_A \leqslant$ 125°C	V_{OH} V^+ = 30V			$R_L = \infty$ On All Op Amps				N/A			N/A	
		26				0.5	1.2						
			$R_L \geqslant 10K\Omega$										
		27	28										
		V_{OL} V^+ = 5V											
			$R_L \leqslant 10K\Omega$										
			5mV	20mV									
SA534	T_A = 25°C		N/A			N/A			N/A		65	100	
	-40 $\leqslant T_A \leqslant$ 85°C	V_{OH} V^+ = 30V			$R_L = \infty$ On All Op Amps				N/A			N/A	
		26				0.8	2						
			$R_L \geqslant 10K\Omega$										
		27	28										
		V_{OL} V^+ = 5V											
			$R_L \leqslant 10K\Omega$										
			5mV	20mV									
NE535	T_A = 25°C	±10	±13			N/A			N/A			N/A	
			R_L = 10KΩ										
		±12	±14										
	0°C $\leqslant T_A$ +70°C		N/A			1.6	3.0		48	90		30	150

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ANALOG-OPERATIONAL AMPLIFIERS

ELECTRICAL CHARACTERISTICS TABLE (Cont'd) V_S = + 15V unless otherwise specified

PARAMETER DEVICE	TEST CONDITIONS	V_{OS} (mV) Offset Voltage $R_S \leq 10K\Omega$			V_{OS} DRIFT ($\mu V/°C$) $R_S = 0\Omega$			I_{OS} (mA) Offset Current			I_{OS} DRIFT pA/°C			I_{BIAS} (nA) Input Current		
	TEMPERATURE	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
SE535	T_A = 25°C		0.7	2.0		N/A			5.0	10		N/A			45	60
	$-55°C \leq T_A \leq +125°C$		0.7	3.0		3.0	1.5			20		N/A				100
NE536	T_A = 25°C		30	90		N/A			5pA			N/A			30pA	100pA[13]
	Over Temp.		30			30			N/A			N/A			N/A	
SU536	V_S = ±6V to ±20V		7.5	20		20			5pA			N/A			5pA	30pA[13]
	Over Temp.		7.5	30		N/A			N/A			N/A			250pA	3000pA
LH2101A[7]	T_A = 25°C	$R_S \leq 50K\Omega$		2.0		N/A				10		N/A				75
	$\pm 5V \leq V_S \leq \pm 20V$ $-55 \leq T_A \leq 125°C$			3.0		15				20			$25°C \leq T_A \leq 125°C$ 0.1nA $-55°C \leq T_A \leq 25°C$ 0.2nA			100
LH2201A[7]	T_A = 25°C	$R_S \leq 50K\Omega$		2.0		N/A				10			$25°C \leq T_A \leq 125°C$ 0.1nA			75
	$\pm 5V \leq V_S \leq \pm 20V$ $-25°C \leq T_A \leq 85°C$			3.0		15				20			$-55°C \leq T_A \leq 25°C$ 0.2nA			100
LH2301A[7]	T_A = 25°C	$R_S \leq 50K\Omega$		7.5		N/A				50			$25°C \leq T_A \leq 125°C$ 0.3nA			250
	$\pm 5V \leq V_S \leq \pm 15V$ $0°C \leq T_A \leq +70°C$			10		30				70			$-55°C \leq T_A \leq 25°C$ 0.6nA			300
LH2108	T_A = 25°C			2.0		N/A				0.2		N/A				2
	$\pm 5 \leq V_S \leq \pm 20V$ $-55 \leq T_A \leq 125°C$			3.0			15			0.4		2.5				3
LH2108A	T_A = 25°C			0.5		N/A				0.2		N/A				2.0
	$\pm 5V \leq V_S \leq \pm 20V$ $-55 \leq T_A \leq 125°C$			1.0			5			0.4		2.5				3.0
LH2208	T_A = 25°C			2.0		N/A				0.2		N/A				2.0
	$\pm 5V \leq V_S \leq \pm 20V$ $-25 \leq T_A \leq 85°C$			3.0			15			0.4		2.5				3.0
LH2208A	T_A = 25°C			0.5		N/A				0.2		N/A				2.0
	$\pm 5V \leq V_S \leq \pm 20V$ $-25 \leq T_A \leq 85°C$			1.0			5			0.4		2.5				3.0

ANALOG-OPERATIONAL AMPLIFIERS

ELECTRICAL CHARACTERISTICS TABLE (Cont'd) V_S = + 15V unless otherwise specified

PARAMETER / DEVICE	TEST CONDITIONS	V_{CM} (V) Common Mode Voltage Range			CMRR (dB) Common Mode Rejection Ratio $R_S \leq \pm 10K\Omega$			R_{IN} (MΩ) INPUT RESISTANCE			A_{VOL} (V/MV) LARGE SIGNAL VOLTAGE GAIN $R_L \geq 2K\Omega$ $V_{OUT} \pm 10V$ $V_S = \pm 15V$		
	TEMPERATURE	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
SE535	$T_A = 25°C$	±12	±13			N/A		3.0	10		50	500	
	$-55°C \leq T_A \leq +125°C$		N/A		70	90			N/A		25		
NE536	$T_A = 25°C$	±10	±11		$V_{IN} = \pm 10V$ 64	80			$10\Omega^{14}$			50	100
	Over Temp.		N/A			N/A			N/A		25	100	
SU536	$V_S = \pm 6V$ to $\pm 20V$	±10	±11		70	80			$10\Omega^{14}$		50	100	
	Over Temp.		N/A			N/A			N/A		50	100	
LH2101A[7]	$T_A = 25°C$ $\pm 5V \leq V_S \leq \pm 20V$		N/A			N/A		1.5			50		
	$-55 \leq T_A \leq 125°C$	$V_S = \pm 20$ ±15			$R_S \leq 50K$ 80				N/A		25		
LH2201A[7]	$T_A = 25°C$ $\pm 5V \leq V_S \leq \pm 20V$		N/A			N/A		1.5			50		
	$-25°C \leq T_A \leq 85°C$	$V_S = \pm 20$ ±15			$R_S \leq 50K$ 80				N/A		25		
LH2301A[7]	$T_A = 25°C$ $\pm 5V \leq V_S \leq \pm 15V$		N/A			N/A		0.5			25		
	$0°C \leq T_A \leq +70°C$	±12			70	$R_S \leq 50K$			N/A		15		
LH2108	$T_A = 25°C$ $\pm 5 \leq V_S \leq \pm 20V$		N/A			N/A		3.0			50	$R_L \geq 10K\Omega$ $V_S = \pm 15$	
	$-55 \leq T_A \leq 125°C$	±13			85				N/A		25		
LH2108A	$T_A = 25°C$ $\pm 5V \leq V_S \leq \pm 20V$		N/A			N/A		3.0			80	$R_L \geq 10K\Omega$ $V_S = \pm 15$	
	$-55 \leq T_A \leq 125°C$	±13.5			96				N/A		40		
LH2208	$T_A = 25°C$ $\pm 5V \leq V_S \leq \pm 20V$					N/A		3.0			50	$R_L \geq 10K\Omega$ $V_S = \pm 15$	
	$-25 \leq T_A \leq 85°C$	±13.5			85				N/A		25		
LH2208A	$T_A = 25°C$ $\pm 5V \leq V_S \leq \pm 20V$		N/A			N/A		3.0			80	$R_L \geq 10K\Omega$ $V_S = \pm 15$	
	$-25 \leq T_A \leq 85°C$	±13.5			96				N/A		40		

ANALOG-OPERATIONAL AMPLIFIERS
ELECTRICAL CHARACTERISTICS TABLE (Cont'd) V_S = + 15V unless otherwise specified

PARAMETER DEVICE	TEST CONDITIONS	V_{OUT} OUTPUT VOLTAGE SWING (V) $R_L \geq 2K\Omega$			I_{CC} SUPPLY CURRENT (MA)			POWER CONSUMPTION			P_{SRR} SUPPLY VOLTAGE REJECTION RATION (μV/V) $R_S \leq 10K\Omega$		
	TEMPERATURE	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
SE535	T_A = 25°C −55°C ≤ T_A ≤ +125°C	±10 ±12	±13 R_L = 10KΩ ±14 N/A			N/A 1.6	3.0		N/A 48	90		N/A 30	150
NE536	T_A = 25°C Over Temp.	±10 ±12	V_S = ± 15V ±11 $R_L \geq$ 10KΩ ±13 N/A			V_{OUT} = 0V 6.0 N/A	8.0		180 N/A	240		±6 ≤ V_S ≤ ±15 100 N/A	300
SU536	V_S = ±6V to ±20V Over Temp.	±10 ±12	V_S = ±15V ±12 $R_L \geq$ 10K ±13 N/A			V_{OUT} = 0V V_S = ±20V 4.5 N/A	5.5		N/A N/A			±6 ≤ V_S ≤ ±20 50 N/A	150
LH2101A	T_A = 25°C ±5V ≤ V_S ≤ ± 20V −55 ≤ T_A ≤ 125°C	±10V ±12	N/A V_S = ±15 $R_L \geq$ 10K			V_S = ±20V T_A = 125°C V_S = ±20V	3.0 2.5			120 100	80dB	N/A $R_S \leq$ 50K	
LH2201A[7]	T_A = 25°C ±5V ≤ V_S ≤ ± 20V −25°C ≤ T_A ≤ 85°C	±10V ±12V	N/A V_S = ±15 $R_L \geq$ 10K			V_S = ±20V T_A = +125°C V_S = ±20V	3.0 2.5			132 100	80dB	N/A $R_S \leq$ 50K	
LH2301A[7]	T_A = 25°C ±5V ≤ V_S ≤ ±15V 0°C ≤ T_A ≤ +70°C	±10V ±12V	N/A V_S = ±15V $R_L \geq$ 10K			V_S = ±15V N/A	3.0		N/A	90	70dB	N/A $R_S \leq$ 50K	
LH2108	T_A = 25°C ±5 ≤ V_S ≤ ±20V −55 ≤ T_A ≤ 125°C	±13	N/A V_S = ±15 $R_L \geq$ 10K			T_A = +125°C	0.6 0.4		N/A N/A		80dB	N/A	
LH2108A	T_A = 25°C ±5V ≤ V_S ≤ ±20V −55 ≤ T_A ≤ 125°C	±13	N/A V_S = ±15 $R_L \geq$ 10K			T_A = +125°C	0.6 0.4		N/A N/A		96dB	N/A	
LH2208	T_A = 25°C ±5V ≤ V_S ≤ ±20V −25 ≤ T_A ≤ 85°C	±13	N/A V_S = ±15 $R_L \geq$ 10K			T_A = +125°C	0.6 0.4		N/A N/A		80dB	N/A	
LH2208A	T_A = 25°C ±5V ≤ V_S ≤ ±20V −25 ≤ T_A ≤ 85°C	±13	N/A V_S = ±15 $R_L \geq$ 10K			T_A = +125°C	0.6 0.4		N/A N/A		96dB	N/A	

ANALOG-OPERATIONAL AMPLIFIERS
ELECTRICAL CHARACTERISTICS TABLE (Cont'd) V_S = + 15V unless otherwise specified

PARAMETER / DEVICE	TEST CONDITIONS	V_{OS} (mV) Offset Voltage $R_S \leq 10K\Omega$			V_{OS} DRIFT ($\mu V/^\circ C$) $R_S = 0\Omega$			I_{OS} (mA) Offset Current			I_{OS} DRIFT $pA/^\circ C$			I_{BIAS} (nA) Input Current		
	TEMPERATURE	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
LH2308	$T_A = 25^\circ C$, $\pm 5V \leq V_S \leq \pm 15V$			7.5		N/A				1.0		N/A				7.0
	$0^\circ C \leq T_A \leq 70^\circ C$			10			30			1.5		7.5				10
LH2308A	$T_A = 25^\circ C$, $\pm 5V \leq V_S \leq \pm 15V$			0.5		N/A				1.0		N/A				7.0
	$0^\circ C \leq T_A \leq 70^\circ C$			0.73			5			1.5		2.5				10
LM101	$T_A = 25^\circ C$, $\pm 5V \leq V_S \leq \pm 20V$, $C_1 = 30pF$		1.0	5.0	$R_S \leq 50\Omega$	3.0			40	200		N/A			120	500
					$R_S \leq 10K\Omega$	6.0										
								$T_A = +125^\circ C$	10nA	200nA				$T_A = -55^\circ C$	280	1500
	$-55^\circ C \leq T_A \leq 125^\circ C$			6.0				$T_A = -55^\circ C$	100	500						
LM101A	$T_A = 25^\circ C$	$R_S \leq 50K\Omega$	0.7	2.0		N/A			1.5	10		N/A			30	75
	$\pm 5V \leq V_S \leq \pm 20V$, $C_1 = 30pF$, $-55^\circ C \leq T_A \leq 125^\circ C$			3.0		3.0	15			20	$25^\circ C \leq T_A \leq 125^\circ C$	0.01	0.1			100
											$-55^\circ C \leq T_A \leq 25^\circ C$	0.02	0.2			
LM201	$T_A = 25^\circ C$, $\pm 5V \leq V_S \leq \pm 20V$, $C_1 = 30pF$		2.0	7.5	$R_S \leq 50\Omega$	6			100	500		N/A			25	1500
					$R_S \leq 10K\Omega$	10										
	$25^\circ C \leq T_A \leq 85^\circ C$			10				$T_A = +70^\circ C$	50	400		N/A		$T_A = 0^\circ C$	320	2000
								$T_A = 0^\circ C$	150	750						
LM201A	$T_A = 25^\circ C$	$R_S \leq 50K\Omega$	0.7	2.0		N/A			1.5	10		N/A			30	75
	$\pm 5V \leq V_S \leq \pm 20V$, $C_1 = 30pF$, $-25^\circ C \leq T_A \leq +85^\circ C$			3.0		3.0	1.5			20	$-25^\circ C \leq T_A \leq 125^\circ C$	0.01	0.1			100
											$-55^\circ C \leq T_A \leq 25^\circ C$	0.02	0.2			
LM301A	$T_A = 25^\circ C$	$R_S \leq 50K\Omega$	2.0	7.5		N/A			3	50		N/A			70	250
	$\pm 5V \leq V_S \leq \pm 15V$, $C_1 = 30pF$, $0^\circ C \leq T_A \leq 70^\circ C$			10		6.0	3.0			70	$25^\circ C \leq T_A \leq 70^\circ C$	0.01	0.3			300
											$0^\circ C \leq T_A \leq 25^\circ C$	0.02	0.6			
LM107[7,8,9,10]	$T_A = 25^\circ C$		0.7	2.0		N/A			1.5	10		N/A			30	75
	$-55^\circ C \leq T_A \leq 125^\circ C$			3.0		3.0	15			20	$25^\circ C \leq T_A \leq 125^\circ C$	0.01	0.1			100
											$-55^\circ C \leq T_A \leq 25^\circ C$	0.02	0.2			

ANALOG-OPERATIONAL AMPLIFIERS

ELECTRICAL CHARACTERISTICS TABLE (Cont'd) V_S = + 15V unless otherwise specified

PARAMETER / DEVICE	TEST CONDITIONS	V_{CM} (V) Common Mode Voltage Range			CMRR (dB) Common Mode Rejection Ratio $R_S \leqslant \pm 10K\Omega$			R_{IN} (MΩ) INPUT RESISTANCE			A_{VOL} (V/MV) LARGE SIGNAL VOLTAGE GAIN $R_L \geqslant 2K\Omega$ $V_{OUT} \pm 10V$ $V_S = \pm 15V$		
	TEMPERATURE	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
LH2308	T_A = 25°C		N/A			N/A		1.0				$V_S = \pm 15$	
	$\pm 5V \leqslant V_S \leqslant \pm 15V$										25		
									N/A		15		
	$0°C \leqslant T_A \leqslant 70°C$	±14			80								
LH2308A	T_A = 25°C		N/A			N/A		1.0			80	$R_L \geqslant 10K\Omega$ $V_S = \pm 15$	
	$\pm 5V \leqslant V_S \leqslant \pm 15V$												
									N/A		60		
	$0°C \leqslant T_A \leqslant 70°C$	±14			76								
LM101	T_A = 25°C		N/A			N/A		0.3	0.8		50	160	
	$\pm 5V \leqslant V_S \leqslant \pm 20V$												
	C_1 = 30pF												
	$-55°C \leqslant T_A \leqslant 125°C$	±12			70	90			N/A		25		
LM101A	T_A = 25°C		N/A			N/A		1.5	4		50	160	
	$\pm 5V \leqslant V_S \leqslant \pm 20V$,	$V_S = \pm 20$			$R_S \leqslant 50K$								
	C_1 = 30pF												
	$-55°C \leqslant T_A \leqslant 125°C$	±15			80	96			N/A		25		
LM201	T_A = 25°C		N/A			N/A		0.1	0.4		20	150	
	$\pm 5V \leqslant V_S \leqslant \pm 20V$,												
	C_1 = 30pF												
									N/A		15		
	$0°C \leqslant T_A \leqslant 70°C$	±12			65	90							
LM201A	T_A = 25°C		N/A			N/A		1.5	4		50	160	
	$\pm 5V \leqslant V_S \leqslant \pm 20V$,												
	C_1 = 30pF	V_S = ±20			$R_S \leqslant 50K$.								
	$-25°C \leqslant T_A \leqslant +85°C$	±15			80	96			N/A		25		
LM301A	T_A = 25°C		N/A			N/A		0.5	2		25	160	
	$\pm 5V \leqslant V_S \leqslant \pm 15V$,				$R_S \leqslant 50K$								
	C_1 = 30pF												
	$0°C \leqslant T_A \leqslant 70°C$	±12			70	90			N/A		15		
LM107[7,8,9,10]	T_A = 25°C		N/A			N/A		1.5	4		50	160	
		$V_S = \pm 20$											
	$-55°C \leqslant T_A \leqslant 125°C$	±15			80	96			N/A		25		

ANALOG-OPERATIONAL AMPLIFIERS
ELECTRICAL CHARACTERISTICS TABLE (Cont'd) V_S = + 15V unless otherwise specified

PARAMETER / DEVICE	TEST CONDITIONS	V_{OUT} OUTPUT VOLTAGE SWING (V) $R_L \geq 2K\Omega$			I_{CC} SUPPLY CURRENT (MA)			POWER CONSUMPTION			PSRR SUPPLY VOLTAGE REJECTION RATION (μV/V) $R_S \leq 10K\Omega$		
	TEMPERATURE	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
LH2308	$T_A = 25°C$		N/A				0.8		N/A			N/A	
	$\pm5V \leq V_S \leq \pm15V$		$V_S = \pm15$										
			$R_L \geq 10K$										
	$0°C \leq T_A \leq 70°C$	±13				N/A			N/A		80dB		
LH2308A	$T_A = 25°C$		N/A				0.8		N/A			N/A	
	$\pm5V \leq V_S \leq \pm15V$		$V_S = \pm15$										
			$R_L \geq 10K$										
	$0°C \leq T_A \leq 70°C$	±13				N/A			N/A		96dB		
LM101	$T_A = 25°C$					$V_S = \pm20V$							
	$\pm5V \leq V_S \leq \pm20V$	±10	±13			1.8	3.0		72	120		N/A	
	$C_1 = 30pF$		$R_L = 10K$										
		±12	±14										
						$T_A = +125°C$							
	$-55°C \leq T_A \leq 125°C$		N/A			1.2	2.5		48	100	70dB	90dB	
LM101A						$V_S = \pm20V$							
	$T_A = 25°C$		N/A			1.8	3.0		72	120		N/A	
	$\pm5V \leq V_S \leq \pm20V$,											$R_S \leq 10K$	
	$C_1 = 30pF$	±10	±13			$T_A = +125°C$							
	$-55°C \leq T_A \leq 125°C$		$R_L \geq 10K$			1.2	2.5		48	100	80dB	96dB	
		±12	±14										
LM201						$V_S = \pm20V$							
	$T_A = 25°C$		N/A			1.8	3.0		72	120		N/A	
	$\pm5V \leq V_S \leq \pm20V$,	±10	±13										
	$C_1 = 30pF$		$R_L = 10K$										
		±12	±14			N/A			N/A		70dB	90dB	
	$-25°C \leq T_A \leq +85°C$												
LM201A						$V_S = \pm20V$							
	$T_A = 25°C$		N/A			1.8	3.0		72	120		N/A	
	$\pm5V \leq V_S \leq \pm20V$,												
	$C_1 = 30pF$	±10	±13										
	$-25°C \leq T_A \leq +85°C$		$R_L = 10K$			$T_A = +125°C$						$R_S \leq 50K$	
		±12	±14			1.2	2.5		48	100	80dB	96dB	
LM301A						$V_S = \pm15V$							
	$T_A = 25°C$		N/A			1.8	3.0		54	90		N/A	
	$\pm5V \leq V_S \leq \pm15V$,												
	$C_1 = 30pF$	±10	±13									$R_S \leq 50K$	
	$0°C \leq T_A \leq 70°C$		$R_L = 10K$			N/A			N/A		70dB	96dB	
		±12	±14										
LM107[7,8,9,10]						$V_S = \pm20V$							
	$T_A = 25°C$		N/A			1.8	3.0		72	120		N/A	
		±10	±13										
	$-55°C \leq T_A \leq 125°C$		$R_L = 10K$			$T_A = +125°C$							
		±12	±14			1.2	2.5		48	100	80dB	96dB	

ANALOG-OPERATIONAL AMPLIFIERS
ELECTRICAL CHARACTERISTICS TABLE (Cont'd) V_S = + 15V unless otherwise specified

PARAMETER DEVICE	TEST CONDITIONS	V_{OS} (mV) Offset Voltage $R_S \leq 10K\Omega$			V_{OS} DRIFT (μV/°C) $R_S = 0\Omega$			I_{OS} (mA) Offset Current			I_{OS} DRIFT pA/°C			I_{BIAS} (nA) Input Current		
	TEMPERATURE	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
LM207[7,8,9,10]	T_A = 25°C		0.7	2.0		N/A			1.5	10		N/A			30	75
	−25°C ≤ T_A ≤ 85°C			3.0		3.0	15			20	25°C ≤ T_A ≤ 85°C	0.01	0.1			100
											−25°C ≤ T_A ≤ 25°C	0.02	0.2			
LM307[7,8,9,10]	T_A = 25°C	$R_S \leq 50K\Omega$	2.0	7.5		N/A			3	50		N/A			70	250
	0°C ≤ T_A ≤ 70°C			10		6.0	3.0			70	25°C ≤ T_A ≤ 70°C	0.01	0.3			300
											0°C ≤ T_A ≤ 25°C	0.02	0.6			
LM108[7]	T_A = 25°C ±5V ≤ V_S ≤ ±20V		0.7	2.0[11]		N/A			0.05	0.2		N/A			0.8	2.0
	−55 ≤ T_A ≤ 125°C			3.0[11]		3.0	15[11]			0.4		0.5	2.5			3.0
LM108A	T_A = 25°C ±5V ≤ V_S ≤ ±20V		0.3	0.5[12]		N/A			0.05	0.2		N/A			0.8	2.0
	−55 ≤ T_A ≤ 125°C			1.0[12]		1.0	5.0[12]			0.4		0.5	2.5			3.0
LM208[7]	T_A = 25°C ±5V ≤ V_S ≤ ±20V		0.7	2.0[11]		N/A			0.05	0.2		N/A			0.8	2.0
	−25 ≤ T_A ≤ 85°C			3.0[11]		3.0	15[11]			0.4		0.5	2.5			3.0
LM208A	T_A = 25°C ±5V ≤ V_S ≤ ±20V		0.3	0.5[12]		N/A			0.05	0.2		N/A			0.8	2.0
	−25°C ≤ T_A ≤ 85°C			1.0[12]		1.0	5.0[12]			0.4		0.5	2.5			3.0
LM308A	T_A = 25°C ±5V ≤ V_S ≤ +15V		0.3	0.5		N/A			0.2	0.1		N/A			1.5	7
	0°C ≤ T_A ≤ 70°C			0.75		1.0	5.0[12]			1.5		2.0	10			10
LM124	T_A = 25°C V^+ = 5V		±2	±5[3]		N/A			±3	±30		N/A		I_{IN^+} or I_{IN^-}[4]	45nA	150nA
	−55 ≤ T_A ≤ 125°C			±7[3]		7				±100		10				300nA
LM224	T_A = 25°C V^+ = 5V		±2	±7[3]		N/A			±5	±50		N/A		I_{IN^+} or I_{IN^-}[4]	45nA	250nA
	−25 ≤ T_A ≤ 85°C			±9[3]		7				±150		10				500nA

ANALOG-OPERATIONAL AMPLIFIERS
ELECTRICAL CHARACTERISTICS TABLE (Cont'd) V_S = + 15V unless otherwise specified

PARAMETER DEVICE	TEST CONDITIONS	V_{CM} (V) Common Mode Voltage Range			CMRR (dB) Common Mode Rejection Ratio $R_S \leq$ 10KΩ			R_{IN} (MΩ) INPUT RESISTANCE			A_{VOL} (V/MV) LARGE SIGNAL VOLTAGE GAIN $R_L \geq 2K\Omega$ V_{OUT} ± 10V V_S = ± 15V		
	TEMPERATURE	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
LM207[7,8,9,10]	T_A = 25°C		N/A			N/A		1.5	4		50	160	
		V_S = ±20											
	−25°C ≤ T_A ≤ 85°C	±15			80	96			N/A		25		
LM307[7,8,9,10]	T_A = 25°C		N/A			N/A		0.5	2		25	160	
					$R_S \leq$ 50K								
	0°C ≤ T_A ≤ 70°C	±12			70	90			N/A		15		
LM108[7]												$R_L \geq$ 10KΩ	
	T_A = 25°C		N/A			N/A		30	70		50	300	
	±5V ≤ V_S ≤ ±20V												
	−55 ≤ T_A ≤ 125°C	±13.5			85	100			N/A		25		
LM108A	T_A = 25°C		N/A			N/A		30	70		80	$R_L \geq$ 10KΩ	
	±5V ≤ V_S ≤ ±20V											300	
	−55 ≤ T_A ≤ 125°C	±13.5			96	110			N/A		40		
LM208[7]	T_A = 25°C		N/A			N/A		30	70		50	$R_L \geq$ 10KΩ	
	±5V ≤ V_S ≤ ±20V											300	
	−25 ≤ T_A ≤ 85°C	±13.5			85	100			N/A		25		
LM208A	T_A = 25°C		N/A			N/A		30	70		80	$R_L \geq$ 10KΩ	
	±5V ≤ V_S ≤ ±20V											300	
	−25°C ≤ T_A ≤ 85°C	±13.5			96	110			N/A		40		
LM308A	T_A = 25°C		N/A			N/A		10	40		80	$R_L \geq$ 10KΩ	
	±5V ≤ V_S ≤ +15V											300	
	0°C ≤ T_A ≤ 70°C	±14			96	110			N/A		60		
LM124	T_A = 25°C		V^+ = 30V[5]									V^+ = 15V	
	V^+ = 5V	0		V^+-1.5	70	85			N/A		50	100	
	−55 ≤ T_A ≤ 125°C	0		V^+ −2		N/A			N/A		25		
LM224	T_A = 25°C		V^+ = 30V[5]									V^+ = 15	
	V^+ = 5V	0		V± 1.5	65	85			N/A		25	100	
	−25 ≤ T_A ≤ 85°C	0		V^+ −2		N/A			N/A		15		

ANALOG-OPERATIONAL AMPLIFIERS
ELECTRICAL CHARACTERISTICS TABLE (Cont'd) V_S = + 15V unless otherwise specified

PARAMETER DEVICE	TEST CONDITIONS	V_{OUT} OUTPUT VOLTAGE SWING (V) $R_L \geq 2K\Omega$			I_{CC} SUPPLY CURRENT (MA)			POWER CONSUMPTION			P_{SRR} SUPPLY VOLTAGE REJECTION RATION (μV/V) $R_S \leq 10K\Omega$		
	TEMPERATURE	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
LM207[7,8,9,10]	T_A = 25°C		N/A			V_S = ±20V						N/A	
						1.8	3.0		72	120			
	−25°C ≤ T_A ≤ 85°C	±10	±13			T_A = +125°C							
			R_L = 10K			1.2	2.5		48	100	80dB	96dB	
		±12	±14										
LM307[7,8,9,10]	T_A = 25°C		N/A			V_S = ±15V						N/A	
		±10	±13			1.8	3.0		54	90		$R_S \leq$ 50K	
			R_L = 10K										
	0°C ≤ T_A ≤ 70°C	±12	±14			N/A			N/A		70dB	96dB	
LM108[7]	T_A = 25°C		N/A			0.3	0.6		N/A			N/A	
	±5V ≤ V_S ≤ ±20V		R_L = 10KΩ			T_A = +125°C							
	−55 ≤ T_A ≤ 125°C	±13	±14			0.15	0.4		N/A		80dB	96dB	
LM108A	T_A = 25°C		N/A			0.3	0.6		N/A			N/A	
	±5V ≤ V_S ≤ ±20V		R_L = 10KΩ			T_A = +125°C			N/A				
	−55 ≤ T_A ≤ 125°C	±13	±14			0.15	0.4				96dB	110dB	
LM208[7]	T_A = 25°C		N/A			0.3	0.6		N/A			N/A	
	±5V ≤ V_S ≤ ±20V		R_L = 10KΩ			T_A = +125°C							
	−25 ≤ T_A ≤ 85°C	±13	±14			0.15	0.4		N/A		80dB	96dB	
LM208A	T_A = 25°C		N/A			0.3	0.6		N/A			N/A	
	±5V ≤ V_S ≤ ±20V												
	−25°C ≤ T_A ≤ 85°C		R_L = 10KΩ			T_A = +125°C							
		±13	±14			0.15	0.4		N/A		96dB	110dB	
LM308A	T_A = 25°C		N/A			V_S = ±15V							
						0.3	0.8		9	24		N/A	
	±5V ≤ V_S ≤ +15V		R_L = 10KΩ										
	0°C ≤ T_A ≤ 70°C	±13	±14			N/A			N/A		96dB	110dB	
LM124	T_A = 25°C		N/A			N/A			N/A		65	100	
	V^+ = 5V		V_{OH} V^+ = 30V										
		26											
			$R_L \geq$ 10KΩ										
		27	28										
			V_{OL} V^+ = 5V			R_L = ∞ On All Op Amps							
			$R_L \leq$ 10KΩ			0.8	2		N/A			N/A	
			5	20									
	−55 ≤ T_A ≤ 125°C												
LM224	T_A = 25°C		N/A			N/A			N/A		65	100	
	V^+ = 5V		V_{OH} V^+ = 30V										
		26											
			$R_L \geq$ 10KΩ										
		27	28										
			V_{OL} V^+ = 5V										
			$R_L \leq$ 10KΩ			R_L = ∞ On All Op Amps							
	−25 ≤ T_A ≤ 85°C		5	20		0.8	2		N/A			N/A	

ANALOG-OPERATIONAL AMPLIFIERS
ELECTRICAL CHARACTERISTICS TABLE (Cont'd) V_S = + 15V unless otherwise specified

PARAMETER DEVICE	TEST CONDITIONS	V_{OS} (mV) Offset Voltage $R_S \leq 10K\Omega$			V_{OS} DRIFT ($\mu V/^{\circ}C$) $R_S = 0\Omega$			I_{OS} (mA) Offset Current			I_{OS} DRIFT $pA/^{\circ}C$			I_{BIAS} (nA) Input Current		
	TEMPERATURE	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
LM324	$T_A = 25^{\circ}C$ $V^+ = 5V$		±2	±7[3]		N/A			±5	±50		N/A		I_{IN^+} or I_{IN^-}[4]	45nA	250nA
	$0^{\circ}C \leq T_A \leq 70^{\circ}C$			±9[3]		7				±150		10				500nA
MC1456	$T_A = 25^{\circ}C$		5.0	10		N/A			5.0	10		N/A			15	30
	$0^{\circ}C \leq T_A \leq 70^{\circ}C$			14		N/A				14		N/A				40
MC1556	$T_A = 25^{\circ}C$		2.0	4.0		N/A			1.0	2.0		N/A			0.8	15
	$-55 \leq T_A \leq 125^{\circ}C$			6.0		N/A		$25 \leq T_A \leq 125^{\circ}C$		3.0 $-55 \leq T_A \leq 25^{\circ}C$ 5.0		N/A				30
MC1458	$T_A = 25^{\circ}C$		2.0	6.0		N/A			30	200		N/A			200	500
	$0^{\circ}C \leq T_A \leq 70^{\circ}C$			7.5		N/A				300		N/A				800
MC1558	$T_A = 25^{\circ}C$		1.0	5.0		N/A			30	200		N/A			200	500
	$-55 \leq T_A \leq 125^{\circ}C$			6.0		N/A				500		N/A				1500
μA709	$T_A = 25^{\circ}C$ $\pm 9 \leq V_S \leq \pm 15$		1	5		$R_S = 50\Omega$ 3.0 $R_S \leq 10K$			50	200		N/A			200nA	500nA
								$T_A = +125^{\circ}C$								
	$-55^{\circ}C \leq T_A \leq +125^{\circ}C$			6		6.0			20	200				$T_A = -55^{\circ}C$	0.5	1.5
								$T_A = -55^{\circ}C$								
						N/A			100	500		N/A				
μA709C	$T_A = 25^{\circ}C$		2	7.5		N/A			100	500		N/A			300nA	1500nA
	$0^{\circ}C \leq T_A \leq 70^{\circ}C$			10		N/A				750		N/A			N/A	
μA740	$T_A = 25^{\circ}C$	$R_S \leq 100K\Omega$	30			N/A			60pA			N/A			0.1nA	2.0nA
	$0^{\circ}C \leq T_A \leq +70^{\circ}C$		30			N/A			60pA			N/A			1.1nA	1.0nA
μA741	$T_A = 25^{\circ}C$		1.0	5.0		N/A			10	200		N/A			80nA	500nA
								$T_A = +125^{\circ}C$						$T_A = +125^{\circ}C$		
	$-55^{\circ}C \leq T_A \leq +125^{\circ}C$		1.0	6.0		N/A			7.0	200		N/A			30	500
								$T_A = -55^{\circ}C$						$T_A = -55^{\circ}C$		
									20	500					300	1500
μA741C	$T_A = 25^{\circ}C$		2.0	6.0		N/A			20	200		N/A			80	500
	$0^{\circ}C \leq T_A \leq +70^{\circ}C$			7.5		N/A				300		N/A				800

ANALOG-OPERATIONAL AMPLIFIERS

ELECTRICAL CHARACTERISTICS TABLE (Cont'd) V_S = + 15V unless otherwise specified

PARAMETER / DEVICE	TEST CONDITIONS	V_{CM} (V) Common Mode Voltage Range			CMRR (dB) Common Mode Rejection Ratio $R_S \leqslant \pm$ 10KΩ			R_{IN} (MΩ) INPUT RESISTANCE			A_{VOL} (V/MV) LARGE SIGNAL VOLTAGE GAIN $R_L \geqslant$ 2KΩ V_{OUT} ± 10V V_S = ± 15V		
	TEMPERATURE	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
LM324	T_A = 25°C		V^+ = 30V[5]		65	85			N/A			V^+ = 15	
	V^+ = 5V	0		V±1.5							25	100	
	0°C ≤ T_A ≤ 70°C	0		V^+ −2		N/A			N/A		15		
MC1456	T_A = 25°C	±11	±12			f = 100 Hz			f = 20 Hz		70	100	
					70	110			3.0				
	0°C ≤ T_A ≤ 70°C		N/A			N/A			N/A		40		
MC1556	T_A = 25°C	±12	±13			f = 100 Hz			f = 20 Hz		100	200	
					80	110			5.0				
	−55 ≤ T_A ≤ 125°C		N/A			N/A			N/A		40		
MC1458	T_A = 25°C	±12	±13			f = 100 Hz			f = 20 Hz		20	100	
					70	90		0.3	1.0				
	0°C ≤ T_A ≤ 70°C		N/A			N/A			N/A		15		
MC1558	T_A = 25°C	±12	±13			f = 100 Hz			f = 20 Hz		50	200	
					70	90		0.3	1.0				
	−55 ≤ T_A ≤ 125°C		N/A			N/A			N/A		25		
μA709	T_A = 25°C		N/A									N/A	
	±9 ≤ V_S ≤ ±15		V_S = ±15			N/A		150	400			$R_L \geqslant$ 25KΩ	
	−55°C ≤ T_A ≤ +125°C	±8.0	±10		70	90		40	100		25	45	70
μA709C												$R_L \geqslant$ 25KΩ	
	T_A = 25°C	±8.0	±10		65	90		50	250		15	45	
	0°C ≤ T_A ≤ 70°C		N/A			N/A		35			12		
μA740	T_A = 25°C		N/A			N/A			1,000,000			1,000	
	0°C ≤ T_A ≤ +70°C		±12			80			N/A			500	
μA741	T_A = 25°C		N/A			N/A		0.3	2.0		50	200	
	−55°C ≤ T_A ≤ +125°C	±12	±13		70	90					25		
μA741C	T_A = 25°C	±12	±13		70	90		0.3	2.0		20	200	
	0°C ≤ T_A ≤ +70°C		N/A			N/A			N/A		15		

ANALOG-OPERATIONAL AMPLIFIERS
ELECTRICAL CHARACTERISTICS TABLE (Cont'd) V_S = + 15V unless otherwise specified

PARAMETER DEVICE	TEST CONDITIONS	V_{OUT} OUTPUT VOLTAGE SWING (V) $R_L \geq 2K\Omega$			I_{CC} SUPPLY CURRENT (MA)			POWER CONSUMPTION			P_{SRR} SUPPLY VOLTAGE REJECTION RATION (μV/V) $R_S \leq 10K\Omega$		
	TEMPERATURE	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
LM324	T_A = 25°C V^+ = 5V		N/A			N/A			N/A		65	100	
			V_{OH} V^+ = 30V										
		26											
			$R_L \geq 10K\Omega$										
		27	28										
			V_{OL} V^+ = 5V										
			$R_L \leq 10K\Omega$			$R_L = \infty$ On All Op Amps							
	0°C ≤ T_A ≤ 70°C		5	20		0.8	2		N/A			N/A	
MC1456	T_A = 25°C	±11	±12			1.3	3.0		40	90		75	200
	0°C ≤ T_A ≤ 70°C		N/A			N/A						N/A	
MC1556	T_A = 25°C	±12	±13			1.0	1.5		30	45		50	100
	−55 ≤ T_A ≤ 125°C		N/A			N/A			N/A			N/A	
MC1458	T_A = 25°C		R_L = 10KΩ			2.3	5.6		70	170		30	150
		±12	±14										
	0°C ≤ T_A ≤ 70°C		R_L = 2KΩ										
		±10	±13			N/A			N/A			N/A	
MC1558	T_A = 25°C		R_L = 10KΩ			2.3	5.0		70	150		30	150
			R_L = 2KΩ										
	−55 ≤ T_A ≤ 125°C	±10	±13			N/A			N/A			N/A	
µA709	T_A = 25°C ±9 ≤ V_S ≤ ±15		N/A			N/A			80	165		N/A	
	−55°C ≤ T_A ≤ +125°C	±10	±13			N/A			N/A		25	150	
			R_L = 10KΩ										
		±12	±14										
µA709C	T_A = 25°C	±10	±13			N/A			80	200		25	200
			R_L = 10KΩ										
		±12	±14										
	0°C ≤ T_A ≤ 70°C		N/A			N/A			N/A			N/A	
µA740	T_A = 25°C		N/A			4.2	3.0		126	240		N/A	
		±10	±13										
	0°C ≤ T_A ≤ +70°C		$R_L \geq 10K\Omega$			N/A			N/A			70	
		±12	±14										
µA741	T_A = 25°C		N/A			1.4	2.8		50	85		N/A	
						T_A = +125°C			T_A = +125°C				
	−55°C ≤ T_A ≤ +125°C	±10	±13			1.5	2.5		45	75		10	150
			$R_L \geq 10K\Omega$			T_A = −55°C			T_A = −55°C				
		±12	±14			2.0	3.3		45	100			
µA741C	T_A = 25°C	±10	±13			1.4	2.8		50	85		10	150
			$R_L \geq 10K\Omega$										
		±12	±14										
	0°C ≤ T_A ≤ +70°C	±10	±13			N/A			N/A			N/A	

ANALOG-OPERATIONAL AMPLIFIERS

ELECTRICAL CHARACTERISTICS TABLE (Cont'd) V_S = + 15V unless otherwise specified

PARAMETER / DEVICE	TEST CONDITIONS	V_{OS} (mV) Offset Voltage $R_S \leq 10K\Omega$			V_{OS} DRIFT ($\mu V/°C$) $R_S = 0\Omega$			I_{OS} (mA) Offset Current			I_{OS} DRIFT pA/°C			I_{BIAS} (nA) Input Current		
	TEMPERATURE	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
μA747	T_A = 25°C		1.0	5.0		N/A			20	200		N/A			80	500
								T_A = +125°C						T_A = +125°C		
	−55°C $\leq T_A \leq$ +125°C		1.0	6.0		N/A			7.0	200		N/A			30	500
								T_A = −55°C						T_A = −55°C		
									85	500					300	1500
μA747C	T_A = 25°C			6		N/A			N/A			N/A			N/A	
	0°C $\leq T_A \leq$ 70°C		1.0	7.5		N/A			7.0	300		N/A			30	800
μA748	T_A = 25°C		1.0	5.0		N/A			20	200		N/A			80	500
								25° $\leq T_A \leq$ 125°C						25° $\leq T_A \leq$ 125°C		
				6.0		N/A			7.0	200					30	500
	−55° $\leq T_A \leq$ 125°C							−55° $\leq T_A \leq$ 25°C				N/A		−55° $\leq T_A \leq$ 25°C		
									8.5	500					300	1500
μA748C	T_A = 25°C		2.0	6.0		N/A			20	200		N/A			80	500
								25°C $\leq T_A \leq$ 70°C						25°C $\leq T_A \leq$ 70°C		
	0°C $\leq T_A \leq$ 70°C			7.5		N/A			9.0	300		N/A			40	800
								0°C $\leq T_A \leq$ 25°C						0°C $\leq T_A \leq$ 25°C		
									35	300					130	800

ANALOG-OPERATIONAL AMPLIFIERS
ELECTRICAL CHARACTERISTICS TABLE (Cont'd) V_S = + 15V unless otherwise specified

PARAMETER DEVICE	TEST CONDITIONS	V_{CM} (V) Common Mode Voltage Range			CMRR (dB) Common Mode Rejection Ratio $R_S \leqslant \pm 10K\Omega$			R_{IN} (MΩ) INPUT RESISTANCE			A_{VOL} (V/MV) LARGE SIGNAL VOLTAGE GAIN $R_L \geqslant 2K\Omega$ $V_{OUT} \pm 10V$ $V_S = \pm 15V$		
	TEMPERATURE	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
µA747	$T_A = 25°C$		N/A			N/A		0.3	2.0		50	200	
	$-55°C \leqslant T_A \leqslant +125°C$	±12	±13		70	90			N/A		25		
µA747C	$T_A = 25°C$		N/A			N/A		0.3	2.0		25	200	
	$0°C \leqslant T_A \leqslant 70°C$	±12	±13		70	90			N/A		15		
µA748	$T_A = 25°C$	±12	±13		70	90		0.3	2.0		50	200	
	$-55° \leqslant T_A \leqslant 125°C$	±12	±13		70	90			N/A		25		
µA748C	$T_A = 25°C$	±12	±13		70	90		0.3	2.0		50	200	
	$0°C \leqslant T_A \leqslant 70°C$	±12	±13		70	90			N/A		25		

ANALOG-OPERATIONAL AMPLIFIERS

ELECTRICAL CHARACTERISTICS TABLE (Cont'd) V_S = + 15V unless otherwise specified

PARAMETER / DEVICE	TEST CONDITIONS	V_{OUT} OUTPUT VOLTAGE SWING (V) $R_L \geq 2K\Omega$			I_{CC} SUPPLY CURRENT (MA)			POWER CONSUMPTION			P_{SRR} SUPPLY VOLTAGE REJECTION RATION (μV/V) $R_S \leq 10K\Omega$		
	TEMPERATURE	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
μA747	T_A = 25°C		N/A			1.7	2.8		50	85		N/A	
		±10	±13		T_A = +125°C			T_A = +125°C					
	−55°C ≤ T_A ≤ +125°C	$R_L \geq 10K\Omega$				1.5	2.5		45	75		30	150
		±12	±14		T_A = −55°C			T_A = −55°C					
						2.0	3.3		60	100			
μA747C	T_A = 25°C		N/A			1.7	2.8		50	85		N/A	
		±10	±13										
	0°C ≤ T_A ≤ 70°C	$R_L \geq 10K\Omega$				2.0	3.3		60	100		30	150
		±12	±14										
μA748	T_A = 25°C		N/A			1.7	2.8		50	85		30	150
		±10	±13		25° ≤ T_A ≤ 125°C			25° ≤ T_A ≤ 125°C					
		$R_L \geq 10K\Omega$				1.5	2.5		45	75		30	150
	−55° ≤ T_A ≤ 125°C	±12	±14		−55° ≤ T_A ≤ 25°C			−55° ≤ T_A ≤ 25°C					
						2.0	3.3		60	100			
μA748C	T_A = 25°C		N/A			1.7	2.8		50	85		30	150
					25° ≤ T_A ≤ 70°C			25° ≤ T_A ≤ 70°C					
		±10	±13			1.6	3.3		48	100		30	150
	0°C ≤ T_A ≤ 70°C	$R_L \geq 10K\Omega$			0° ≤ T_A ≤ 25°C			0° ≤ T_A ≤ 25°C					
		±12	±14			1.8	3.3		54	100			

ANALOG-COMPARATORS

ELECTRICAL CHARACTERISTICS TABLE T_A = 0°C to 70°C, V+ =5V, V− =−5V unless otherwise specified.

PARAMETER DEVICE	TEST CONDITIONS	V_{OS} (mV)[7] Offset Voltage V^+ = 4.75 V^- = −4.75			I_{OS} (μA) Offset Current V^+ = 5.25 V^- = −5.25			I_{BIAS} (μA)[8] Input Current V^+ = 5.25 V^- = −5.25			V_{CM} (V) Common Mode Voltage Range V^+ = 4.75 V^- = −4.75			A_{VOL} (V/mV) Large Signal Voltage Gain		
	TEMPERATURE	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
NE521	AT 25°C		6	7.5		1.0	5		7.5	20	±3				5	
	0°C ≤ T_A ≤ 70°C			10			12			40						
NE522	AT 25°C		6	7.5		1.0	5		7.5	20	±3				5	
	OVER TEMP			10			12			40						
NE526																
	0°C		2.0	5.0		0.6	5.0		30.0	35.0	4.2	4.7				
	+25°C		2.0	5.0		0.5	5.0		25.0	35.0	4.2	4.5			N/A	
	70°C		2.0	5.0		0.4	5.0		22.0	35.0	4.2	4.4				
	0°C										−3.2	−3.5				
	25°C										−3.2	−3.5				
	+70°C										−3.2	−3.5				
SE526																
	−55°C		2.0	5.0		0.6	0.5		30.0	35.0	4.2	4.7				
	+25°C		2.0	5.0		0.5	5.0		25.0	35.0	4.2	4.5			N/A	
	125°C		2.0	5.0		0.4	5.0		22.0	35.0	4.2	4.4				
	−55°C										−3.2	−3.5				
	25°C										−3.2	−3.5				
	+125°C										−3.2	−3.5				
NE527	V_1^+ = 10V, V_1^- = −10V															
	V_2^+ = 5V, V_{IN} = 0V															
	AT 25°C			6			0.75			2		N/A			5	
	0°C ≤ T_A 70°C			10			1			4						
SE527	V_1^+ = 10V, V_1^- = −10V															
	V_2^+ = 5V, V_{IN} = 0V															
	AT 25°C			4			0.5			2		N/A			5	
	−55°C ≤ T_A ≤ 125°C			6			1			4						
NE529	V_1^+ = 10V, V_1^- = −10V															
	V_2^+ = 5V, V_{IN} = 0V															
	AT 25°C			6		2	5		5	20		N/A			5	
	0°C ≤ 70°C			10			15			20						
SE529	V_1^+ = 10V, V_1^- = 10V															
	V_2^+ = 5V, V_{IN} = 0V															
	AT 25°C			4		2	3		5	12		N/A			5	
	−55 ≤ T_A ≤ 125°C			6			9			36						

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ELECTRICAL CHARACTERISTICS TABLE (Cont'd) T_A = 0°C to 70°C, V+ =5V, V− =−5V unless otherwise specified.

PARAMETER DEVICE	TEST CONDITIONS	V_{IDR} Differential Input Voltage (V)			I_{IL} (mA) LOW LEVEL V^+ = 5.25, V = −5.25 V_{IL} = 0.5V			I_{IH} (μA) HIGH LEVEL V^+ = 5.25, V^- = −5.25 V_{IN} = 0.5V			V_{OL} (V) LOW LEVEL V^+ = 5.25, V^- = −5.25 I_{LOAD} = 20 mA			V_{OH} HIGH LEVEL V^+ = 4.75, V^- = −4.75 I_{LOAD} = −1 mA V_{IS} = 2.0V		
	TEMPERATURE	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
NE521	AT 25°C 0°C ≤ T_A ≤ 70°C		N/A			 Common Strobes	 −2.0 −4.0		Strobe S Common Strobe S	 50 100			0.5	2.7	3.4	
NE522	AT 25°C OVER TEMP		N/A			 Common Strobes	 −2.0 −4.0		Strobe Common Strobe S	 50 100			0.5		N/A	
NE526	 0°C +25°C 70°C 0°C 25°C +70°C		 N/A		 −0.1 −0.1 −0.1	 −1.2 −1.4 −1.2	 −1.6 −1.6 −1.6		 5 10 15	 25 25 25		GATE 0.3 0.2 0.3 AMPLIFIER	 0.4 0.4 0.4 0.6 0.5 0.4	 2.8 2.8 2.8 3.5 3.5 3.5	GATE 3.5 3.2 3.0 AMPLIFIER	
SE526	 −55°C +25°C 125°C −55°C 25°C +125°C		 N/A		 −0.1 −0.1 −0.1	 −1.2 −1.4 −1.2	 −1.6 −1.6 −1.6		 5 10 15	 25 25 25		GATE 0.3 0.2 0.3 AMPLIFIER	 0.4 0.4 0.4 0.6 0.5 0.4	 2.8 2.8 2.8 3.5 3.5 3.5	GATE 3.5 3.2 3.0 AMPLIFIER	
NE527	V_1^+ = 10V, V_1^- = −10V V_2^+ = 5V, V_{IN} = 0V AT 25°C 0°C ≤ T_A 70°C		N/A				−2		V_{STROBE} = 2.7V	 100 200	V_2^+ = 4.75V I_{SINK} = 10mA		 0.5	2.7	3.3	
SE527	V_1^+ = 10V, V_1^- = −10V V_2^+ = 5V, V_{IN} = 0V AT 25°C −55°C ≤ T_A ≤ 125°C		N/A				−2		V_{STROBE} = 2.7V	 50 200	V_2^+ = 4.75V I_{SINK} = 10mA		 0.5	2.5	3.3	
NE529	V_1^+ = 10V, V_1^- = −10V V_2^+ = 5V, V_{IN} = 0V AT 25°C 0°C ≤ 70°C		N/A				−2		V_{STROBE} = 2.7V	 100 200	V_2^+ = 4.75V I_{SINK} = 10mA		 0.5	2.7	3.3	
SE529	V_1^+ = 10V, V_1^- = 10V V_2^+ = 5V, V_{IN} = 0V AT 25°C −55 ≤ T_A ≤ 125°C		N/A				−2		V_{STROBE} = 2.7V	 50 200	V_2^+ = 4.75V I_{SINK} = 10mA		 0.5	2.5	3.3	

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ELECTRICAL CHARACTERISTICS TABLE (Cont'd) T_A = 0°C to 70°C, V+ =5V, V− =−5V unless otherwise specified.

PARAMETER DEVICE	TEST CONDITIONS	V_{IL} LOW LEVEL			V_{IH} HIGH LEVEL			LEAKAGE CURRENT (nA)			OUTPUT CURRENT[4] SOURCE (mA)			SINK (mA)		
	TEMPERATURE	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
NE521	AT 25°C 0°C ≤ T_A ≤ 70°C		N/A			N/A			N/A			N/A			N/A	
NE522	AT 25°C OVER TEMP		N/A			N/A			N/A		V_S = ±4.75V	 N/A	 250µA		N/A	
NE526	0°C +25°C 70°C	1.0 0.9 0.8			2.0 2.0 2.0				N/A		1.0			16.0		
SE526	−55°C +25°C 125°C	1.0 0.9 0.8			2.0 2.0 2.0				N/A		1.0			16.0		
NE527	V_1^+ = 10V, V_1^- = −10V V_2^+ = 5V, V_{IN} = 0V AT 25°C 0°C ≤ T_A 70°C	V_2^+ = 4.75V		0.8	2.0				N/A			N/A			N/A	
SE527	V_1^+ = 10V, V_1^- = −10V V_2^+ = 5V, V_{IN} = 0V AT 25°C −55°C ≤ T_A ≤ 125°C	V_2^+ = 4.75V		0.8	2.0				N/A			N/A			N/A	
NE529	V_1^+ = 10V, V_1^- = −10V V_2^+ = 5V, V_{IN} = 0V AT 25°C 0°C ≤ 70°C			0.8	2.0				N/A			N/A			N/A	
SE529	V_1^+ = 10V, V_1^- = 10V V_2^+ = 5V, V_{IN} = 0V AT 25°C −55 ≤ T_A ≤ 125°C			0.8	2.0				N/A			N/A			N/A	

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ELECTRICAL CHARACTERISTICS TABLE (Cont'd) T_A = 0°C to 70°C, V+ =5V, V– =–5V unless otherwise specified.

PARAMETER DEVICE	TEST CONDITIONS	Pd POWER CONSUMPTION (mW)			V^- (V)			V^+ (V)			I_{CC^-} (mA) T_A = 25°C V^+ = 5.25V, V^- = –5.2V			I_{CC^+} (mA)			I_{OS} (mA) Short Circuit CURRENT T_A = 20°C V_{OUT} = 0V		
	TEMPERATURE	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
NE521	AT 25°C 0°C ≤ T_A ≤ 70°C		N/A		–4.75	–5.00	–5.25	4.75	5.00	5.25		–15	–28		27	50	V_S = ±5.25V –40		 –100
NE522	AT 25°C		N/A		–4.75	–5.00	–5.25	4.75	5.00	5.25		–15	–28		27	50		N/A	
NE526	 0°C +25°C 70°C		AMPLIFIER 90 100 110	 120 120 120		–5			5						V_2^+	 5.0 5.0 5.0	–10.0		–70.0
SE526	 –55°C +25°C 125°C		AMPLIFIER 90 100 110	 120 120 120		–5			5						V_2^+	 5.0 5.0 5.0	–10.0		–70.0
NE527	V_1^+ = 10V, V_1^- = –10V V_2^+ = 5V, V_{IN} = 0V AT 25°C 0°C ≤ T_A 70°C		N/A		–6	V_1^-	–10	 5 4.75	V_1^+ V_2^+ 5	 10 5.25	0°C ≤ T_A ≤ 70°C	I_1^-	10	0°C ≤ T_A ≤ 70°C	I_1^+ I_2^+	5.0 20	V_2^+ = 5.25V –40		 –100
SE527	V_1^+ = 10V, V_1^- = –10V V_2^+ = 5V, V_{IN} = 0V AT 25°C –55°C ≤ T_A ≤ 125°C AT 25°C –55 ≤ T_A ≤ 125		N/A		–6	V_1^-	–10	 5 4.5	V_1^+ V_2^+ 5	 10 5.5	 T_A = 125°C T_A = –55°C	I_1^-	7.5mA 7.0mA 8.5mA	 T_A = 125°C T_A = –55°C T_A = 125°C T_A = –55°C	I_1^+ I_2^+	3.75 3.25 4.0 16 15 18	V_2^+ = 5.25V –40		 –100
NE529	V_1^+ = 10V, V_1^- = –10V V_2^+ = 5V, V_{IN} = 0V AT 25°C 0°C ≤ 70°C		N/A		–6	V_1^-	–10	 5 4.75	V_1^+ V_2^+ 5	 10 5.25	0°C ≤ T_A ≤ 70°C	I_1^-	10	0°C ≤ T_A ≤ 70°C	I_1^+ I_2^+	5 20	–18	–35	–70
SE529	V_1^+ = 10V, V_1^- = 10V V_2^+ = 5V, V_{IN} = 0V AT 25°C –55 ≤ T_A ≤ 125°C		N/A		–6	V_1^-	–10	 5 4.5	V_1^+ V_2^+ 5	 10 5.5	 T_A = 125°C T_A = –55°C	I_1^-	7.5 7.0 8.5	 T_A = 125°C T_A = –55°C T_A = 125°C T_A = –55°C	I_1^+ I_2^+	3.75 3.25 4.0 16 15 18	–18	–35	–70

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ELECTRICAL CHARACTERISTICS TABLE (Cont'd) T_A = 0°C to 70°C, V+ =5V, V− =−5V unless otherwise specified.

PARAMETER DEVICE	TEST CONDITIONS	V_{OS} (mV)[7] Offset Voltage $V^+ = 4.75$ $V^- = -4.75$			I_{OS} (μA) Offset Current $V^+ = 5.25$ $V^- = -5.25$			I_{BIAS} (μA)[8] Input Current $V^+ = 5.25$ $V^- = -5.25$			V_{CM} (V) Common Mode Voltage Range $V^+ = 4.75$ $V^- = -4.75$			A_{VOL} (V/mV) Large Signal Voltage Gain		
	TEMPERATURE	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
LM111[14]	$V_S = \pm15V$		$R_S \leq 50K$													
	AT 25°C		0.7	3.0[13]		4.0	10[13]		60nA	100nA[13]					200	
	$-55 \leq T_A \leq 125°C$			4.0			20			150nA		±14				
LM211[14]	$V_S = \pm15V$		$R_S \leq 50K$													
	AT 25°C		0.7	3.0[13]		4.0nA	10[13]nA		60nA	100nA[13]					200	
	$-25 \leq T_A \leq 85°C$			4.0			20nA			150nA		±14				
LM119[14]	$V_S = \pm15V$		$R_S \leq 5K$									±13 $V^+ = 5V$, $V^- = 0$				
	AT 25°C		0.7	4.0[13]		30[13]	75		150nA[13]	500nA	1		3	10	40	
	$-55°C \leq T_A \leq 125°C$			7			100			1000nA						
LM219[14]	$V_S = \pm15V$		$R_S \leq 5K$									±13				
	AT 25°C		0.7[13]	4.0		30[13]	75		150nA[13]	500nA	1		3	10	40	
	$-25°C \leq T_A \leq 85°C$			7			100			1000nA						
LM139	$V^+ = 5V$	$V_O \cong 1.4V$, $V_{REF} = 1.4V$, $R_S = 0\Omega$						$I_{IN}+$ or $I_{IN}-$[15]							$R_L \geq 15K\Omega$	
	AT 25°C		±2.0	±5.0		±30nA	±25nA		25nA	100nA	0		$V^+ - 1.5$[17]		200	
	$-55 \leq T_A \leq 125°c$			9.0			±100nA			300nA	0		$V^+ - 2.0$			
LM239	$V^+ = 5V$	$V_O \cong 1.4V$, $V_{REF} = 1.4V$, $R_S = 0\Omega$						$I_{IN}+$ or $I_{IN}-$[16]							$R_L \geq 15K\Omega$	
	AT 25°C		±2.0	±5.0		±5.0nA	±50nA		25nA	250nA	0		$V^+ - 1.5$[17]		200	
	$-25°C \leq T_A \leq 85°C$			±9.0			±150			400nA	0		$V^+ - 2.0$			
LM311[14]	$V_S = \pm15V$		$R_S \leq 50K$													
	AT 25°C		2.0[13]	7.5		6.0nA[13]	50nA		100nA	250nA		N/A			200	
	$0° \leq T_A \leq 70°C$			10			70nA			300nA		±14			N/A	

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ELECTRICAL CHARACTERISTICS TABLE (Cont'd) T_A = 0°C to 70°C, V+ =5V, V- =-5V unless otherwise specified.

PARAMETER DEVICE	TEST CONDITIONS	V_{IDR} Differential Input Voltage (V)	I_{IL} (mA) LOW LEVEL V^+ = 5.25, V = -5.25 V_{IL} = 0.5V	I_{IH} (μA) HIGH LEVEL V^+ = 5.25, V^- = -5.25 V_{IN} = 0.5V	V_{OL} (V) LOW LEVEL V^+ = 5.25, V^- = -5.25 I_{LOAD} = 20 mA	V_{OH} HIGH LEVEL V^+ = 4.75, V^- = -4.75 I_{LOAD} = -1 mA V_{IS} = 2.0V
	TEMPERATURE	MIN TYP MAX	MIN TYP MAX	MIN TYP MAX	MIN TYP MAX	MIN TYP MAX
LM111[14]	V_S = ±15V AT 25°C $-55 \leq T_A \leq 125°C$	N/A	$V_{IN} \geq$ 5mV V_{OUT} = 35V -3.0	N/A	$V_{IN} \leq$ -5mV, I_{OUT} = 50mA 0.75 1.5 $V^+ \geq$ 4.5V, V^- = 0 $V_{IN} \leq$ -6mV, $I_{SINK} \leq$ 8mA 0.23 0.4	N/A
LM211[14]	V_S = ±15V AT 25°C $-25 \leq T_A \leq 85°C$	N/A	$V_{IN} \geq$ 5mV V_{OUT} = 35V -3.0	N/A	$V_{IN} \leq$ -5mV, I_{OUT} = 50mA 0.75 1.5 $V^+ \geq$ 4.5V, V^-=0 $V_{IN} \leq$ -6mV, $I_{SINK} \leq$ 8mA 0.23 0.4	N/A
LM119[14]	V_S = ±15V AT 25°C $-55°C \leq T_A \leq 125°C$	±5	N/A	N/A	$V_{IN} \leq$ -5mV, I_{OUT} = 25mA 0.75 1.5 $V^+ \geq$ 4.5V, V^-=0 $V_{IN} \leq$ -6mV, $I_{SINK} \leq$ 3.2mA $T_A \geq$ 0°C 0.23 0.4 $T_A \leq$ 0°C 0.6	N/A
LM219[14]	V_S = ±15V AT 25°C $-25°C \leq T_A \leq 85°C$	±5	N/A		$V_{IN} \leq$ -5mV, I_{OUT} = 25mA 0.75 1.5 $V^+ \geq$ 4.5V, V^-=0 $V_{IN} \leq$ -6mV, $I_{SINK} \leq$ 3.2mA $T_A \geq$ 0°C 0.23 0.4 $T_A \leq$ 0°C 0.6	N/A
LM139	V^+ = 5V AT 25°C $-55 \leq T_A \leq 125°c$	Keep All V_{IN}'s $\geq$ V- 36	N/A	N/A	$V_{IN-} \geq$ 1.0V V_{IN+} = 0, $I_{Sink} \leq$ 4mA 250 500 700	N/A
LM239	V^+ = 5V AT 25°C $-25°C \leq T_A \leq 85°C$	Keep All V_{IN}'s $\geq$ V- 36	N/A	N/A	$V_{IN-} \geq$ 1.0V, V_{IN+} = 0, $I_{SINK} \leq$ 4mA 250 500 700	N A
LM311[14]	V_S = ±15V AT 25°C $0° \leq T_A \leq 70°C$	N/A N/A	-3.0 N/A	N/A N/A	$V_{IN} \leq$ -10mV I_{OUT} = 50mA 0.75 1.5 $V_T \geq$ 4.5V, V^- = 0, $V_{IN} \leq$ -10mV, $I_{SINK} \leq$ 8mA 0.23 0.4	N A N A

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ELECTRICAL CHARACTERISTICS TABLE (Cont'd) T_A = 0°C to 70°C, V+ =5V, V− =−5V unless otherwise specified.

PARAMETER / DEVICE	TEST CONDITIONS	V_{IL} LOW LEVEL			V_{IH} HIGH LEVEL			LEAKAGE CURRENT (nA)			OUTPUT CURRENT[4] SOURCE (mA)			SINK (mA)		
	TEMPERATURE	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
LM111[14]								$V_{IN} \geq 5mV$, $V_{OUT} = 35V$,								
	$V_S = \pm15V$ AT 25°C		N/A			N/A			0.2	10		N/A			N/A	
	$-55 \leq T_A \leq 125°C$								10	50						
LM211[14]								$V_{IN} \geq 5mV$, $V_{OUT} = 35V$								
	$V_S = \pm15V$ AT 25°C		N/A			N/A			0.2	10		N/A			N/A	
	$-25 \leq T_A \leq 85°C$								10	50						
LM119[14]								$V_{IN} \geq 5mV$, $V_{OUT} = 35V$								
	$V_S = \pm15V$ AT 25°C		N/A			N/A			0.2µA	2µA		N/A			N/A	
	$-55°C \leq T_A \leq 125°C$								1µA	10µA						
LM219[14]								$V_{IN} \geq 5mV$, $V_{OUT} = 35V$								
	$V_S = \pm15V$ AT 25°C		N/A			N/A			0.2µA	2µA		N/A			N/A	
	$-25°C \leq T_A \leq 85°C$								1µA	10µA						
LM139	$V^+ = 5V$							$V_{IN+} \geq 1.0V$, $V_{IN-} = 0$, $V_{OUT} = 5V$						$V_{IN-} \geq 1.0V$, $V_{IN+} = 0$, $V_O \leq 1.5V$		
	AT 25°C $-55 \leq T_A \leq 125°C$		N/A			N/A			0.1µA			N/A		6	16	
								$V_{OUT} = 30V$		1µA						
LM239	$V^+ = 5V$							$V_{IN+} \geq 1.0V$, $V_{IN-} = 0$, $V_{OUT} = 5V$						$V_{IN-} \geq 1.0V$, $V_{IN+} = 0$, $V_O \leq 1.5V$		
	AT 25°C $-25°C \leq T_A \leq 85°C$		N/A			N/A			0.1µA			N/A		6	16	
								$V_{OUT} = 30V$		1µA						
LM311[14]	$V_S = \pm15V$ AT 25°C		N/A			N/A		$V_{IN} \geq 10mV$, $V_{OUT} = 35V$	0.2	50		N/A			N/A	
	$0° \leq T_A \leq 70°C$		N/A			N/A			N/A			N/A			N/A	

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ELECTRICAL CHARACTERISTICS TABLE (Cont'd) T_A = 0°C to 70°C, V+ =5V, V− =−5V unless otherwise specified.

PARAMETER DEVICE	TEST CONDITIONS	Pd POWER CONSUMPTION (mW)			V^- (V)			V^+ (V)			I_{CC^-} (mA) T_A = 25°C V^+ = 5.25V, V^- = −5.2V			I_{CC^+} (mA)			I_{OS} (mA) Short Circuit CURRENT T_A = 20°C V_{OUT} = 0V		
	TEMPERATURE	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
LM111[14]	V_S = ±15V AT 25°C −55 ≤ T_A ≤ 125°C		N/A			−15			+15			4.1	5.0		5.1	6.0		N/A	
LM211[14]	V_S = ±15V AT 25°C −25 ≤ T_A ≤ 85°C		N/A			−15			+15			4.1	5.0		5.1	6.0		N/A	
LM119[14]	V_S = ±15V AT 25°C −55°C ≤ T_A ≤ 125°C		N/A			−15			+15			3	4.5		8 T_A = 25°C V^+ = 5V, V^- = 0 4.3	11.5		N/A	
LM219[14]	V_S = ±15V AT 25°C −25 ≤ T_A ≤ 85°C		N/A			−15			+15			3	4.5		8 T_A = 25°C V^+ = 5V, V^- = 0 4.3	11.5		N/A	
LM139	V^+ = 5V AT 25°C −55 ≤ T_A ≤ 125°c		N/A			N/A			N/A		R_L = ∞ On All Comparators	0.8	2.0		N/A			N/A	
LM239	V^+ = 5V AT 25°C −25°C ≤ T_A ≤ 85°C		N/A			N/A			N/A		R_L = ∞ On All Comparators	0.8	2.0		N/A			N/A	
LM311[14]	V_S = ±15V AT 25°C		N/A			−15			+15			4.1	5.0		5.1	7.5		N/A	
	0° ≤ T_A ≤ 70°C		N/A			N/A			N/A			N/A			N/A			N/A	

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ELECTRICAL CHARACTERISTICS TABLE (Cont'd) T_A = 0°C to 70°C, V+ =5V, V- =-5V unless otherwise specified.

PARAMETER DEVICE	TEST CONDITIONS	V_{OS} (mV)[7] Offset Voltage V+ = 4.75 V- = -4.75			I_{OS} (μA) Offset Current V+ = 5.25 V- = -5.25			I_{BIAS} (μA)[8] Input Current V+ = 5.25 V- = -5.25			V_{CM} (V) Common Mode Voltage Range V+ = 4.75 V- = -4.75			A_{VOL} (V/mV) Large Signal Voltage Gain		
	TEMPERATURE	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
LM319[14]	V_S = ±15V AT 25°C	R_S ≤ 5K	2.0[13]	8.0		80nA[13]	200nA		0.25	1.0		±13		8	40	
	0° ≤ T_A ≤ 70°C			10			300nA			1.2		N/A			N/A	
LM339		V_O ≅ 1.4V, V_{REF} = 1.4V, R_S = 0Ω						I_{IN+} or I_{IN-}[16]						R_L ≥ 15KΩ		
	AT 25°C		±2.0	±5.0		±5.0nA	±50nA		25nA	250nA	0		V+-1.5[17]		200	
	0° ≤ T_A ≤ 70°C			±9.0			±150nA			400nA	0		V+-2.0			
LM139A	V+ = 15V	V_O ≅ 1.4V, V_{REF} = 1.4V, R_S = 0Ω						I_{IN+} or I_{IN-}[16]						R_L ≥ 15KΩ		
	AT 25°C		±1	±2		±3nA	±25nA		25nA	100nA	0		V+-1.5[17]		200	
	-55° ≤ T_A ≤ 125°C			±4			±100nA			300nA	0		V+ -2.0			
LM229A	V+ = 15V	V_O ≅ 1.4V, V_{REF} = 1.4V, R_S = 0Ω						I_{IN+} or I_{IN-}[16]						R_L ≥ 15KΩ		
	AT 25°C		±1	±2		±5nA	±50nA		25nA	250nA	0		V+-1.5[17]		200	
	0° ≤ T_A ≤ 70°C			±4			±150nA			400nA	0		V+ -2.0			
LM339A	V+ = 15V	V_O ≅ 1.4V, V_{REF} = 1.4V, R_S = 0Ω						I_{IN+} or I_{IN-}[16]						R_L = 15KΩ		
	AT 25°C		±1	±2		±5nA	±50nA		25nA	250nA	0		V+-1.5[17]		200	
	-25°C ≤ 85°C			±4			±150nA			400nA	0		V+ -2.0			
MC3302	V_{CC} = 15V	V_{REF} = 1.2V									V_{CC} = 20V			R_L = 15KΩ		
	AT 25°C		3.0	20		3.0nA			0.3	0.5	0		26	2,000	3,000 V/V	
	-40°C ≤ T_A ≤ 85°C			40						1.0						
μA710	V+ = 12V, V- = -6.0V	NOTE 21 R_S ≤ 200Ω			NOTE 21						V- = -7.0V					
	AT 25°C		0.6	2.0		0.75	3.0		13	20		N/A		1250	1700	
	-55°C ≤ T_A ≤ +125°C			3.0		T_A = +125°C 0.25	3.0		T_A = -55°C 27	45	±5.0			1000		
						T_A = -55°C 1.8	7.0									
μA 710C	V+ = 12V, V- = -6.0V	NOTE 21 R_S ≤ 200Ω			NOTE 21						V- = -7.0V					
	AT 25°C		1.6	5.0					16	25		N/A		1000	1500	
	0°C ≤ T_A ≤ +75°C			6.5			7.5		T_A = 0°C 25	40	±5.0			800		
μA711[20]	V+ = 12V, V- = -6.0V	R_S ≤ 200Ω V_{OUT} = 1.4V			V_{OUT} = 1.4V						V- = -7.0V					
	AT 25°C		1.0	5.0[21]		0.5	10.0[21]		25	75	±5.0			750	1500	
		V_{CM} = 0	1.0	3.5												
	-55°C ≤ T_A ≤ +125°C			6.0[21]			20[21]			150		N A		500		
		V_{CM} = 0	4.5	6.0												

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ELECTRICAL CHARACTERISTICS TABLE (Cont'd) T_A = 0°C to 70°C, V+ =5V, V− =−5V unless otherwise specified.

PARAMETER DEVICE	TEST CONDITIONS	V_{IDR} Differential Input Voltage (V)	I_{IL} (mA) LOW LEVEL V^+ = 5.25, V = −5.25 V_{IL} = 0.5V	I_{IH} (μA) HIGH LEVEL V^+ = 5.25, V^- = −5.25 V_{IN} = 0.5V	V_{OL} (V) LOW LEVEL V^+ = 5.25, V^- = −5.25 I_{LOAD} = 20 mA	V_{OH} HIGH LEVEL V^+ = 4.75, V^- = −4.75 I_{LOAD} = −1 mA V_{IS} = 2.0V
	TEMPERATURE	MIN TYP MAX	MIN TYP MAX	MIN TYP MAX	MIN TYP MAX	MIN TYP MAX
LM319[14]	V_S = ±15V AT 25°C 0° ≤ T_A ≤ 70°C	±5 N/A	N/A N/A	N/A N/A	V_{IN} ≤ −10mV I_{OUT} = 25mA 0.75 1.5 V^+ ≥ 4.5V, V^- = 0V, V_{IN} ≤ −10V, I_{SINK} ≤ 3.2mA 0.3 0.4	N/A N/A
LM339	AT 25°C 0° ≤ T_A ≤ 70°C	Keep All V_{IN}'s ≥ V^- 36	N/A	N/A	V_{IN^-} ≥ 1.0V, V_{IN^+} = 0 I_{SINK} ≤ 4mA 250 500 700	N/A N/A
LM139A	V^+ = 15V AT 25°C −55° ≤ T_A ≤ 125°C	Keep All V_{IN}'s ≥ V^- V^+	N/A	N/A	V_{IN^-} = 1V, V_{IN^+} = 0 I_{SINK} = 4mA 250 500 700	N/A
LM229A	V^+ = 15V AT 25°C −25°C ≤ T_A ≤ 85°C	Keep All V_{IN}'s ≥ V^- V^+	N/A	N/A	V_{IN^-} = 1V, V_{IN^+} = 0 I_{SINK} = 4mA 250 500 700	N/A
LM339A	V^+ = 15V AT 25°C 0° ≤ T_A ≤ 70°C	Keep All V_{IN}'s ≥ V^- V^+	N/A	N/A	V_{IN^-} = 1V, V_{IN^+} = 0 I_{SINK} = 4mA 250 500 700	N/A
MC3302	V_{CC} = 15V AT 25°C −40°C ≤ T_A ≤ 85°C	±V_{CC}	N/A	N/A	V_{CC} = 5 −28V I_S = 2.0mA 150mV 400mV	N/A
μA710	V^+ = 12V, V^- = −6.0V AT 25°C −55°C ≤ T_A ≤ +125°C	N/A ±5.0	N/A N/A	N/A N/A	V_{IN} ≥ 5mV N/A −1.0 −0.5 0	V_{IN} ≥ 5mV, 0 ≤ I_{out} ≤ 5.0mA N/A 2.5 3.2 4.0
μA 710C	V^+ = 12V, V^- = −6.0V AT 25°C 0°C ≤ T_A ≤ +75°C	N/A ±5.0	N/A N/A	N/A N/A	V_{IN} ≥ 5mV N/A −1.0 −0.5 0	V_{IN} ≥ 5mV, 0 ≤ I_{out} ≤ 5.0mA N/A 2.5 3.2 4.0
μA711[20]	V^+ = 12V, V^- = −6.0V AT 25°C −55°C ≤ T_A ≤ +125°C	N/A N/A	N/A N/A	N/A N/A	V_{IN} ≥ 10mV −1.0 −0.5 0 STROBES V_{Strobe} < 0.3V −1.0 0 N/A	V_{IN} ≥ 10mV 4.5 5.0 LOADED I_O = 5mA 2.5 3.5 N/A

ANALOG-COMPARATORS

ELECTRICAL CHARACTERISTICS TABLE (Cont'd) T_A = 0°C to 70°C, V+ =5V, V− =−5V unless otherwise specified.

PARAMETER / DEVICE	TEST CONDITIONS / TEMPERATURE	V_{IL} LOW LEVEL (MIN TYP MAX)	V_{IH} HIGH LEVEL (MIN TYP MAX)	LEAKAGE CURRENT (nA) (MIN TYP MAX)	OUTPUT CURRENT[4] SOURCE (mA) (MIN TYP MAX)	OUTPUT CURRENT[4] SINK (mA) (MIN TYP MAX)
LM319[14]	V_S = ±15V AT 25°C	N/A	N/A	$V_{IN} \geq$ 10mV, V_{OUT} = 35mV: 0.2 (TYP) 10 (MAX)	N/A	N/A
	0° ≤ T_A ≤ 70°C	N/A	N/A	N/A	N/A	N/A
LM339	AT 25°C	N/A	N/A	$V_{IN+} \geq$ 1.0V, V_{IN} = 0, V_{OUT} = 5V: 0.1µA	N/A	$V_{IN-} \geq$ 1.0V, V_{IN+} = 0, $V_O \leq$ 1.5V: 6 (MIN) 16 (TYP)
	0° ≤ T_A ≤ 70°C			V_{OUT} = 30V: 1µA		
LM139A	V^+ = 15V AT 25°C	N/A	N/A	V_{IN+} = 1V, V_{IN-} = 0, V_{OUT} = 5V: 0.1µA	N/A	$V_{IN-} \geq$ 1V, V_{IN+} = 0, $V_O \leq$ 1.5V: 6 (MIN) 16 (TYP)
	−55° ≤ T_A ≤ 125°C			V_{OUT} = 30V: 1µA		
LM229A	V^+ = 15V AT 25°C	N/A	N/A	V_{IN+} = 1V, V_{IN-} = 0, V_{OUT} = 5V: 0.1µA	N/A	$V_{IN-} \geq$ 1V, V_{IN+} = 0, $V_O \leq$ 1.5V: 6 (MIN) 16 (TYP)
	0° ≤ T_A ≤ 70°C			V_{OUT} = 30V: 1µA		
LM339A	V^+ = 15V AT 25°C	N/A	N/A	V_{IN+} = 1V, V_{IN-} = 0, V_{OUT} = 5V: 0.1µA	N/A	$V_{IN-} \geq$ 1V, V_{IN+} = 0, $V_O \leq$ 1.5V: 6 (MIN) 16 (TYP)
	−25 ≤ T_A ≤ 85°C			V_{OUT} = 30V: 1µA		
MC3302	V_{CC} = 15V AT 25°C	N/A	N/A	V_{OUT} = High: 1µA	N/A	V_{CC} = 5V, V_{OL} = 400mV: 6.0; V_{OL} = 800mV: 2.0
	−40°C ≤ T_A ≤ 85°C					
µA710	V^+ = 12V, V^- = −6.0V AT 25°C	N/A	N/A	N/A	N/A	$V_{IN} \geq$ 5mV, V_{out} = 0: 2.0 (MIN) 2.5 (TYP)
	−55°C ≤ T_A ≤ +125°C	N/A	N/A	N/A	N/A	T_A = +125°C: 0.5 (MIN) 1.7 (TYP); T_A = −55°C: 1.0 (MIN) 2.3 (TYP)
µA 710C	V^+ = 12V, V^- = −6.0V AT 25°C	N/A	N/A	N/A	N/A	$V_{IN} \geq$ 5mV, V_{out} = 0: 1.6
	0°C ≤ T_A ≤ +75°C	N/A	N/A	N/A	N/A	0.5
µA711[20]	V^+ = 12V, V^- = −6.0V AT 25°C	N/A	N/A	N/A	N/A	$V_{IN} \geq$ 10mV, $V_{out} \geq$ 0: 0.5 (MIN) 0.8 (TYP)
	−55°C ≤ T_A ≤ +125°C	N/A	N/A	N/A	N/A	N/A

ANALOG-COMPARATORS

ELECTRICAL CHARACTERISTICS TABLE (Cont'd) T_A = 0°C to 70°C, V+ =5V, V– =-5V unless otherwise specified.

PARAMETER DEVICE	TEST CONDITIONS	Pd POWER CONSUMPTION (mW)			V^- (V)			V^+ (V)			I_{CC^-} (mA) T_A = 25°C V^+ = 5.25V, V^- = -5.2V			I_{CC^+} (mA)			I_{OS} (mA) Short Circuit CURRENT T_A = 20°C V_{OUT} = 0V		
	TEMPERATURE	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
LM319[14]	V_S = ±15V AT 25°C		N/A			-15			+15			3.0	5.0		8	12.5		N/A	
														V^+ = 5V, V^- = 0					
	0° ≤ T_A ≤ 70°C		N/A			N/A			N/A			N/A			4.3			N/A	
LM339											R_L = ∞ On All Comparators								
	AT 25°C		N/A			N/A			N/A			0.8	2.0		N/A			N/A	
	0° ≤ T_A ≤ 70°C																		
LM139A	V^+ = 15V										R_L = ∞ On All Comparators								
	AT 25°C -55° ≤ T_A ≤ 125°C		N/A			N/A			N/A			0.8	2		N/A			N/A	
LM229A	V^+ = 15V										R_L = ∞ On All Comparators								
	AT 25°C -25 ≤ T_A ≤ 85°C					N/A			N/A			0.8	2		N/A			N/A	
LM339A	V^+ = 15V										R_L = ∞ On All Comparators								
	AT 25°C 0° ≤ T_A ≤ 70°C		N/A			N/A			N/A			0.8	2		N/A			N/A	
MC3302	V_{CC} = 15V													5V ≤ V_{CC} ≤ 28V					
	AT 25°C -40°C ≤ T_A ≤ 85°C		N/A			N/A			N/A			N/A			0.7	1.5		N/A	
μA710	V^+ = 12V, V^- = -6.0V																		
	AT 25°C		N/A			N/A			N/A			N/A			N/A			N/A	
	-55°C ≤ T_A ≤ +125°C		90	150		N/A			N/A			4.6	7.0		5.2	9.0		N/A	
μA 710C	V^+ = 12V, V^- = -6.0V																		
	AT 25°C		N/A 90	150		N/A			N/A			N/A			N/A			N/A	
	0°C ≤ T_A ≤ +75°C					N/A			N/A			4.6	7.0		5.2	9.0		N/A	
μA711[20]	V^+ = 12V, V^- = -6.0V																		
	AT 25°C		130	200		3.9 STROBE V_{Strobe} = 100mV 1.2	2.5		V_{OUT} ≤ 0 8.6			3.9			8.6			N/A	
	-55°C ≤ T_A ≤ +125°C		N/A			N/A			N/A			N/A			N/A			N/A	

ANALOG-COMPARATORS

ELECTRICAL CHARACTERISTICS TABLE (Cont'd) T_A = 0°C to 70°C, V+ =5V, V- =-5V unless otherwise specified.

PARAMETER DEVICE	TEST CONDITIONS	V_{OS} (mV)[7] Offset Voltage $V^+ = 4.75$ $V^- = -4.75$ MIN	TYP	MAX	I_{OS} (μA) Offset Current $V^+ = 5.25$ $V^- = -5.25$ MIN	TYP	MAX	I_{BIAS} (μA)[8] Input Current $V^+ = 5.25$ $V^- = -5.25$ MIN	TYP	MAX	V_{CM} (V) Common Mode Voltage Range $V^+ = 4.75$ $V^- = -4.75$ MIN	TYP	MAX	A_{VOL} (V/mV) Large Signal Voltage Gain MIN	TYP	MAX
	TEMPERATURE	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
μA711C[20]	$V^+ = 12V$, $V^- = -6.0V$															
	AT 25°C	$R_S \leq 200\Omega$ $V_{OUT} = 1.4V$	1.0	7.5[21] $V_{CM} = 0$ 5.0	$V_{OUT} = 1.4V$	0.5	15.0		25	100	$V^- = -7.0V$ ±5.0			700	1500	
	$0°C \leq T_A \leq +75°C$			10.0[21] $V_{CM} = 0$ 6.0			25[21]			150		N/A		500		

PARAMETER DEVICE	TEST CONDITIONS	V_{IDR} Differential Input Voltage (V) MIN	TYP	MAX	I_{IL} (mA) LOW LEVEL $V^+ = 5.25$, $V = -5.25$ $V_{IL} = 0.5V$ MIN	TYP	MAX	I_{IH} (μA) HIGH LEVEL $V^+ = 5.25$, $V^- = -5.25$ $V_{IN} = 0.5V$ MIN	TYP	MAX	V_{OL} (V) LOW LEVEL $V^+ = 5.25$, $V^- = -5.25$ $I_{LOAD} = 20$ mA MIN	TYP	MAX	V_{OH} HIGH LEVEL $V^+ = 4.75$, $V^- = -4.75$ $I_{LOAD} = -1$ mA $V_{IS} = 2.0V$ MIN	TYP	MAX
	TEMPERATURE	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
μA711C[20]	$V^+ = 12V$, $V^- = -6.0V$										$V_{IN} \geq 10mV$			$V_{IN} \geq 10mV$		
	AT 25°C	±5.0				N/A		N/A			-1.0 STROBES $V_{Strobe} < 0.3V$ -1.0	-0.5	0 0	 LOADED $I_O = 5mA$ 2.5	4.5 3.5	5.0
	$0°C \leq T_A \leq +75°C$		N/A			N/A			N/A			N/A			N/A	

PARAMETER DEVICE	TEST CONDITION	V_{IL} LOW LEVEL MIN	TYP	MAX	V_{IH} HIGH LEVEL MIN	TYP	MAX	LEAKAGE CURRENT (nA) MIN	TYP	MAX	OUTPUT CURRENT[4] SOURCE (mA) MIN	TYP	MAX	SINK (mA) MIN	TYP	MAX
	TEMPERATURE	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
μA711C[20]	$V^+ = 12V$, $V^- = -$													$V_{IN} \geq 10mV$, $V_{out} \geq 0$		
	AT 25°C		N/A			N/A			N/A			N/A		0.5	0.8	
	$0°C \leq T_A \leq +75°C$		N/A			N/A			N/A			N/A			N/A	

PARAMETER DEVICE	TEST CONDITIONS	P_d POWER CONSUMPTION (mW) MIN	TYP	MAX	V^- (V) MIN	TYP	MAX	V^+ (V) MIN	TYP	MAX	I_{CC^-} (mA) $T_A = 25°C$ $V^+ = 5.25V$, $V^- = -5.2V$ MIN	TYP	MAX	I_{CC^+} (mA) MIN	TYP	MAX
	TEMPERATURE	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
μA711C[20]	$V^+ = 12V$, $V^- = -6.0V$															
	AT 25°C		130	200		3.9			$V_{OUT} \leq 0$ 8.6			3.9			8.6	
	$0°C \leq T_A \leq +75°C$		N/A			N/A			N/A			N/A			N/A	

D-MOS ABSOLUTE MAXIMUM RATINGS T_A = 25°C (unless otherwise noted) (cont'd)

Parameter	V_{DS} (V) Drain-to-Source	V_{SD} (V) Source-to-Drain	V_{DB} (V) Drain-to-Substrate	V_{SB} (V) Source-to-Substrate	V_{GS} (V) Gate-to-Source	V_{GB} (V) Gate-to-Substrate
SD200	+25	N/A	N/A	N/A	N/A	±40
SD201	+25	N/A	N/A	N/A	N/A	−0.3, +10
SD202	+20	N/A	N/A	N/A	N/A	±40
SD203	+20	N/A	N/A	N/A	N/A	−0.3, +10
SD210	+30	+10	+15	+15	±40	±40
SD211	+30	+10	+15	+15	−15, +25	−0.3, +25
SD212	+10	+10	+15	+15	±40	±40
SD213	+10	+10	+15	+15	−15, +25	−0.3, +25
SD214	+20	+20	+25	+25	±40	±40
SD215	+20	+20	+25	+25	−25, +30	−0.3, +30
SD300	+25	N/A	N/A	N/A	N/A	Gate 1 −0.3, +10 Gate 2 −0.3, +15
SD301	+20	N/A	N/A	N/A	N/A	Gate 1 −0.3, +10 Gate 2 −0.3, +15
SD303	+20	N/A	N/A	N/A	N/A	Gate 1 −0.3, +10 Gate 2 −0.3, +15
SD304	+25	N/A	N/A	N/A	N/A	Gate 1 −0.3, +10 Gate 2 −0.3, +15
SD305	+20	N/A	N/A	N/A	N/A	Gate 1 −0.3, +20 Gate 2 −0.3, +20
SD306	+20	N/A	N/A	N/A	N/A	Gate 1 −0.3, +20 Gate 2 −0.3, +20
SD5000	+20	+20	+25	+25	−25, +25	−0.3, +30
SD5001	+10	+10	+15	+15	−15, +20	−0.3, +25
SD5100	+30	+.5	+30	+.5	+20	−0.3, +20
SD5101	+15	+.5	+15	+.5	+20	−0.3, +20
SD5200	+30	+.5	+30	+.5	+20	−0.3, +20
SD6000	+20	N/A	N/A	N/A	N/A	Gate 1 −0.3, +20 Gate 2 −0.3, +20

1. Derate linearly at 5mW/°C
2. Derate linearly at 2mW/°C
3. Derate linearly at 2.4mW/°C

D-MOS ABSOLUTE MAXIMUM RATINGS T_A = 25°C (unless otherwise noted) (cont'd)

Parameter	V_{GD} (V) Gate-to-Drain	I_D (mA) Drain Current	T_A Ambient Temperature Range		P_T Power Dissipation	
			Storage (°C)	Operating (°C)	Total of Devices[1] @ 25°C Free Air Temperature	Individual Transistor[2] @ 25°C Free Air Temperature
SD200	N/A	50	−65 to +175	−65 to +125	N/A	300
SD201	N/A	50	−65 to +175	−65 to +125	N/A	300
SD202	N/A	50	−65 to +175	−65 to +125	N/A	300
SD203	N/A	50	−65 to +175	−65 to +125	N/A	300
SD210	±40	50	−65 to +175	−65 to +125	N/A	300
SD211	−15, +25	50	−65 to +175	−65 to +125	N/A	300
SD212	±40	50	−65 to +175	−65 to +125	N/A	300
SD213	−15, +25	50	−65 to +175	−65 to +125	N/A	300
SD214	±40	50	−65 to +175	−65 to +125	N/A	300
SD215	−25, +30	50	−65 to +175	−65 to +125	N/A	300
SD300	N/A	50	−65 to +175	−65 to +125	N/A	300
SD301	N/A	50	−65 to +175	−65 to +125	N/A	300
SD303	N/A	50	−65 to +175	−65 to +125	N/A	300
SD304	N/A	50	−65 to +175	−65 to +125	N/A	300
SD305	N/A	150	−65 to +175	−65 to +125	N/A	300
SD306	N/A	50	−65 to +175	−65 to +125	N/A	300
SD5000	−25, +25	50	−55 to +150	0 to +85	625	300[3]
SD5001	−15, +20	50	−55 to +150	0 to +85	625	300[3]
SD5100	+20	50	−55 to +150	0 to +85	625	300[3]
SD5101	+20	50	−55 to +150	0 to +85	625	300[3]
SD5200	+20	50	−55 to +150	0 to +85	625	300[3]
SD6000	N/A	50	−65 to +150	0 to +85	625	300[3]

1. Derate linearly at 5mW/°C
2. Derate linearly at 2mW/°C
3. Derate linearly at 2.4mW/°C

DMOS

ELECTRICAL CHARACTERISTICS T_A = +25°C unless otherwise specified

PARAMETER	BV_{DS} (V) Drain-To-Source V_{GS} = 0V I_D < 1μA			BV_{SD} (V) Source-To-Drain V_{GD}=V_{BD}=−5V I_D = 10nA			BV_{DB} (V) Drain-To-Substrate V_{GB} = 0V Source = Open I_D = 10nA			BV_{SB} (V) Source-To-Substrate V_{GB} = 0V Drain = Open I_S = 10μA			I_{DSS} (μA) Zero Bias Drain Current V_{DS} = +15V V_{GS} = 0V			I_{SD} (Off) (nA) Drain-To-Source V_{GS}=V_{BS}= −5V V_{DS} = +10V			I_{SD} (Off) (nA) Source-To-Drain V_{GD}=V_{BD}= −5V V_{DS} = +10V			I_{GBS} (μA) Gate V_{GS} = ±10V V_{DS} = 0V		
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max
SD200	25	30			N/A			N/A			N/A			0.001	1.0		N/A			N/A				0.0001
SD201	25	30			N/A			N/A			N/A			0.001	1.0		N/A			N/A		V_{GS} = +10V	0.001	1.0
SD202	20	25			N/A			N/A			N/A			0.001	1.0		N/A			N/A				0.0001
SD203	20 V_{GS} = V_{BS} = −5V I_S = 10nA	25			N/A			N/A			N/A			0.001	1.0		N/A			N/A		V_{GS} = +10V V_{DB}=V_{SB} = 0V V_{GB} = ±40V	0.001	1.0
SD210	10 V_{GS} = V_{BS} = 0V I_S = 10μA 30	25 35		10			15			15				N/A			1	10		1	10			0.0001
SD211	10 V_{GS} = V_{BS} = 0V I_S = 10μA 30	25 35		10			15			15				N/A			1	10		1	10	V_{GB} = +25V	10	
SD212	10	25		10			15			15				N/A			1	10		1	10			0.0001
SD213	10	25		10			15			15				N/A			1	10		1	10	V_{GB} = +25V	10	
SD214	20	25		20			25			25				N/A		V_{SD} = +20V	1	10	V_{DSD} = +20V	1	10			0.0001
SD215	20	25		20			25			25				N/A		V_{DS} = +20V	1	10	V_{SD} = +20V	1	10	V_{GB} = +25V	10	

DMOS

ELECTRICAL CHARACTERISTICS (Cont'd) T_A = +25°C unless otherwise specified

PARAMETER	I_{GB} (µA) Gate-To-Substrate Drain & Source Open V_{GB} = +30V			V_T (V) Threshold Voltage $V_{DS} = V_{GS} = V_T$ I_D = 1µA			gfs (mmhos) Forward Transconductance V_{DS} = +15V, I_D = 20 mA f = 1 KHz $V_{GS} \cong +4V$			$C_{(GS+GD+GB)}$ (pF) Gate Node V_{DS} = +10V, $V_{GS}=V_{BS}=-15V$ f = 1 MHz			$C_{(GD+DB)}$ (pF) Drain Node V_{DS} = +10V, $V_{GS}=V_{BS}=-15V$ f = 1 MHz			$C_{(GS+SB)}$ (pF) Source Node V_{DS} = +10V, $V_{GS}=V_{BS}=-15V$ f = 1 MHz			C_T (dB) Cross Talk f = 3 KHz			C_{ISS} (pF) Input I_D = 20mA V_{DS} = +15V, f = 1 MHz		
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max
SD200		N/A		0.1	1.0	2.0	13.0	15.0															2.4	3.0
SD201		N/A		0.1	1.0	2.0	13.0	15.0															2.4	3.0
SD202		N/A		0.1	1.0	2.0	$V_{GS} \cong +2.5V$ 17.0	20.0															3.0	3.6
SD203		N/A		0.1	1.0	2.0	$V_{GS} \cong +2.5V$ 17.0	20.0															3.0	3.6
				I_S = 1µA V_{SB} = 0V			V_D = 10V V_{SB} = 0V																	
SD210		N/A		0.5	1.0	2.0	10	15			2.4	3.5		1.3	1.5		3.5	4.0		N/A			N/A	
SD211		N/A		0.5	1.0	2.0	10	15			2.4	3.5		1.3	1.5		3.5	4.0		N/A			N/A	
SD212		N/A		0.1	1.0	2.0	10	15			2.4	3.5		1.3	1.5		3.5	4.0		N/A			N/A	
SD213		N/A		0.1	1.0	2.0	10	15			2.4	3.5		1.3	1.5		3.5	4.0		N/A			N/A	
SD214		N/A		0.1	1.0	2.0	10	15			2.4	3.5		1.3	1.5		3.5	4.0		N/A			N/A	
SD215		N/A		0.1	1.0	2.0	10	15			2.4	3.5		1.3	1.5		3.5	4.0		N/A			N/A	

DMOS

ELECTRICAL CHARACTERISTICS (Cont'd) T_A = +25°C unless otherwise specified

PARAMETER	C_{OSS} (pF) Output I_D = 0A V_{DS} = +15V, f = 1 MHz			C_{RSS} (pF) Reverse Transfer I_D = 0A V_{DS} = +15V, f = 1 MHz			r_{DS} (On) (Ω) Drain-To-Source V_{GS} = +5V I_D = 0.1mA			r_{DSM} (On) (Ω) Match I_D = 0.1mA V_{SB} = 0 V_{GS} = +5V			Gps[1] (dB) Power Gain V_{DS}=+15V, I_D=20 mA f = 1 GHz V_{GS} ≅ +4V			NF[1] (dB) Noise Figure V_{DS}=+15V, I_D=20mA V_{GS} ≅ +4V f = 1 GHz		
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max
SD200		1.0	1.2		0.20	0.30		50	70		N/A		8	10			4.5	6.0
SD201		1.0	1.2		0.20	0.30		50	70		N/A		8	10			5.0	6.5
SD202		1.0	1.2		0.20	0.30		35	50		N/A		V_{GS} ≅ +2.5V 8	 10		V_{GS} ≅ +2.5V	 3.5	 4.5
SD203		1.0	1.2		0.20	0.30		35	50		N/A		V_{GS} ≅ +2.5V 8	 10		V_{GS} ≅ +2.5V	 4.0	 5.0
				V_{DS} = +10V V_{GS}=V_{BS}=−15V, f = 1 MHz			V_{SB} = 0V											
SD210		N/A			0.3	0.5		50 V_{GS} = +10V 30 V_{GS} = +15V 23 V_{GS} = +20V 19 V_{GS} = +25V 17	70 45		N/A			N/A			N/A	
SD211		N/A			0.3	0.5		50 V_{GS} = +10V 30 V_{GS} = +15V 23 V_{GS} = +20V 19	70 45		N/A			N/A			N/A	
SD212		N/A			0.3	0.5		50 V_{GS} = +10V 30 V_{GS} = +15V 23 V_{GS} = +20V 19 V_{GS} = +25V 17	70 45		N/A			N/A			N/A	
SD213		N/A			0.3	0.5		50 V_{GS} = +10V 30 V_{GS} = +15V 23 V_{GS} = +20V 19	70 45		N/A			N/A			N/A	
SD214		N/A			0.3	0.5		50 V_{GS} = +10V 30 V_{GS} = +15V 23 V_{GS} = +20V 19 V_{GS} = +25V 17	70 45		N/A			N/A			N/A	
SD215		N/A			0.3	0.5		50 V_{GS} = +10V 30 V_{GS} = +15V 23 V_{GS} = +20V 19 V_{GS} = +25V 17	70 45		N/A			N/A			N/A	

DMOS ELECTRICAL CHARACTERISTICS (Cont'd) T_A = +25°C unless otherwise specified

PARAMETER	BV_{DS} (V) Drain-To-Source V_{GS} = 0V $I_D < 1\mu A$	BV_{SD} (V) Source-To-Drain $V_{GD}=V_{BD}$= −5V I_D = 10nA	BV_{DB} (V) Drain-To-Substrate V_{GB} = 0V Source = Open I_D = 10nA	BV_{SB} (V) Source-To-Substrate V_{GB} = 0V Drain = Open I_S = 10μA	I_{DSS} (μA) Zero Bias Drain Current V_{DS} = +15V V_{GS} = 0V	I_{SD} (Off) (nA) Drain-To-Source $V_{GS}=V_{BS}$= −5V V_{DS} = +10V	I_{SD} (Off) (nA) Source-To-Drain $V_{GD}=V_{BD}$= −5V V_{DS} = +10V	I_{GBS} (μA) Gate V_{GS} = ±10V V_{DS} = 0V
	Min Typ Max	Min Typ Max	Min Typ Max	Min Typ Max	Min Typ Max	Min Typ Max	Min Typ Max	Min Typ Max
	$V_{G1S}=V_{G2S}$=0V I_D = 5μA							Gate 1 V_{G1S}=+5V $V_{G2S}=V_{DS}$=0V Gate 2 V_{G2S}=+10V $V_{G1S}=V_{DS}$=0V
SD300	25 30	N/A	N/A	N/A	0.001 1.0	N/A	N/A	0.001 0.1
SD301	20 25	N/A	N/A	N/A	0.001 1.0	N/A	N/A	0.001 0.1
SD303	20 25	N/A	N/A	N/A	0.001 1.0	N/A	N/A	0.001 0.1
SD304	25 30	N/A	N/A	N/A	0.001 1.0	N/A	N/A	0.001 0.1
SD305	20 30	N/A	N/A	N/A	0.001 1.0	N/A	N/A	0.001 0.1
SD306	20 25	N/A	N/A	N/A	0.001 1.0	N/A	N/A	0.001 0.1
SD5000	$V_{GS}=V_{BS}$= −5V I_S = 10nA 20 25	20	25	25	N/A	V_{DS} = +20V 1 10	V_{SD} = +20V 1 10	$V_{DB}=V_{SB}$=0V V_{GB} = 20V V_{GB} = 25V 10
SD5001	10 25	10	15	15	N/A	V_{DS} = +10V 1 10	V_{SD} = +10V 1 10	V_{GB} = +25V 10
SD5100	$V_{GB}=V_{BS}$= 0V I_S = 1μA 30 35	$V_{GD}=V_{BD}$= 0V I_D = 10nA .5	I_D = 1μA 30	I_S = 100nA .5	N/A	V_{GS} = V_{BS} = 0V V_{DS} = +10V 1 10	N/A	10
SD5101	$V_{GB}=V_{BS}$= 0V I_S = 1μA 15 30	$V_{GD}=V_{BD}$= 0V I_D = 10nA .5	I_D = 1μA 15	I_S = 100nA .5	N/A	V_{GS} = V_{BS} = 0V V_{DS} = +10V 1 10	N/A	10
SD5200	$V_{GB}=V_{BS}$= 0V I_S = 10μA 30 35	N/A	N/A	N/A	N/A	N/A	N/A	10
SD6000	$V_{G1S}=V_{G2S}$=0V I_S = 5μA 20 30	N/A	N/A	N/A	0.001 1.0	N/A	N/A	Gate 1 V_{G1S}=+5V $V_{G2S}=V_{DS}$ = 0V Gate 2 V_{G2S}=+10V $V_{G1S}=V_{DS}$= 0V 0.001 0.1

DMOS ELECTRICAL CHARACTERISTICS (Cont'd) T_A = +25°C unless otherwise specified

PARAMETER	I_{GB} (μA) Gate-To-Substrate Drain & Source Open V_{GB} = +30V			V_T (V) Threshold Voltage V_{DS} = V_{GS} = V_T I_D = 1μA			gfs (mmhos) Forward Transconductance V_{DS} = +15V, I_D = 20 mA f = 1 KHz V_{GS} ≅ +4V			$C_{(GS+GD+GB)}$ (pF) Gate Node V_{DS} = +10V, V_{GS}=V_{BS}=−15V f = 1 MHz			$C_{(GD+DB)}$ (pF) Drain Node V_{DS} = +10V, V_{GS}=V_{BS}=−15V f = 1 MHz			$C_{(GS+SB)}$ (pF) Source Node V_{DS} = +10V, V_{GS}=V_{BS}=−15V f = 1 MHz			C_T (dB) Cross Talk f = 3 KHz			C_{ISS} (pF) Input I_D = 20mA V_{DS} = +15V, f = 1 MHz		
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max
				Gate 1 V_{G2S}=+10V V_{DS}= V_{G1S}= V_T Gate 2 V_{G1S}=+4V V_{DS}=V_{G2S} = V_T			I_D = 18mA V_{G1S}≅+3.5V V_{G2S} = +10V															V_{G1S}≅3.5V, V_{G2S} = +10V I_D = 18mA	2.0	2.5
SD300		N/A		0.1	1.0	2.0	8.0	10.0			N/A			N/A			N/A			N/A				
SD301		N/A		0.1	1.0	2.0	8.0	10.0			N/A			N/A			N/A			N/A			2.0	2.5
SD303		N/A		0.1	1.0	2.0	V_{G1S}≅ +2.5V V_{G2S} = +10V 13.0	15.0			N/A			N/A			N/A			N/A		V_{G1S}≅+2.5V	3.0	3.5
SD304		N/A		0.1	1.0	2.0	8.0	10.0			N/A			N/A			N/A			N/A			2.5	3.0
SD305		N/A		0.1	1.0	2.0	V_{G2S} = +10V I_D = 50mA 24 Conversion V_{G1S} = V_{G2S} I_D = 8mA E_{LO}(RMS)=750mV	27 10			N/A			N/A			N/A			N/A		Gate 2 AC Grounded I_D = 50mA V_{G1S} = V_{G2S} I_D = 8mA	4.0 4.0	5.0 5.0
SD306		N/A		0.1	1.0	2.0	V_{G2S} = +10V 13	15			N/A			N/A			N/A			N/A			3.3	3.6
SD5000			1	I_S = 1μA V_{SB} = 0V 0.1	1.0	2.0	V_{DS} = +10V, V_{SB} = 0V 10	15			2.4	3.5		1.3	1.5		3.5	4.0		−107			N/A	
SD5001			1	0.1	1.0	2.0	10	15			2.4	3.5		1.3	1.5		3.5	4.0		−107			N/A	
SD5100		N/A		0.5	1.0	2.0	10	15			2.4	3.5		1.3	1.5		N/A			−107			N/A	
SD5101		N/A		0.5	1.0	2.0	10	15			2.4	3.5		1.3	1.5		N/A			−107			N/A	
SD5200		N/A		0.5	1.0	2.0	10	15			2.4	3.5		1.3	1.5		N/A			−107			N/A	
SD6000		N/A		Gate 1 V_{G2S}=+10V V_{DS} = V_{G1S} = V_T Gate 2 V_{G1S}=+5V V_{DS}=V_{G2S}= V_T RF AMP 0.1 Mixer 0.1	0.5 1.0	1.5 2.0	I_D = 18mA V_{G2S}=+10V 12 Conversion I_D = 8mA V_{G1S}=V_{G2S} E_{LO} (RMS) = 750mV	15 10			N/A			N/A			N/A			N/A		V_{G2S} = +10V I_D = 18mA	3.0	3.5

DMOS ELECTRICAL CHARACTERISTICS (Cont'd) T_A = +25°C unless otherwise specified

PARAMETER	C_{OSS} (pF) Output I_D = 0A V_{DS} = +15V, f = 1 MHz	C_{RSS} (pF) Reverse Transfer I_D = 0A V_{DS} = +15V, f = 1 MHz	r_{DS} (On) (Ω) Drain-To-Source V_{GS} = +5V I_D = 0.1mA	r_{DSM} (On) (Ω) Match I_D = 0.1mA V_{SB} = 0 V_{GS} = +5V	Gps[1] (dB) Power Gain V_{DS}=+15V, I_D=20 mA f = 1 GHz V_{GS} ≅ +4V	NF[1] (dB) Noise Figure V_{DS}=+15V, I_D=20mA V_{GS} ≅ +4V f = 1 GHz
	Min Typ Max	Min Typ Max	Min Typ Max	Min Typ Max	Min Typ Max	Min Typ Max
	V_{G1S} = 0V, V_{G2S} = +10V f = 1 MHz 1.0 1.2	V_{G1S} = 0V, V_{G2S} = +10V f = 1 MHz 0.02	V_{G1S} = +5V, V_{G2S} = +10V 90 130	N/A	I_D = 18mA V_{G1S} ≅ +3.5V, V_{G2S} = +10V 9.0 13.0 f = 200 MHz	V_{G1S} ≅ +3.5V V_{G2S} = +10V I_D = 18mA 8.0[1] 9.0 f = 200 MHz
SD300					22.0 24.0	3.0 4.0
SD301	0.6 0.8	0.02	90 130	N/A	10.0 14.0 f = 200 MHz 22.0 25.0	6.0[1] 7.0 f = 200 MHz 2.0 3.0
SD303	0.6	0.02	65 80	N/A	V_{G1S} ≅ +2.5V 10.0 14.0[1]	V_{G1S} ≅ +2.5V 5.5[1] 7.0
SD304	1.0 1.2	0.03	90 130	N/A	f = 500 MHz 13.0 16.0	f = 500 MHz 5.0 6.0
SD305	1.3 1.7	0.03	30 60	N/A	Conversion[2] V_{G1S} = V_{G2S} I_D = 8mA, f_{rf} = 200 MHz 14 17	N/A
SD306	1.0 1.3	0.03	65 100	N/A	V_{G2S} = +10V f = 200 MHz 17 20	f = 200 MHz 1.5 2.5
SD5000	N/A	V_{DS} = +10V, V_{GS}=V_{BS}=−15V f = 1 MHz 0.3 0.5	V_{SB} = 0V 50 70 V_{GS} = +10V 30 45 V_{GS} = +15V 23 V_{GS} = +20V 19	1 5	N/A	N/A
SD5001	N/A	0.3 0.5	50 70 V_{GS} = +10V 30 45 V_{GS} = +15V 23 V_{GS} = +20V 19	1 5	N/A	N/A
SD5100	N/A	0.3 0.5	50 70 V_{GS} = +10V 30 45 V_{GS} = +15V 23 V_{GS} = +20V 19	1 5	N/A	N/A
SD5101	N/A	0.3 0.5	50 70 V_{GS} = +10V 30 45 V_{GS} = +15V 23 V_{GS} = +20V 19	1 5	N/A	N/A
SD5200	N/A	0.3 0.5	50 70 V_{GS} = +10V 30 45 V_{GS} = +15V 23 V_{GS} = +20V 19	1 5	N/A	N/A
SD6000	V_{G1S} = 0V, V_{G2S} = 10V 1.0 1.3	V_{G1S} = 0V, V_{G2S} = 10V 0.025	V_{G1S} = +5V V_{G2S} = +10V RF Amp 65 100 Mixer 30 60	N/A	I_D = 18mA V_{G2S} = +10V f = 100 MHz 20 25 Conversion[2] I_D = 8mA, f_{rf} = 100 MHz f_{LO} = 89.3 MHz 14 19	V_{DS} = +15V I_D = 18mA V_{G2S} = +10V f = 100 MHz 2.5 3.0

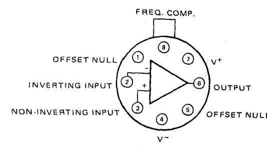
SE531-T • NE531-T,V

FEATURES

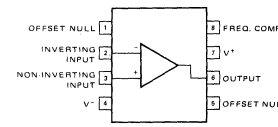
- 35V/μsec SLEW RATE AT UNITY GAIN
- PIN FOR PIN REPLACEMENT FOR μA709, μA748 OR LM101
- COMPENSATED WITH A SINGLE CAPACITOR
- SAME LOW DRIFT OFFSET NULL CIRCUITRY AS μA741
- SMALL SIGNAL BANDWIDTH 1MHz
- LARGE SIGNAL BANDWIDTH 500KHz
- TRUE OP AMP D.C. CHARACTERISTICS MAKE THE 531 THE IDEAL ANSWER TO ALL SLEW RATE LIMITED OPERATIONAL AMPLIFIER APPLICATIONS

PIN CONFIGURATION

T PACKAGE



V PACKAGE



ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±22V
Internal Power Dissipation (Note 1)	300mW
Differential Input Voltage	±15V
Common Mode Input Voltage (Note 2)	±15V
Voltage Between Offset Null and V—	±0.5V
Operating Temperature Range	
NE531	0°C to +70°C
SE531	—55°C to +125°C
Storage Temperature Range	—65°C to +150°C
Lead Temperature (Solder, 60 sec.)	300°C
Output Short Circuit Duration (Note 3)	Indefinite

NOTES:

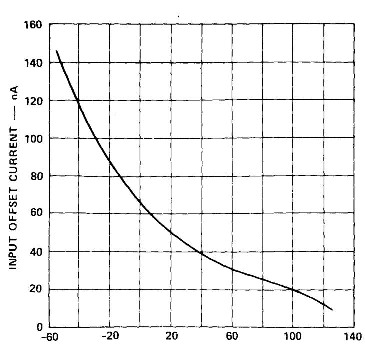
1. Rating applies for case temperatures to 125°C, derate linearly at 6.5mW/°C for ambient temperatures above +75°C.
2. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
3. Short circuit may be to ground or either supply. Rating applies to +125°C case temperature or +75°C ambient temperature.

ELECTRICAL CHARACTERISTICS

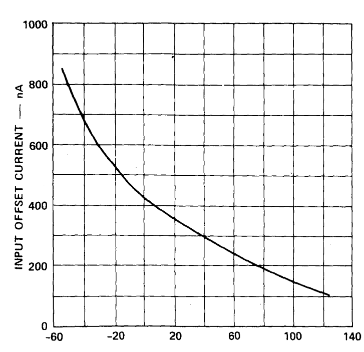
		LIMITS						
		SE531			NE 531			
Parameter	Test Conditions	Min	Typ	Max	Min	Typ	Max	Units
Output Resistance			75			75		Ω
Full Power Bandwidth			500			500		kHz
Settling Time 1%	AV=+1, VIN=±10V		1.5			1.5		μsec
Settling Time .01%	AV=+1, VIN=±10V		2.5			2.5		μsec
Large Signal Overshoot	AV=+1, VIN=±10V		2			2		%
Small Signal Overshoot	AV=+1, VIN=400mV		5			5		%
Small Signal Risetime	AV=+1, VIN=400mV		300			300		nsec
Slew Rate	AV=100		35			35		V/μs
	AV=10		35			35		V/μs
	AV=1 (non-inverting)	20	30			30		V/μs
	AV=1 (inverting)	25	35			35		V/μs

TYPICAL PERFORMANCE CHARACTERISTICS ($V_S = \pm 15V$, $T_A = +25°C$, unless otherwise noted)

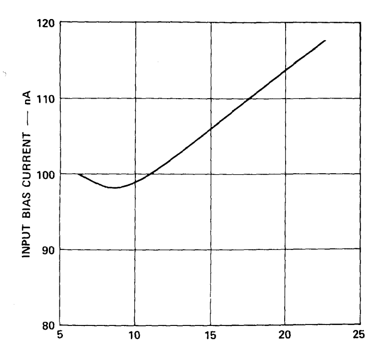
INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE

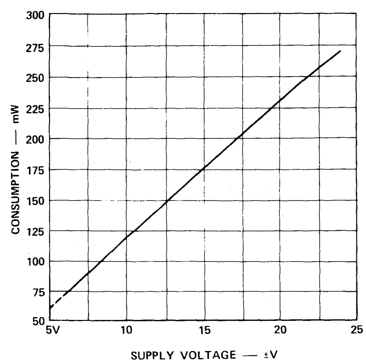


INPUT BIAS CURRENT AS A FUNCTION OF SUPPLY VOLTAGE

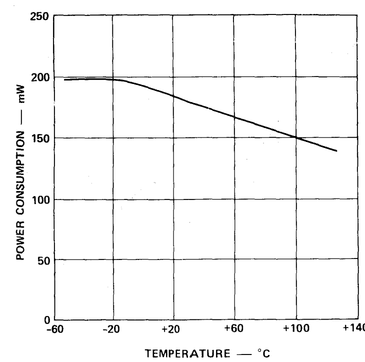


TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

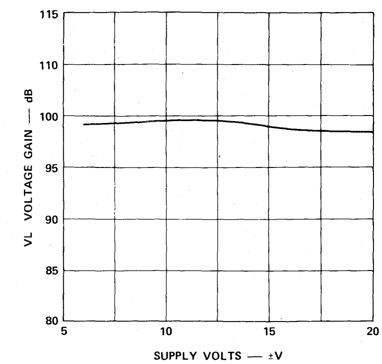
POWER CONSUMPTION AS A FUNCTION OF SUPPLY VOLTAGE



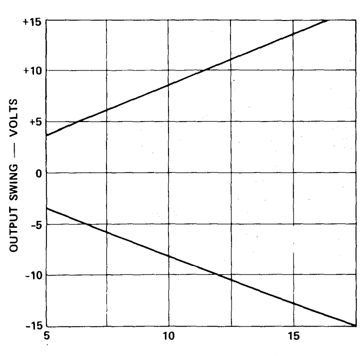
POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE



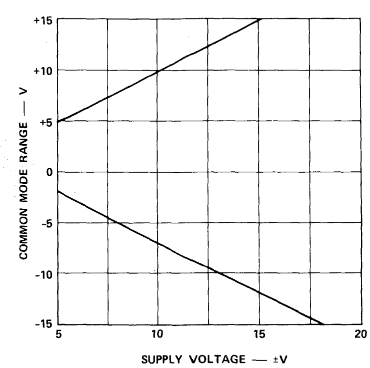
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE



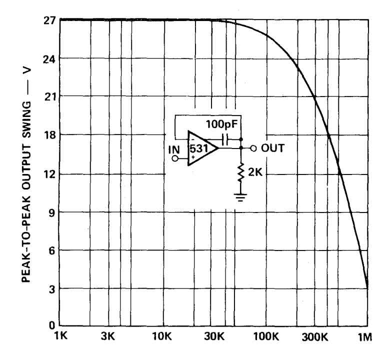
OUTPUT VOLTAGE SWING AS A FUNCTION OF SUPPLY VOLTAGE



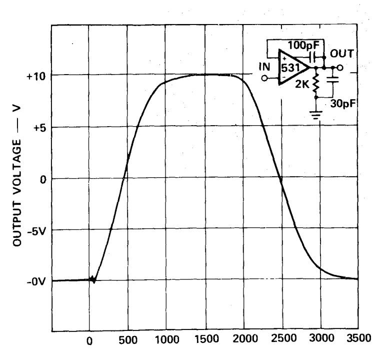
INPUT VOLTAGE RANGE AS A FUNCTION OF SUPPLY VOLTAGE



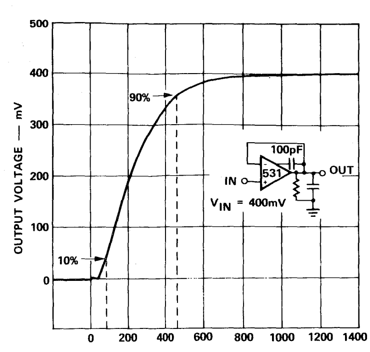
OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY



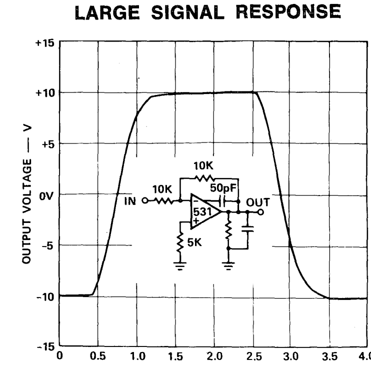
VOLTAGE FOLLOWER LARGE SIGNAL RESPONSE



VOLTAGE FOLLOWER TRANSIENT RESPONSE



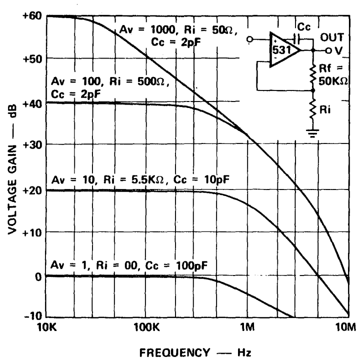
UNITY GAIN INVERTING AMPLIFIER LARGE SIGNAL RESPONSE



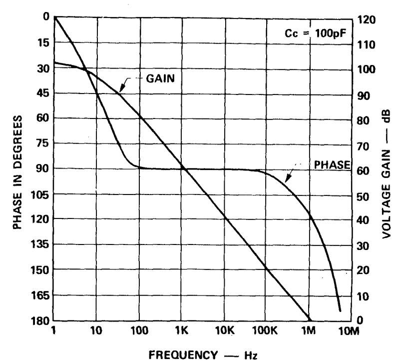
ANALOG

TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

CLOSED LOOP NON-INVERTING VOLTAGE GAIN AS A FUNCTION OF FREQUENCY

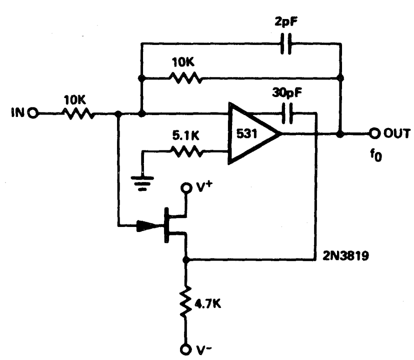


OPEN LOOP PHASE RESPONSE AND VOLTAGE GAIN AS A FUNCTION OF FREQUENCY



TYPICAL APPLICATIONS

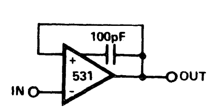
HIGH SPEED INVERTER (10MHz BANDWIDTH)



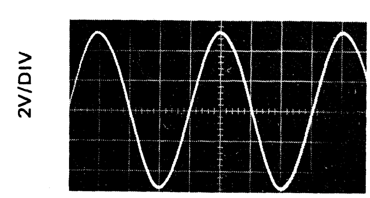
PULSE RESPONSE HIGH SPEED INVERTER

200nsec/DIV

FAST SETTLING VOLTAGE FOLLOWER



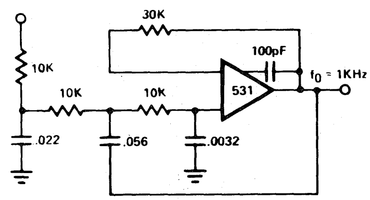
LARGE SIGNAL RESPONSE VOLTAGE FOLLOWER



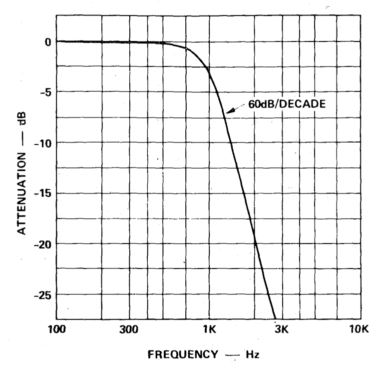
0.5μs/DIV ƒ = 500KHz

TYPICAL APPLICATIONS (Cont'd)

3 POLE ACTIVE LOW PASS FILTER BUTTERWORTH MAXIMALLY FLAT RESPONSE*



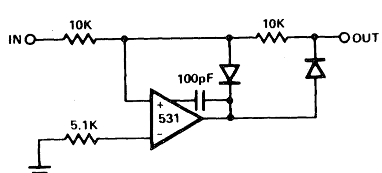
RESPONSE OF 3-POLE ACTIVE BUTTERWORTH MAXIMALLY FLAT FILTER



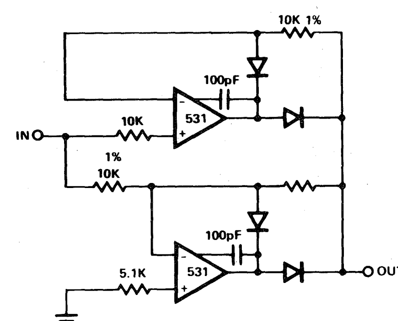
*Reference — EDN Dec. 15, 1970
Simplify 3-Pole Active Filter Design
A. Paul Brokow

PRECISION RECTIFIERS

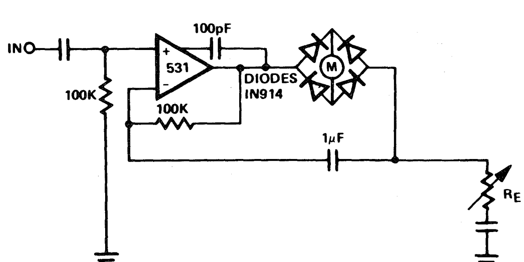
(a) HALF WAVE



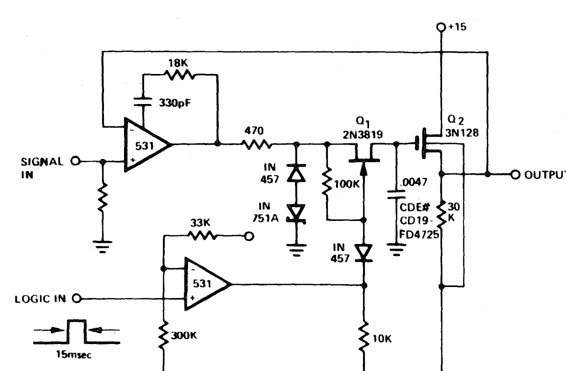
(b) FULL WAVE



AC MILLIVOLTMETER

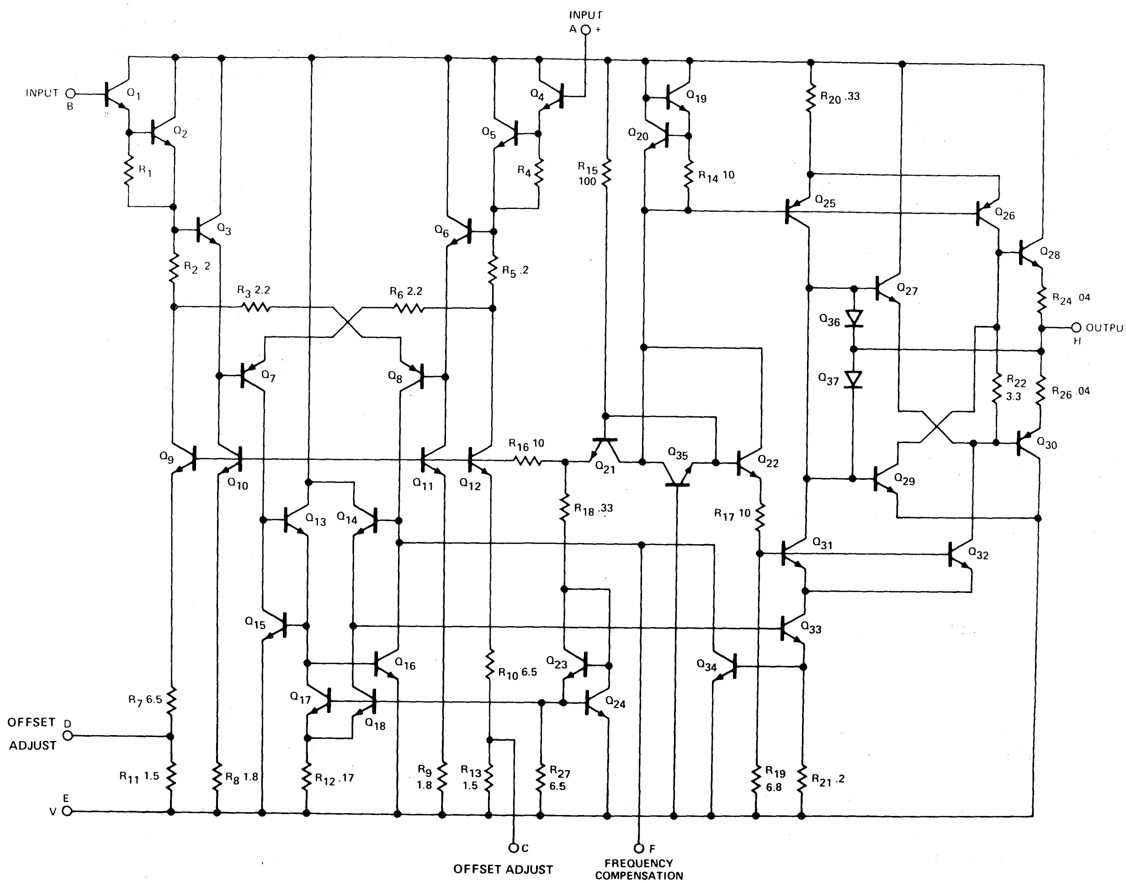


SAMPLE AND HOLD



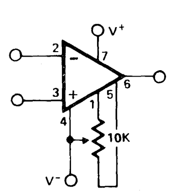
SE531-T • NE531-T,V

SCHEMATIC DIAGRAM

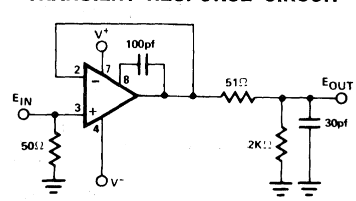


TEST CIRCUITS

OFFSET NULL CIRCUIT



TRANSIENT RESPONSE CIRCUIT



SE532-T,V • SU532-T,V • NE532-T,V

FEATURES

- INTERNALLY FREQUENCY COMPENSATED FOR UNITY GAIN
- LARGE DC VOLTAGE GAIN—(100dB)
- WIDE BANDWIDTH (UNITY GAIN)—1MHz (TEMPERATURE COMPENSATED)
- WIDE POWER SUPPLY RANGE SINGLE SUPPLY—(3V DC to 30V DC) OR DUAL SUPPLIES—(±1.5V DC to ±15V DC)
- VERY LOW SUPPLY CURRENT DRAIN (400μA)—ESSENTIALLY INDEPENDENT OF SUPPLY VOLTAGE (1mW/OP AMP AT +5V DC)
- LOW INPUT BIASING CURRENT—(45nA DC TEMPERATURE COMPENSATED)
- LOW INPUT OFFSET VOLTAGE—(2mV DC) AND OFFSET CURRENT—(5nA DC)
- DIFFERENTIAL INPUT VOLTAGE RANGE EQUAL TO THE POWER SUPPLY VOLTAGE
- LARGE OUTPUT VOLTAGE—(0V DC to V+ —1.5V DC SWING)

UNIQUE FEATURES

IN THE LINEAR MODE THE INPUT COMMON-MODE VOLTAGE RANGE INCLUDES GROUND AND THE OUTPUT VOLTAGE CAN ALSO SWING TO GROUND, EVEN THOUGH OPERATED FROM ONLY A SINGLE POWER SUPPLY VOLTAGE.

THE UNITY GAIN CROSS FREQUENCY IS TEMPERATURE COMPENSATED.

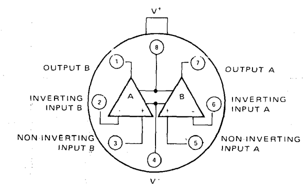
THE INPUT BIAS CURRENT IS ALSO TEMPERATURE COMPENSATED.

ABSOLUTE MAXIMUM RATINGS

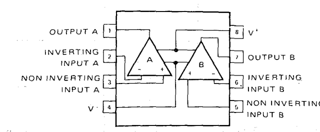
Supply Voltage, V+	32V DC or ±16V DC
Differential Input Voltage	32V DC
Input Voltage	—0.3V DC to +32V DC
Power Dissipation	
T Package	680mW
V Package	625mW
Output Short-Circuit to GND V+ < 15V DC and TA=25°C	Continuous
Operating Temperature Range	
NE532	0°C to +70°C
SU532	—25°C to +85°C
SE532	—55°C to +125°C
Storage Temperature Range	—65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	300°C

PIN CONFIGURATION

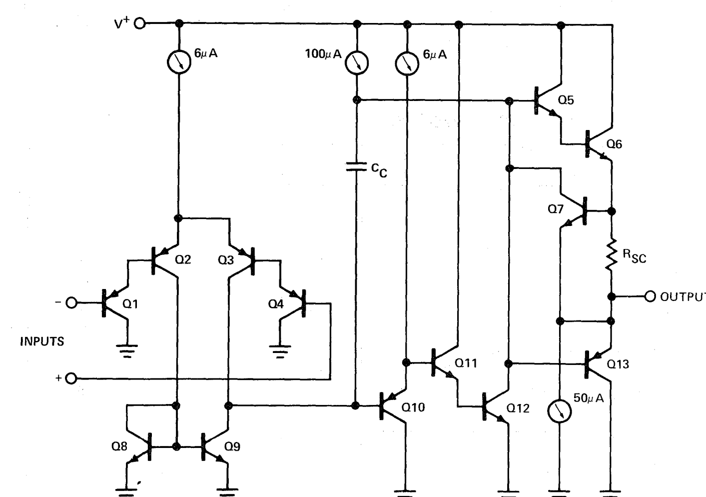
T PACKAGE



V PACKAGE



EQUIVALENT CIRCUIT

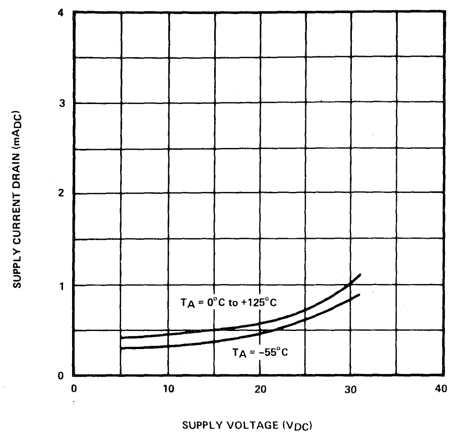


ELECTRICAL CHARACTERISTICS

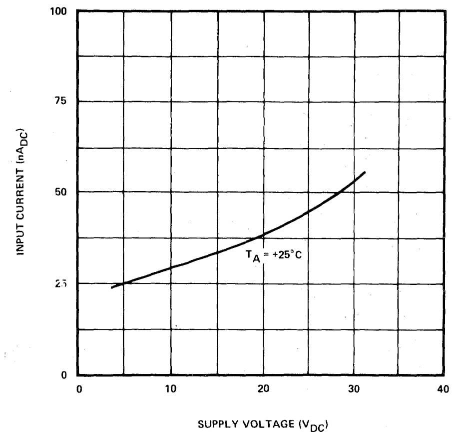
Parameter	Test Conditions	LIMITS			Units
		Min	Typ	Max	
Amplifier-to-Amplifier Coupling	f-1kHz to 20kHz, $T_A=25°C$ (Input Referred)		-120		dB
Output Current Source	$V_{IN}+=1V_{DC}$, $V_{IN}-=0V_{DC}$, $V+=15V_{DC}$, $T_A=+25°C$	20	40		mA_{DC}
	$V_{IN}+=+1V_{DC}$, $V_{IN}-=0V_{DC}$, $V+=15V_{DC}$	10	20		mA
Output Current Sink	$V_{IN}-=+1V_{DC}$, $V_{IN}+=0V_{DC}$, $V+=15V_{DC}$, $T_A=+25°C$	10	20		mA_{DC}
	$V_{IN}-=+1V_{DC}$, $V_{IN}+=0V_{DC}$, $T_A=+25°C$, $V_O=200mV_{DC}$	12	50		μA_{DC}
	$V_{IN}-=+1V_{DC}$, $V_{IN}+=0V_{DC}$, $V+=15V_{DC}$	5	8		mA
Differential Input Voltage	See Note 5			V+	

TYPICAL PERFORMANCE CURVES

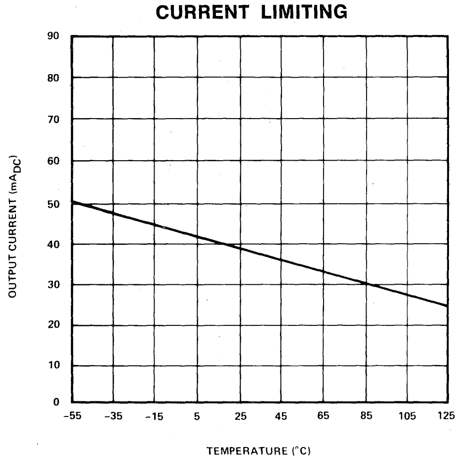
SUPPLY CURRENT



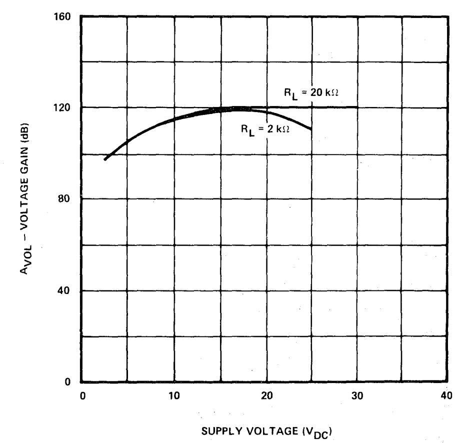
INPUT CURRENT



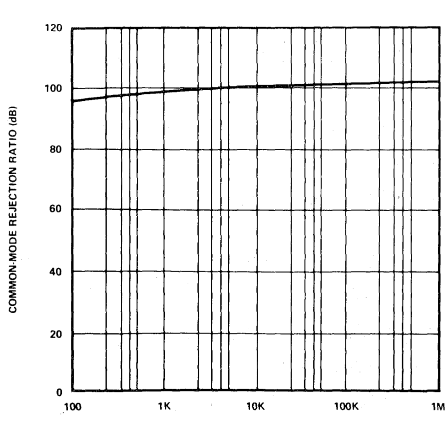
CURRENT LIMITING



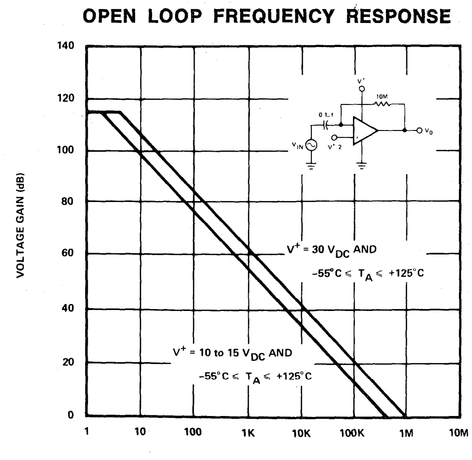
VOLTAGE GAIN



COMMON-MODE REJECTION RATIO

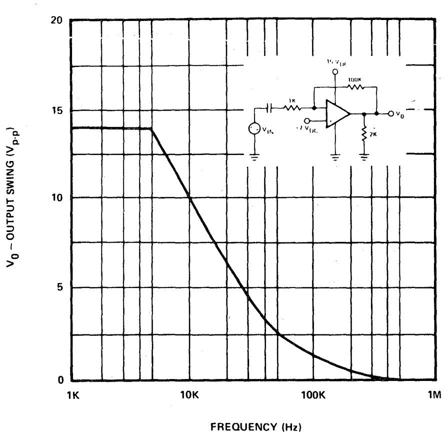


OPEN LOOP FREQUENCY RESPONSE

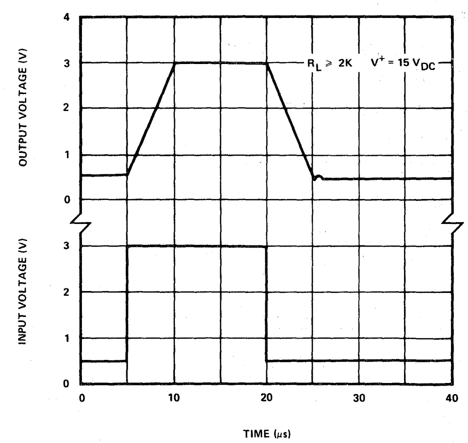


TYPICAL PERFORMANCE CURVES (Cont'd)

LARGE SIGNAL FREQUENCY RESPONSE



VOLTAGE FOLLOWER PULSE RESPONSE



ANALOG

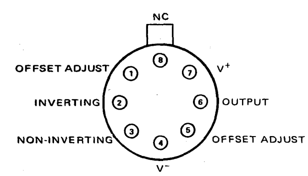
OBJECTIVE SPECIFICATION

FEATURES

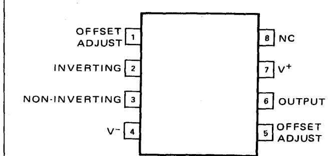
- 15V/μS UNITY GAIN SLEW RATE
- INTERNAL FREQUENCY COMPENSATION
- LOW INPUT OFFSET VOLTAGE — 2 mV MAXIMUM
- LOW INPUT BIAS CURRENT — 60nA MAXIMUM
- SHORT CIRCUIT PROTECTED
- OFFSET NULL CAPABILITY
- LARGE COMMON MODE AND DIFFERENTIAL VOLTAGE RANGES

PIN CONFIGURATION

T PACKAGE



V PACKAGE

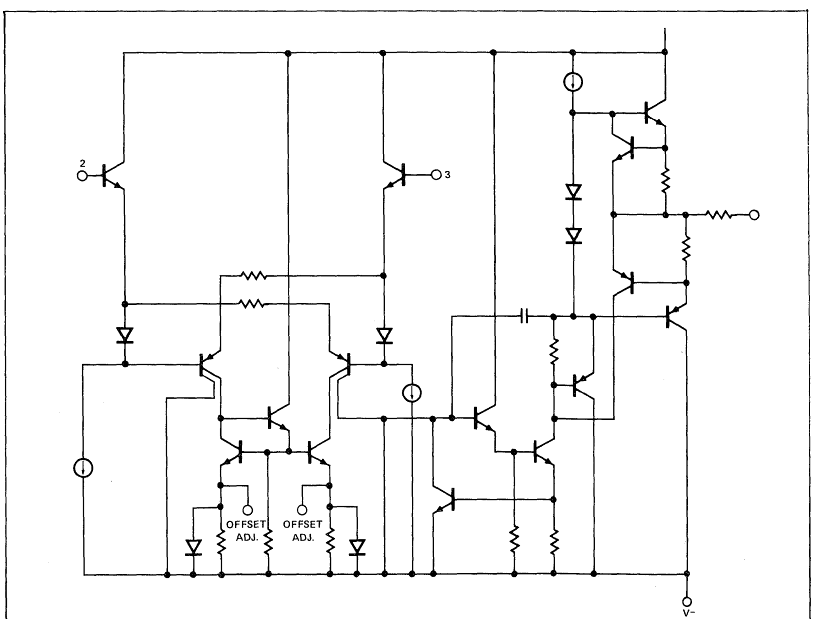


ELECTRICAL CHARACTERISTICS

Parameter	Test Conditions	LIMITS Min	Typ	Max	Units
Output Short Circuit Current			25		mA
Output Resistance			100		Ω
Settling Time	To 0.1%		3		μS
Slew Rate	Unity gain non-inverting, $R_L > 10K$	10	15		V/μS

ABSOLUTE MAXIMUM RATINGS

Supply Voltage:	SE535	±22V
	NE535	±18V
Internal Power Dissipation (Note 1)		500mW
Differential Input Voltage		±30V
Input Voltage (Note 2)		±15V
Operating Temperature Range		
	SE535	−55°C to +125°C
	NE535	0°C to +70°C
Storage Temperature Range		−65°C to +150°C
Lead Temperature (Solder, 60 sec.)		300°C
Output Short Circuit (Note 3)		Indefinite



NOTES:

1. Rating applies for case temperatures to 125°C; derate linearly at 6.5mW/°C for ambient temperatures above 75°C.
2. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
3. Short circuit may be to ground or either supply. Rating applies to +125°C case temperature or 75°C ambient temperature.

NE536-T • SU536-T

FEATURES

- 5pA INPUT BIAS CURRENT
- INPUT AND OUTPUT PROTECTION
- OFFSET NULL CAPABILITY
- INTERNALLY COMPENSATED
- 6V/μsec SLEW RATE
- STANDARD PINOUT
- 1 MHz UNITY GAIN BANDWIDTH

MAXIMUM GUARANTEED RATINGS

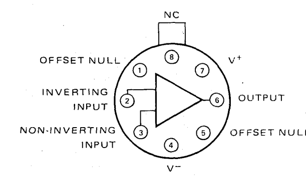
Supply Voltage	±22V
Differential Input Voltage Range	±30V
Common Mode Input Voltage Range	±Vs
Power Dissipation (Note 1)	500mW
Operating Temperature Range	
SU536T	—55°C to +85°C
NE536T	0°C to +70°C
Storage Temperature Range	—65°C to +150°C
Lead Temperature (Solder, 60 sec.)	300°C
Output Short Circuit Duration (Note 2)	Indefinite

NOTES:

1. Rating applies for case temperatures to +25°C; derate linearly at 6.5mW/°C for ambient temperatures above 75°C.
2. Short circuit may be to ground or either supply. Rating applies to +125°C case temperature or +75°C ambient temperature.

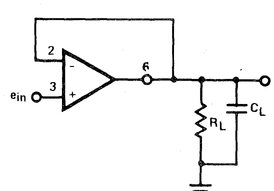
PIN CONFIGURATION

T PACKAGE

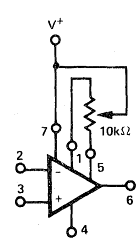


TEST CIRCUITS

VOLTAGE FOLLOWER CIRCUIT



OFFSET NULL CIRCUIT

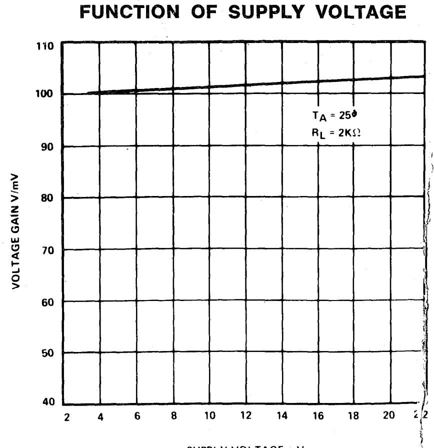


ELECTRICAL CHARACTERISTICS

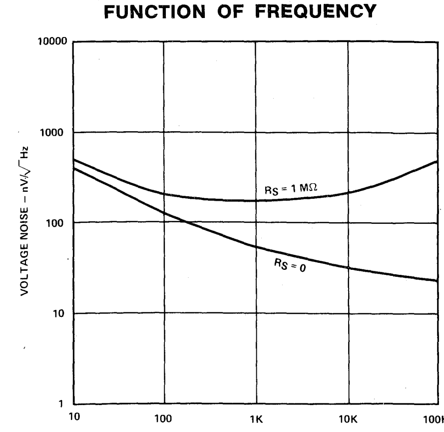
Parameter	Test Conditions	NE536 Min	NE536 Typ	NE536 Max	SU536 Min	SU536 Typ	SU536 Max	Units
Differential Capacitance	$T_A = +25°C$		6			6		pF
Input Noise (0.1Hz= 100kHz) Voltage Noise			20			20		μVrms
Output Impedance			100			100		
Gain Bandwidth Product	$V_S = \pm15V$, $T_A = +25°C$, A=100		1			1		MHz
Full Power Bandwidth	$V_S = \pm15V$, $T_A = +25°C$		100			100		KHz
Slew Rate Inverter	$V_S = \pm15V$, $T_A = +25°C$, A=−1V		6			6		V/μs
Follower	$V_S = \pm15V$, $T_A = +25°C$, A=+1		6			6		V/μs
Power Supply Range		±6		±18	±6		±20	V

TYPICAL CHARACTERISTIC CURVES

OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE

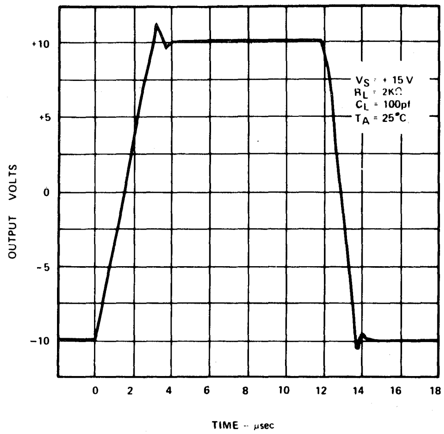


INPUT VOLTAGE NOISE AS A FUNCTION OF FREQUENCY

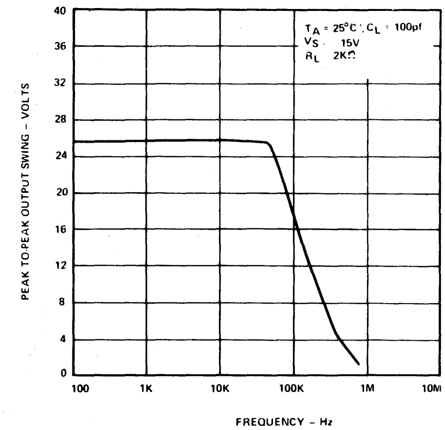


TYPICAL CHARACTERISTIC CURVES (Cont'd)

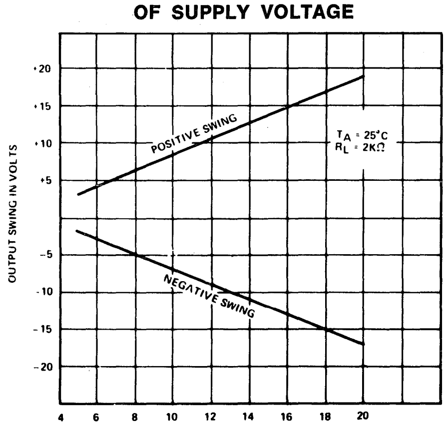
LARGE SIGNAL VOLTAGE FOLLOWER PULSE RESPONSE



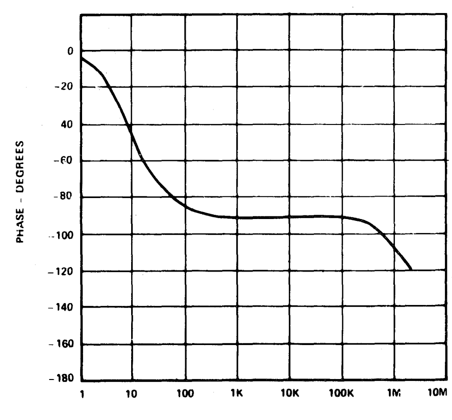
OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY



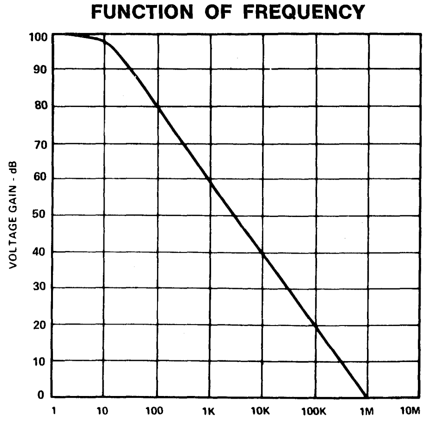
OUTPUT VOLTAGE SWING AS A FUNCTION OF SUPPLY VOLTAGE



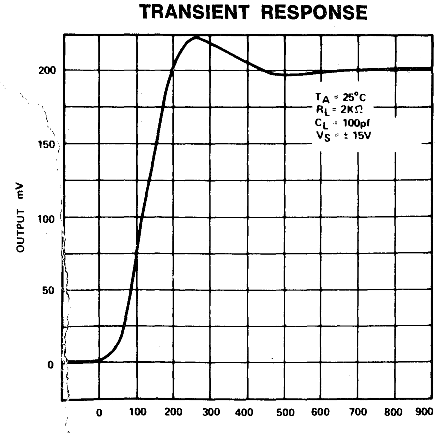
OPEN LOOP PHASE RESPONSE AS A FUNCTION OF FREQUENCY



OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF FREQUENCY

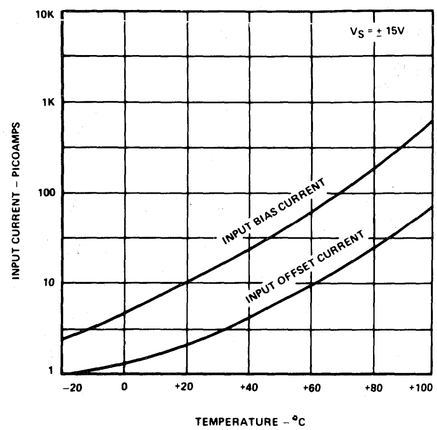


VOLTAGE FOLLOWER TRANSIENT RESPONSE

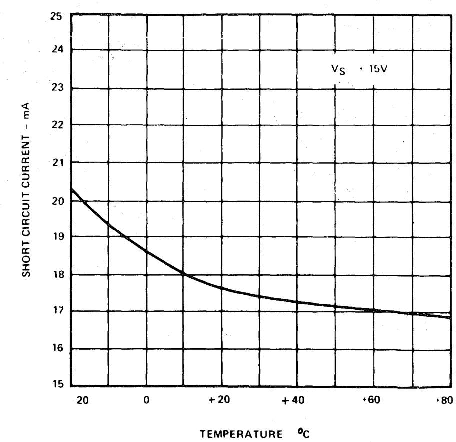


TYPICAL CHARACTERISTIC CURVES (Cont'd)

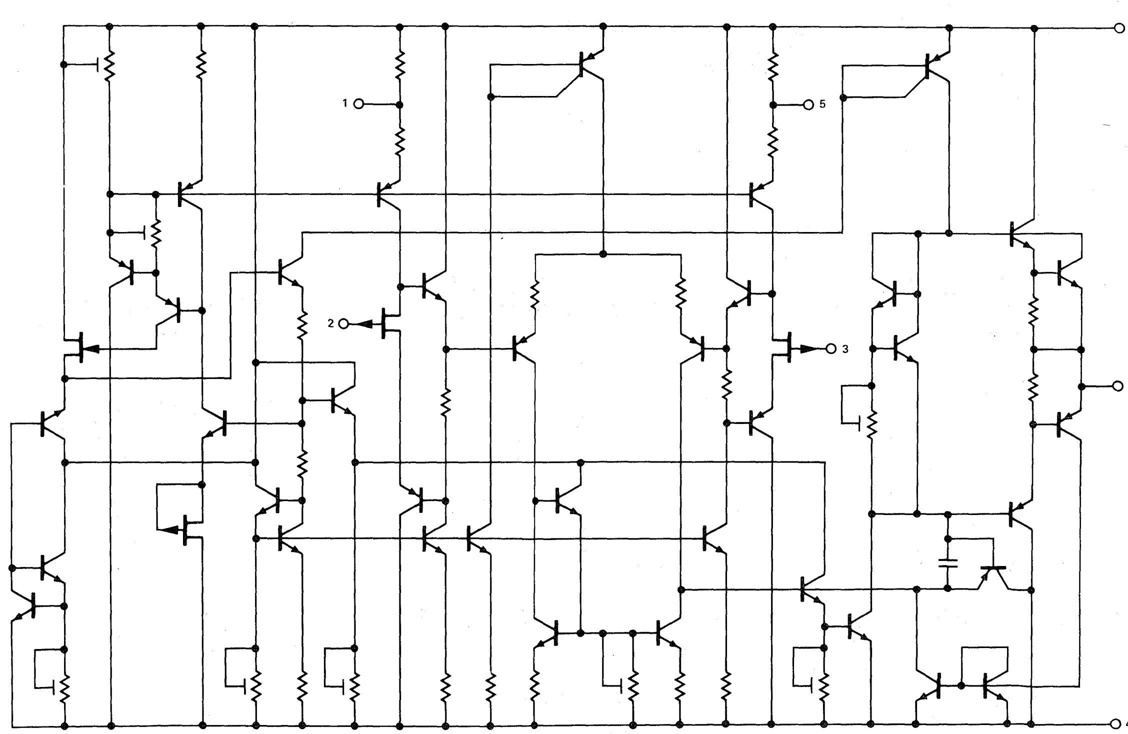
INPUT CURRENTS AS A FUNCTION OF AMBIENT TEMPERATURE



OUTPUT SHORT-CIRCUIT CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



CIRCUIT SCHEMATIC



LH2101A • LH2201A • LH2301A-A,F

FEATURES

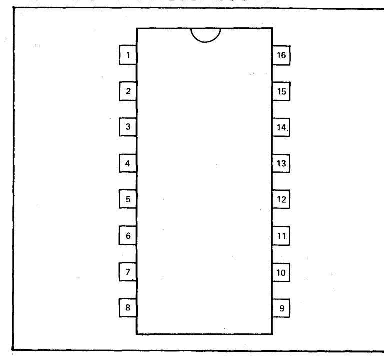
- LOW OFFSET VOLTAGE
- LOW OFFSET CURRENT
- GUARANTEED DRIFT CHARACTERISTICS
- OFFSETS GUARANTEED OVER ENTIRE COMMON MODE AND SUPPLY VOLTAGE RANGES
- SLEW RATE OF 10V/μs AS A SUMMING AMPLIFIER

ABSOLUTE MAXIMUM RATINGS

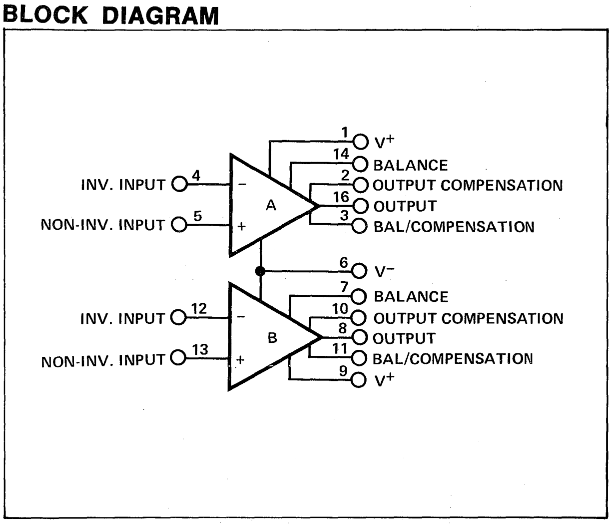
Supply Voltage	±22V
Power Dissipation	500mW
Differential Input Voltage	±30V
Input Voltage (Note 2)	±15V
Output Short Circuit Duration	Continuous
Operating Temperature Range	
LH2101A	—55°C to 125°C
LH2201A	—25°C to 85°C
LH2301A	0°C to 70°C
Storage Temperature Range	—65°C to 150°C
Lead Temperature (Soldering, 10 sec.)	300°C

NOTES:
1. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

PIN CONFIGURATION

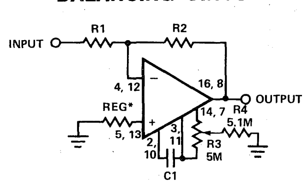


BLOCK DIAGRAM



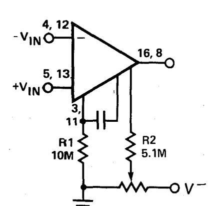
TYPICAL APPLICATIONS

INVERTING AMPLIFIER WITH BALANCING CIRCUIT

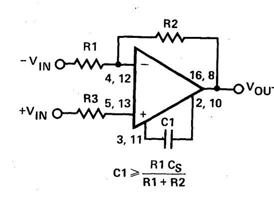


*MAY BE ZERO OR EQUAL TO PARALLEL COMBINATION OF R1 AND R2 FOR MINIMUM OFFSET.

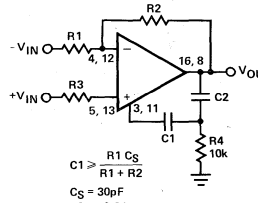
ALTERNATE BALANCING CIRCUIT



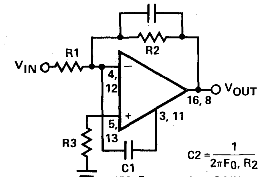
SINGLE POLE COMPENSATION



TWO POLE COMPENSATION



FEED FORWARD COMPENSATION



FEATURES

- **LOW OFFSET CURRENT 50pA**
- **LOW OFFSET VOLTAGE 0.7mV**
- **LOW OFFSET VOLTAGE**
  - **LH2108A 0.3mV**
  - **LH2108 0.7mV**
- **WIDE INPUT VOLTAGE RANGE ±15V**
- **WIDE OPERATING SUPPLY RANGE ±3V to ±20V**

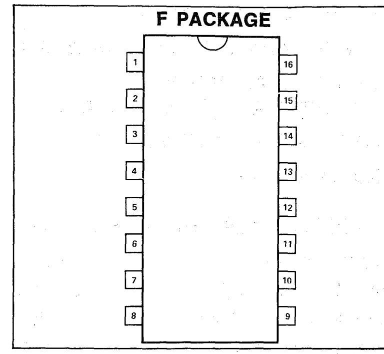
ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±20V
Power Dissipation	500mW
Differential Input Current (Note 1)	±10mA
Input Voltage (Note 2)	±15V
Output Short Circuit Duration	Continuous
Operating Temperature Range	
LH2108A/LH2108	—55°C to +125°C
LH2208A/LH2208	—25°C to +85°C
LH2308A/LH2308	0°C to +70°C
Storage Temperature Range	—65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	300°C

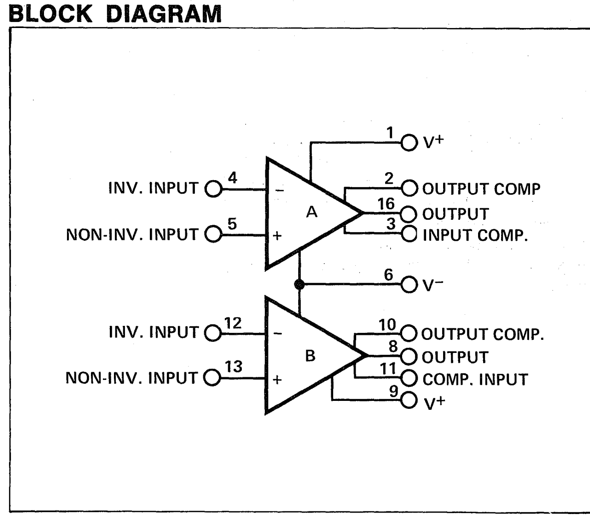
NOTES:

1. The inputs are shunted with back-to-back diodes for overvoltage protection. Therefore, excessive current will flow if a differential input voltage in excess of 1V is applied between the inputs unless some limiting resistance is used.
2. For supply voltage less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

PIN CONFIGURATION

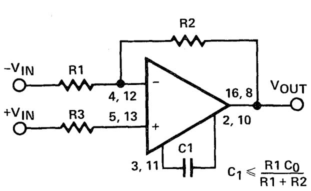


BLOCK DIAGRAM

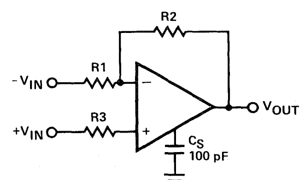


TYPICAL APPLICATIONS

STANDARD COMPENSATION CIRCUIT

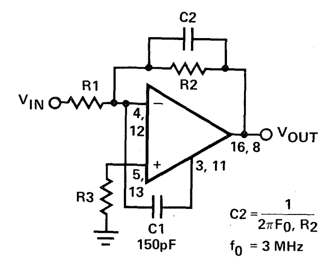


ALTERNATE FREQUENCY COMPENSATION



*IMPROVES REJECTION OF POWER SUPPLY NOISE BY A FACTOR OF TWO.

FEED FORWARD COMPENSATION



FEATURES

- SHORT CIRCUIT PROTECTION
- OFFSET VOLTAGE NULL CAPABILITY
- LARGE COMMON-MODE AND DIFFERENTIAL VOLTAGE RANGES
- LOW POWER CONSUMPTION
- NO LATCH UP

ABSOLUTE MAXIMUM RATINGS

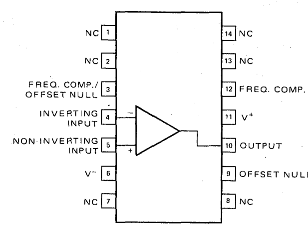
Supply Voltage	±22V
Power Dissipation (Note 1)	500mW
Differential Input Voltage	±30V
Input Voltage (Note 2)	±15V
Output Short Circuit Duration	Indefinite
Operating Temperature Range	
LM101	—55°C to 125°C
LM201	0°C to 70°C
Storage Temperature Range	—65°C to 150°C
Lead Temperature (Soldering, 60 sec.)	300°C

NOTES:

1. Absolute maximum rating holds for all packages. The maximum junction temperature is 150°C for the LM101 and 100°C for the LM201. For operation at elevated temperatures, derate according to appropriate thermal resistances given under package information.
2. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

PIN CONFIGURATION

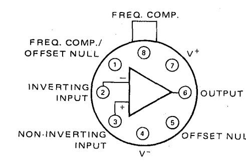
A PACKAGE



ORDER PART NOS.

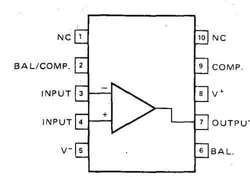
LM101A, LM201A } Silicone   LM101F, LM201F } Ceramic

T PACKAGE



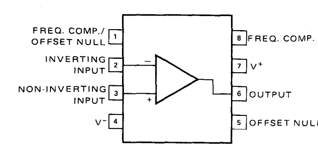
ORDER PART NOS.
LM101T/LM201T

Q PACKAGE



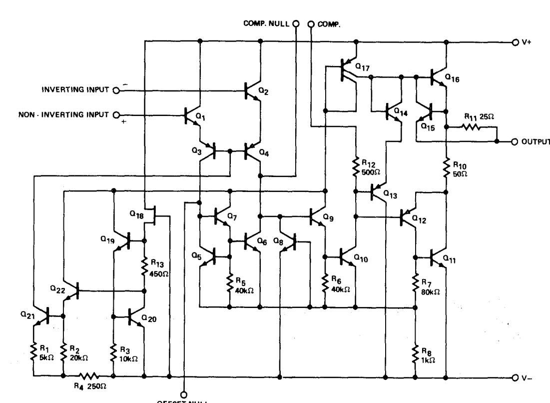
ORDER PART NOS.
LM101Q/LM201Q

V PACKAGE



ORDER PART NO. LM201V

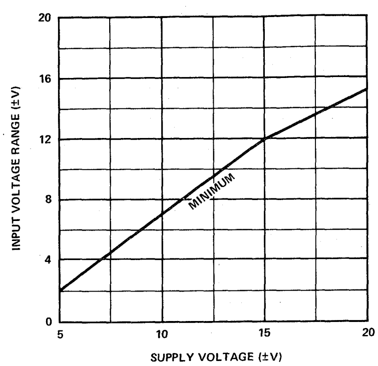
EQUIVALENT CIRCUIT



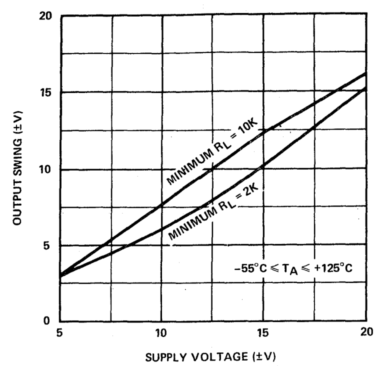
TYPICAL CHARACTERISTIC CURVES

LM101

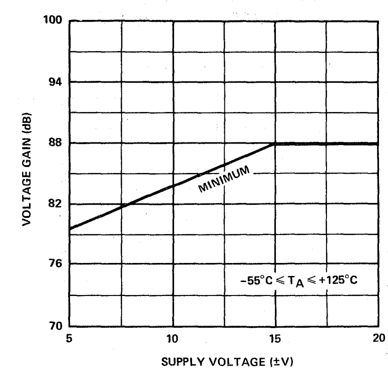
INPUT VOLTAGE RANGE VERSUS SUPPLY VOLTAGE



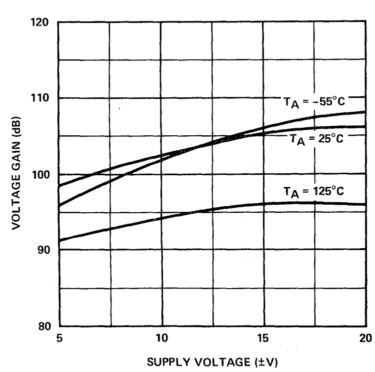
OUTPUT SWING VERSUS SUPPLY VOLTAGE



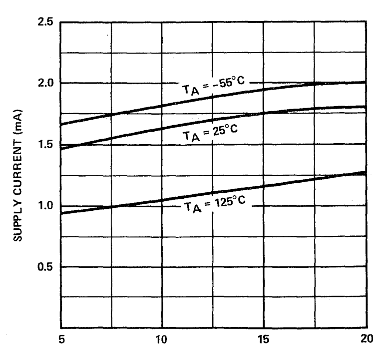
VOLTAGE GAIN VERSUS SUPPLY VOLTAGE



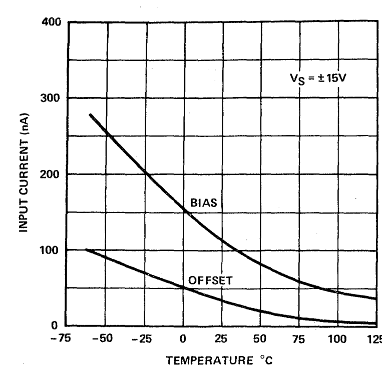
VOLTAGE GAIN



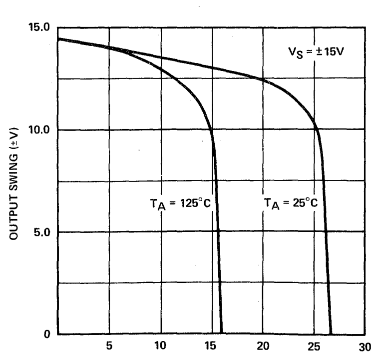
SUPPLY CURRENT



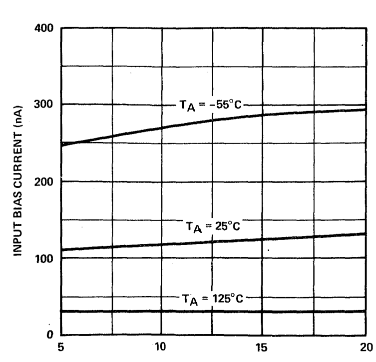
INPUT CURRENT



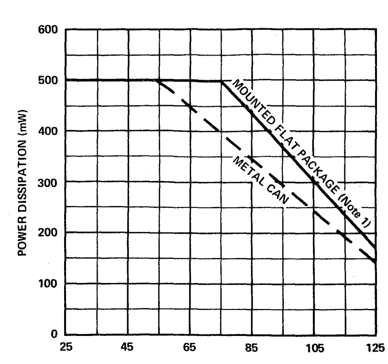
CURRENT LIMITING



INPUT CURRENT



MAXIMUM POWER DISSIPATION

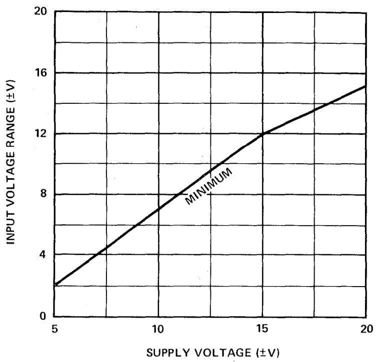


ANALOG

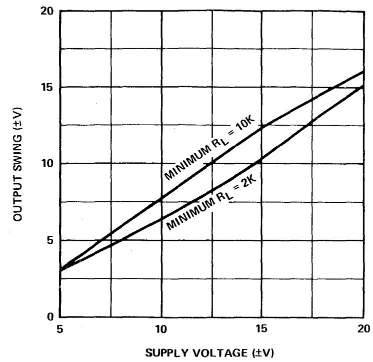
TYPICAL CHARACTERISTIC CURVES (Cont'd)

LM201

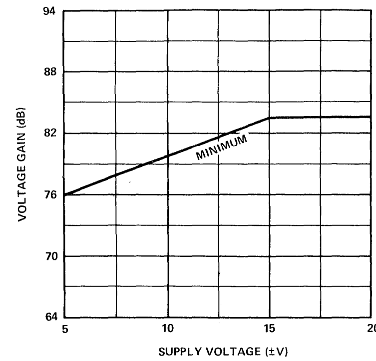
INPUT VOLTAGE RANGE VERSUS SUPPLY VOLTAGE



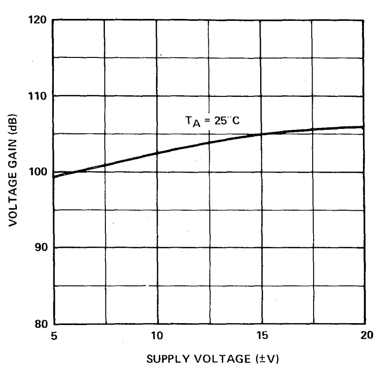
OUTPUT SWING VERSUS SUPPLY VOLTAGE



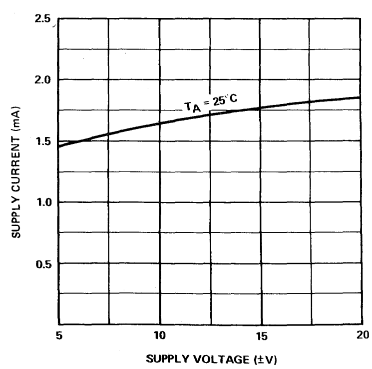
VOLTAGE GAIN VERSUS SUPPLY VOLTAGE



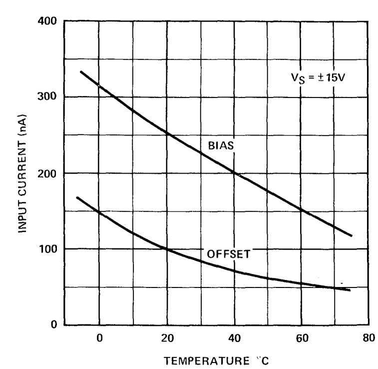
VOLTAGE GAIN



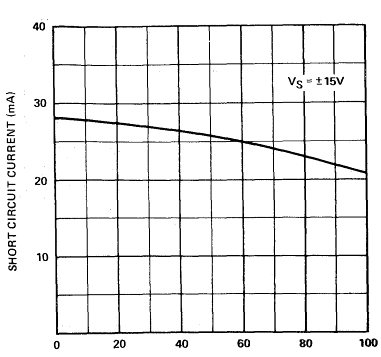
SUPPLY CURRENT



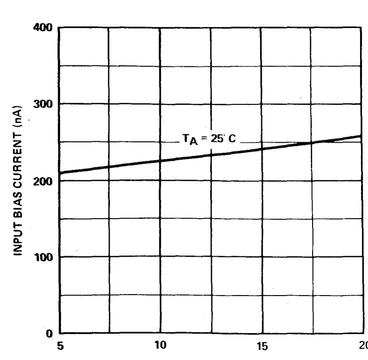
INPUT CURRENT



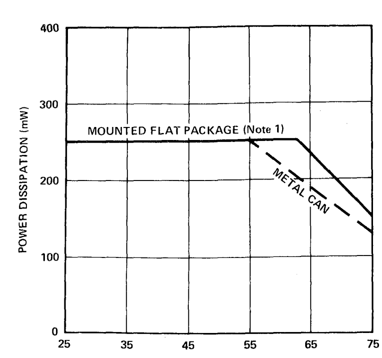
SHORT CIRCUIT CURRENT



INPUT CURRENT

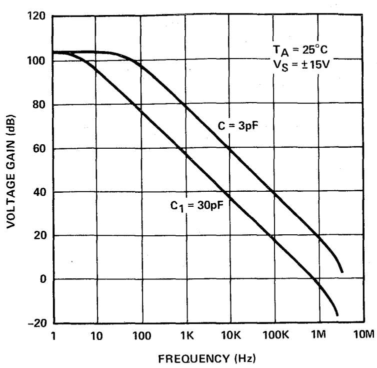


MAXIMUM POWER DISSIPATION

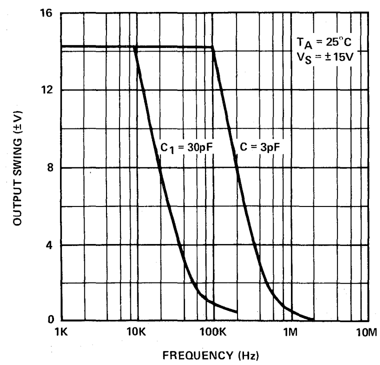


TYPICAL CHARACTERISTIC CURVES (Cont'd)

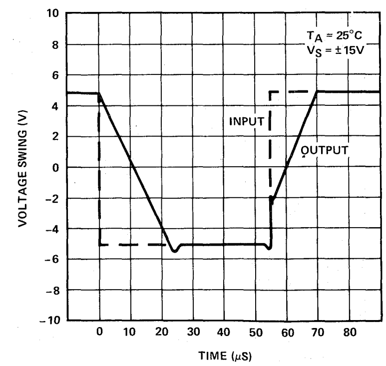
OPEN LOOP FREQUENCY RESPONSE



LARGE SIGNAL FREQEENCY RESPONSE

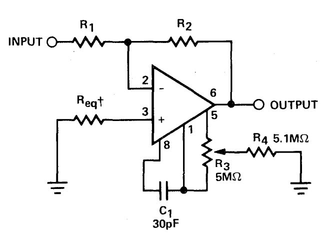


VOLTAGE FOLLOWER PULSE RESPONSE



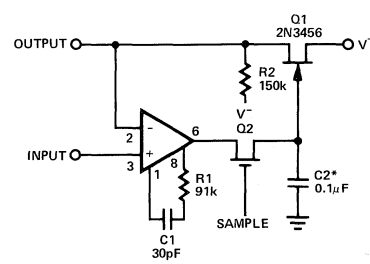
TYPICAL APPLICATIONS (Pin numbers shown refer to T or V package only)

INVERTING AMPLIFIER WITH BALANCING CIRCUIT



†May be zero or equal to parallel combination of R_1 and R_2 for minimum offset.

LOW DRIFT SAMPLE AND HOLD



*Polycarbonate Dielectric Capacitor

ANALOG

LM101A-F,T • LM201A-F,T,V • LM301A-F,T,V

ABSOLUTE MAXIMUM RATINGS

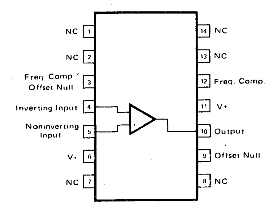
Supply Voltage		
	LM101A/LM201A	±22V
	LM301A	±18V
Power Dissipation (Note 1)		500mW
Differential Input Voltage		±30V
Input Voltage (Note 2)		±15V
Output Short Circuit Duration		Indefinite
Operating Temperature Range		
	LM101A	—55°C to 125°C
	LM201A	—25°C to 85°C
	LM301A	0°C to 70°C
Storage Temperature Range		—65°C to 150°C
Lead Temperature (Soldering, 60 sec.)		300°C

NOTES:

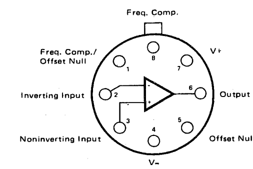
1. Absolute maximum rating holds for all packages. The maximum junction temperature is 150°C for the LM101A and 100°C for the LM201A and the LM301A. For operation at elevated temperatures, derate according to appropriate thermal resistances given under package information.
2. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

PIN CONFIGURATION

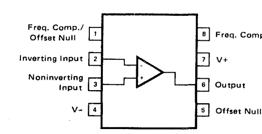
F PACKAGE



T PACKAGE



V PACKAGE

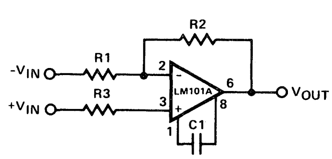


FEATURES

- SHORT CIRCUIT PROTECTION
- OFFSET VOLTAGE NULL CAPABILITY
- LARGE COMMON-MODE AND DIFFERENTIAL VOLTAGE RANGES
- LOW POWER CONSUMPTION
- NO LATCH UP

COMPENSATION CIRCUITS

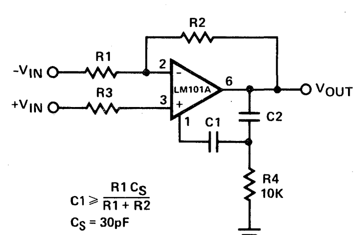
SINGLE POLE COMPENSATION



$C1 \geq \frac{R1\,C_S}{R1 + R2}$

$C_S = 30pF$

TWO POLE COMPENSATION

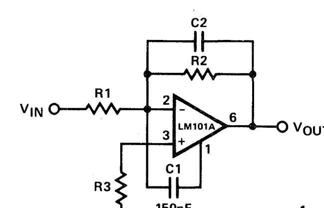


$C1 \geq \frac{R1\,C_S}{R1 + R2}$

$C_S = 30pF$

$C2 = 10\,C1$

FEED FORWARD COMPENSATION

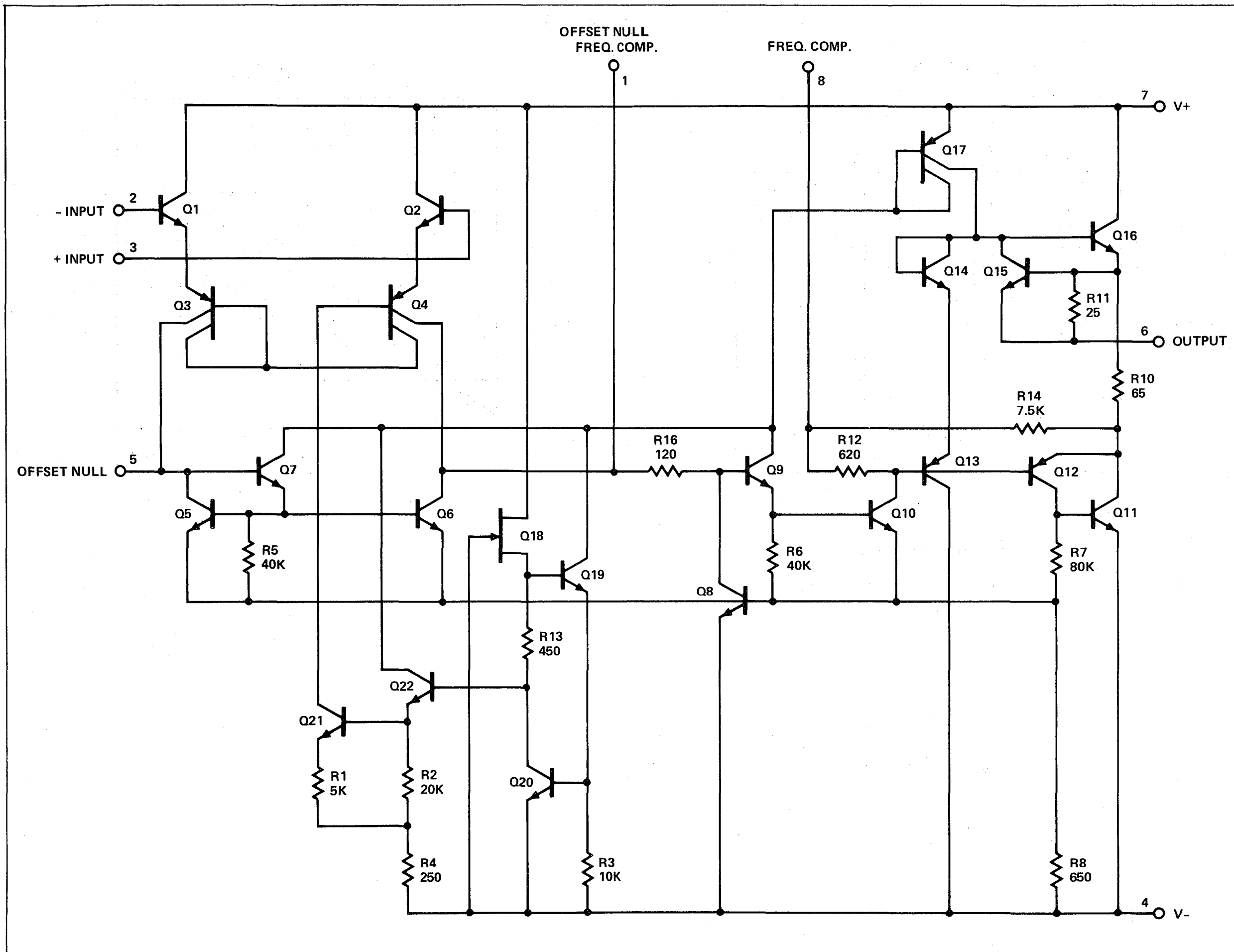


$C2 = \frac{1}{2\pi f_o R2}$

$f_o = 3\,MHz$

NOTE: Pin connections shown are for T Package.

SCHEMATIC DIAGRAM



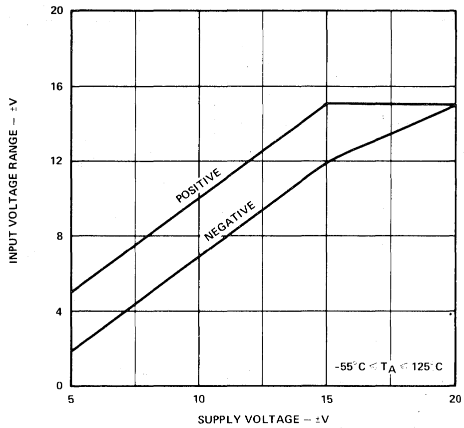
NOTE: Pin numbers for T Package.

ANALOG

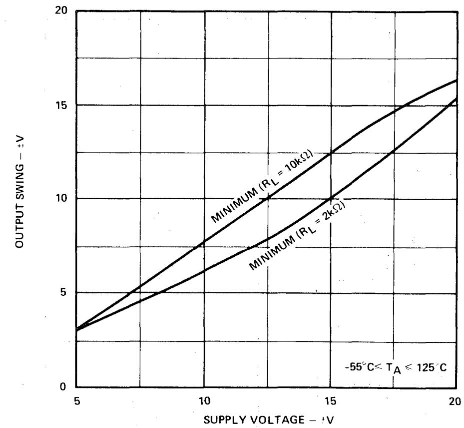
GUARANTEED PERFORMANCE CHARACTERISTICS

LM101A/LM201A

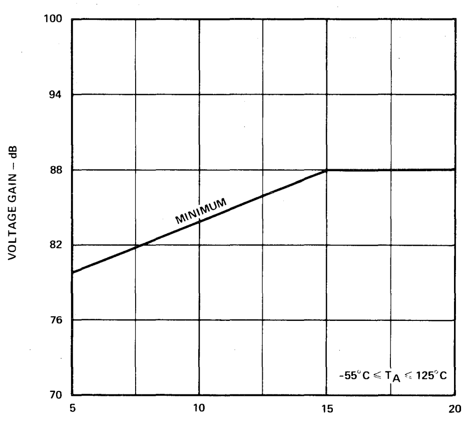
INPUT VOLTAGE RANGE



OUTPUT SWING



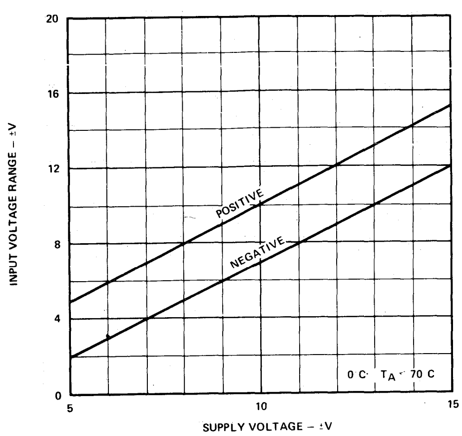
VOLTAGE GAIN



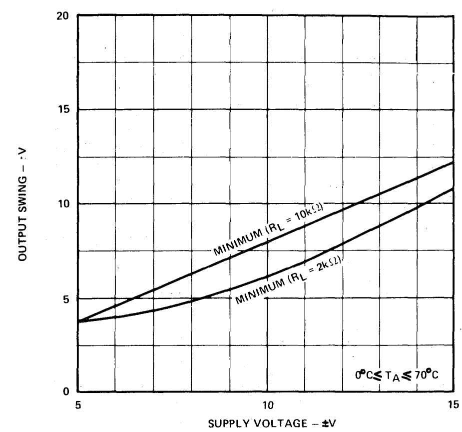
GUARANTEED PERFORMANCE CHARACTERISTICS (Cont'd)

LM301A

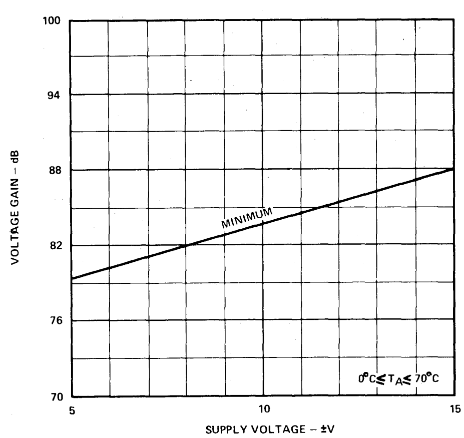
INPUT VOLTAGE RANGE



OUTPUT SWING



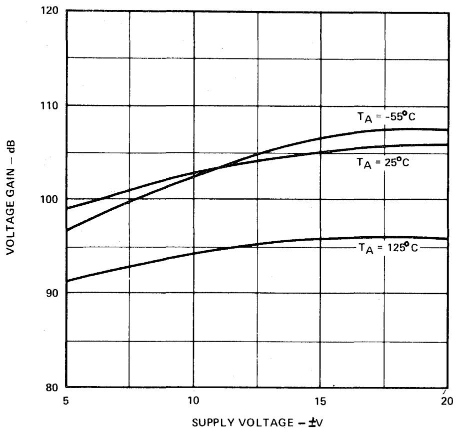
VOLTAGE GAIN



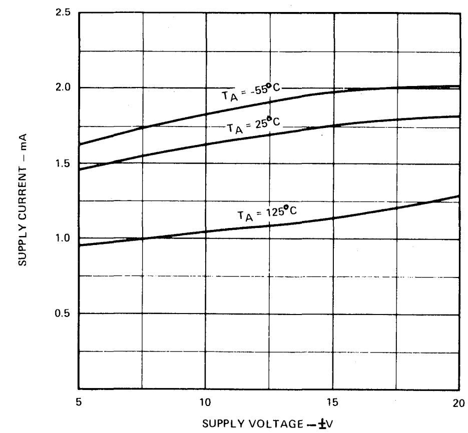
TYPICAL PERFORMANCE CHARACTERISTICS

LM101A/LM201A

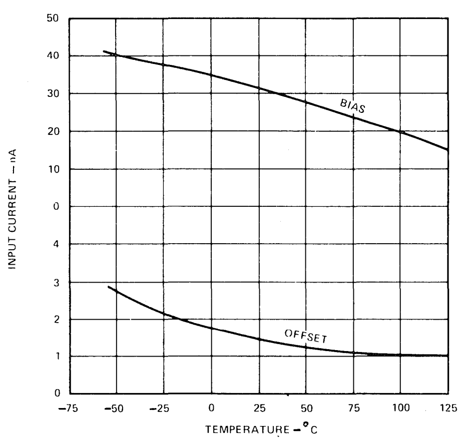
VOLTAGE GAIN



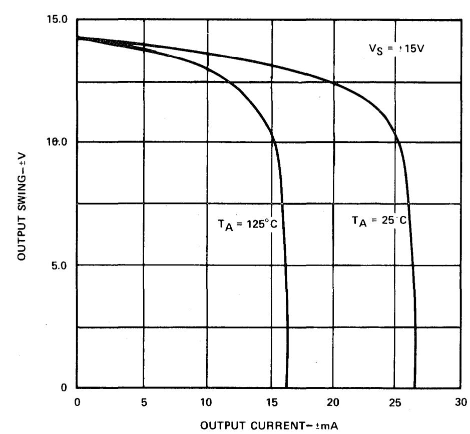
SUPPLY CURRENT



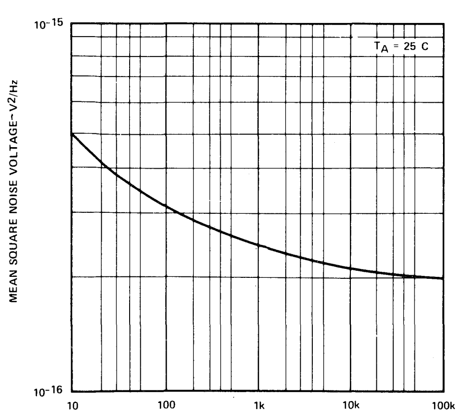
INPUT CURRENT



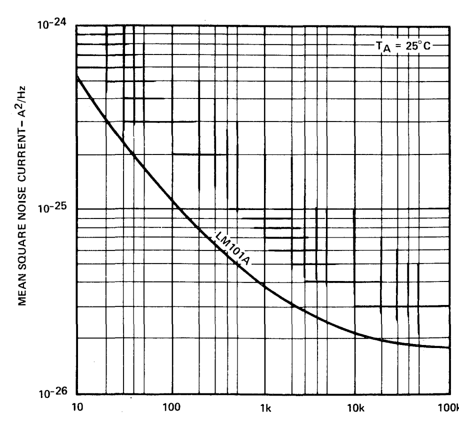
CURRENT LIMITING



INPUT NOISE VOLTAGE



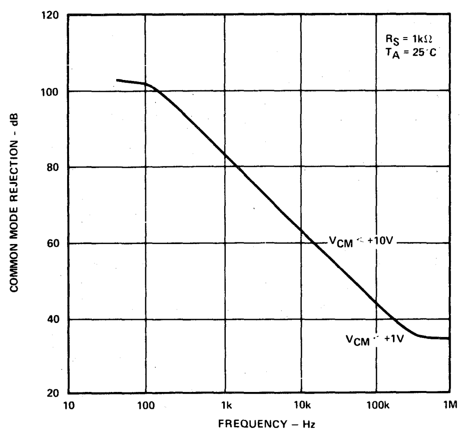
INPUT NOISE CURRENT



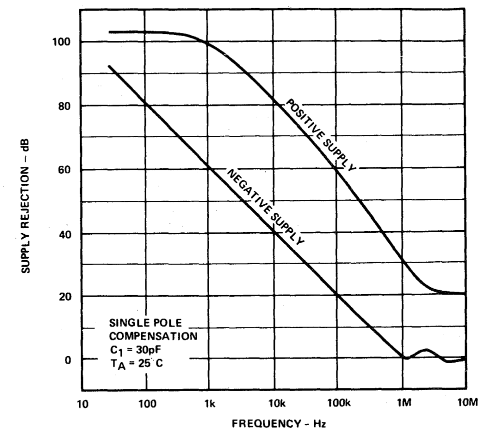
TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

LM101A/LM201A

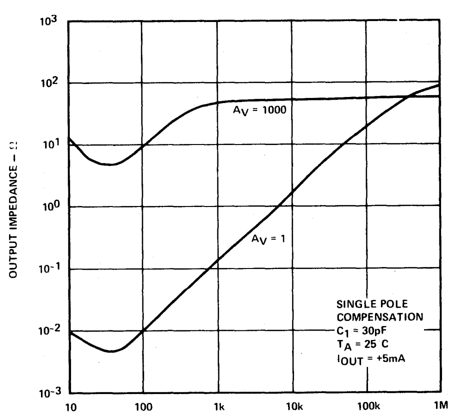
COMMON MODE REJECTION



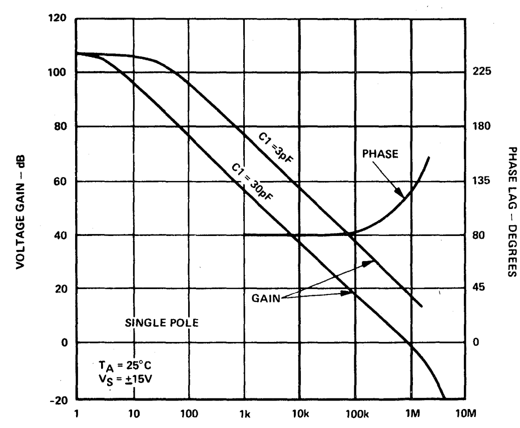
POWER SUPPLY REJECTION



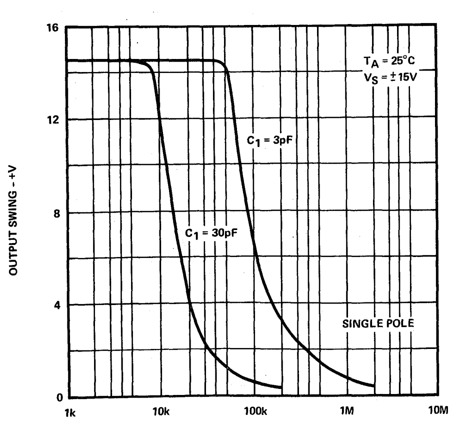
CLOSED LOOP OUTPUT IMPEDANCE



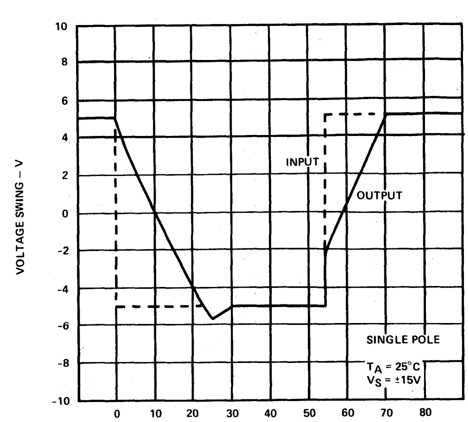
OPEN LOOP FREQUENCY RESPONSE



LARGE SIGNAL FREQUENCY RESPONSE



VOLTAGE FOLLOWER PULSE RESPONSE

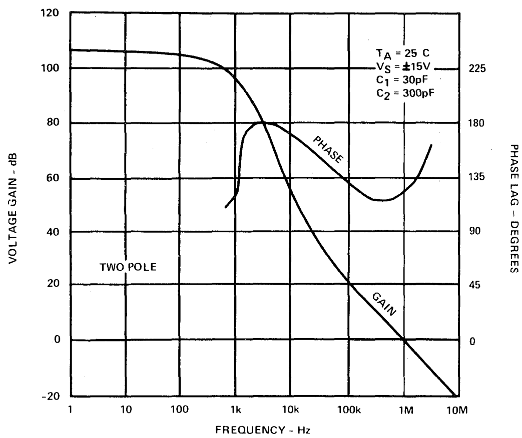


ANALOG

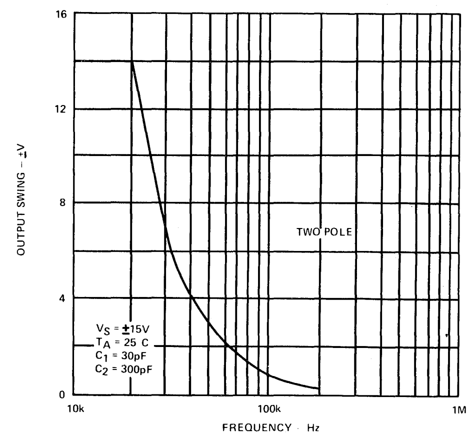
TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

LM101A/LM201A

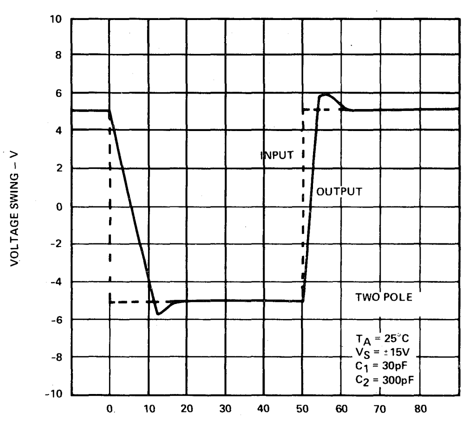
OPEN LOOP FREQUENCY RESPONSE



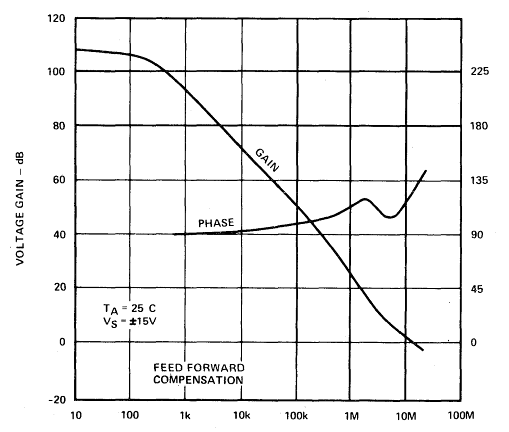
LARGE SIGNAL FREQUENCY RESPONSE



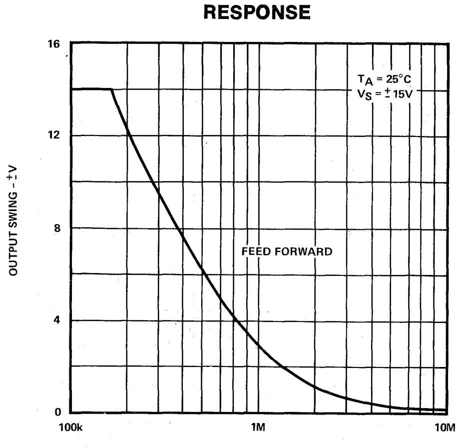
VOLTAGE FOLLOWER PULSE RESPONSE



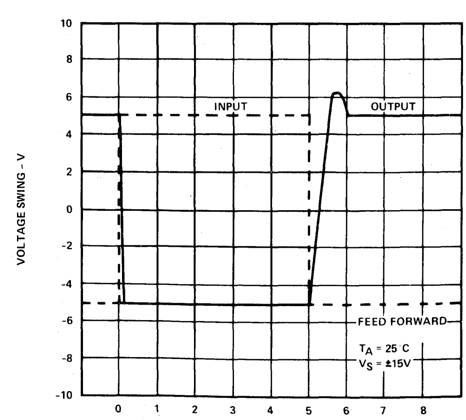
OPEN LOOP FREQUENCY RESPONSE



LARGE SIGNAL FREQUENCY RESPONSE



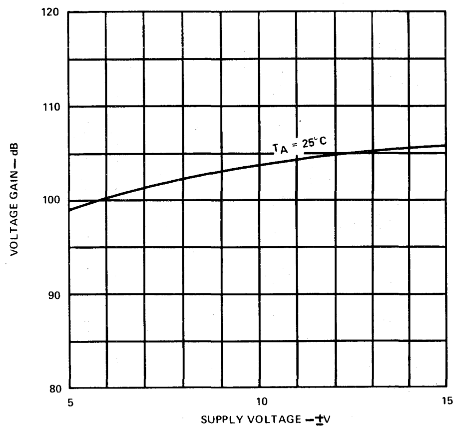
INVERTER PULSE RESPONSE



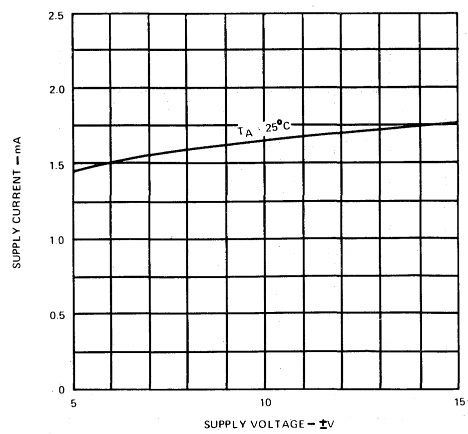
TYPICAL PERFORMANCE CHARACTERISTICS

LM301A

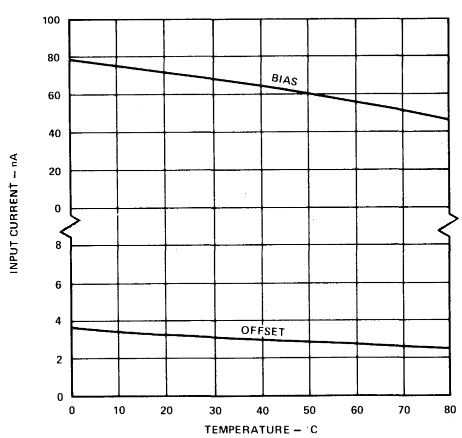
VOLTAGE GAIN



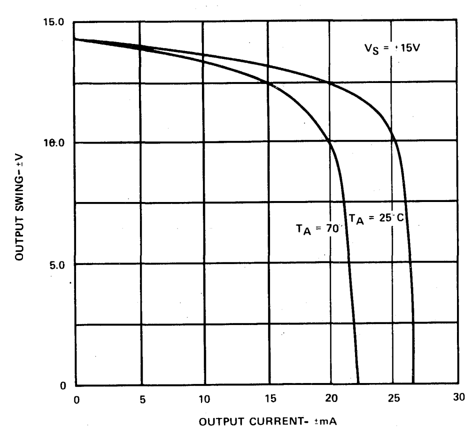
SUPPLY CURRENT



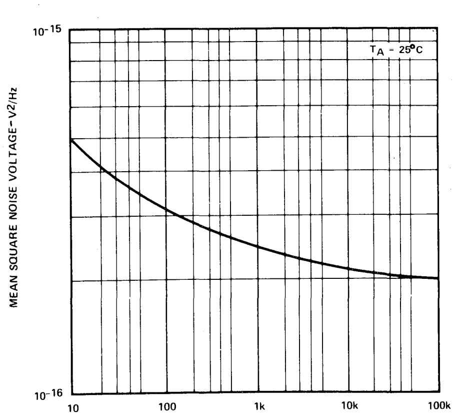
INPUT CURRENT



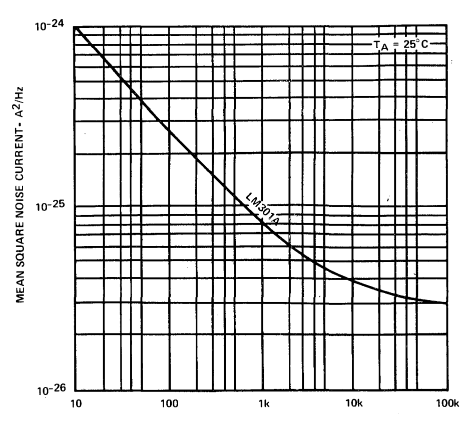
CURRENT LIMITING



INPUT NOISE VOLTAGE



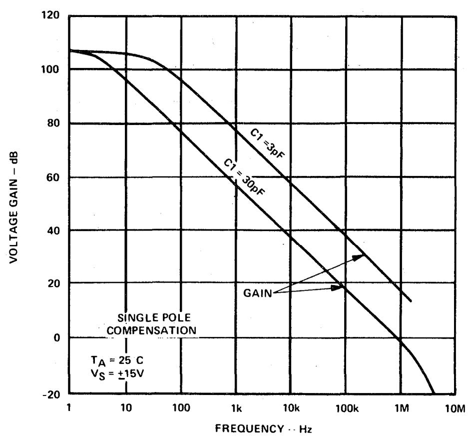
INPUT NOISE CURRENT



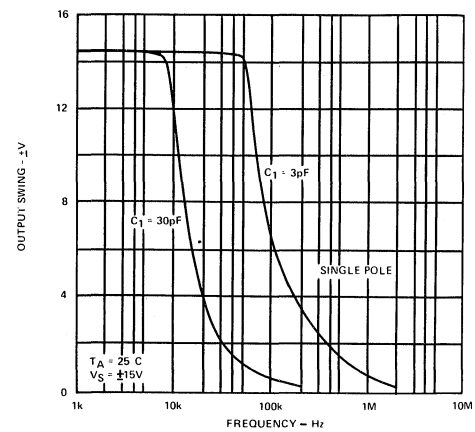
TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

LM301A

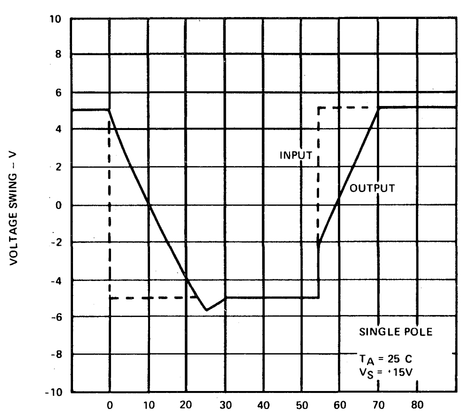
OPEN LOOP FREQUENCY RESPONSE



LARGE SIGNAL FREQUENCY RESPONSE



VOLTAGE FOLLOWER PULSE RESPONSE



FEATURES

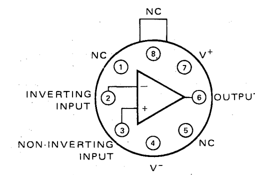
- 3mV MAX OFFSET VOLTAGE OVER TEMP
- 100nA MAX INPUT CURRENT OVER TEMP
- 20nA MAX INPUT OFFSET CURRENT OVER TEMP
- OFFSETS GUARANTEED OVER COMMON MODE RANGE
- INPUT/OUTPUT SHORT CIRCUIT PROTECTED

ABSOLUTE MAXIMUM RATINGS

Supply Voltage LM107	±22V
LM307	±18V
Power Dissipation	500mW
Differential Input Voltage	±30V
Input Voltage	±15V
Output Short Circuit Duration	Indefinite
Operating Temperature Range	
LM107	—55°C to 125°C
LM207	—25°C to 85°C
LM307	0°C to 70°C
Storage Temperature Range	—65°C to 150°C
Lead Temperature (Soldering, 60 sec.)	300°C

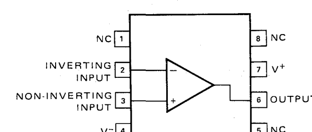
PIN CONFIGURATION

T PACKAGE



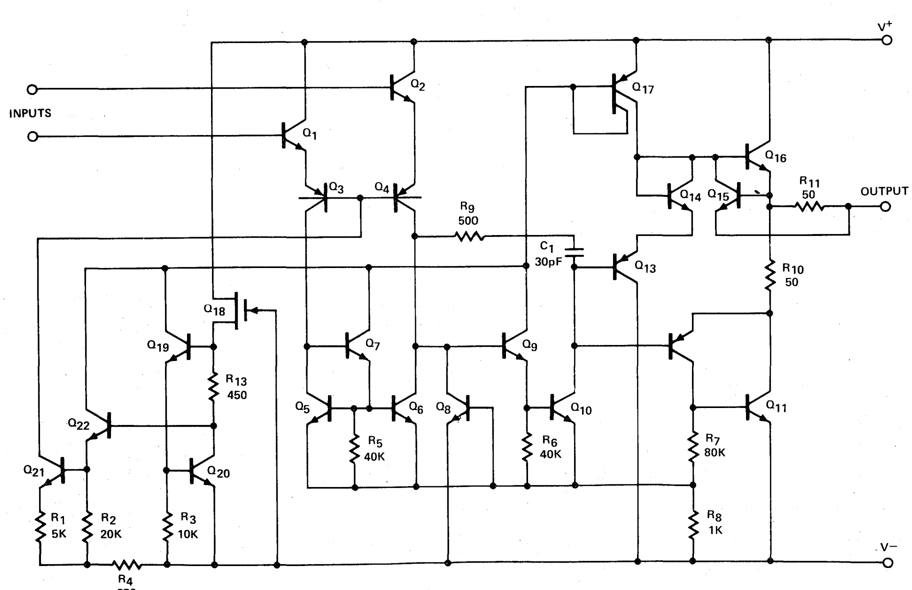
ORDER PART NOS.
LM107T/LM207T/LM307T

V PACKAGE



ORDER PART NOS.
LM107V/LM207V/LM307V

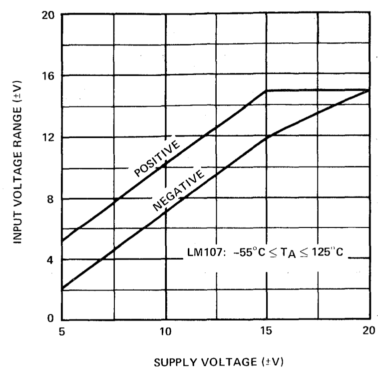
EQUIVALENT SCHEMATIC



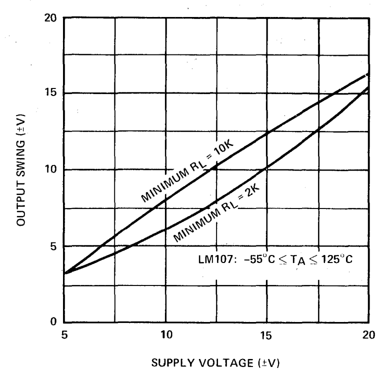
GUARANTEED PERFORMANCE CURVES

LM107/LM207

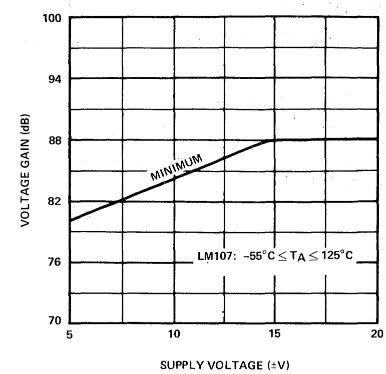
INPUT VOLTAGE RANGE



OUTPUT SWING

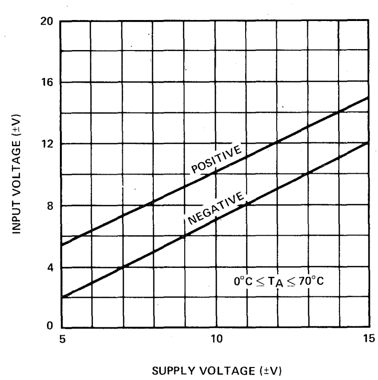


VOLTAGE GAIN

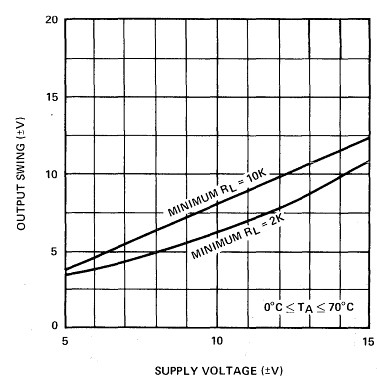


LM307

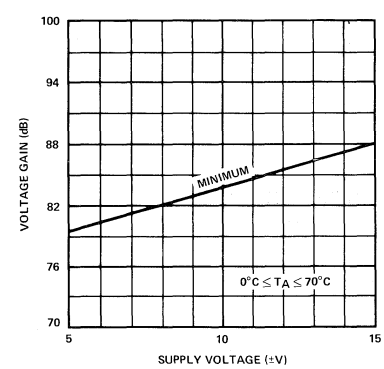
INPUT VOLTAGE RANGE



OUTPUT SWING

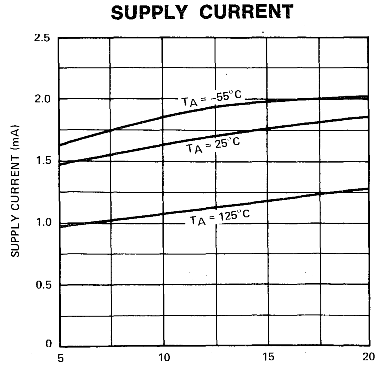


VOLTAGE GAIN

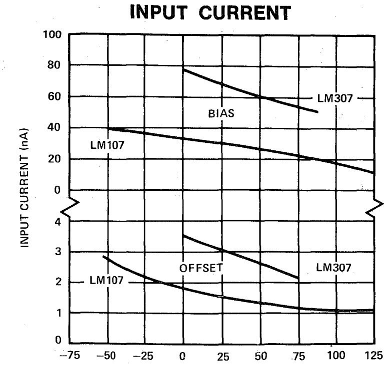


TYPICAL PERFORMANCE CURVES

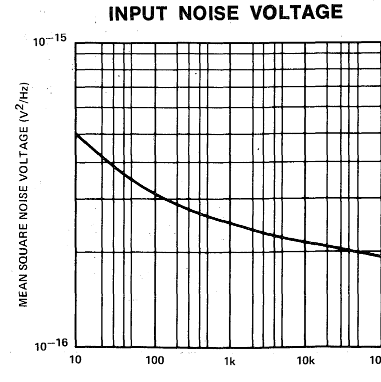
SUPPLY CURRENT



INPUT CURRENT

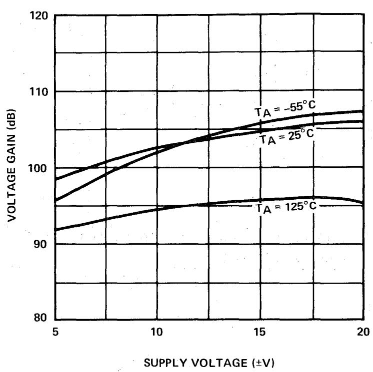


INPUT NOISE VOLTAGE

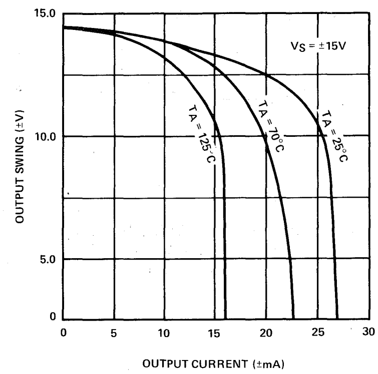


TYPICAL PERFORMANCE CURVES (Cont'd)

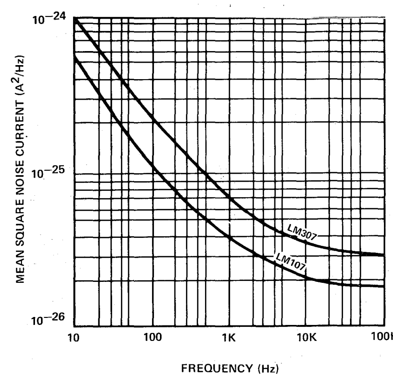
VOLTAGE GAIN



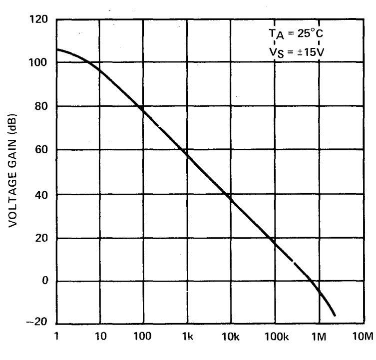
CURRENT LIMITING



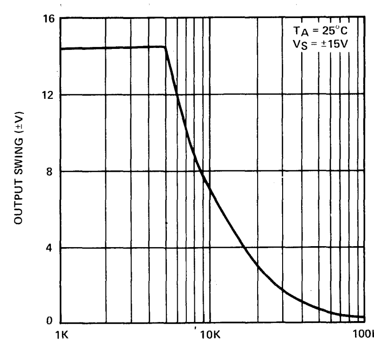
INPUT NOISE CURRENT



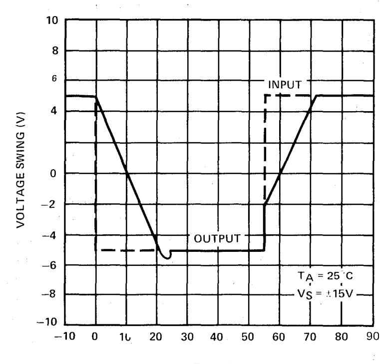
OPEN LOOP FREQUENCY RESPONSE



LARGE SIGNAL FREQUENCY RESPONSE

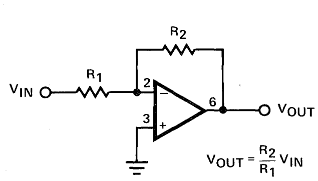


VOLTAGE FOLLOWER PULSE RESPONSE



TYPICAL APPLICATIONS

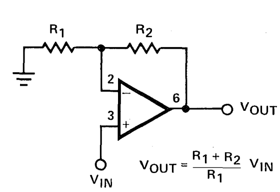
INVERTING AMPLIFIER



$V_{OUT} = \frac{R_2}{R_1} V_{IN}$

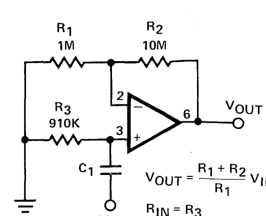
$R_{IN} = R_1$

NON-INVERTING AMPLIFIER



$V_{OUT} = \frac{R_1 + R_2}{R_1} V_{IN}$

NON-INVERTING AC AMPLIFIER



$V_{OUT} = \frac{R_1 + R_2}{R_1} V_{IN}$

$R_{IN} = R_3$

$R_3 = R_1 \parallel R_2$

LM108-F,T • LM208-F,T

FEATURES

- MAXIMUM INPUT BIAS CURRENT OF 3.0nA OVER TEMPERATURE
- OFFSET CURRENT LESS THAN 400pA OVER TEMPERATURE
- SUPPLY CURRENT OF ONLY 300μA, EVEN IN SATURATION
- GUARANTEED DRIFT CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

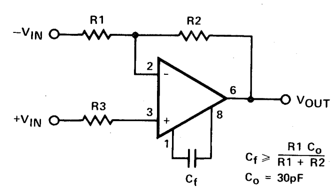
	LM108/LM208
Supply Voltage	±20V
Power Dissipation (Note 1)	500mW
Differential Input Current (Note 2)	±10mA
Input Voltage (Note 3)	±15V
Output Short-Circuit Duration	Indefinite
Operating Temperature Range	
LM108	—55°C to 125°C
LM208	—25°C to 85°C
Storage Temperature Range	—65°C to 150°C
Lead Temperature (Soldering, 60 sec.)	300°C

NOTES:

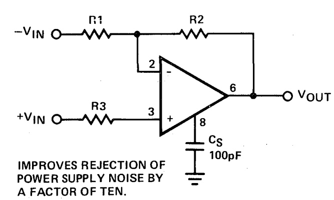
1. The maximum junction temperature of the LM108 is 150°C, while that of the LM208 is 100°C. For operating at elevated temperatures, devices in the TO-5 package must be derated based on a thermal resistance of 150°C/W, junction to ambient, or 45°C/W, junction to case. For the flat package, the derating is based on a thermal resistance of 185°C/W when mounted on a 1/16-inch-thick epoxy glass board with ten, 0.03-inch-wide, 2-ounce copper conductors. The thermal resistance of the dual-in-line package is 100°C/W, junction to ambient.
2. The inputs are shunted with back-to-back diodes for overvoltage protection. Therefore, excessive current will flow if a differential input voltage in excess of 1V is applied between the inputs unless some limiting resistance is used.
3. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

COMPENSATION CIRCUITS

STANDARD COMPENSATION CIRCUIT

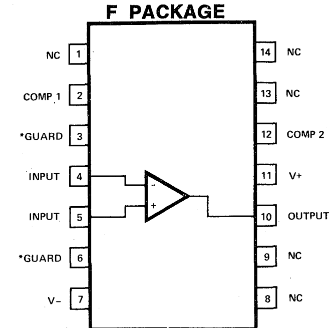


ALTERNATE FREQUENCY COMPENSATION



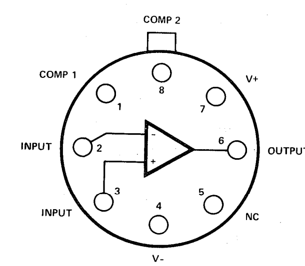
PIN CONFIGURATION

F PACKAGE

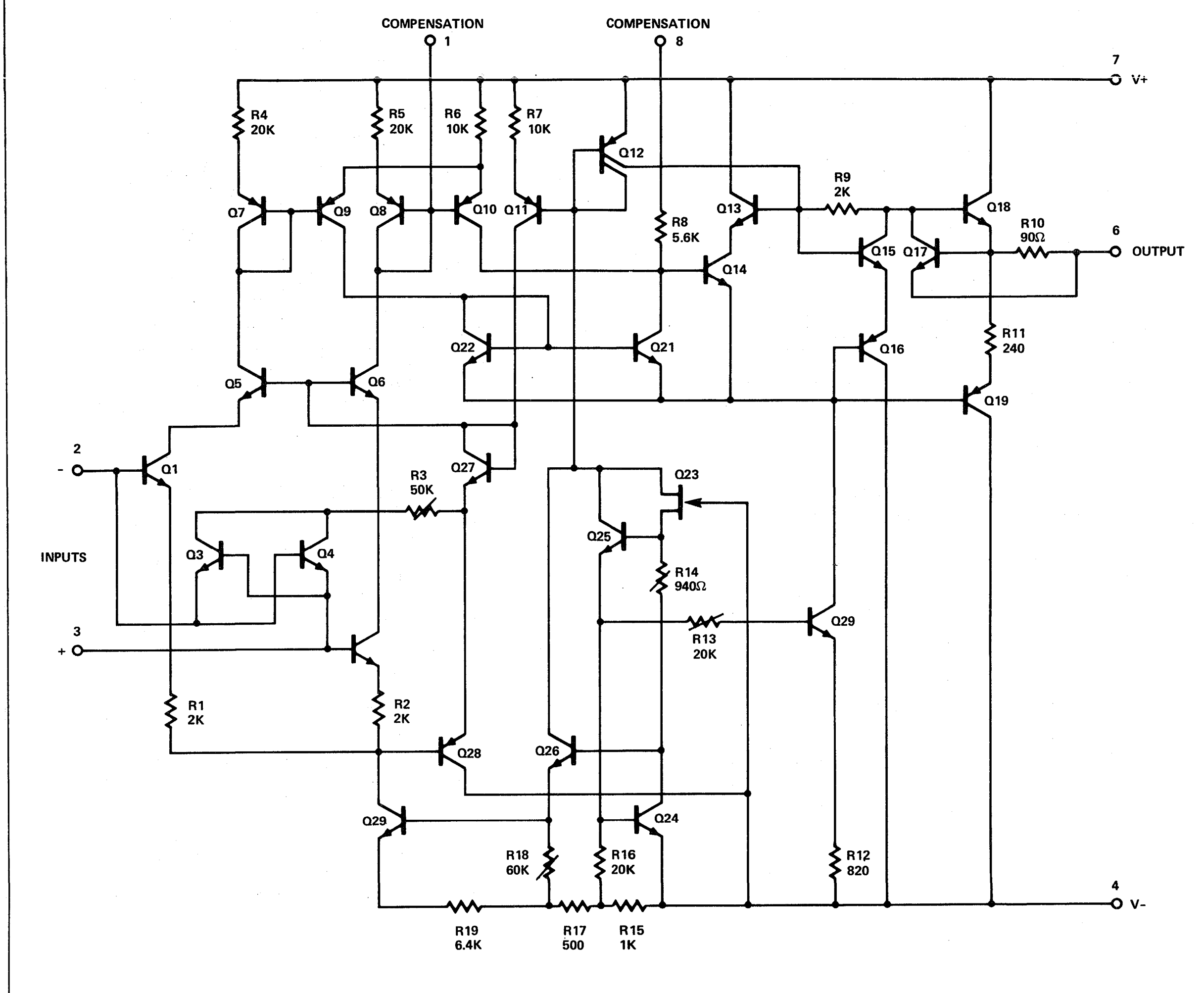


*Unused pin (no internal connection) to allow for input anti-leakage.

T PACKAGE



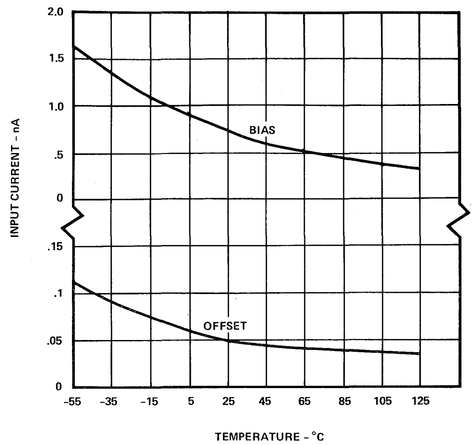
SCHEMATIC DIAGRAM



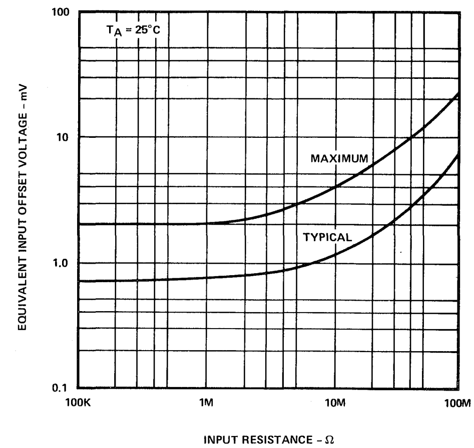
NOTE: Pin numbers for T Package.

TYPICAL CHARACTERISTICS

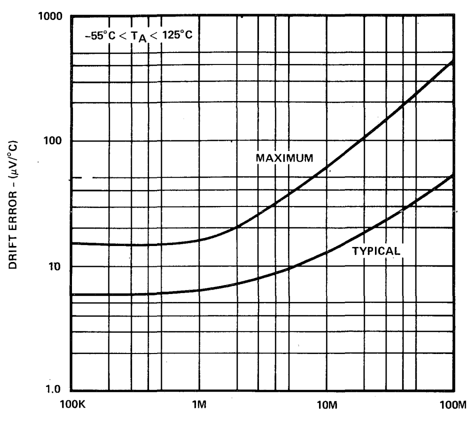
INPUT CURRENTS



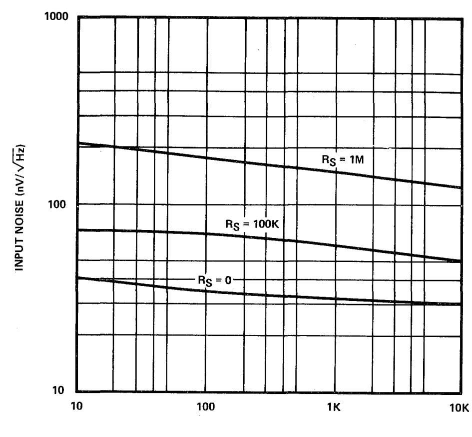
OFFSET ERROR



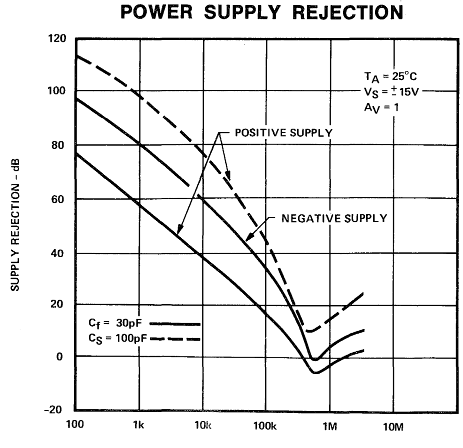
DRIFT ERROR



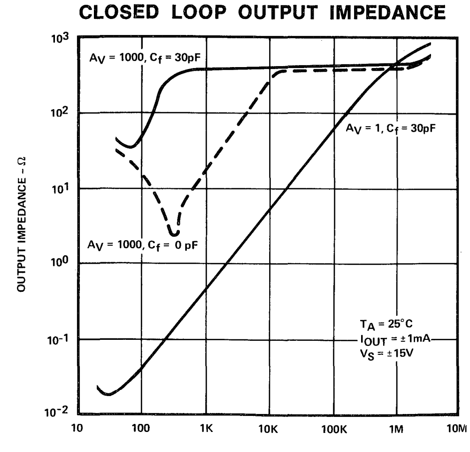
INPUT NOISE VOLTAGE



POWER SUPPLY REJECTION

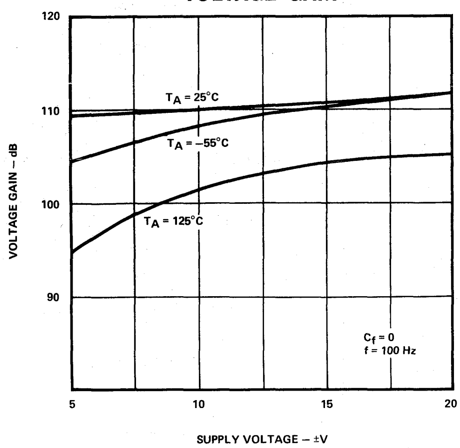


CLOSED LOOP OUTPUT IMPEDANCE

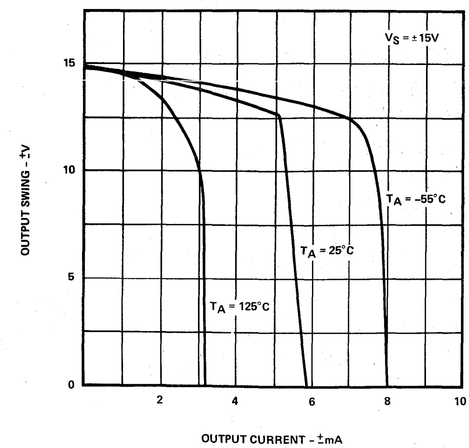


TYPICAL CHARACTERISTICS (Cont'd)

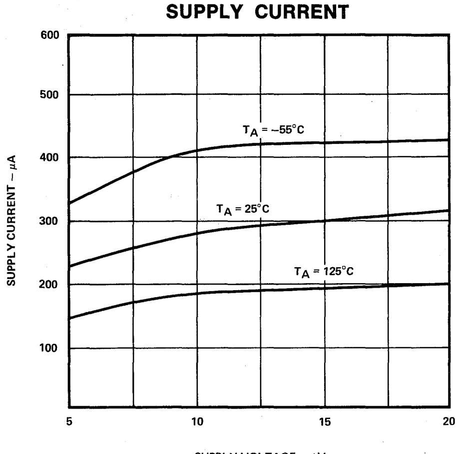
VOLTAGE GAIN



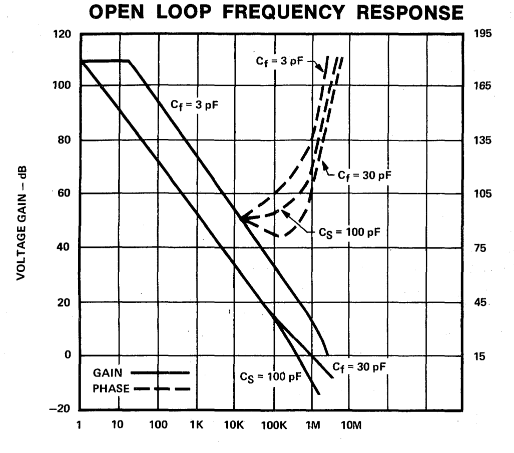
OUTPUT SWING



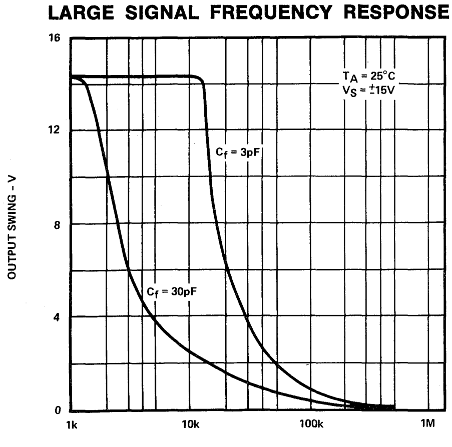
SUPPLY CURRENT



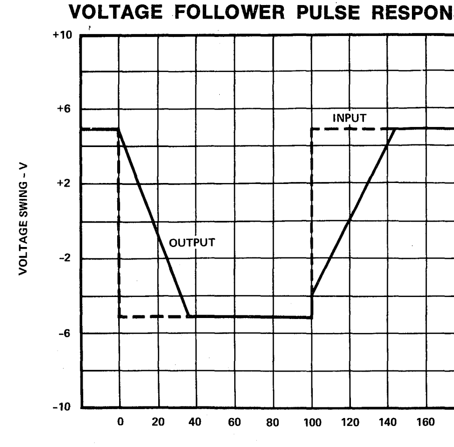
OPEN LOOP FREQUENCY RESPONSE



LARGE SIGNAL FREQUENCY RESPONSE



VOLTAGE FOLLOWER PULSE RESPONSE



LM308-T.V

FEATURES

- **MAXIMUM INPUT BIAS CURRENT OF 7.0nA**
- **OFFSET CURRENT LESS THAN 1.0nA**
- **SUPPLY CURRENT OF ONLY 300μA, EVEN IN SATURATION**
- **GUARANTEED DRIFT CHARACTERISTICS**
- **LOW CURRENT ERROR**

ABSOLUTE MAXIMUM RATINGS

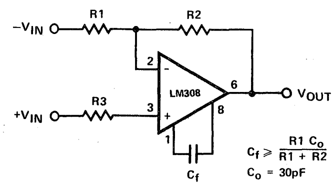
Supply Voltage	±18V
Power Dissipation (Note 1)	500mW
Differential Input Current (Note 2)	±10mA
Input Voltage (Note 3)	±15V
Output Short Circuit Duration	Indefinite
Operating Temperature Range	0°C to 70°C
Storage Temperature Range	—65°C to 150°C
Lead Temperature (Soldering, 60 sec.)	300°C

NOTES:

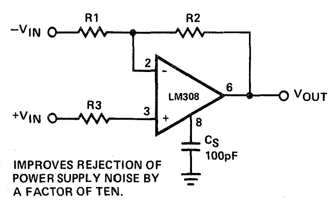
1. The maximum junction temperature of the LM308 is 85°C. For operation at elevated temperatures, devices in the TO-5 package must be derated based on a thermal resistance of 150°C/W, junction to ambient, or 45°C/W, junction to case. The thermal resistance of the dual-in-line package is 100°C/W, junction to ambient.
2. The inputs are shunted with back-to-back diodes for overvoltage protection. Therefore, excessive current will flow if a differential input voltage in excess of 1V is applied between the inputs unless some limiting resistance is used.
3. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

COMPENSATION CIRCUITS

STANDARD COMPENSATION CIRCUIT

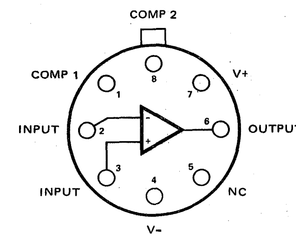


ALTERNATE FREQUENCY COMPENSATION

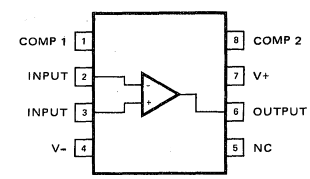


PIN CONFIGURATION

T PACKAGE

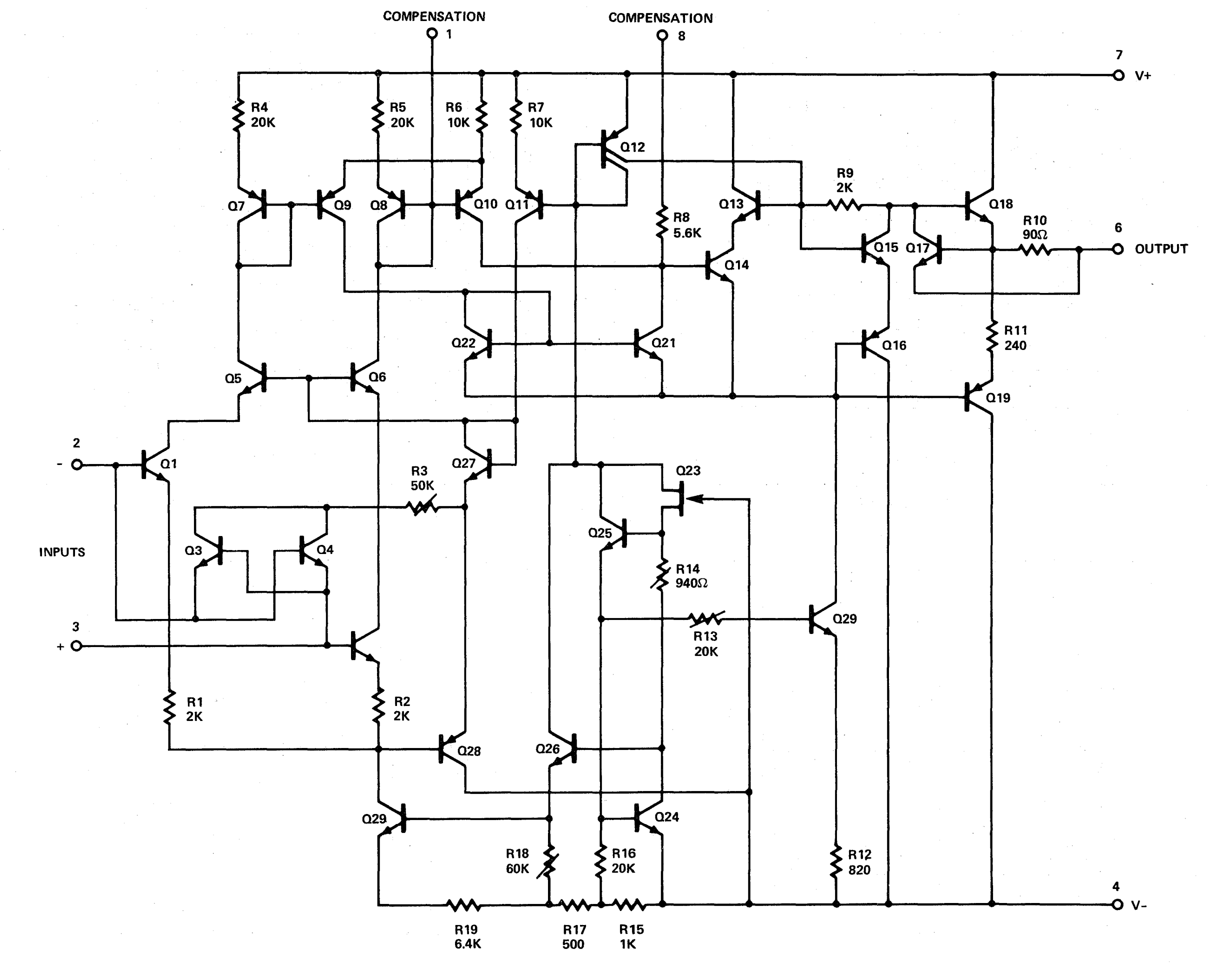


V PACKAGE



LM308-T.V

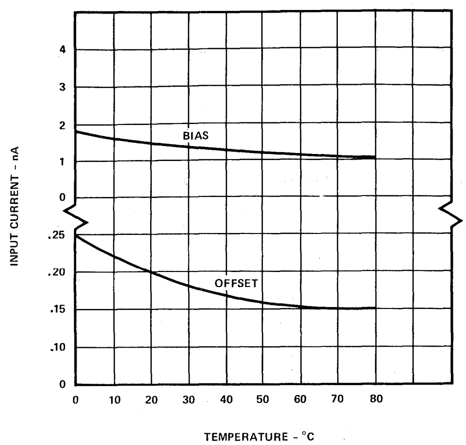
SCHEMATIC DIAGRAM



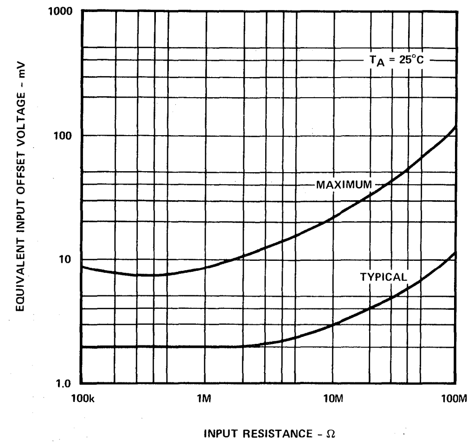
NOTE: Pin numbers for T Package.

TYPICAL PERFORMANCE CHARACTERISTICS

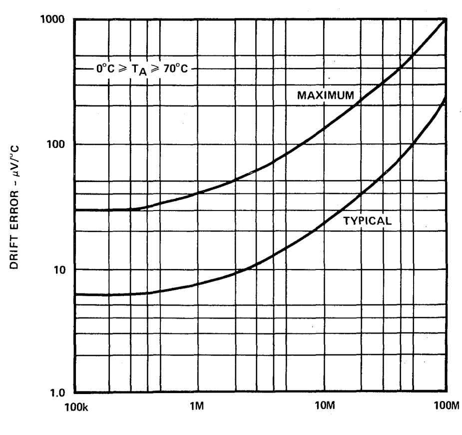
INPUT CURRENTS



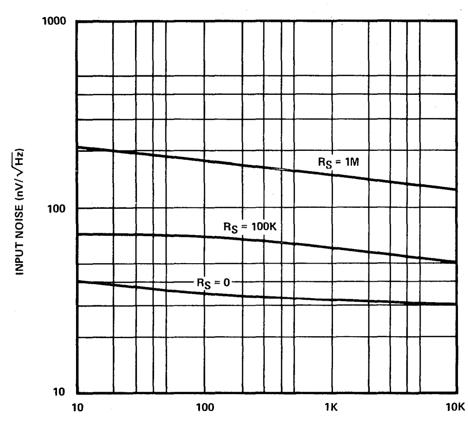
OFFSET ERROR



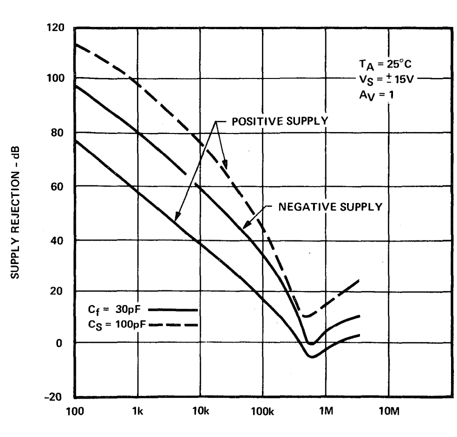
DRIFT ERROR



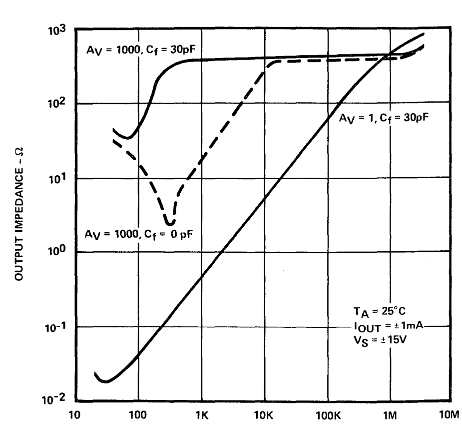
INPUT NOISE VOLTAGE



POWER SUPPLY REJECTION

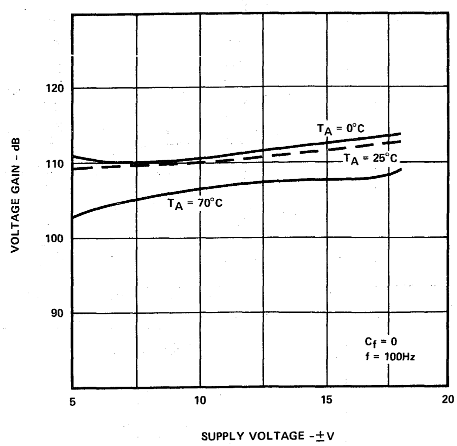


CLOSED LOOP OUTPUT IMPEDANCE

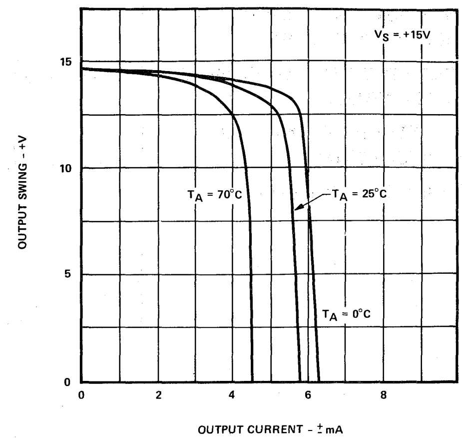


TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

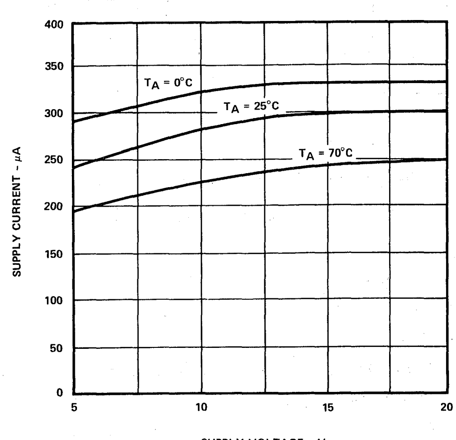
VOLTAGE GAIN



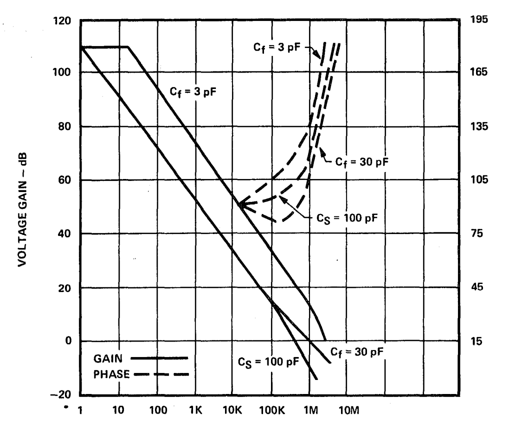
OUTPUT SWING



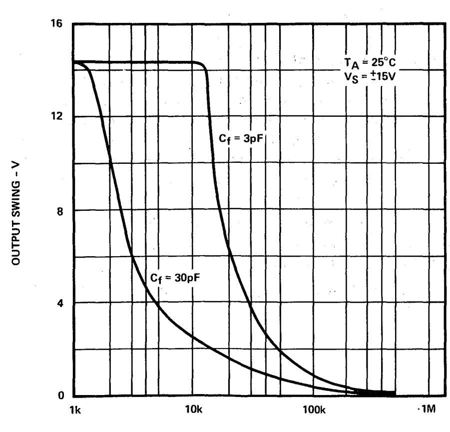
SUPPLY CURRENT



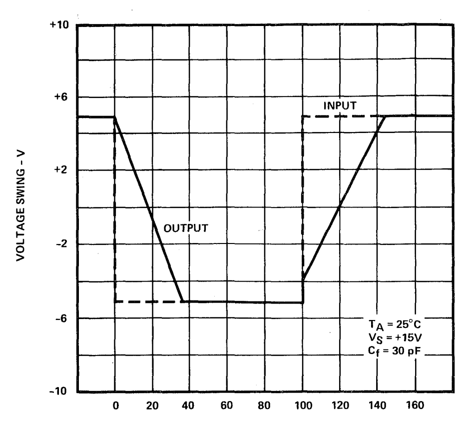
OPEN LOOP FREQUENCY RESPONSE



LARGE SIGNAL FREQUENCY RESPONSE



VOLTAGE FOLLOWER PULSE RESPONSE



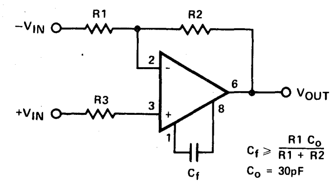
LM108A-F,T • LM208A-F,T • LM308A-F,T

FEATURES

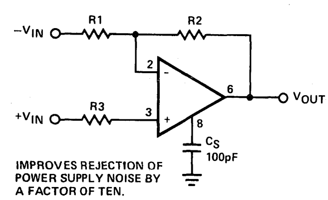
- OFFSET VOLTAGE GUARANTEED LESS THAN 0.5mV
- MAXIMUM INPUT BIAS CURRENT OF 3.0nA OVER TEMPERATURE
- OFFSET CURRENT LESS THAN 400pA OVER TEMPERATURE
- SUPPLY CURRENT OF ONLY 300μA, EVEN IN SATURATION
- GUARANTEED 5μV/°C DRIFT

COMPENSATION CIRCUITS

STANDARD COMPENSATION CIRCUIT

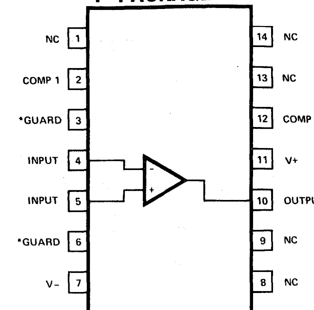


ALTERNATE FREQUENCY COMPENSATION



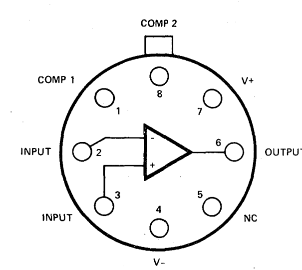
PIN CONFIGURATION

F PACKAGE



•Unused pin (no internal connection) to allow for input anti-leakage.

T PACKAGE



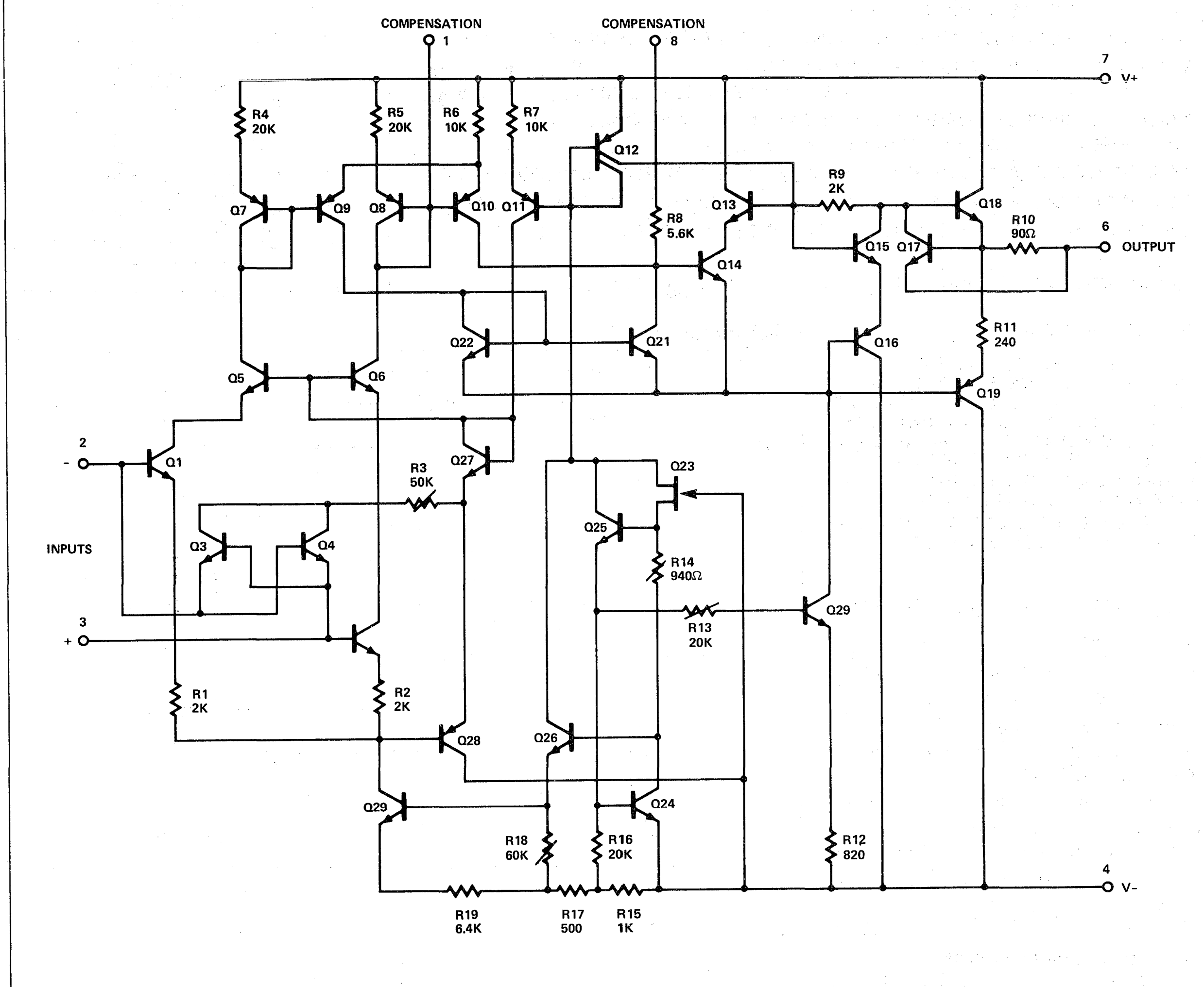
ABSOLUTE MAXIMUM RATINGS

	LM108A, LM208A	LM308A
Supply Voltage	±20V	±18V
Power Dissipation (Note 1)	500mW	500mW
Differential Input Current (Note 2)	±10mA	±10mA
Input Voltage (Note 3)	±15V	±15V
Output Short Circuit Duration	Indefinite	Indefinite
Operating Temperature Range		
LM108A	—55°C to 125°C	
LM208A	—25°C to 85°C	0°C to 70°C
Storage Temperature Range	—65°C to 150°C	—65°C to 150°C
Lead Temperature (Soldering, 10 sec.)	300°C	300°C

NOTES:

1. The maximum junction temperature of the LM108A is 150°C, while that of the LM208A is 100°C. For operating at elevated temperatures, devices in the TO-5 package must be derated based on a thermal resistance of 150°C/W, junction to ambient, or 45°C/W, junction to case. For the flat package, the derating is based on a thermal resistance of 185°C/W when mounted on a 1/16-inch-thick epoxy glass board with ten, 0.03-inch-wide, 2-ounce copper conductors. The thermal resistance of the dual-in-line package is 100°C/W, junction to ambient.
2. The inputs are shunted with back-to-back diodes for overvoltage protection. Therefore, excessive current will flow if a differential input voltage in excess of 1V is applied between the inputs unless some limiting resistance is used.
3. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

SCHEMATIC DIAGRAM



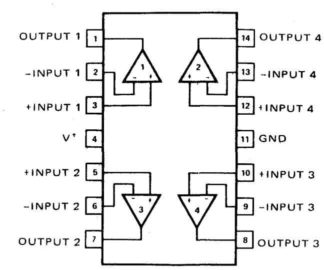
LM124-F • LM224-A,F • LM324-A,F

FEATURES

- INTERNALLY FREQUENCY COMPENSATED FOR UNITY GAIN
- LARGE DC VOLTAGE GAIN — 100dB
- WIDE BANDWIDTH (UNITY GAIN) — 1MHz (TEMPERATURE COMPENSATED)
- WIDE POWER SUPPLY RANGE: SINGLE SUPPLY $3V_{DC}$ to $30V_{DC}$ OR DUAL SUPPLIES $\pm1.5V_{DC}$ to $\pm15V_{DC}$
- VERY LOW SUPPLY CURRENT DRAIN (800μA) — ESSENTIALLY INDEPENDENT OF SUPPLY VOLTAGE (1mW/op amp at $+5V_{DC}$)
- LOW INPUT BIASING CURRENT — $45nA_{DC}$ (TEMPERATURE COMPENSATED)
- LOW INPUT OFFSET VOLTAGE — $2mV_{DC}$ AND OFFSET CURRENT — $5nA_{DC}$
- DIFFERENTIAL INPUT VOLTAGE RANGE EQUAL TO THE POWER SUPPLY VOLTAGE
- LARGE OUTPUT VOLTAGE — $0V_{DC}$ to V+ —$1.5V_{DC}$ SWING

PIN CONFIGURATION

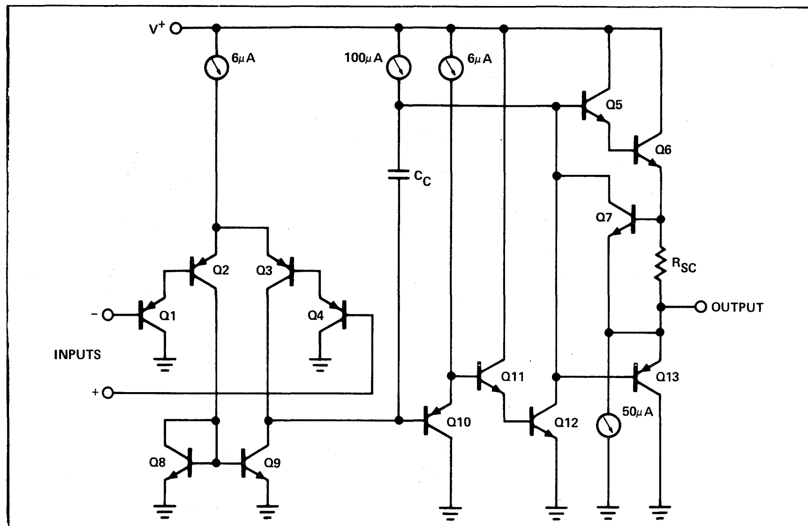
A, F PACKAGE



UNIQUE FEATURES

IN THE LINEAR MODE THE INPUT COMMON-MODE VOLTAGE RANGE INCLUDES GROUND AND THE OUTPUT VOLTAGE CAN ALSO SWING TO GROUND, EVEN THOUGH OPERATED FROM ONLY A SINGLE POWER SUPPLY VOLTAGE.
THE UNITY GAIN CROSS FREQUENCY IS TEMPERATURE COMPENSATED.
THE INPUT BIAS CURRENT IS ALSO TEMPERATURE COMPENSATED.

EQUIVALENT CIRCUIT



ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V+	$32V_{DC}$ or $\pm16V_{DC}$
Differential Input Voltage	$32V_{DC}$
Input Voltage	$-0.3V_{DC}$ to $+32V_{DC}$
Power Dissipation (Note 1)	
Molded DIP (LM224A, LM324A)	570mW
Cavity DIP (LM124F, LM224F, and LM324F)	900mW
Output Short-Circuit to GND	
1 Amplifier (Note 2)	Continuous
V+ < $15V_{DC}$ and $T_A = 25°C$	
Input Current ($V_{IN} < -0.3V$) (Note 3)	50mA
Operating Temperature Range	
LM324	0°C to +70°C
LM224	—25°C to +85°C
LM124	—55°C to +125°C
Storage Temperature Range	—65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	300°C

NOTES:

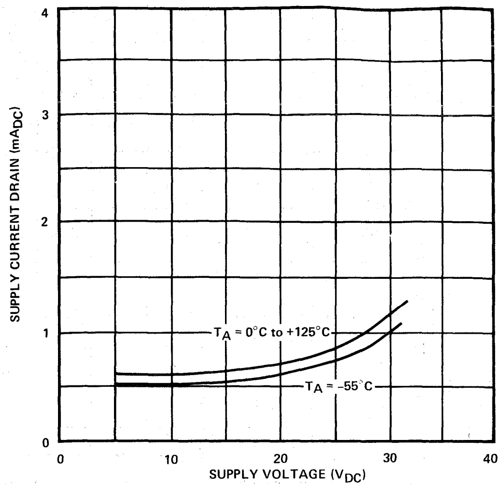
1. For operating at high temperatures, the LM324 must be derated based on a +125°C maximum junction temperature and a thermal resistance of 175°C/W which applies for the device soldered in a printed circuit board, operating in a still air ambient. The LM224 and LM124 can be derated based on a +150°C maximum junction temperature.
2. Short circuits from the output to V+ can cause excessive heating and eventual destruction. The maximum output current is approximately 40 mA independent of the magnitude of V+. At values of supply voltage in excess of $+15V_{DC}$, continuous short-circuits can exceed the power dissipation ratings and cause eventual destruction.
3. The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the input lines.

ELECTRICAL CHARACTERISTICS

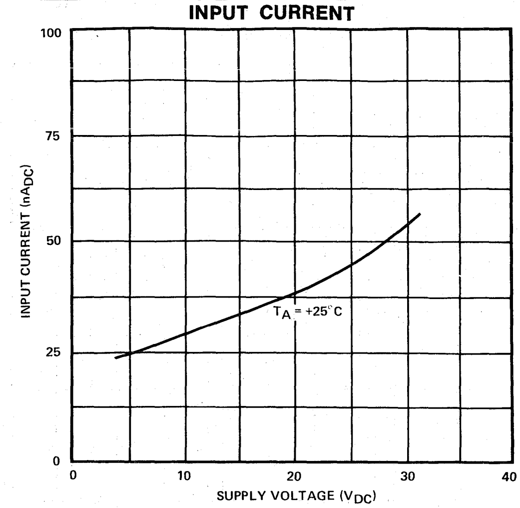
Parameter	Test Conditions	LIMITS Min	Typ	Max	Units
Amplifier-to-Amplifier Coupling	f=1kHz to 20kHz, $T_A=+25°C$ (input Referred)		-120		dB
Output Current Source	$V_{IN}+=1V_{DC}$, $V_{IN}-=0V_{DC}$, $V+=15V_{DC}$, $T_A=+25°C$	20	40		mA_{DC}
	$V_{IN}+=+1V_{DC}$, $V_{IN}-=0V_{DC}$ $V+=15V_{DC}$	10	20		mA
Output Current Sink	$V_{IN}-=+1V_{DC}$, $V_{IN}+=0V_{DC}$ $V+=15V_{DC}$, $TA=+25°C$	10	20		mA_{DC}
	$V_{IN}-=+1V_{DC}$, $V_{IN}+=0V_{DC}$ $T_A=+25°C$, $V_O=200mV_{DC}$	12	50		μA_{DC}
	$V_{IN}-=+1V_{DC}$, $V_{IN}+=0V_{DC}$ $V+=15V_{DC}$	5	8		mA
Differential Input Voltage	See Note 5				

TYPICAL PERFORMANCE CURVES

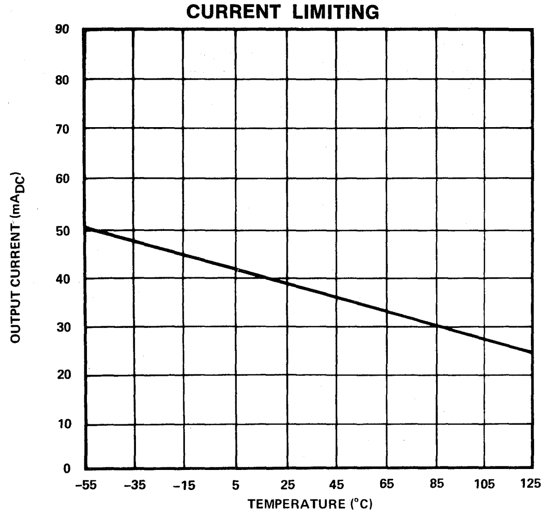
SUPPLY CURRENT



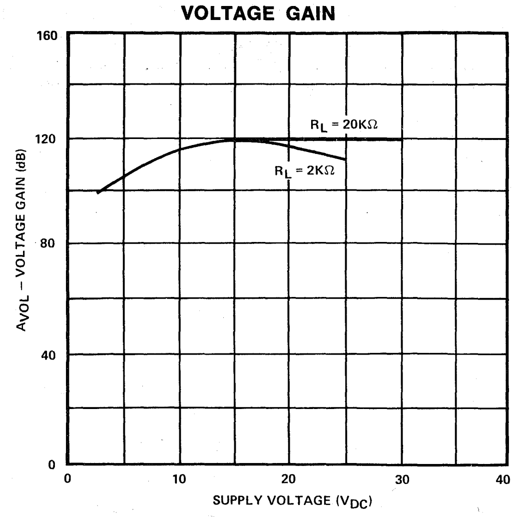
INPUT CURRENT



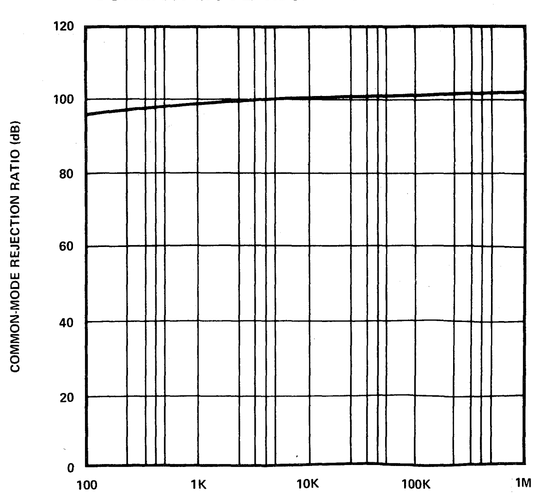
CURRENT LIMITING



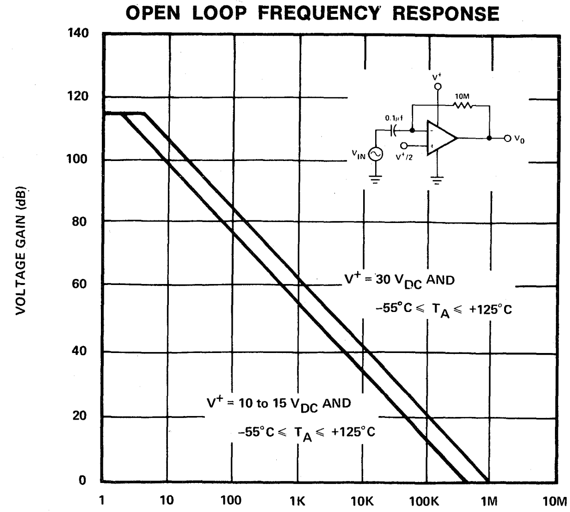
VOLTAGE GAIN



COMMON-MODE REJECTION RATIO



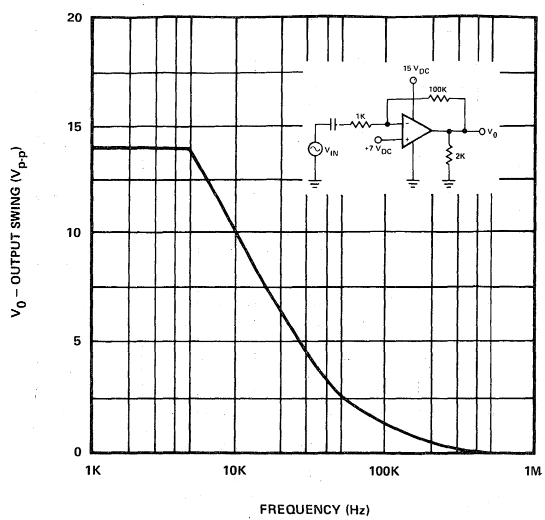
OPEN LOOP FREQUENCY RESPONSE



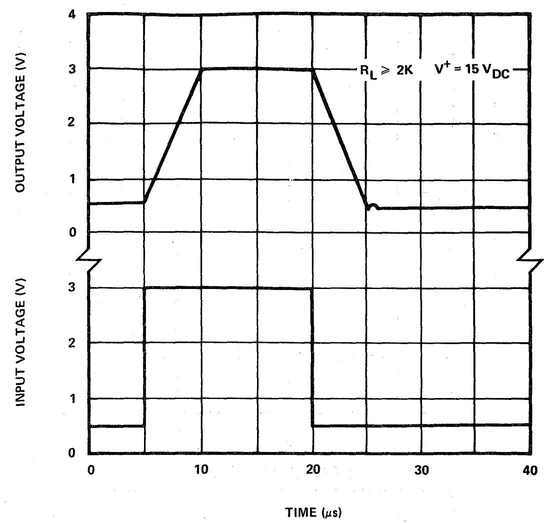
ANALOG

TYPICAL PERFORMANCE CURVES (Cont'd)

LARGE SIGNAL FREQUENCY RESPONSE



VOLTAGE FOLLOWER PULSE RESPONSE



MC1456-T.V • MC1556-T.V

FEATURES

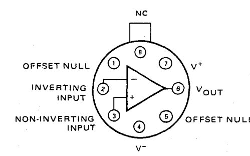
- LOW INPUT BIAS CURRENT — 15nA MAXIMUM
- LOW INPUT OFFSET CURRENT — 2.0nA MAXIMUM
- LOW INPUT OFFSET VOLTAGE — 4.0mV MAXIMUM
- HIGH SLEW RATE — 2.5V/μs TYPICAL
- LARGE POWER BANDWIDTH — 40kHz TYPICAL
- LOW POWER CONSUMPTION — 45mW MAXIMUM
- OFFSET VOLTAGE NULL CAPABILITY

ABSOLUTE MAXIMUM RATINGS

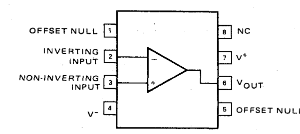
Power Supply Voltage MC1556	±22V
MC1456	±18V
Differential Input Voltage	±V
Common Mode Input Voltage	±V
Load Current	20mA
Output Short Circuit Duration	Indefinite
Power Dissipation	680mW
Derate Above $T_A = 25°C$	4.6mW/°C
Operating Temperature Range	
MC1556	−55°C to +125°C
MC1456	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

PIN CONFIGURATION

T PACKAGE



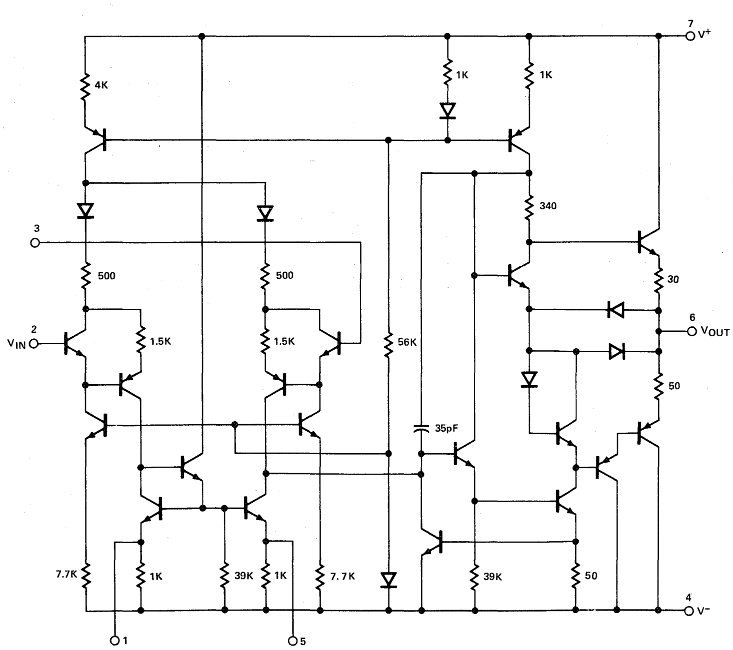
V PACKAGE



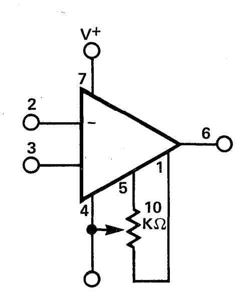
ELECTRICAL CHARACTERISTICS

Parameter	Test Conditions	MC1456 Min	MC1456 Typ	MC1456 Max	MC1556 Min	MC1556 Typ	MC1556 Max	Units
Parallel Input Capacitance			6.0			6.0		pF
Common Mode Input Impedance	f=20Hz		250			250		meg Ω
Equivalent Input Noise Voltage	$A_V=100$, $R_S=10K\Omega$, F=1.0kHz,, BW=1.0Hz		45			45		nV/√Hz
Power Bandwidth	$A_V=1$, $R_L=2K\Omega$, THD<5%, $V_{OUT}=\pm10V$		40			40		kHz
Phase Margin			70			70		degrees
Gain Margin			18			18		dB
Slew Rate			2.5			2.5		V/μsec
Output Impedance	f=20Hz		1.0	2.5		1.0	2.0	kΩ

EQUIVALENT CIRCUIT

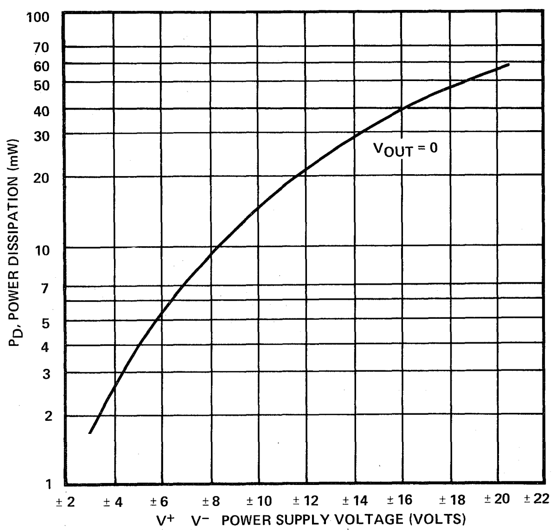


OFFSET ADJUST CIRCUIT

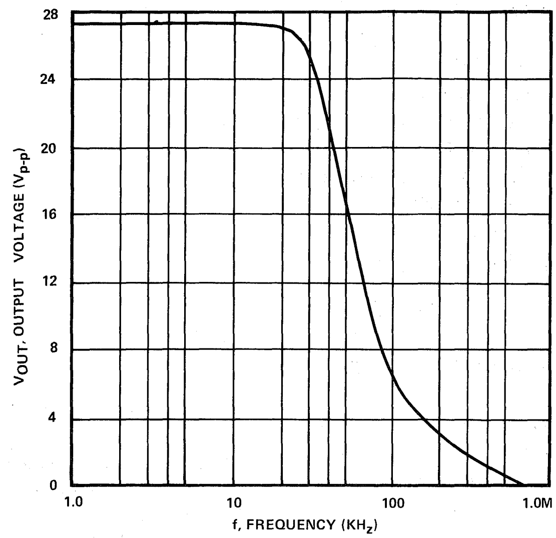


TYPICAL PERFORMANCE CHARACTERISTICS

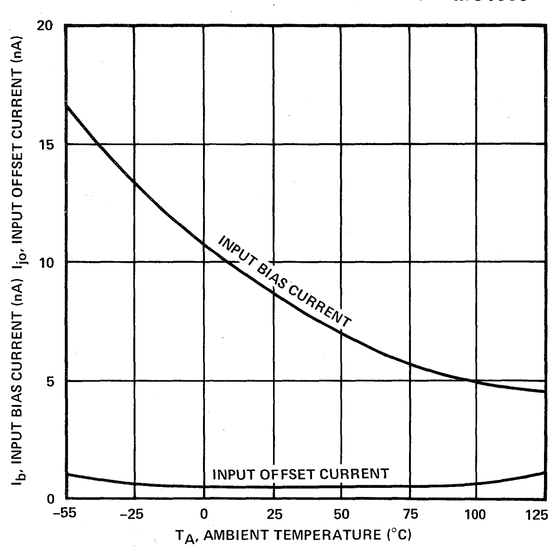
POWER DISSIPATION VERSUS POWER SUPPLY VOLTAGE



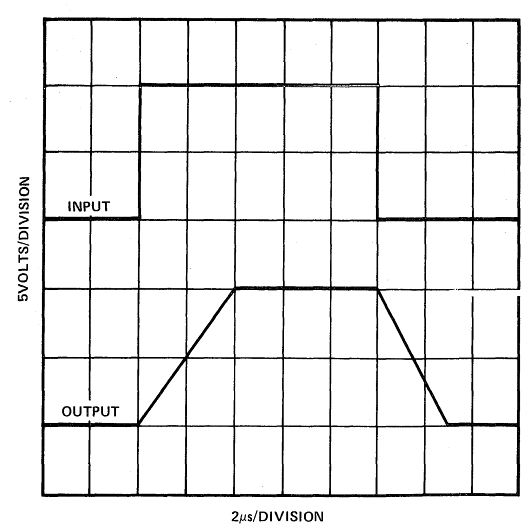
POWER BANDWIDTH



TYPICAL INPUT BIAS CURRENT AND INPUT OFFSET CURRENT VERSUS TEMPERATURE FOR MC1556



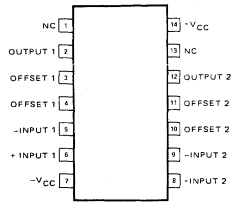
VOLTAGE FOLLOWER PULSE RESPONSE



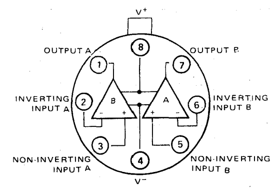
MC1458-A,F,T,V • MC1558-A,F,T,V

PIN CONFIGURATION

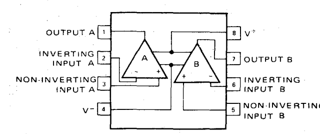
A, F PACKAGE



T PACKAGE



V PACKAGE



FEATURES

- 2 "OP AMPS" IN SPACE OF ONE 741 V PACKAGE
- NO FREQUENCY COMPENSATION REQUIRED
- SHORT CIRCUIT PROTECTION
- LOW POWER CONSUMPTION
- LARGE COMMON MODE AND DIFFERENTIAL VOLTAGE RANGES
- NO LATCH-UP

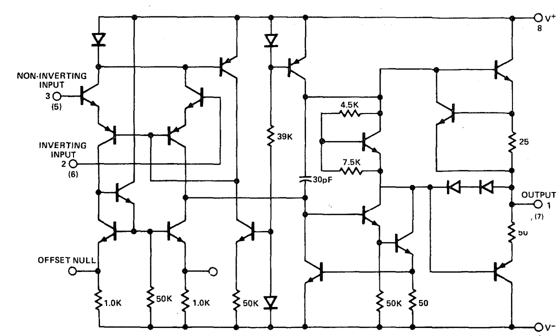
ABSOLUTE MAXIMUM RATINGS

Power Supply Voltages	MC1558	±22V
	MC1458	±18V
Differential Input Voltage		±30V
Common Mode Input Swing		±15V
Output Short Circuit Duration		Continuous
Power Dissipation (Note 1)		
T Package—(MO-002-AG)		680mW
V Package		625mW
Operating Temperature Range		
MC1558		—55°C to +125°C
MC1458		0°C to +75°C
Storage Temperature Range		—65°C to +150°C
Lead Temperature (Soldering, 60 sec.)		300°C

NOTES:

1. Derate T package linearly at 4.6mW/°C for ambient temperatures above +25°C.
2. Derate V package at 5mW/°C above 25°C.

EQUIVALENT CIRCUITS



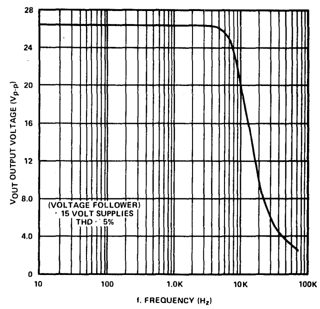
The numbers without parenthesis represent the pin numbers for ½ of the dual circuit. The numbers in parenthesis represent the pin numbers for the other half.

ELECTRICAL CHARACTERISTICS

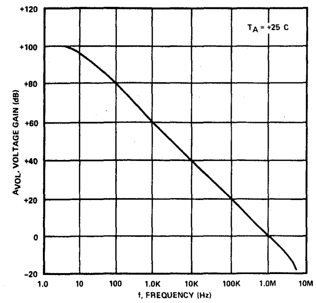
Parameter	Test Conditions	LIMITS Typ	Units
Parallel Input Capacitance		6.0	pF
Common Mode Input Impedance	f=20Hz	200	MegΩ
Equivalent Input	A_V=100, R_S=10KΩ, f=1.0kHz, BW=1.0Hz	45	$nV/\sqrt{Hz}$
Power Bandwidth	A_V=1, R_L=2.0KΩ, THD<5%,	14	kHz
Noise Voltage	V_{OUT}=20Vp-p		
Phase Margin		65	degrees
Gain Margin		11	dB
Slew Rate		0.8	V/μs
Output Impedance	f=20Hz	300	ohms
Channel Separation		120	dB

TYPICAL CHARACTERISTIC CURVES

POWER BANDWIDTH (Large Signal Swing Versus Frequency)



OPEN LOOP FREQUENCY RESPONSE



μA709-A,T • μA709C-A,T

FEATURES

- **OPEN LOOP VOLTAGE GAIN = 45,000**
- **OUTPUT VOLTAGE SWING = ±14V**
- **INPUT COMMON MODE RANGE = ±10V**
- **DIFFERENTIAL INPUT RESISTANCE =**
  μA709 250kΩ
  μA709C 400kΩ

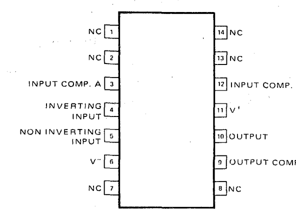
ABSOLUTE MAXIMUM RATINGS

Supply Voltage ±18V
Internal Power Dissipation (Note 1) μA709C 250mW, μA709 300mW
Differential Input Voltage ±5.0V
Input Voltage ±10V
Open Short Circuit Duration ($T_A = 25°C$) —25°C
Storage Temperature Range —65°C to +150°C
Operating Temperature Range
μA709C 0°C to +75°C
μA709 —55°C to +125°C
Lead Temperature (Soldering, 60 sec.) 300°C

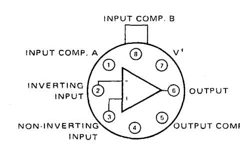
NOTE:
1. Rating applied for case temperatures to +125°C; derate linearly at 5.6mW/°C for ambient temperatures above +95°C.

PIN CONFIGURATION

A PACKAGE



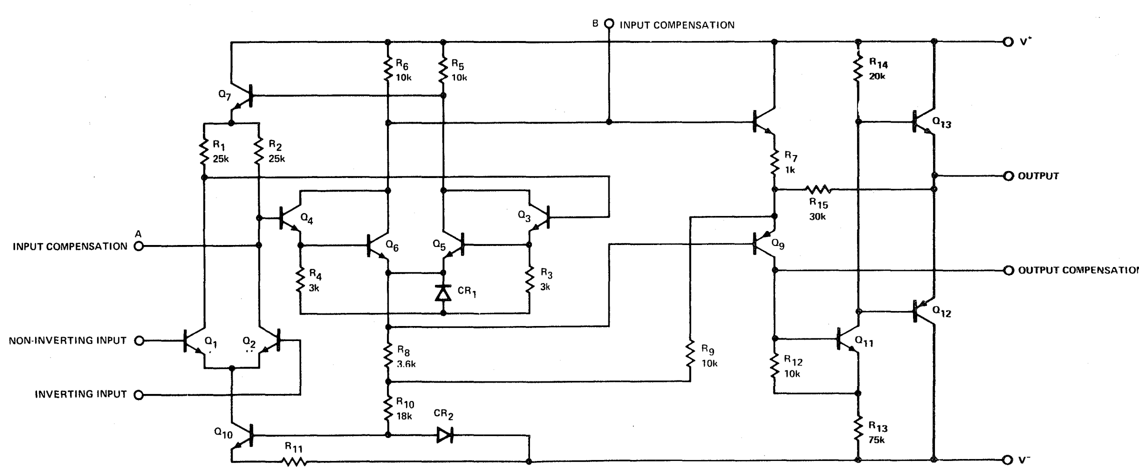
T PACKAGE



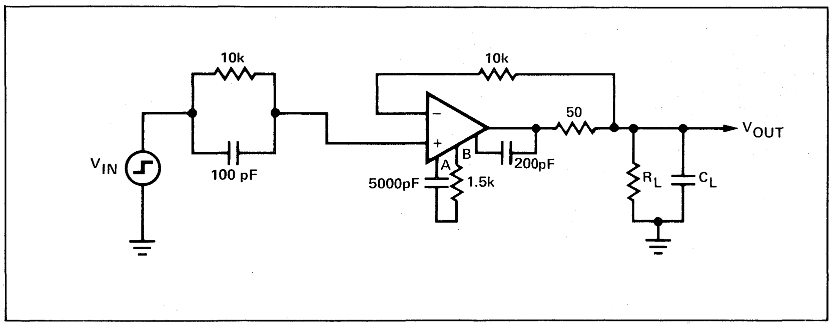
ELECTRICAL CHARACTERISTICS

Parameter	Test Conditions	LIMITS μA709 Min	μA709 Typ	μA709 Max	μA709C Min	μA709C Typ	μA709C Max	Units
Output Resistance	25°C		150			150		Ω
Transient Response Rise Time	$V_{IN} = 10mV$, $R_L = 2K\Omega$		0.3	1.0		0.3		μs
Overshoot	$C_L < 100pF$		10	30		10	30	%

CIRCUIT SCHEMATIC



TEST CIRCUIT



FEATURES

- 0.1nA INPUT BIAS CURRENT
- INPUT AND OUTPUT PROTECTION
- OFFSET NULL CAPABILITY
- INTERNALLY COMPENSATED
- 6V/μsec SLEW RATE
- STANDARD PINOUT
- NO LATCH-UP

ABSOLUTE MAXIMUM RATINGS

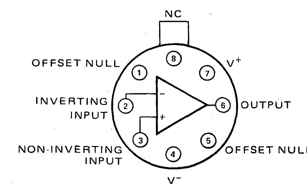
Supply Voltage	±22V
Differential Input Voltage Range	±30V
Common Mode Input Voltage Range	$\pm V_S$
Power Dissipation (Note 1)	500mW
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	—65°C to +150°C
Lead Temperature (Solder, 60 sec.)	300°C
Output Short Circuit Duration (Note 2)	Indefinite

NOTES:

1. Rating applies for case temperatures to +25°C; derate linearly at 6.5mW/°C for ambient temperatures above 75°C.
2. Short circuit may be to ground or either supply. Rating applies to +125°C case temperature or +75°C ambient temperature.

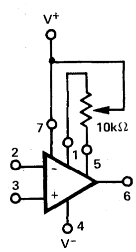
PIN CONFIGURATION

T PACKAGE

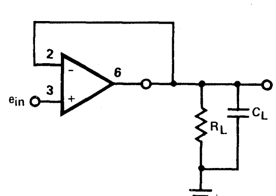


TEST CIRCUITS

OFFSET NULL CIRCUIT



VOLTAGE FOLLOWER CIRCUIT

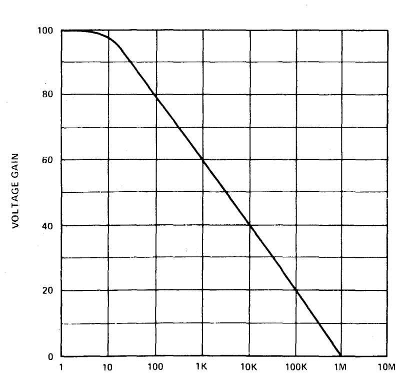


ELECTRICAL CHARACTERISTICS

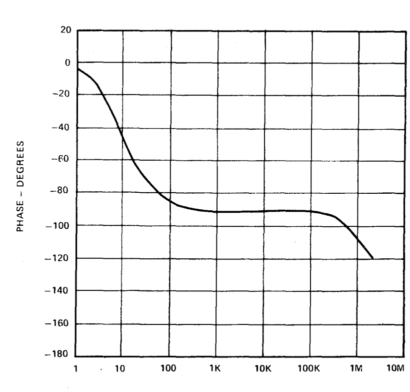
Parameter	Test Conditions	LIMITS Min	Typ	Max	Units
Output Resistance			75		Ω
Slew Rate			6.0		V/μs
Transient Response	$C_L<100pF$, $R_L=2K\Omega$, $V_{IN}=100mV$				
Rise Time			300		ns
Overshoot			10		%

TYPICAL CHARACTERISTIC CURVES

OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF FREQUENCY

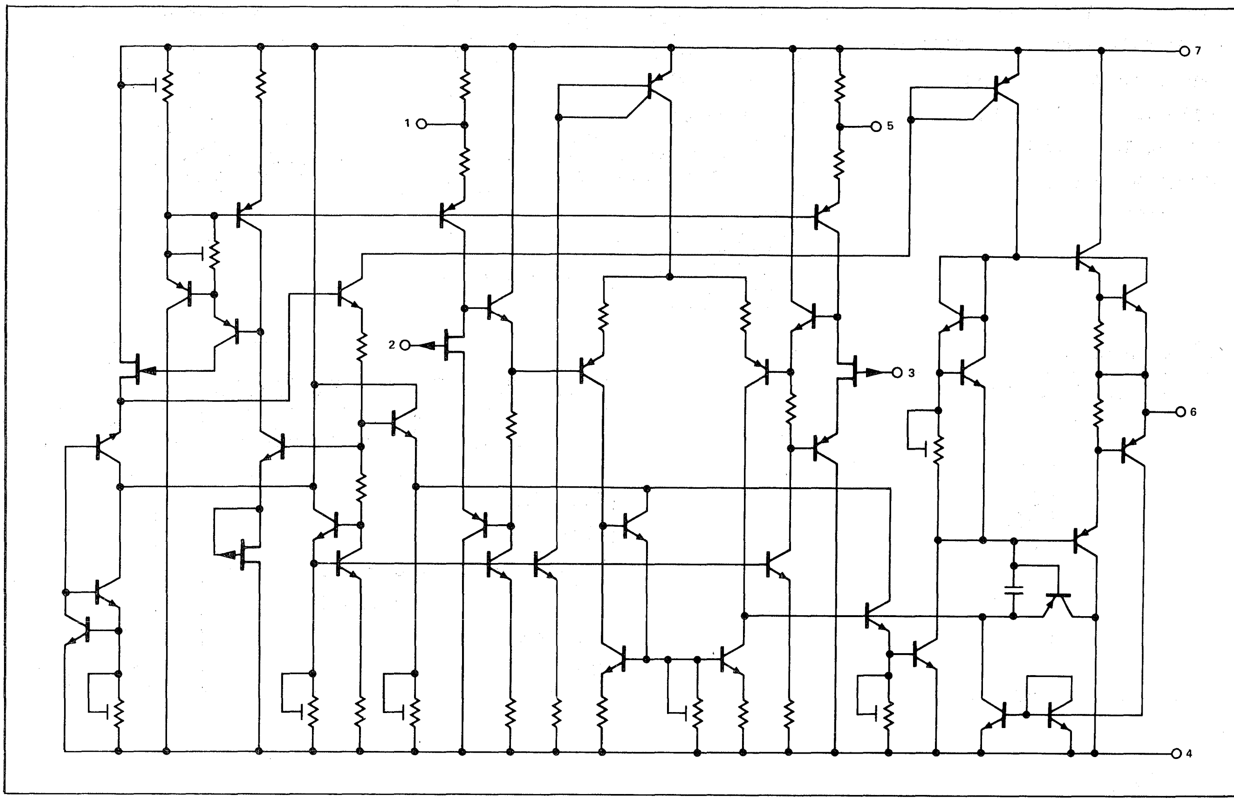


OPEN LOOP PHASE RESPONSE AS A FUNCTION OF FREQUENCY



μA740-T

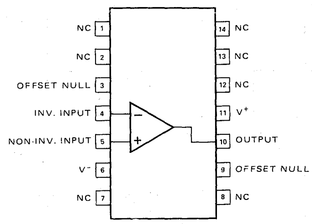
CIRCUIT SCHEMATIC



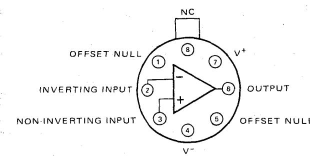
μA741-T • μA741C-A,T,V

PIN CONFIGURATION

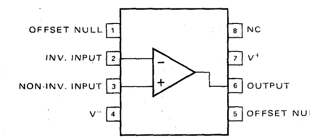
A PACKAGE



T PACKAGE



V PACKAGE



FEATURES

- **INTERNAL FREQUENCY COMPENSATION**
- **SHORT CIRCUIT PROTECTION**
- **OFFSET VOLTAGE NULL CAPABILITY**
- **EXCELLENT TEMPERATURE STABILITY**
- **HIGH INPUT VOLTAGE RANGE**
- **NO LATCH-UP**

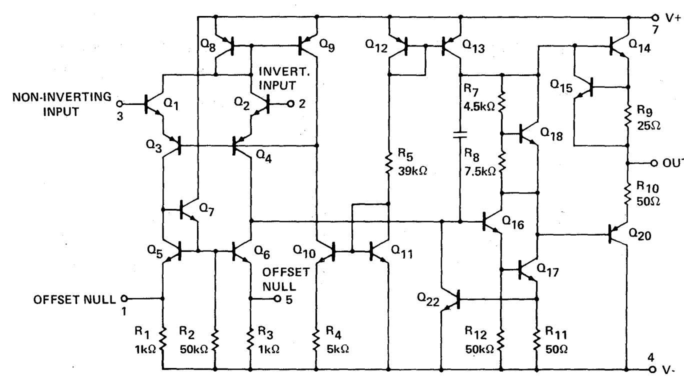
ABSOLUTE MAXIMUM RATINGS

Supply Voltage	μA741C	±18V
	μA741	±22V
Internal Power Dissipation (Note 1)		500mW
Differential Input Voltage		±30V
Input Voltage (Note 2)		±15V
Voltage between Offset Null and V—		±0.5V
Operating Temperature Range		
μA741C		0°C to +70°C
μA741		—55°C to +125°C
Storage Temperature Range		—65°C to +150°C
Lead Temperature (Solder, 60 sec.)		300°C
Output Short Circuit Duration (Note 3)		Indefinite

NOTES:

1. Rating applies for case temperatures to 125°C; derate linearly at 6.5mW/°C for ambient temperatures above +75°C.
2. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
3. Short circuit may be to ground or either supply. Rating applies to +125°C case temperature or +75°C ambient temperature.

EQUIVALENT CIRCUIT

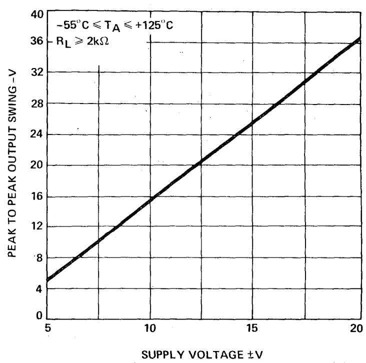


ELECTRICAL CHARACTERISTICS

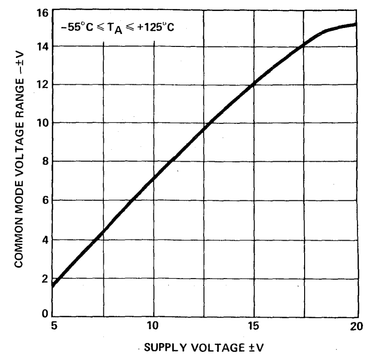
Parameter	Test Conditions	LIMITS Typ	Units
Input Capacitance		1.4	pF
Offset Voltage Adjustment Range		±15	mV
Output Resistance		75	
Transient Response	V_{IN}=20mV, R_L=2KΩ, $C_L \leq$ 100pF		
Rise Time		0.3	μs
Overshoot		5.0	%
Slew Rate	$R_L \geq$ 2KΩ	0.5	V/μs

TYPICAL CHARACTERISTIC CURVES

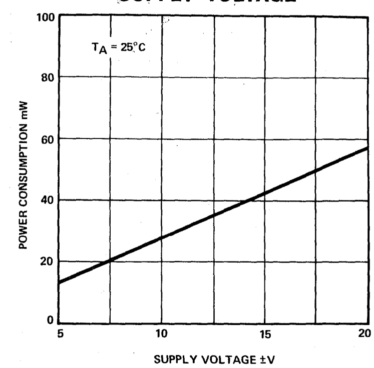
OUTPUT VOLTAGE SWING AS A FUNCTION OF SUPPLY VOLTAGE



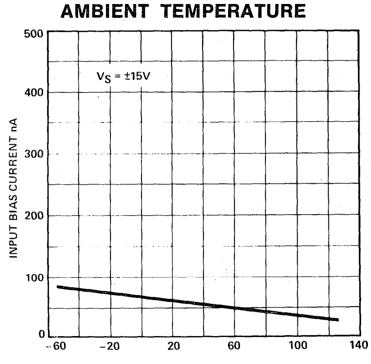
INPUT COMMON MODE VOLTAGE RANGE AS A FUNCTION OF SUPPLY VOLTAGE



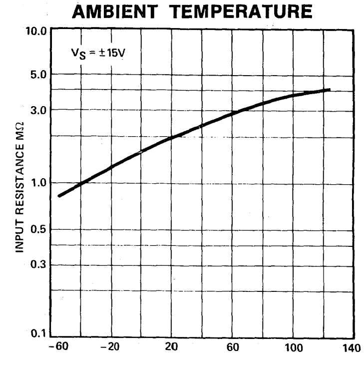
POWER CONSUMPTION AS A FUNCTION OF SUPPLY VOLTAGE



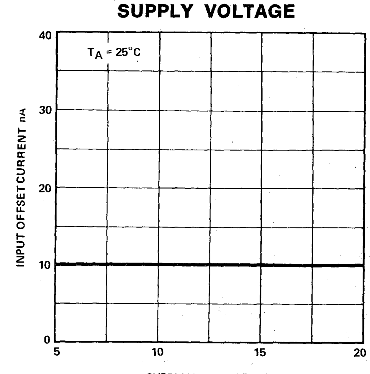
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



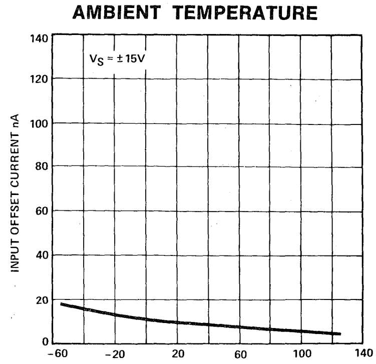
INPUT RESISTANCE AS A FUNCTION OF AMBIENT TEMPERATURE



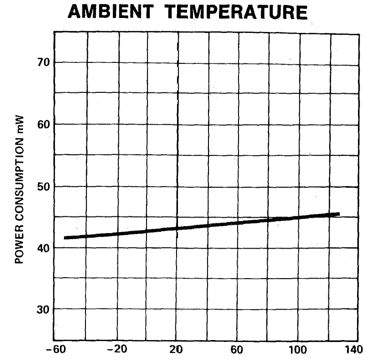
INPUT OFFSET CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



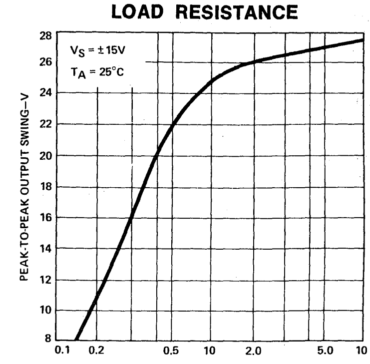
INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE

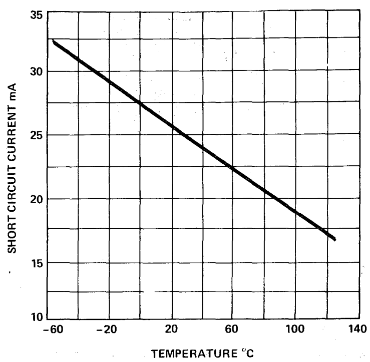


OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE

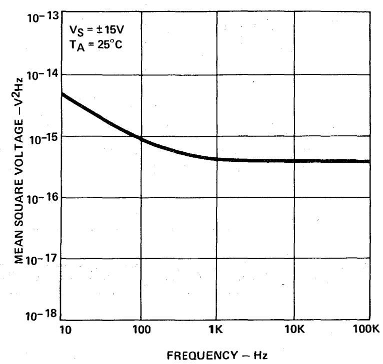


TYPICAL CHARACTERISTIC CURVES (Cont'd)

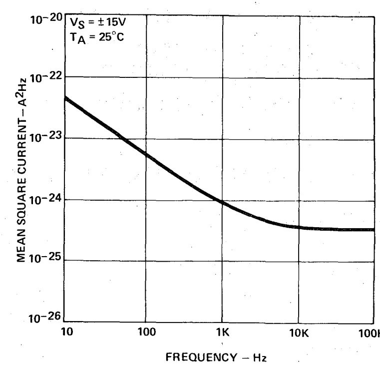
OUTPUT SHORT-CIRCUIT CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



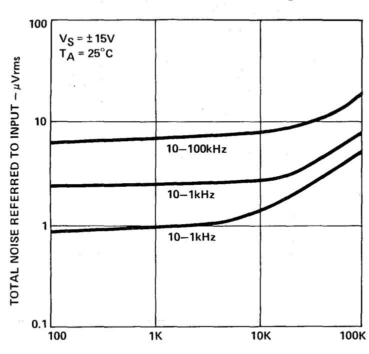
INPUT NOISE VOLTAGE AS A FUNCTION OF FREQUENCY



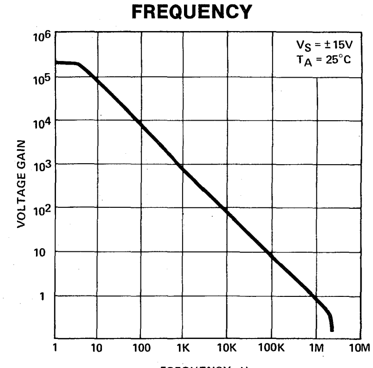
INPUT NOISE CURRENT AS A FUNCTION OF FREQUENCY



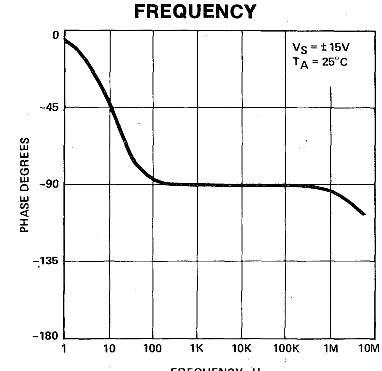
BROADBAND NOISE FOR VARIOUS BANDWIDTHS



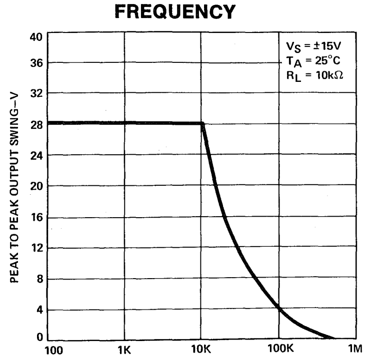
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF FREQUENCY



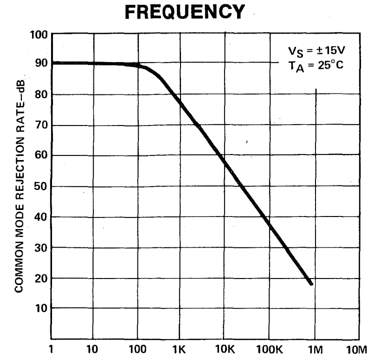
OPEN LOOP PHASE RESPONSE AS A FUNCTION OF FREQUENCY



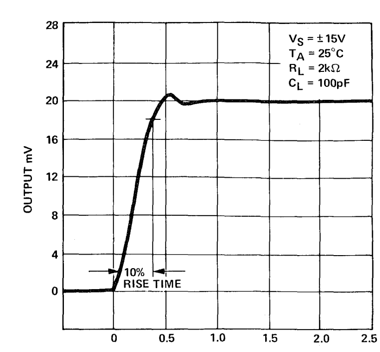
OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY



COMMON MODE REJECTION RATIO AS A FUNCTION OF FREQUENCY



TRANSIENT RESPONSE



FEATURES

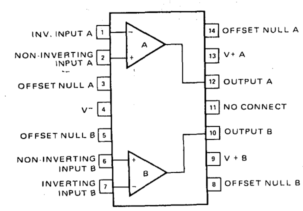
- NO FREQUENCY COMPENSATION REQUIRED
- SHORT-CIRCUIT PROTECTION
- OFFSET VOLTAGE NULL CAPABILITY
- LARGE COMMON-MODE AND DIFFERENTIAL VOLTAGE RANGES
- LOW POWER CONSUMPTION
- NO LATCH-UP

ABSOLUTE MAXIMUM RATINGS

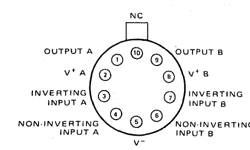
Supply Voltage	$\mu A747$	±22V
	$\mu A747C$	±18V
Internal Power Dissipation		
Metal Can		500mW
DIP		670mW
Differential Input Voltage		±30V
Input Voltage		±15V
Voltage between Offset Null and V—		±0.5V
Storage Temperature Range		—65°C to +155°C
Operating Temperature Range		
	$\mu A747$	—55°C to +125°C
	$\mu A747C$	0°C to +70°C
Lead Temperature (Soldering, 60 seconds)		300°C
Output Short Circuit Duration		Indefinite

PIN CONFIGURATION

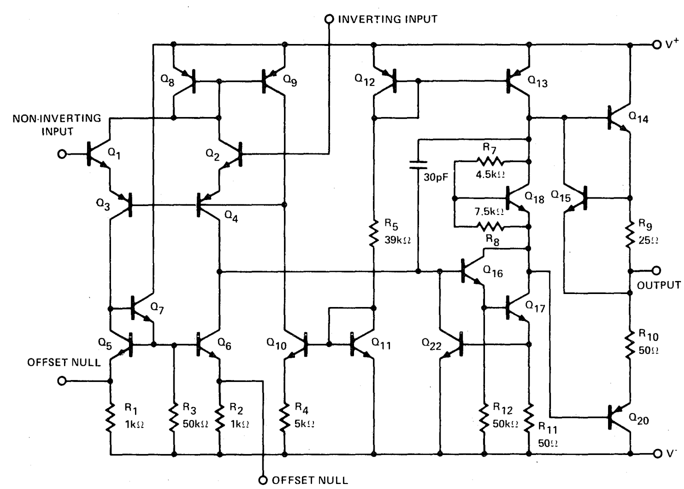
A PACKAGE



K PACKAGE



EQUIVALENT CIRCUIT (EACH SIDE)

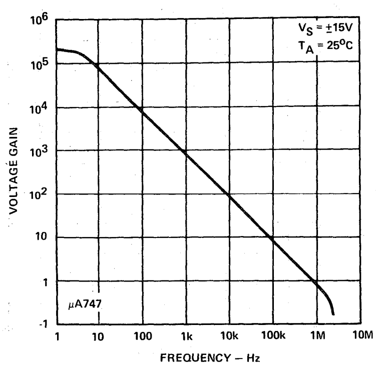


ELECTRICAL CHARACTERISTICS

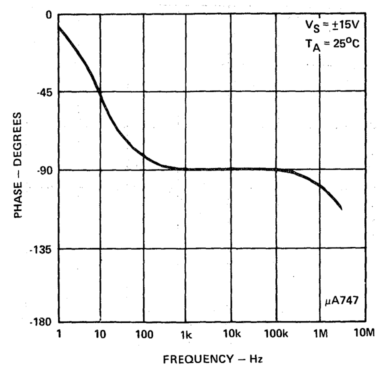
Parameter	Test Conditions	LIMITS Typ	Units
Input Capacitance		1.4	pF
Offset Voltage Adjustment Range		±15	mV
Output Resistance		75	
Transient Response	$V_{IN}=20mV$, $R_L=2K\Omega$, $C_L < 100pF$		
Rise Time		0.3	μs
Overshoot		5.0	%
Slew Rate	RL > 2K	0.5	V/μs

TYPICAL CHARACTERISTIC CURVES

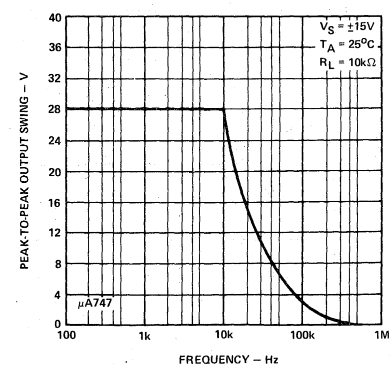
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF FREQUENCY



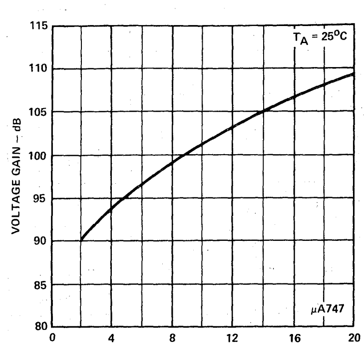
OPEN LOOP PHASE RESPONSE AS A FUNCTION OF FREQUENCY



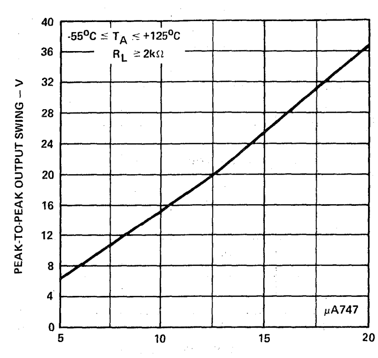
OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY



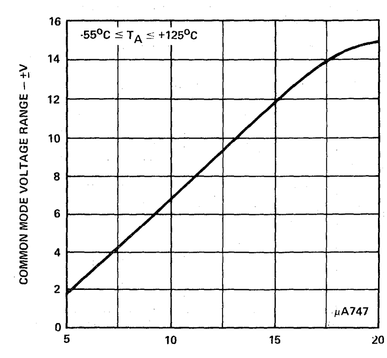
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE



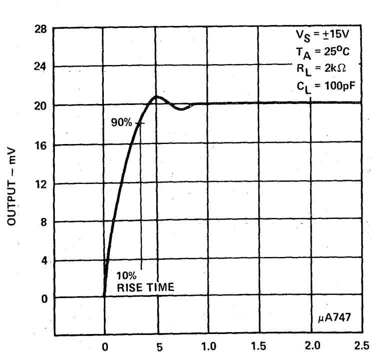
OUTPUT VOLTAGE SWING AS A FUNCTION OF SUPPLY VOLTAGE



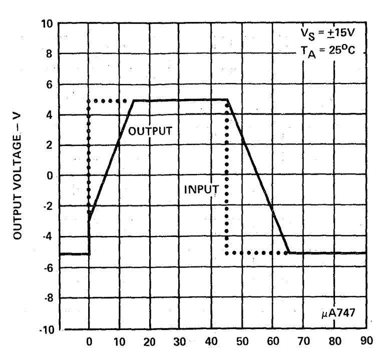
INPUT COMMON MODE VOLTAGE RANGE AS A FUNCTION OF SUPPLY VOLTAGE



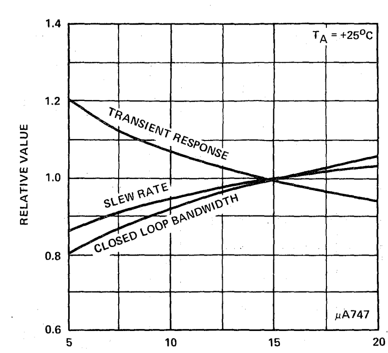
TRANSIENT RESPONSE



VOLTAGE FOLLOWER LARGE SIGNAL PULSE RESPONSE

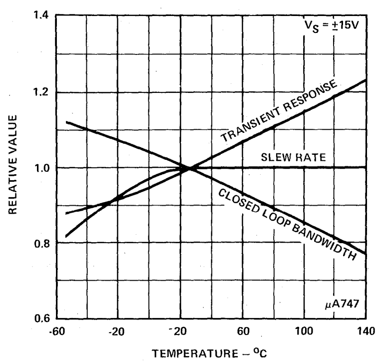


FREQUENCY CHARACTERISTICS AS A FUNCTION OF SUPPLY VOLTAGE

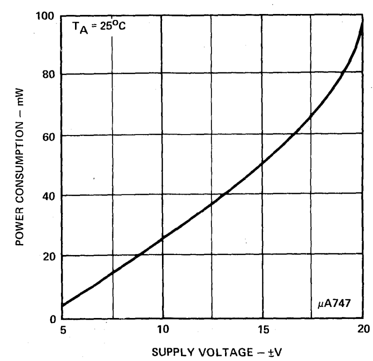


TYPICAL CHARACTERISTIC CURVES (Cont'd)

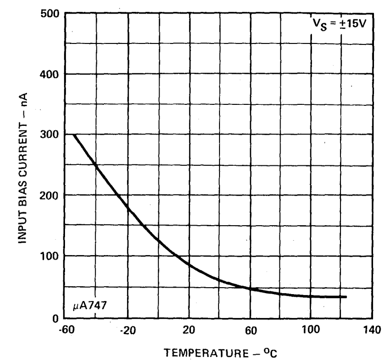
FREQUENCY CHARACTERISTICS AS A FUNCTION OF AMBIENT TEMPERATURE



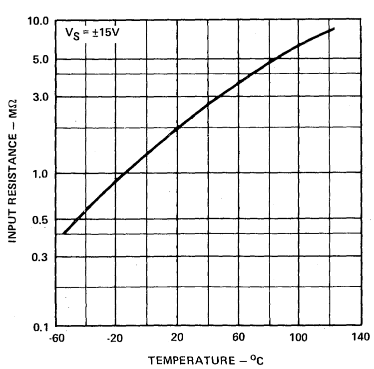
POWER CONSUMPTION AS A FUNCTION OF SUPPLY VOLTAGE



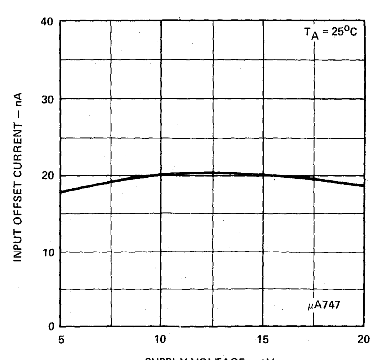
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



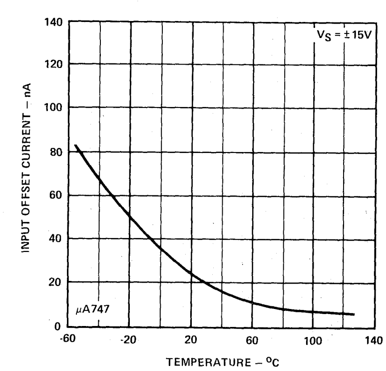
INPUT RESISTANCE AS A FUNCTION OF AMBIENT TEMPERATURE



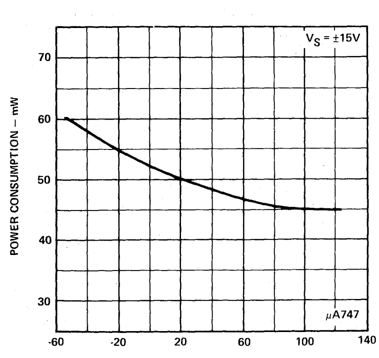
INPUT OFFSET CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



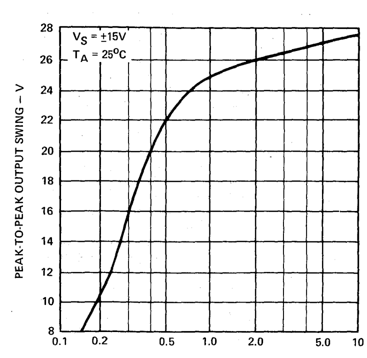
INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



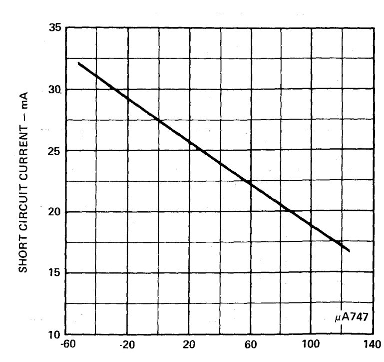
POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE



OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE

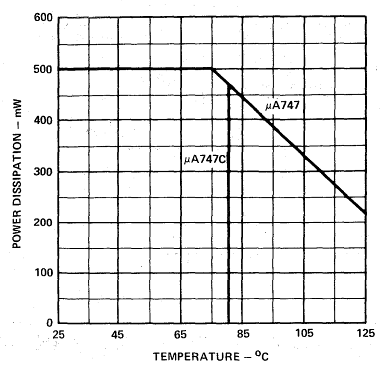


OUTPUT SHORT-CIRCUIT CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE

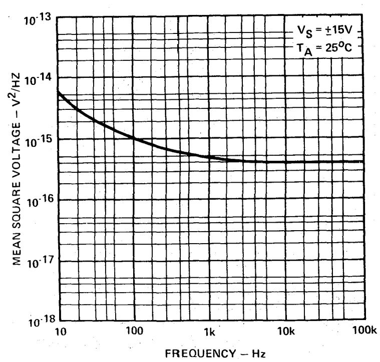


TYPICAL CHARACTERISTIC CURVES (Cont'd)

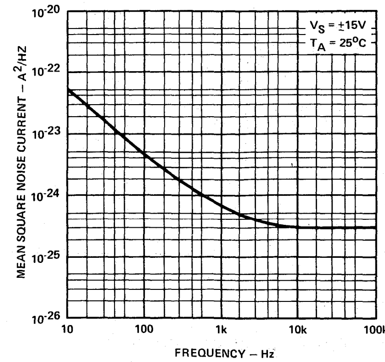
ABSOLUTE MAXIMUM POWER DISSIPATION AS A FUNCTION OF AMBIENT TEMPERATURE



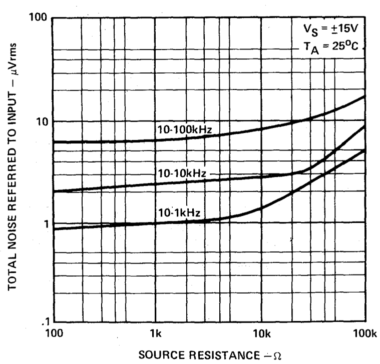
INPUT NOISE VOLTAGE AS A FUNCTION OF FREQUENCY



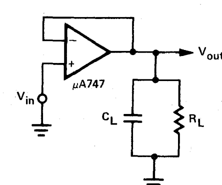
INPUT NOISE CURRENT AS A FUNCTION OF FREQUENCY



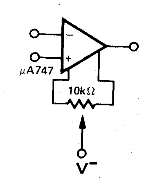
BROADBAND NOISE FOR VARIOUS BANDWIDTHS



TRANSIENT RESPONSE TEST CIRCUIT



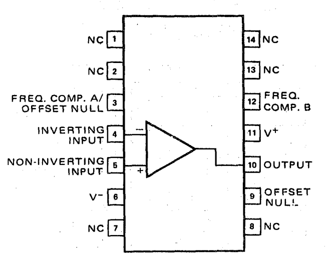
VOLTAGE OFFSET NULL CIRCUIT



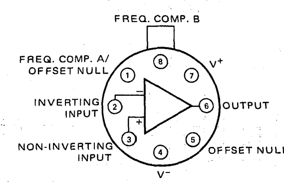
μA748-A,T • μA748C-A,T,V

PIN CONFIGURATION

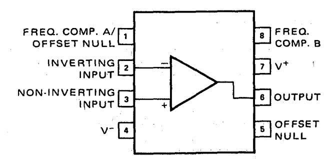
A PACKAGE



T PACKAGE



V PACKAGE



FEATURES

- **SHORT CIRCUIT PROTECTION**
- **OFFSET VOLTAGE NULL CAPABILITY**
- **LARGE COMMON-MODE AND DIFFERENTIAL VOLTAGE RANGES**
- **LOW POWER CONSUMPTION**
- **NO LATCH-UP**

ABSOLUTE MAXIMUM RATINGS

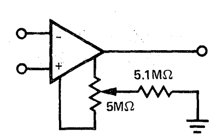
Supply Voltage	μA748	±22V
	μA748C	±18V
Internal Power Dissipation (Note 1)		500mW
Differential Output Voltage		±30V
Input Voltage (Note 2)		±15V
Storage Temperature Range		—65°C to +150°C
Operating Temperature Range	μA748	—55°C to +125°C
	μA748C	0°C to +70°C
Lead Temperature		300°C
Output Short Circuit Duration (Note 3)		Indefinite

NOTES:

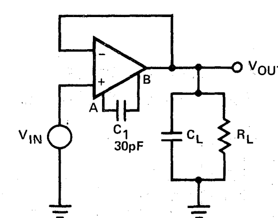
1. Rating applies for case temperatures to +70°C.
2. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
3. Short circuit may be to ground or either supply. Rating applies to +70°C ambient temperature.

TEST CIRCUITS

VOLTAGE OFFSET NULL CIRCUIT



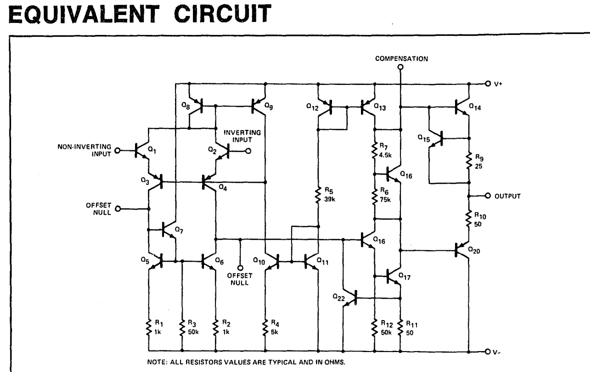
TRANSIENT RESPONSE TEST CIRCUIT



ELECTRICAL CHARACTERISTICS

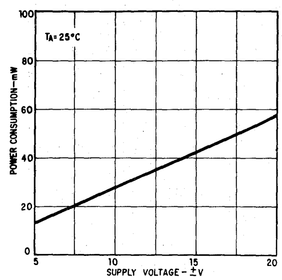
Parameter	Test Conditions	LIMITS Typ	Units
Input Capacitance		1.4	pF
Offset Voltage Adjustment Range		±15	mV
Output Resistance		75	Ω
Transient Response	$V_{IN}=20mV$, $R_L=2K\Omega$, $C_L<100pF$		
Rise Time		0.3	μs
Overshoot	$C_1=30pF$	5.0	%
Slew Rate	$R_L>2K\Omega$, $C_1=20pF$	0.5	V/μs

EQUIVALENT CIRCUIT

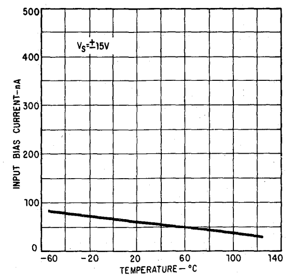


TYPICAL CHARACTERISTIC CURVES

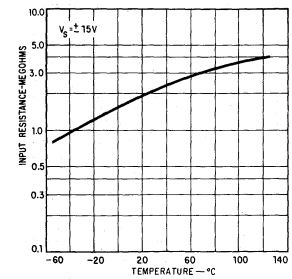
POWER CONSUMPTION AS A FUNCTION OF SUPPLY VOLTAGE



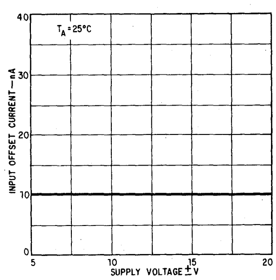
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



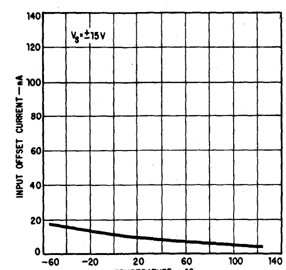
INPUT RESISTANCE AS A FUNCTION OF AMBIENT TEMPERATURE



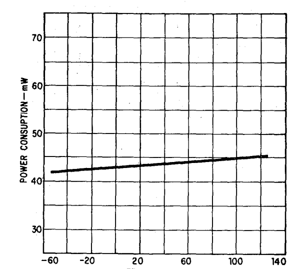
INPUT OFFSET CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



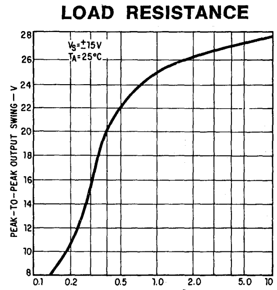
INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



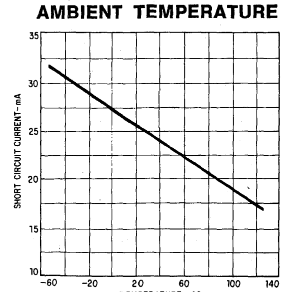
POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE



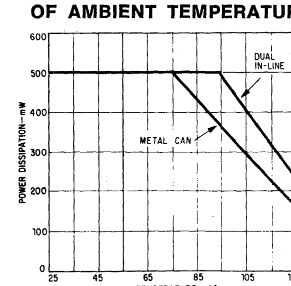
OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE



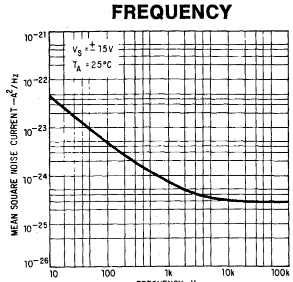
OUTPUT SHORT-CIRCUIT CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



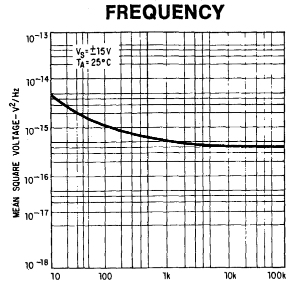
ABSOLUTE MAXIMUM POWER DISSIPATION AS A FUNCTION OF AMBIENT TEMPERATURE



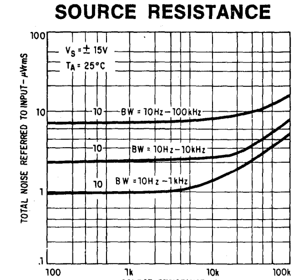
INPUT NOISE CURRENT AS A FUNCTION OF FREQUENCY



INPUT NOISE VOLTAGE AS A FUNCTION OF FREQUENCY



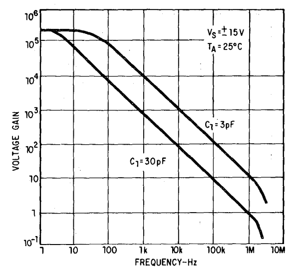
BROADBAND NOISE AS A FUNCTION OF SOURCE RESISTANCE



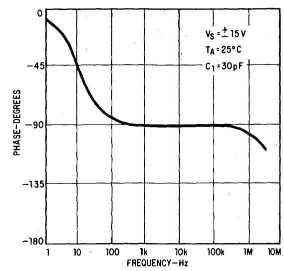
ANALOG

TYPICAL CHARACTERISTIC CURVES (Cont'd)

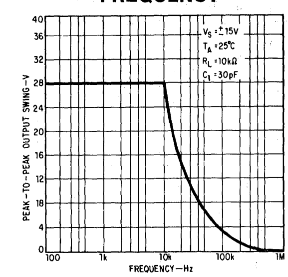
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF FREQUENCY



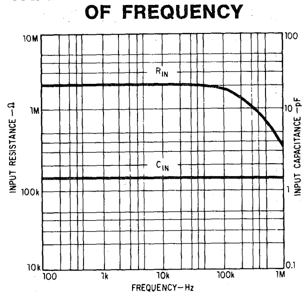
OPEN LOOP PHASE RESPONSE AS A FUNCTION OF FREQUENCY



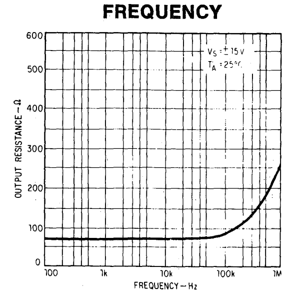
OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY



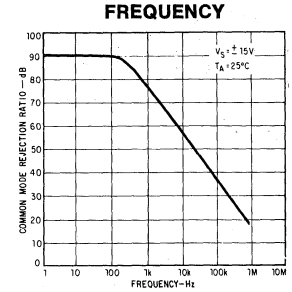
INPUT RESISTANCE AND INPUT CAPACITANCE AS A FUNCTION OF FREQUENCY



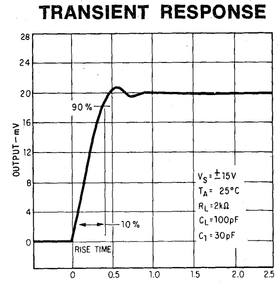
OUTPUT RESISTANCE AS A FUNCTION OF FREQUENCY



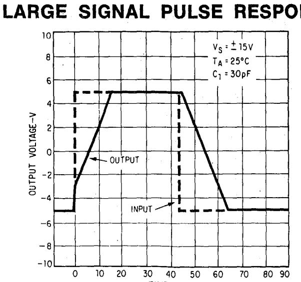
COMMON MODE REJECTION RATIO AS A FUNCTION OF FREQUENCY



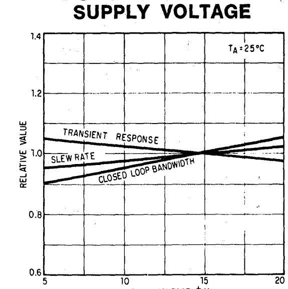
TRANSIENT RESPONSE



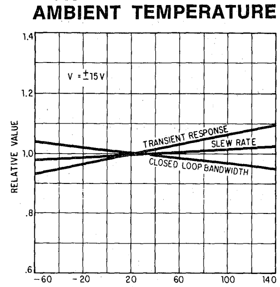
VOLTAGE FOLLOWER LARGE SIGNAL PULSE RESPONSE



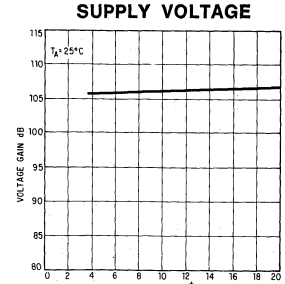
FREQUENCY CHARACTERISTICS AS A FUNCTION OF SUPPLY VOLTAGE



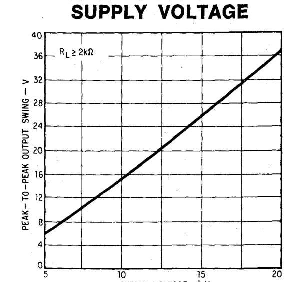
FREQUENCY CHARACTERISTICS AS A FUNCTION OF AMBIENT TEMPERATURE



OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE



OUTPUT VOLTAGE SWING AS A FUNCTION OF SUPPLY VOLTAGE



SA534-A,F

FEATURES

- INTERNALLY FREQUENCY COMPENSATED FOR UNITY GAIN
- LARGE DC VOLTAGE GAIN — 100 dB
- WIDE BANDWIDTH (UNITY GAIN) — 1 MHz (TEMPERATURE COMPENSATED)
- WIDE POWER SUPPLY RANGE: SINGLE SUPPLY — $3V_{DC}$ to $30V_{DC}$ OR DUAL SUPPLIES — $\pm1.5V_{DC}$ to $\pm15V_{DC}$
- VERY LOW SUPPLY CURRENT DRAIN (800μA) — ESSENTIALLY INDEPENDENT OF SUPPLY VOLTAGE (1 mW/op amp at $+5V_{DC}$)
- LOW INPUT BIASING CURRENT — $45nA_{DC}$ (TEMPERATURE COMPENSATED)
- LOW INPUT OFFSET VOLTAGE — $2mV_{DC}$ AND OFFSET CURRENT — $5nA_{DC}$
- DIFFERENTIAL INPUT VOLTAGE RANGE EQUAL TO THE POWER SUPPLY VOLTAGE
- LARGE OUTPUT VOLTAGE — $0V_{DC}$ to V+ —$1.5V_{DC}$ SWING

UNIQUE FEATURES

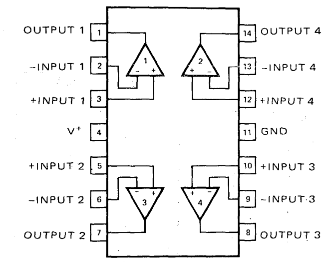
IN THE LINEAR MODE THE INPUT COMMON-MODE VOLTAGE RANGE INCLUDES GROUND AND THE OUTPUT VOLTAGE CAN ALSO SWING TO GROUND, EVEN THOUGH OPERATED FROM ONLY A SINGLE POWER SUPPLY VOLTAGE. THE UNITY GAIN CROSS FREQUENCY IS TEMPERATURE COMPENSATED. THE INPUT BIAS CURRENT IS ALSO TEMPERATURE COMPENSATED.

ABSOLUTE MAXIMUM RATINGS

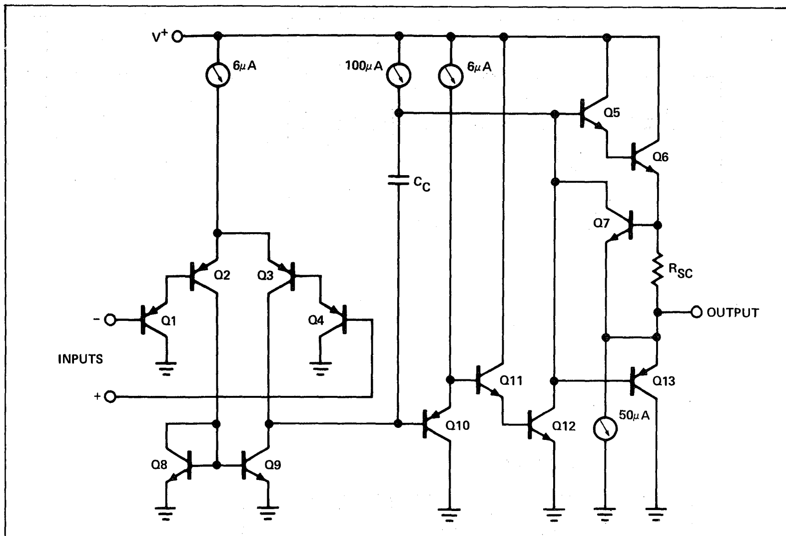
Supply Voltage, V+	$32V_{DC}$ or $\pm16V_{DC}$
Differential Input Voltage	$32V_{DC}$
Input Voltage	$-0.3V_{DC}$ to $+32V_{DC}$
Power Dissipation	
Molded DIP	570mW
Cavity DIP	900mW
Output Short Circuit to GND 1 Amplifier	Continuous
V+ $<15V_{DC}$ and $T_A=25°C$	
Operating Temperature Range	—40°C to +85°C
Storage Temperature Range	—65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	300°C

PIN CONFIGURATION

A, F PACKAGE



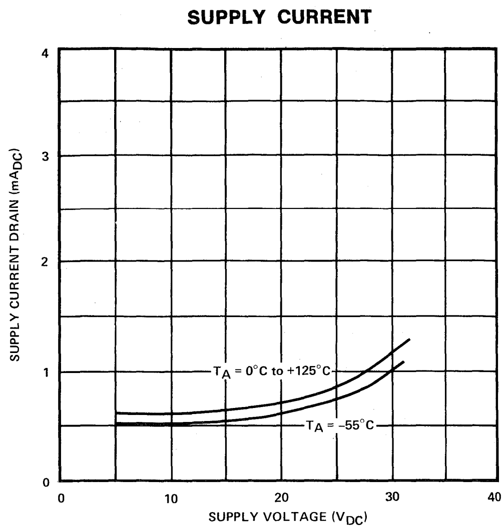
EQUIVALENT CIRCUIT

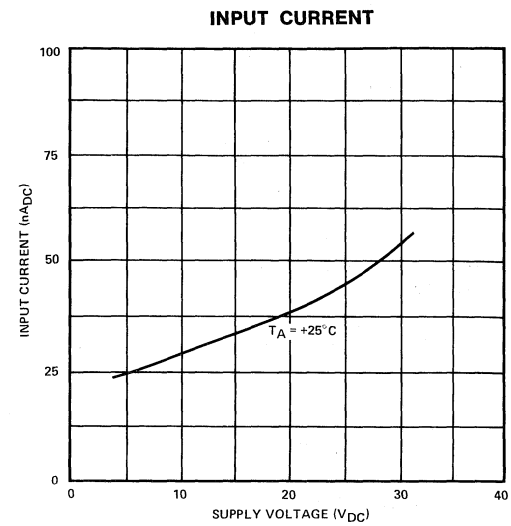


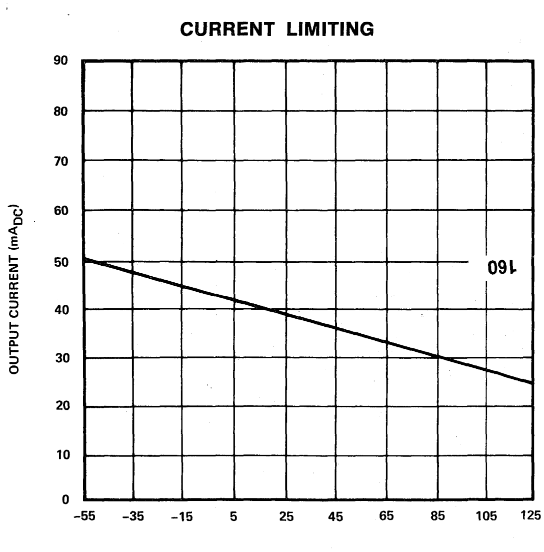
ELECTRICAL CHARACTERISTICS

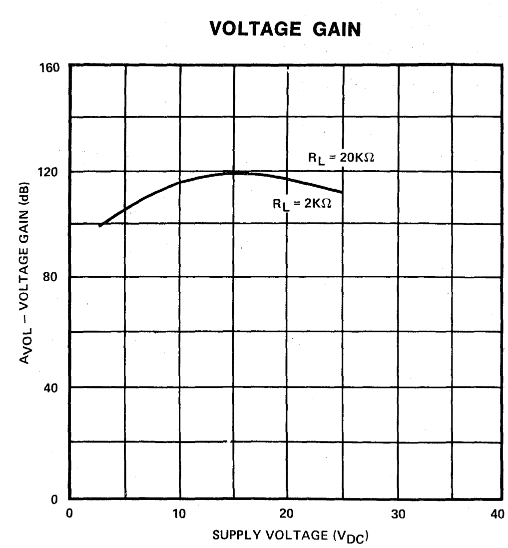
Parameter	Test Conditions	LIMITS SA534 Min	Typ	Max	Units
Amplifier-to-Amplifier Coupling	f=1kHz to 20 kHz, $T_A=25°C$ (input Referred)		−120		dB
Output Current Source	$V_{IN}+=+1V_{DC}$, $V_{IN}-=0V_{DC}$, $V+=15V_{DC}$, $T_A=25°C$	20	40		mA_{DC}
	$V_{IN}+=+1V_{DC}$, $V_{IN}-=0V_{DC}$, $V+=15V_{DC}$	10	20		mA
Output Current Sink	$V_{IN}-=+1V_{DC}$, $V_{IN}+=0V_{DC}$, $V+=15V_{DC}$, $T_A=25°C$	10	20		mA_{DC}
	$V_{IN}-=+1V_{DC}$, $V_{IN}+=0V_{DC}$, $T_A=+25°C$, $V_D=200mV_{DC}$	12	50		μA_{DC}
	$V_{IN}-=+1V_{DC}$, $V_{IN}+=0V_{DC}$, $V+=15V_{DC}$	5	8		mA
Differential Input Voltage				V+	V_{DC}

TYPICAL PERFORMANCE CURVES



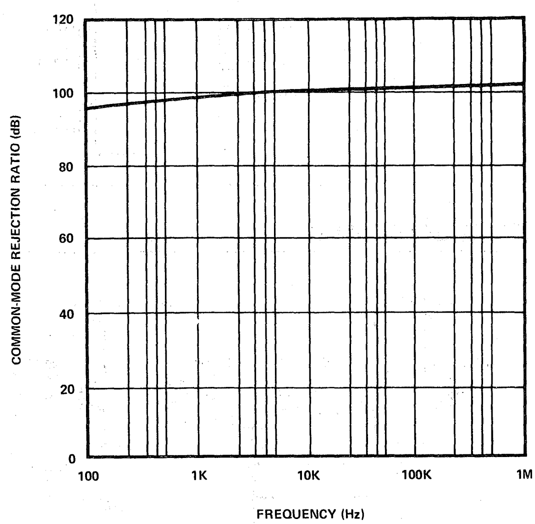




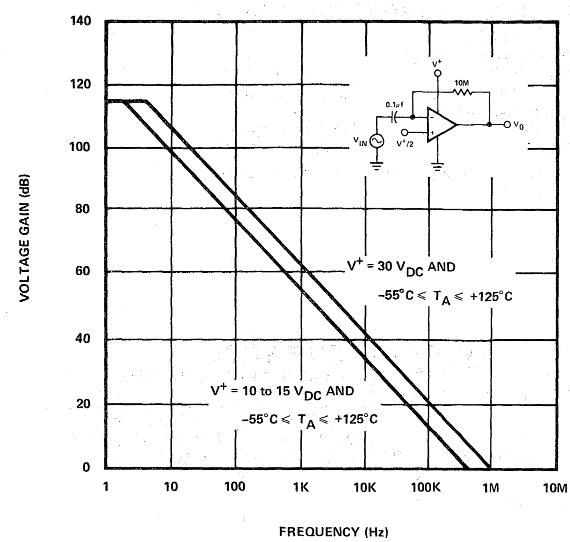


TYPICAL PERFORMANCE CURVES (Cont'd)

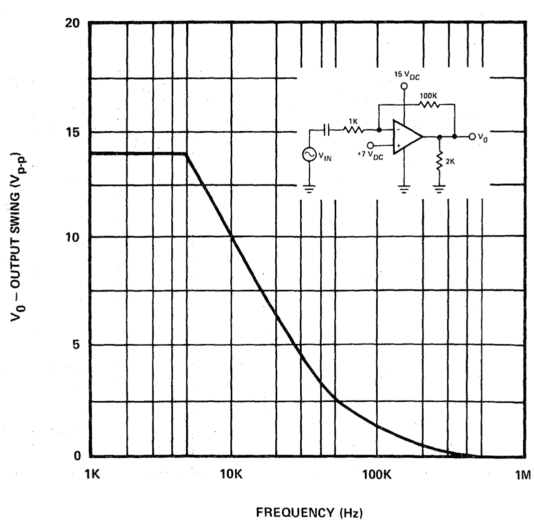
COMMON-MODE REJECTION RATIO



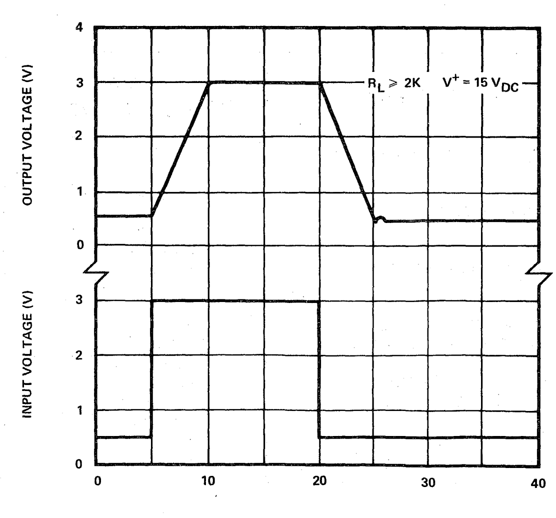
OPEN LOOP FREQUENCY RESPONSE



LARGE SIGNAL FREQUENCY RESPONSE



VOLTAGE FOLLOWER PULSE RESPONSE



FEATURES
- LOW INPUT OFFSET VOLTAGE = ±2mV
- LOW INPUT OFFSET CURRENT = ±3µA
- SINGLE POWER SUPPLY
- AGC CAPABILITY
- HIGH FORWARD TRANSADMITTANCE
- LOW FEEDBACK CAPACITANCE

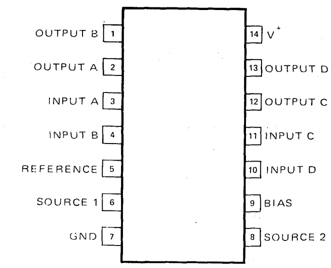
ABSOLUTE MAXIMUM RATINGS

Applied Voltage (V+)	20V
Differential Input Voltage	±5V
Current (All Pins)	±15mA
Storage Temperature	−65°C to +150°C
Operating Tempreature	
SE510A	−55°C to +125°C
NE510A	0°C to +75°C

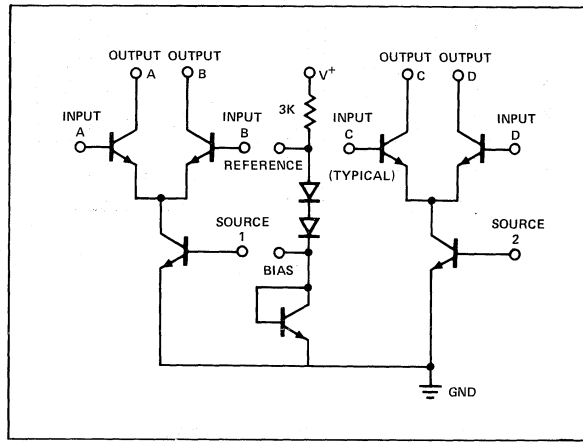
Maximum ratings are limiting values above which serviceability may be impaired.

PIN CONFIGURATION

A PACKAGE



CIRCUIT SCHEMATIC



ELECTRICAL CHARACTERISTICS
(V+ = +12V, T = 25°C applicable from DC to 10 MHz, unless otherwise noted)

PARAMETER	EMITTER COUPLED CONFIGURATION	CASCODE CONFIGURATION VAGC = 0V	UNITS
Input Conductance [Re(Y11)]	0.7	3.0	mmho
Output Conductance [Re(Y22)]	0.01	0.01	mmho
Input Capacitance	4.5	10	pF
Output Capicitance	2.5	2.5	pF
Reverse Transfer Capacitance	0.05	0.05	pF
Forward Transconductance	25	90	mmho

PARAMETERS	TEST CONDITIONS		LIMITS NE510 MIN	NE510 TYP	NE510 MAX	SE510 MIN	SE510 TYP	SE510 MAX	UNITS
Input Offset Voltage	+25°C			0.5	3		0.5	2	mV
	0°C to +70°C			1.0	4				
	−55°C to +125°C						1.5	3.5	
Input Offset Current	+25°C			2.0	6		2.0	3.5	µA
	0°C to +70°C			2.5	9				
	−55°C to +125°C						2.5	7.5	
Input Bias Current	+25°C			8.0	25		8.0	20	µA
	0°C to +70°C			10.0	40				
	−55°C to +125°C						16.0	40	
Differential Collector Current per Differential Pair	+25°C	$V_{in} = 0$		45	75		45	62.5	µA
	0°C to +70°C			50	100				
	−55°C to +125°C						50	100	
Differential Current in the Current Sources	+25°C			30	75		30	62.5	νA
	0°C to +70°C			35	100				
	−55°C to +125°C						35	100	
Total Current	+25°C			11.0	15.0		11.0	15.0	mA
Common Mode Rejection	+25°C		60	80		60	80		dB

FEATURES

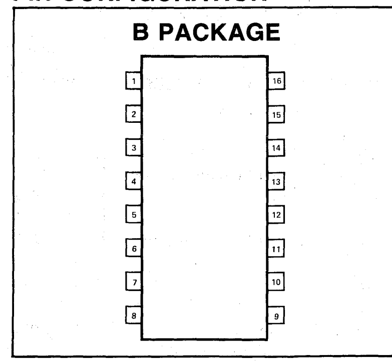
- LOW INPUT OFFSET VOLTAGE = ±2mV
- LOW INPUT OFFSET CURRENT = ±3μA
- AGC CAPABILITY
- HIGH FORWARD TRANSADMITTANCE
- LOW FEEDBACK CAPACITANCE
- SINGLE POWER SUPPLY

ABSOLUTE MAXIMUM RATINGS

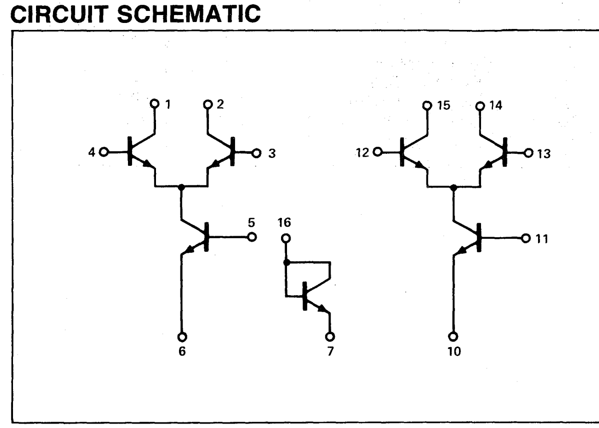
Applied Voltage (V+)	20V
Differential Input Voltage	±5V
Current (All Pins)	±15mA
Storage Temperature	−65°C to +150°C
Operating Temperature	
SE511B	−55°C to +125°C
NE511B	0°C to +75°C

Maximum ratings are limiting values above which serviceability may be impaired.

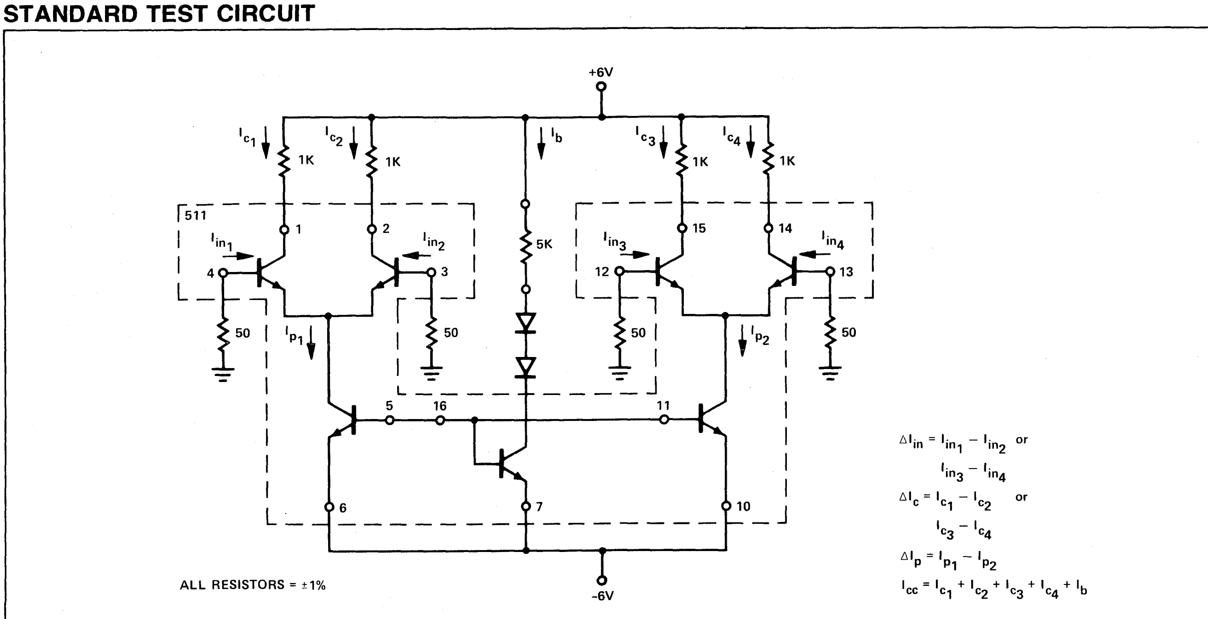
PIN CONFIGURATION



CIRCUIT SCHEMATIC



STANDARD TEST CIRCUIT



ELECTRICAL CHARACTERISTICS (Standard Test Circuit)

SYMBOL	PARAMETER	ACCEPTANCE TEST SUBGROUP	TEST CONDITIONS		LIMITS MIN SE511	LIMITS MIN NE511	LIMITS TYP SE511	LIMITS TYP NE511	LIMITS MAX SE511	LIMITS MAX NE511	UNITS
ΔV_{in}	Input Offset Voltage	A-3	+25°C				0.5	0.5	2	3	mV
ΔV_{in}		A-4	0°C to +75°C					1.0		4.0	
ΔV_{in}		A-5	−55°C to +125°C				1.5		3.5		
ΔI_{in}	Input Offset Current	A-3	+25°C				2.0	2.0	3.5	6	µA
ΔI_{in}		A-4	0°C to +75°C					2.5		9	
ΔI_{in}		A-5	−55°C to +125°C				2.5		7.5		
I_{in}	Input Bias Current	A-3	+25°C				8.0	8.0	20	25	µA
I_{in}		A-4	0°C to +75°C					10.0		40	
I_{in}		A-5	−55°C to +125°C				16.0		40		
ΔI_C	Differential Collector	A-3	+25°C	$V_{in}=0$;			45	45	62.5	75	µA
ΔI_C	Current per	A-4	0°C to +75°C	$I_p = 2mA$				50		100	
ΔI_C	differential pair	A-5	−55°C to +125°C				50		100		
ΔI_p	Differential Current in	A-3	+25°C				30	30	62.5	75	µA
ΔI_p	the Current Sources	A-4	0°C to +75°C					35		100	
ΔI_p		A-5	−55°C to +125°C				35		100		
I_{CC}	Total Current	A-2	+25°C				11.0	11.0	15.0	15.0	mA
CMRR	Common Mode Rejection Ratio	A-3	+25°C		60	60	80	80			dB
G_{22}	Output Conductance	A-3	+25°C				0.01	0.01			mmho
C_{ob}	Output Capacitance	C-2	+25°C				2.5	2.5			pF
C_{ib}	Input Capacitance	C-2	+25°C				10	10			pF

DESCRIPTION

The 515 is a general purpose high-gain amplifier with differential input and output. It is fabricated within a monolithic silicon substrate by planar and epitaxial techniques. A pair of compensation points is provided to allow frequency compensation for stable closed loop operation.

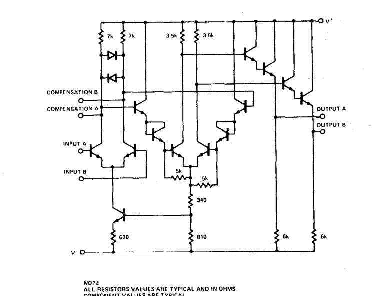
This device is not internally referenced to ground and with proper input bias may be operated from a single power supply.

ABSOLUTE MAXIMUM RATINGS

Applied Voltage (V+ to V-)	12V
Differential Input Voltage (V_5 to V_7)	±5.0V
Input Current (I_5, I_7)	±2.0mA
Output Current (I_2, I_{10})	± 30mA
Storage Temperature	-65°C to +150°C
Operating Temperature	0°C to +75°C
Junction Temperature	150°C

Maximum ratings are limiting values above which serviceability may be impaired.

EQUIVALENT CIRCUIT

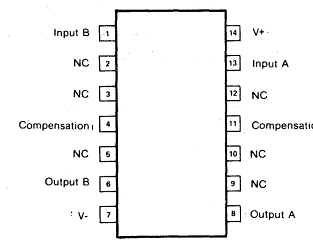


FEATURES

- **DIFFERENTIAL VOLTAGE GAIN (Open Loop) = 4,500**
- **INPUT OFFSET VOLTAGE = 0.5mV**
- **INPUT OFFSET VOLTAGE STABILITY = 5.0 V/°C**
- **INPUT COMMON MODE RANGE = +1.5V, -1.0V**
- **COMMON MODE REJECTION RATIO = 100dB**
- **BANDWIDTH (Open Loop) = 1.0 mHz**

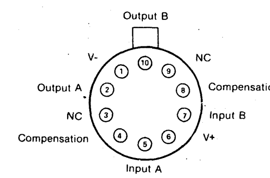
PIN CONFIGURATIONS

A PACKAGE



ORDER PART NO. NE515A

K PACKAGE



ORDER PART NOS. SE515K/NE515K

SE515
ELECTRICAL CHARACTERISTICS (Standard Conditions: V_7 = 0V, V_1 = -3.0V; Notes: 4, 5, 6, 7, 8, 9)

CHARACTERISTICS	V_6 = +4.0V TYP	V_6 = +6.0V MIN	V_6 = +6.0V TYP	V_6 = +6.0V MAX	Units	TEMP	TEST CONDITIONS
Open Loop Voltage Gain (dc)	2,500	3,500	4,500		V/V	+25°C	Note 2
	1,800		3,000		V/V	+125°C	
Open Loop Voltage Gain (ac)	2,000	2,500	3,500		V/V	+25°C	f = 800 kHz
Input Offset Voltage	0.5		0.5	3.0	mV	-55°C	Note 1
	0.5		0.5	2.0	mV	+25°C	
	0.5		0.5	3.0	mV	+125°C	
Input Bias Current	18		25	40	μA	-55°C	Note 1
	12		16	24	μA		
Differential Input Resistance	2.0	1.0	1.5		kΩ	-55°C	Note 10
	4.0	2.0	3.2		kΩ	+25°C	
Input Common Mode Range	±1.0		+1.5		V	+25°C	
			-1.0				
Balanced Output dc Level	-0.1		+1.2		V	-55°C	Note 1
	+0.3		+1.6	+1.8	V	+25°C	
	+0.6		+1.9		V	+125°C	
Output Voltage Swing	4.7	5.7	6.3		V	-55°C	Note 3
	4.7	5.7	6.3		V	+25°C	
	4.7	5.7	6.3		V	+125°C	
High Output Level	+2.3	+4.0	+4.3		V	-55°C	V_5 = 10mV
	+2.6	+4.3	+4.6		V	+25°C	
	+3.0	+4.7	+5.0		V	+125°C	
Low Output Level	-2.4	-1.7	-2.0		V	-55°C	V_5 = 10mV
	-2.1	-1.4	-1.7		V	+25°C	
	-1.7	-1.0	-1.3		V	+125°C	
Output Resistance	100		100		Ω	+25°C	Note 1
Common Mode Rejection Ratio	100		100		dB		
Power Supply Current				7.0	mA		Note 1
	3.5		5.5	7.0	mA		
				7.0	mA		

NOTES:
1. Adjust V5 to obtain $V_2 = V_{10}$.
2. Output voltage swing = 1.3V peak to peak.
3. Output voltage swing is guaranteed by output voltage limit tests.
4. Voltage and current subscripts refer to pin numbers.
5. All measurements are referenced to power supply common. Positive current flow is defined as into the terminal indicated.
6. All specifications herein apply for interchange of voltages and currents at Pins 5 and 7.
7. Acceptance Test Sub-Group references apply to minimum and maximum limits only.
8. The SE515k has Pins 1, 3 and 9 connected to the case. The SE515Q has Pins 3 and 9 open.
9. See Signetics SURE Program Bulletin No. 5001 for definition of Acceptance Test Sub-Groups. Sub-Group A-7 is used for electrical end points for Linear Products.
10. Differential Input Resistance is computed from input bias current.

NE515

ELECTRICAL CHARACTERISTICS (Standard Conditions: V_B = 0V, V_A = 3.0V; Notes: 4, 5, 6, 7, 8, 9)

CHARACTERISTICS	V_F = +4.0V	V_F = +6.0V			UNITS	TEMP	TEST CONDITIONS
	TYP	MIN	TYP	MAX			
Open Loop Voltage Gain (dc)	1,800	2,500	3,200		V/V	+25°C	Note 2
	1,350		2,200		V/V	+75°C	
Open Loop Voltage Gain (ac)	1,500	1,700	2,500		V/V	+25°C	f = 800 kHz
Input Offset Voltage	0.5		0.5	4.0	mV	0°C	Note 1
	0.5		0.5	3.0	mV	+25°C	
	0.5		0.5	4.0	mV	+75°C	
Input Bias Current	18		25	40	μA	0°C	Note 1
	15		20	31	μA	+25°C	
Differential Input Resistance	3.2	1.4	2.3		kΩ	0°C	Note 10
	3.5	1.7	2.6		kΩ	+25°C	
Input Common Mode Range	±1.0		+1.5		V	+25°C	
			-1.0				
Balanced Output dc Level	-0.1		+1.2		V	0°C	Note 1
	+0.3		+1.6	+1.8	V	+25°C	
	+0.6		+1.9		V	+75°C	
Output Voltage Swing	4.5	5.3	6.1		V	0°C	Note 3
	4.5	5.3	6.1		V	+25°C	
	4.5	5.3	6.1		V	+75°C	
High Output Level	+2.3	+3.9	+4.3		V	0°C	V_C = 10mV
	+2.5	+4.1	+4.5		V	+25°C	
	+2.8	+4.3	+4.8		V	+75°C	
Low Output Level	-2.2	-1.4	-1.8		V	0°C	V_C = 10mV
	-2.0	-1.2	-1.6		V	+25°C	
	-1.7	-1.0	-1.3		V	+75°C	
Output Resistance	100		100		Ω	+25°C	Note 1
Common Mode Rejection Ratio	100		100		dB	+25°C	
Power Supply Current				7.0	mA	0°C	Note 1
	3.5		5.5	7.0	mA	+25°C	
				7.0	mA	+75°C	

Letter subscripts refer to pins on circuit schematic.

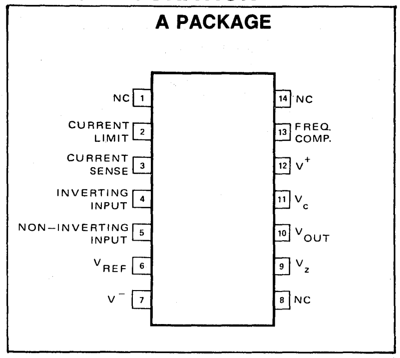
NOTES:
1. Adjust V_C to obtain V_G = V_H.
2. Output voltage swing = 1.3V peak to peak.
3. Output voltage swing is guaranteed by output voltage limit tests.
4. Voltage and current subscripts refer to pin numbers.
5. All measurements are referenced by power supply common. Positive current flow is defined as into the terminal indicated.
6. All specifications herein apply for interchange of voltages and currents at Pins B and C.
7. Acceptance Test Sub-Group references apply to minimum and maximum limits only.
8. The NE515k has Pins 1, 3 and 9 connected to the case. The NE515G has Pins 3 and 9 open.
9. See Signetics SURE Program Bulletin No. 5001 for definition of Acceptance Test Sub-Groups. Sub-Group A-7 is used for electrical end points for Linear Products.
10. Differential Input Resistance is computed from input bias current.

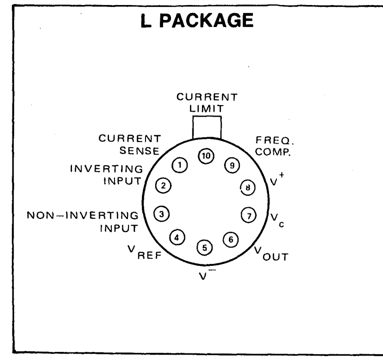
SE550-L · NE550-A, L

FEATURES

- LINE REGULATION GUARANTEED OVER INPUT VOLTAGE RANGE OF 8.5 VOLTS TO AS HIGH AS 50 VOLTS.
- OUTPUT VOLTAGE CONTINUOUSLY ADJUSTABLE FROM 2 VOLTS TO 40 VOLTS
- .01%LINE AND LOAD REGULATION
- ADJUSTABLE LIMITING OF SHORT CIRCUIT CURRENT
- FOLDBACK CURRENT LIMITING WITH ONE EXTERNAL RESISTOR
- REMOTE AND LATCHING SHUTDOWN
- OUTPUT CURRENT UP TO 150mA WITHOUT EXTERNAL POWER TRANSISTORS

PIN CONFIGURATION



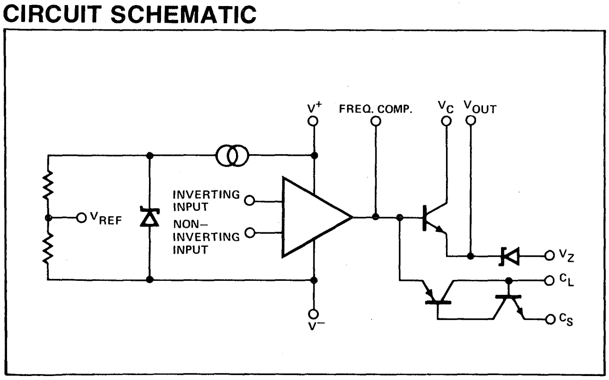


ABSOLUTE MAXIMUM RATINGS

	SE550	NE550
Voltage from V+ to V−	50V	40V
Input-Output Voltage Differential	45V	37V
Maximum Output Current	150mA	150mA
Current from V_Z	15mA	15mA
Internal Power Dissipation (Note 1)	800mW	800mW
Operating Temperature Range	−55° to +125°C	−0°C to 70°C
Storage Temperature Range	−65°C to +150°C	−65°C to +150°C
Lead Temperature	300°C	300°C

NOTE:
1. Rating applies for case temperatures to 125°C; derate linearly at 6.5mW/°C for ambient temperatures above +75°C.

CIRCUIT SCHEMATIC



ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified) (Notes 1 and 2)

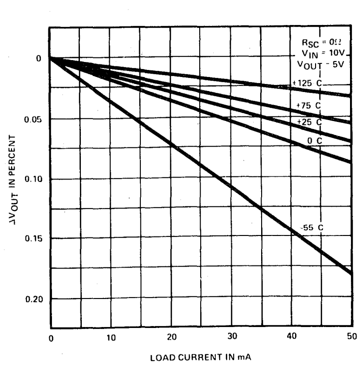
PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
NE550					
Line Regulation		.08	0.3	$\%V_{out}$	V_{in} = 8.5 to 40V
			0.35	$\%V_{out}$	0°C≤T_A≤70°C, V_{in} = 12 to 40V
Load Regulation		.03	0.2	$\%V_{out}$	IL =1mA to 50mA
			0.4	$\%V_{out}$	0°C≤T_A≤70°C, I_L = 1mA to 50mA
Ripple Rejection		75		dB	f = 50 Hz to 10 kHz, CREF = 0
		90		dB	f = 50 Hz to 10 kHz, CREF = 5μF
Average Temperature Coefficient of Output Voltage		.002	.015	%/°C	0°C≤T_A≤70°C
Short Circuit Current Limit	50	60	70	mA	RSC = 10Ω, V_{out} = 0
Reference Voltage	1.53	1.63	1.73	V	
Output Noise Voltage		20		μV rms	BW = 100 Hz to 10 kHz, CREF = 0
		2.5		μV rms	BW = 100 Hz to 10 kHz, CREF = 5μF
Long Term Stability		0.1		%/1000 hrs.	
Standby Current Drain		1.6	3.0	mA	I_L = 0, V_{in} =40V
Input Voltage Range	8.5		40	V	
Output Voltage Range	2.0		37	V	
Input Output Voltage Differential	3.0		38	V	
SE550					
Line Regulation		0.05	0.1	$\%V_{out}$	V_{in} = 12 to 40V
		0.2	0.6	$\%V_{out}$	V_{in} = 8.5 to 50V
			0.25	$\%V_{out}$	−55°C≤T_A≤+125°C, V_{in} = 12 to 40V
Load Regulation		0.03	.10	$\%V_{out}$	IL = 1mA to 50mA
			.6	$\%V_{out}$	−55°C≤T_A≤+125°C, I_L =1mAto 50mA
Ripple Rejection		75		dB	F = 50 Hz to 10 kHz, CREF = 0
		90		dB	F = 50 Hz to 10 kHz, CREF = 5μF
Average Temperature Coefficient of Output Voltage		.002	.012	%/°C	−55°C≤T_A≤+125°C
Short Circuit Limit	50	60	70	mA	RSC = 10Ω, V_{out} = 0
Reference Voltage	1.58	1.63	1.68	V	
Output Noise Voltage		20		μVrms	BW = 100 Hz to 10 kHz, CREF = 0
		2.5		μVrms	BW = 100 Hz to 10 kHz, CREF = 5μF
Long Term Stability		0.1		%/1000 hrs.	
Standby Current Drain		1.3	2.0	mA	I_L = 0, V_{in} = 50V
Input Voltage Range	8.5		50	V	
Output Voltage Range	2.0		40	V	
Input-Output Voltage Differential	3.0		45	V	

NOTES

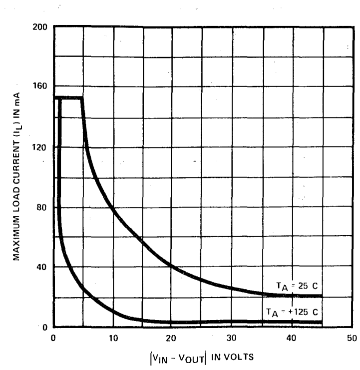
1. Unless otherwise specified, TA = 25°C, Vin = V+ = 12V, V− = OV, Vout = 5V, IL = 1mA, Rsc = 0, C1 = 100pF, and divider impedance as seen by error amplifier − 2kΩ when connected as shown in Figure 1.
2. The load and line regulation specifications are for constant junction temperature. Temperature drift effects must be taken into account separately when the unit is operating under conditions of high or varying dissipation.

TYPICAL CHARACTERISTIC CURVES

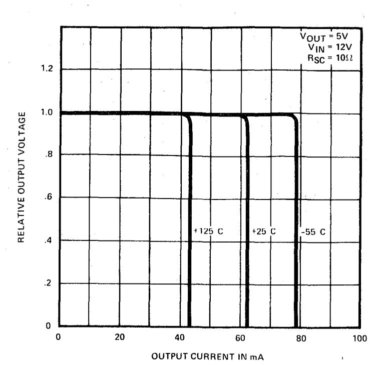
LOAD REGULATION AS A FUNCTION OF LOAD CURRENT



MAXIMUM LOAD CURRENT AS A FUNCTION OF INPUT-OUTPUT VOLTAGE DIFFERENTIAL



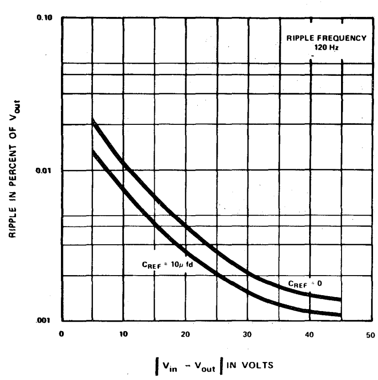
RELATIVE OUTPUT VOLTAGE AS A FUNCTION OF LIMITED OUTPUT CURRENT



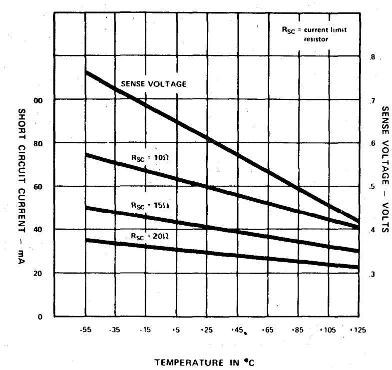
ANALOG

TYPICAL CHARACTERISTIC CURVES (CONT'D)

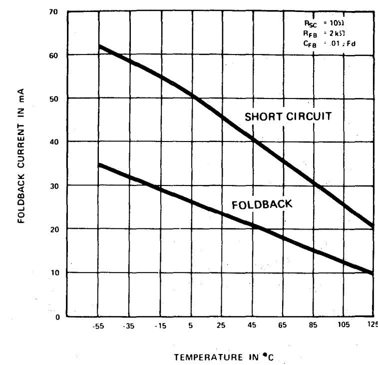
RIPPLE REJECTION AS A FUNCTION OF INPUT-OUTPUT VOLTAGE DIFFERENTIAL



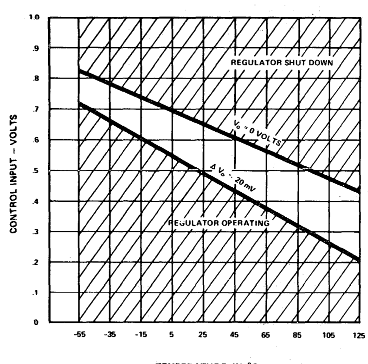
SENSE VOLTAGE AND SHORT CIRCUIT CURRENT LIMIT AS A FUNCTION OF TEMPERATURE



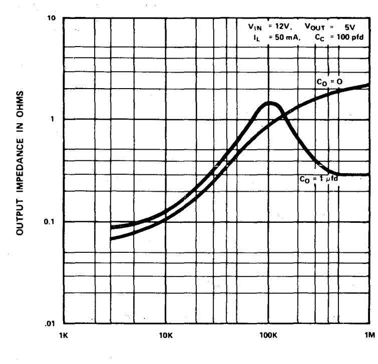
SHORT CIRCUIT AND FOLDBACK CURRENTS AS A FUNCTION OF TEMPERATURE



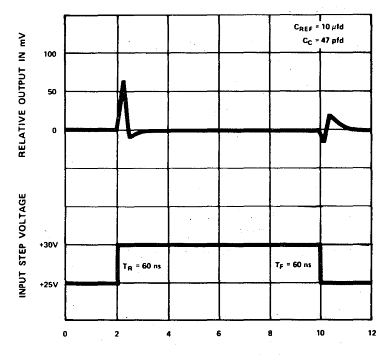
REMOTE CONTROL CHARACTERISTICS AS A FUNCTION OF TEMPERATURE



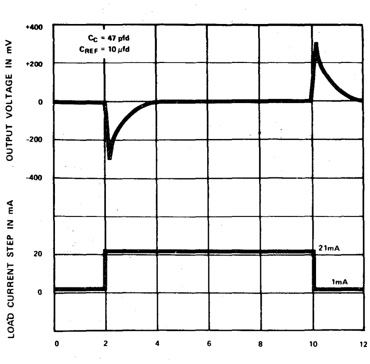
OUTPUT IMPEDANCE AS A FUNCTION OF FREQUENCY



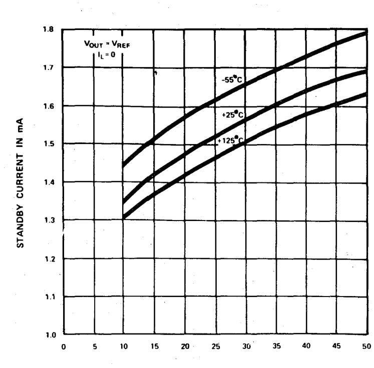
LINE TRANSIENT RESPONSE



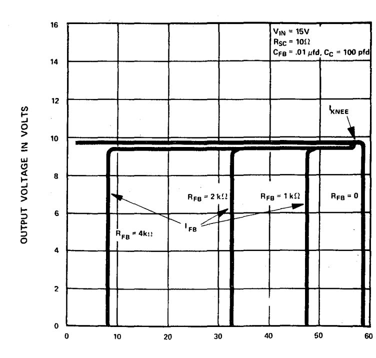
LOAD TRANSIENT RESPONSE



STANDBY CURRENT AS A FUNCTION OF INPUT VOLTAGE

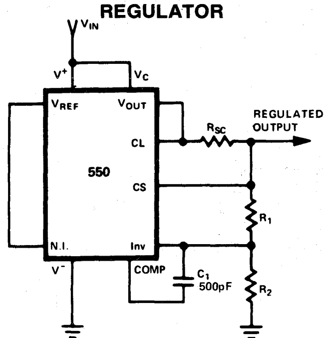


FOLDBACK CURRENT LIMITED OUTPUT VOLTAGE AS A FUNCTION OF OUTPUT CURRENT



TYPICAL APPLICATIONS

BASIC POSITIVE VOLTAGE REGULATOR

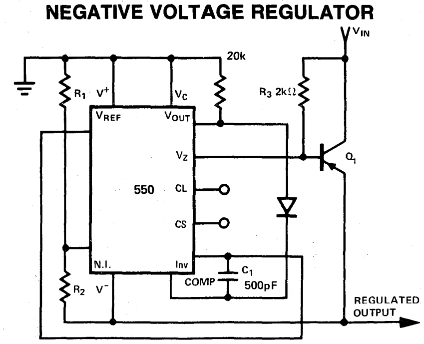


$$V_{out} = V_{REF} \frac{R_1 + R_2}{R_2} \qquad I_{SC} = \frac{V_{SENSE}}{R_{SC}}$$

$$\frac{R_1 R_2}{R_1 - R_2} = 2k\Omega \text{ for minimum temperature drift}$$

FIGURE 1

NEGATIVE VOLTAGE REGULATOR



$$V_{out} = -V_{REF} X \frac{R_1 + R_2}{R_2}$$

$$\frac{R_1 R_2}{R_1 + R_2} = 2k\Omega \text{ for minimum temperature drift}$$

NOTE 1

FIGURE 2

POSITIVE VOLTAGE REGULATOR (External PNP Pass Transistor)

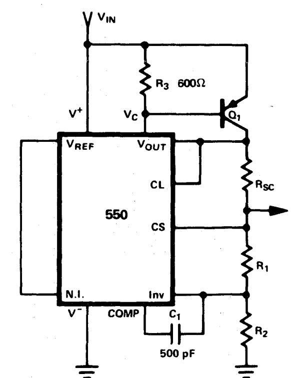


FIGURE 3

POSITIVE VOLTAGE REGULATOR (External NPN Pass Transistor)

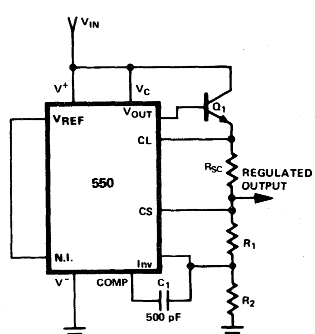
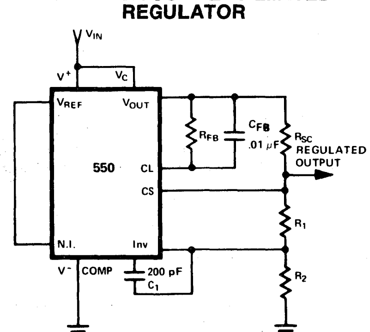


FIGURE 4

FOLDBACK CURRENT LIMITED REGULATOR



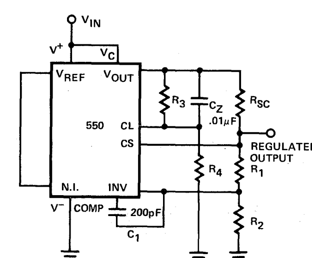
$$I_{KNEE} = \frac{V_{SENSE}}{R_{SC}}$$

$$I_{FB} = \frac{V_{SENSE} - (R_{FB} \cdot I_{CL})}{R_{SC}}$$

$I_{CL} = 125\ \mu A$

FIGURE 5A

SECOND ORDER FOLDBACK CURRENT LIMITED REGULATOR



$$R_3 = \frac{V_{SENSE} (I_{KNEE} - I_{FB}) V_{OUT}}{I_{CL} [(I_{KNEE} - I_{FB} + I_{SC}) V_{OUT} - (I_{FB} - I_{SC}) V_{SENSE}]}$$

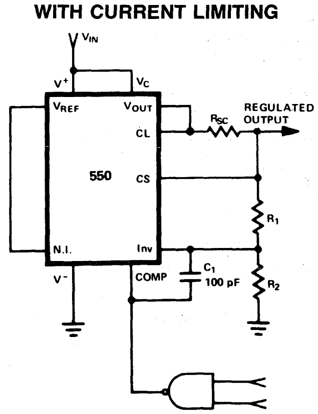
$$\frac{R_3}{R_4} = \frac{(V_{SENSE} - I_{CL} R_3)(I_{FB} - I_{SC})}{V_{OUT} I_{SC} - V_{SENSE} (I_{FB} - I_{SC})}$$

$$R_{SC} = \frac{(V_{OUT} + V_{SENSE}) R_3/R_4 + V_{SENSE}}{I_{KNEE}}$$

$I_{CL} = 125\mu A$

FIGURE 5B

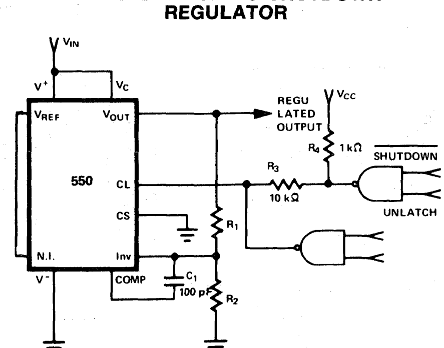
REMOTE SHUTDOWN REGULATOR WITH CURRENT LIMITING



1/4 8T80, 1/6 8T90, 1/10 8T01B, etc.

FIGURE 6

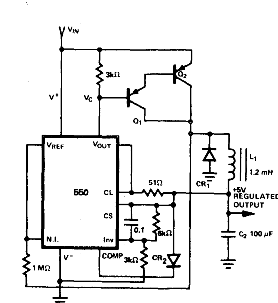
REMOTE LATCHING SHUTDOWN REGULATOR



8415, 8417, 2/3 8471, 1/3 8891, 8T90, 1/2 8481, 8881, 8T90
NOTE 2

FIGURE 7

POSITIVE SWITCHING REGULATOR



L_1 is 50 turns of # 22 wire wound on Ferroxcube. 42/29-377 A400

FIGURE 8

TYPICAL APPLICATIONS (CONT'D)

POSITIVE FLOATING REGULATOR

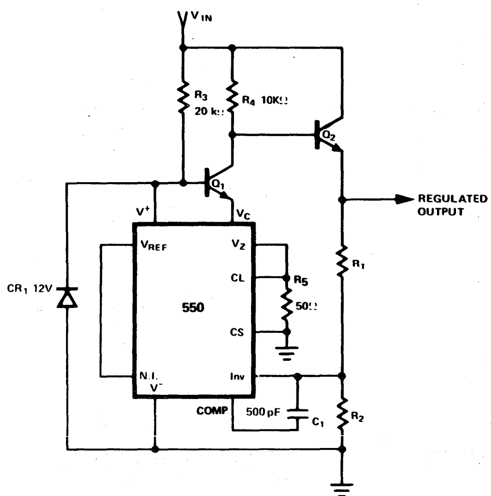


FIGURE 9

NEGATIVE FLOATING REGULATOR

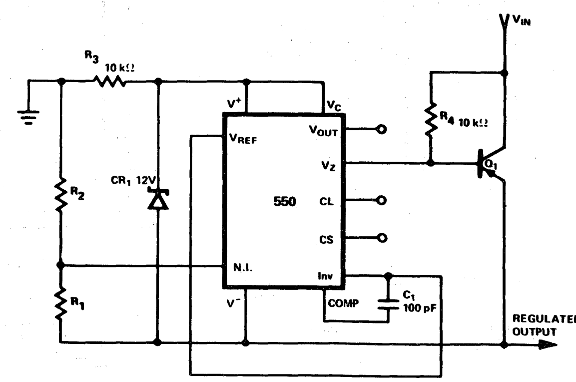
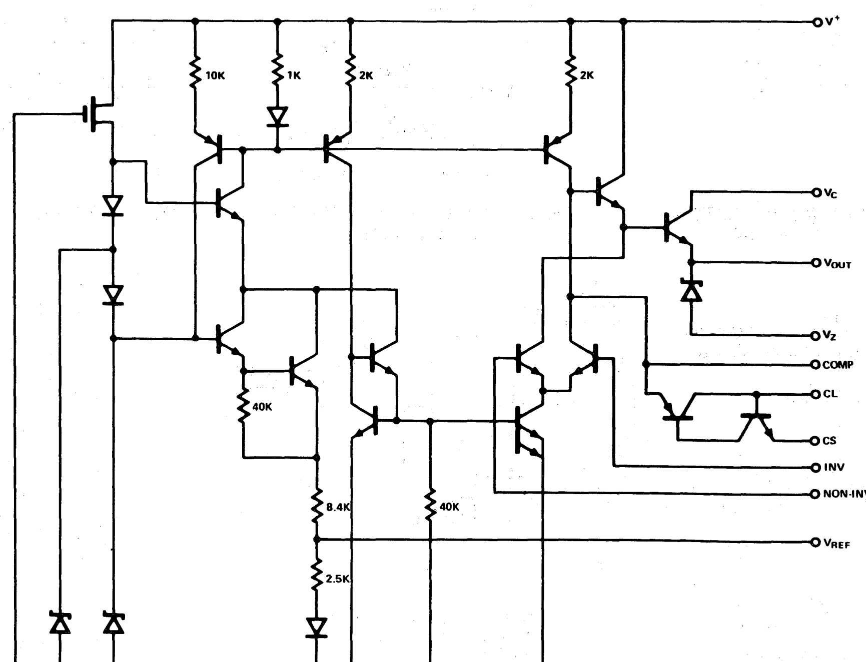


FIGURE 10

NOTES:
1. To utilize the SE550L in applications which require Vz, an external 6.2 volt zener diode should be connected in series with VOUT.
2. The "Shut-down" gate need only be pulsed to latch the regulator output to zero. R4 may be omitted for active pull-up devices. The "Unlatch" gate must have an open collector.

EQUIVALENT CIRCUIT

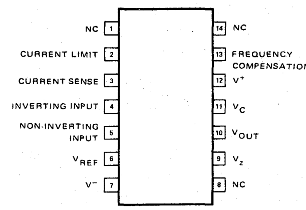


FEATURES

- POSITIVE OR NEGATIVE SUPPLY OPERATION
- SERIES, SHUNT, SWITCHING OR FLOATING OPERATION
- .01% LINE AND LOAD REGULATION
- OUTPUT VOLTAGE ADJUSTABLE FROM 2 TO 37 VOLTS
- OUTPUT CURRENT TO 150mA WITHOUT EXTERNAL PASS TRANSISTOR

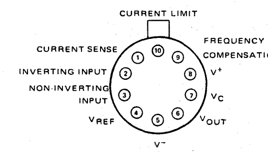
PIN CONFIGURATION

A PACKAGE



ORDER PART NOS. μA723A/μA723CA

L PACKAGE

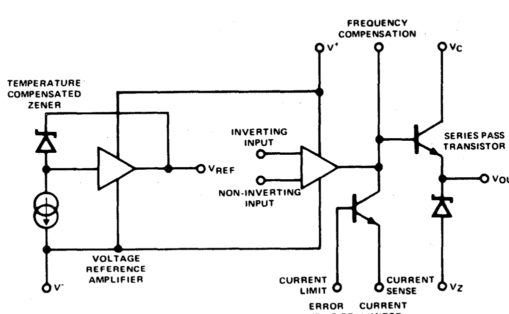


ORDER PART NOS. μA723L/μA723CL

ABSOLUTE MAXIMUM RATINGS

	μA723	μA723C
Pulse Voltage from V+ to V− (50ms)	50V	
Continuous Voltage from V+ to V−	40V	40V
Input-Output Voltage Differential	40V	40V
Maximum Output Current	150mA	150mA
Current from V_{REF}	15mA	
Current from V_Z		25mA
Internal Power Dissipation (Note 1)	800mW	800mW
Operating Temperature Range	−55 to +125°C	0 to 70°C
Storage Temperature Range	−65°C to +150°C	−65°C to +150°C
Lead Temperature	300°C	300°C

EQUIVALENT CIRCUIT



ELECTRICAL CHARACTERISTICS ($T_A = 25°C$ unless otherwise specified — Note 1)

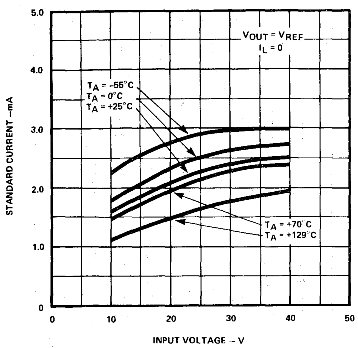
PARAMETER (See definitions)	TEST CONDITIONS	MIN	TYP	MAX	UNITS
				μA723C	
Line Regulation (Note 2)	V_{in} = 12V to V_{in} = 15V		0.01	0.1	% V_{out}
	V_{in} = 12V to V_{in} = 40V		0.1	0.5	% V_{out}
Load Regulation (Note 2)	I_L = 1mA to I_L = 50mA		0.03	0.2	% V_{out}
Ripple Rejection	f = 50 Hz to 10 kHz, C_{REF} = 0		74		dB
	f = 50 Hz to 10 kHz, C_{REF} = 5μF		86		dB
Short Circuit Current Limit	R_{SC} = 10Ω, V_{out} = 0		65		mA
Reference Voltage		6.80	7.15	7.50	V
Output Noise Voltage	BW = 100 Hz to 10 kHz, C_{REF} = 0		20		μV rms
	BW = 100 Hz to 10 kHz, C_{REF} = 5μF		2.5		μV rms
Long Term Stability			0.1	0.1	%/1000 hrs.
Standby Current Drain	I_L = 0, V_{in} = 30V		2.3	4.0	mA
Input Voltage Range		9.5		40	V
Output Voltage Range		2.0		37	V
Input-Output Voltage Differential		3.0		38	V
The Following Specifications Apply Over the Operating Temperature Ranges					
Line Regulation				0.3	%V_{out}
Load Regulation				0.6	%V_{out}
Average Temperature Coefficient of Output Voltage	V_{in} = 12V to V_{in} = 15V; I_L = 1mA to I_L = 50mA		0.003	0.015	%/°C
				μA723	
Line Regulation (Note 2)	V_{in} = 12V to V_{in} = 15V		0.01	0.1	%V_{out}
	V_{in} = 12V to V_{in} = 40V		0.02	0.2	%V_{out}
Load Regulation (Note 2)	I_L = 1mA to I_L = 50mA		0.03	0.15	%V_{out}
Ripple Rejection	f = 50 Hz to 10 kHz, C_{REF} = 0		74		dB
	f = 50 Hz to 10 kHz, C_{REF} = 5μF		86		dB
Short Circuit Current Limit	R_{SC} = 10Ω, V_{out} = 0		65		mA
Reference Voltage		6.95	7.15	7.35	V
Output Noise Voltage	BW = 100 Hz to 10 kHz, C_{REF} = 0		20		μV rms
	BW = 100 Hz to 10 kHz, C_{REF} = 5μF		2.5		μV rms
Long Term Stability			0.1		%/1000 hrs
Standby Current Drain	I_L = 0, V_{in} = 30V		2.3	3.5	mA
Input Voltage Range		9.5		40	V
Output Voltage Range		2.0		37	V
Input-Output Voltage Differential		3.0		38	V
The Following Specifications Apply Over the Operating Temperature Ranges					
Line Regulation				0.3	%V_{out}
Load Regulation				0.6	%V_{out}
Average Temperature Coefficient of Output Voltage	V_{in} = 12V to V_{in} = 15V; I_L = 1mA to I_L = 50mA		0.002	0.015	%/°C

NOTES

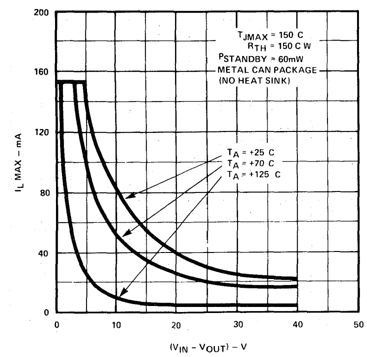
1. Unless otherwise specified, T_A = 25°C, V_{in} = V+ = Vc = 12V, V− = 0V, V_{out} = 5V, I_L = 1mA, R_{SC} = 0, C_1 = 100pF, C_{REF} = 0 and divider impedance as seen by error amplifier ≤ 10kΩ when connected as shown in Figure 3.
2. The load and line regulation specifications are for constant junction temperature. Temperature drift effects must be taken into account separately when the unit is operating under conditions of high dissipation.

TYPICAL CHARACTERISTIC CURVES

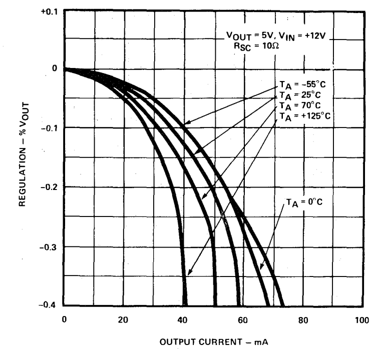
STANDBY CURRENT DRAIN AS A FUNCTION OF INPUT VOLTAGE



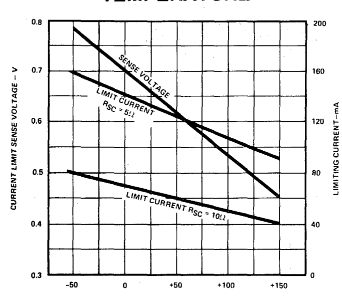
MAXIMUM LOAD CURRENT AS A FUNCTION OF INPUT-OUTPUT VOLTAGE DIFFERENTIAL



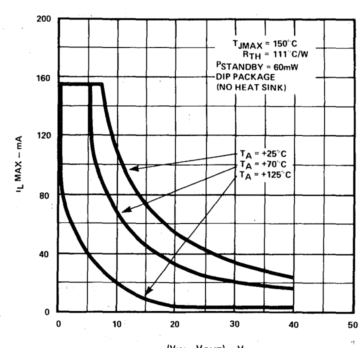
LOAD REGULATION CHARACTERISTICS WITH CURRENT LIMITING



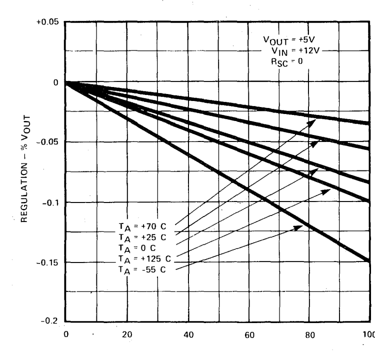
CURRENT LIMITING CHARACTERISTICS AS A FUNCTION OF JUNCTION TEMPERATURE



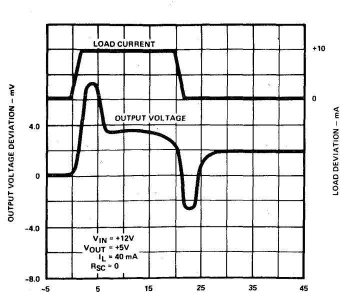
MAXIMUM LOAD CURRENT AS A FUNCTION OF INPUT-OUTPUT VOLTAGE DIFFERENTIAL



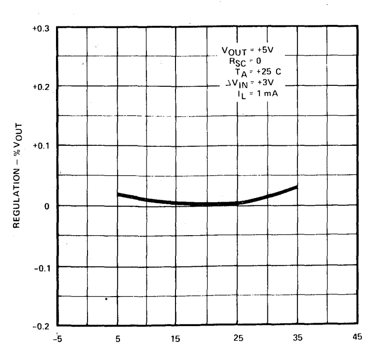
LOAD REGULATION CHARACTERISTICS WITHOUT CURRENT LIMITING



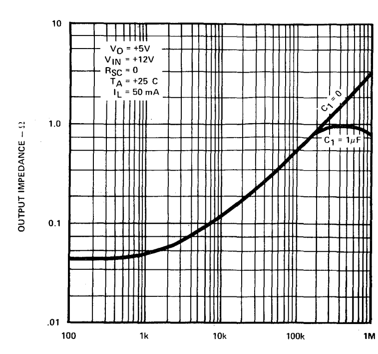
LOAD TRANSIENT RESPONSE



LINE REGULATION AS A FUNCTION OF INPUT-OUTPUT VOLTAGE DIFFERENTIAL



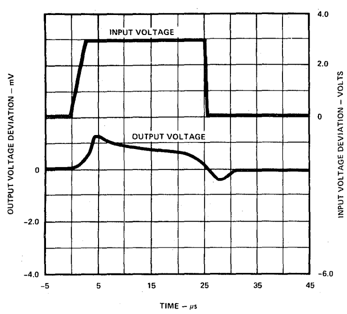
OUTPUT IMPEDANCE AS A FUNCTION OF FREQUENCY



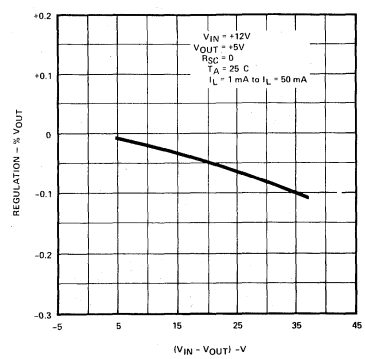
ANALOG

TYPICAL CHARACTERISTIC CURVES (CONT'D)

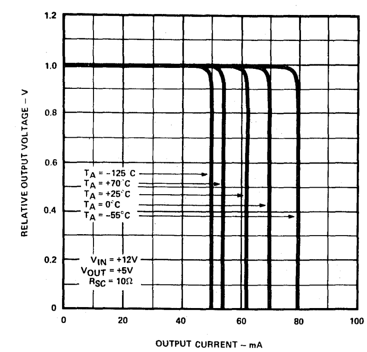
LINE TRANSIENT RESPONSE



LOAD REGULATION AS A FUNCTION OF INPUT-OUTPUT VOLTAGE DIFFERENTIAL

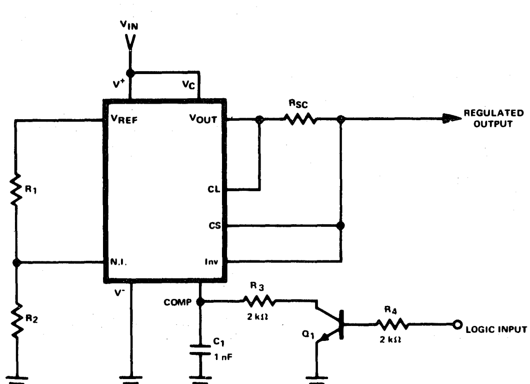


CURRENT LIMITING CHARACTERISTICS



APPLICATIONS

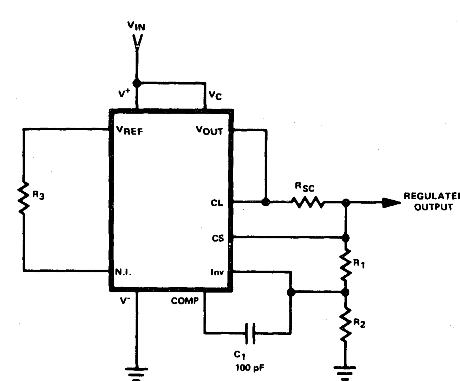
REMOTE SHUTDOWN REGULATOR WITH CURRENT LIMITING (V_{out} = 2 to 7 Volts)



$$V_{out} = \left[V_{REF} \times \frac{R_2}{R_1 + R_2}\right]$$

FIGURE 1

HIGH VOLTAGE REGULATOR (V_{out} = 7 to 37 Volts)



$$V_{out} = \left[V_{REF} \times \frac{R_1 + R_2}{R_2}\right]$$

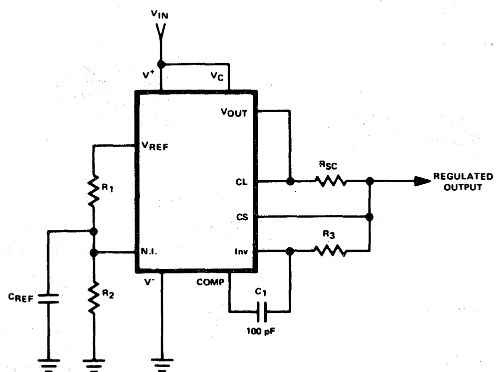
$$R_3 = \frac{R_1 R_2}{R_1 + R_2}$$ for minimum temperature drift

R_3 may be eliminated for minimum component count

FIGURE 2

APPLICATIONS (CONT'D)

LOW VOLTAGE REGULATOR (V_{out} = 2 to 7 Volts)

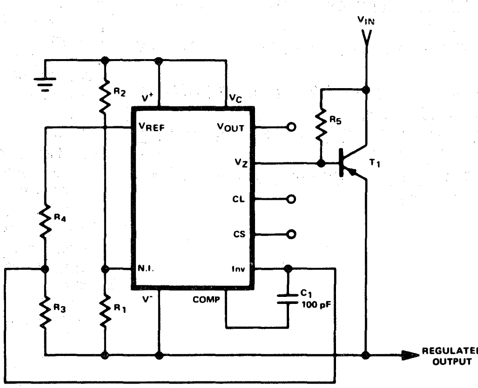


$$V_{out} = \left[V_{REF} \times \frac{R_2}{R_1 + R_2}\right]$$

$$R_3 = \frac{R_1 \ R_2}{R_1 + R_2}$$ for minimum temperature drift

FIGURE 3

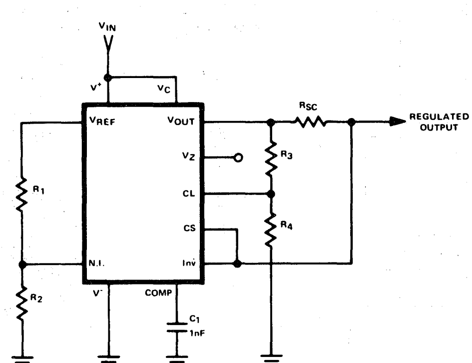
NEGATIVE VOLTAGE REGULATOR

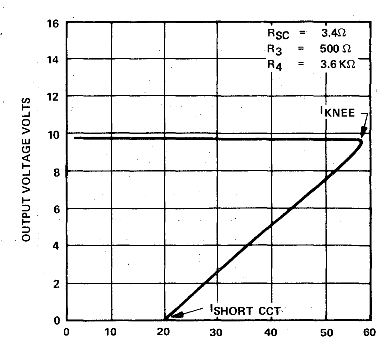


$$V_{out} = \left[\frac{V_{REF}}{2} \times \frac{R_1 + R_2}{R_1}\right]; \quad R_3 = R_4$$

FIGURE 4

FOLDBACK CURRENT LIMITING REGULATOR (Vout = 2 to 7 Volts)





$$I_{KNEE} = \left[\frac{V_{out} R_3}{R_{sc} R_4} + \frac{V_{SENSE}(R_3 + R_4)}{R_{sc} R_4}\right]$$

$$V_{out} = \left[V_{REF} \times \frac{R_1 + R_2}{R_2}\right]$$

$$I_{SHORT\ CKT} = \left[\frac{V_{SENSE}}{R_{sc}} \times \frac{R_3 + R_4}{R_4}\right]$$

$$\frac{R_4}{R_3} = \frac{V_{OUT} \ I_{SC}}{V_{SENSE} \ (I_{KNEE} - I_{SHORTCKT})} - 1$$

$$R_{SC} = \frac{V_{SENSE}}{I_{SC}}\left[1 + \frac{R_3}{R_4}\right]$$

FIGURE 5

FEATURES

- OUTPUT CURRENT IN EXCESS OF 1 AMP
- NO EXTERNAL COMPONENTS
- INTERNAL THERMAL OVERLOAD PROTECTION
- INTERNAL SHORT CIRCUIT CURRENT LIMITING
- OUTPUT TRANSISTOR SAFE-AREA COMPENSATION
- AVAILABLE IN THE TO-220 AND THE TO-3 PACKAGE
- OUTPUT VOLTAGES OF 5, 6, 8, 12, 15, 18, AND 24 VOLTS

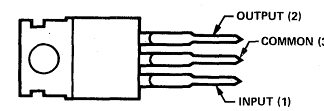
ABSOLUTE MAXIMUM RATINGS

Input Voltage (5V through 18V)	35V
(24V)	40V
Internal Power Dissipation (Note 1)	Internally Limited
Storage Temperature Range	−65°C to +150°C
Operating Junction Temperature Range (Note 2)	
7800	−55°C to +150°C
7800C	0°C to +125°C
Lead Temperature	
TO-3 Package (Soldering, 60 second time limit)	300°C
TO-220 Package (Soldering, 10 second time limit)	230°C

NOTES:
1. Thermal resistance of the packages (without a heat sink)
   Junction to Case: TO-3 Package 4° C/W; TO-220 Package 2°C/W
   Junction to Ambient: TO-3 Package 35°C/W; TO-220 Package 50°C/W
2. Operating Ambient Temperature Range
   7800 −55°C to +125°C
   7800C 0°C to +85°C

PIN CONFIGURATION

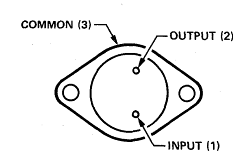
TO-220 PACKAGE
PACKAGE OUTLINE U



ORDER INFORMATION

OUTPUT VOLTAGE	ORDER PART NO.
5V	7805CU
6V	7806CU
8V	7808CU
12V	7812CU
15V	7815CU
18V	7818CU
24V	7824CU

TO-3 PACKAGE
PACKAGE OUTLINE DA

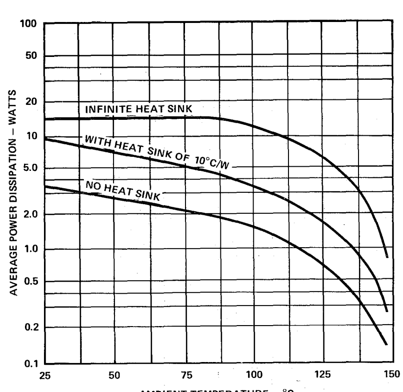


ORDER INFORMATION

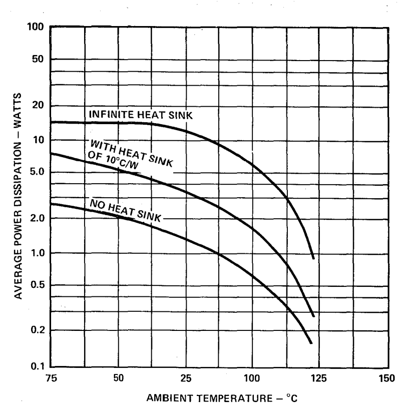
OUTPUT VOLTAGE	ORDER PART NO.
5V	7805DA
6V	7806DA
8V	7808DA
12V	7812DA
15V	7815DA
18V	7818DA
24V	7824DA
5V	7805CDA
6V	7806CDA
8V	7808CDA
12V	7812CDA
15V	7815CDA
18V	7818CDA
24V	7824CDA

TYPICAL CURVES

MAXIMUM AVERAGE POWER DISSIPATION AS A FUNCTION OF AMBIENT TEMPERATURE (TO-3, 7800)



MAXIMUM AVERAGE POWER DISSIPATION AS A FUNCTION OF AMBIENT TEMPERATURE (TO-3, 7800C)



ELECTRICAL CHARACTERISTICS I_{OUT} = 500mA, −55°C ≤T_J≤150°C (Unless Otherwise Noted)

PARAMETER UNITS	7805			7805C			7806			7806C			7808		
TEST CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
V_{OUT} (V)	V_{IN}=10V			V_{IN}=10V			V_{IN}=IIV			V_{IN}=IIV			V_{IN}=14V		
	4.8	5.0	5.2	4.8	4.0	5.2	5.75	6.0	6.25	5.75	6.0	6.25	7.7	8.0	8.3
T_J=25°C P≤15W 5mA≤I_{OUT}≤1.0A	8V≤V_{IN}≤20V			7V≤V_{IN}≤25V			9V≤V_{IN}≤21V			8V≤V_{IN}≤25V			11.5V≤V_{IN}≤23V		
	4.65		5.35	4.75		5.25	5.65		6.35	5.7		6.3	7.6		8.4
LINE REGULATION mV T_J=25°C	7V≤V_{IN}≤25V			7V≤V_{IN}≤25V			8V≤V_{IN}≤25V			8V≤V_{IN}≤25V			10.5V≤V_{IN}≤25V		
		3	50		3	100		5	60		5	120		6	80
	8V≤V_{IN}≤12V			8V≤V_{IN}≤12V			9V≤V_{IN}≤13V			9V≤V_{IN}≤13V			11V≤V_{IN}≤17V		
		1	25		1	50		1.5	30		1.5	60		2	40
LOAD REGULATION mV T_J=25°C 5mA≤I_{OUT}≤1.5A		15	50		15	100		14	60		14	120		12	80
250mA I_{OUT} 750mA		5	25		5	50		4	30		4	60		4	40
I_{CC} mA		4.2	6.0		4.2	8.0		4.3	6.0		4.3	8.0		4.3	6.0
with line T_J=25°C	8V≤V_{IN}≤25V		0.8	7V≤V_{IN}≤25V		1.3	9V≤V_{IN}≤25V		0.8	8V≤V_{IN}≤V		1.3	11.5≤V_{IN}≤25V		0.8
with load 5mA≤I_{OUT}≤1.0A			0.5			0.5			0.5			0.5			0.5
OUTPUT NOISE VOLTAGE uV T_J=25°C 10Hz≤f≤ 100kHz		40			40			45			45			52	
VOLTAGE DRIFT mV/1000HR			20			20			24			24			32
RIPPLE REJECTION dB f=120Hz	8V≤V_{IN}≤18V			8V≤V_{IN}≤18V			9V≤V_{IN}≤19V			9V≤V_{IN}≤19V			11.5V≤V_{IN}≤21.5V		
	68	78		62	78		65	75		59	75		62	72	
DROPOUT VOLTAGE V T_J=25°C I_{OUT}=1.0A		2.0			2.0			2.0			2.0			2.0	
OUTPUT RESISTANCE mΩ f=1kHz		17			17			19			19			16	
I_{OS} mA T_J=25°C		750			750			550			550			450	
PEAK OUTPUT CURRENT A T_J=25°C		2.2			2.2			2.2			2.2			2.2	
V_{OUT} OUTPUT TEMPERATURE DRIFT mV/°C I_{OUT}=5mA	0°C≤T_J≤150°C			0°C≤T_J≤125°C			0°C≤T_J≤150°C			0°C≤T_J≤125°C			0°C≤T_J≤150°C		
		−1.1			−1.1			−0.8			−0.8			−0.8	

ELECTRICAL CHARACTERISTICS (CONT'D)

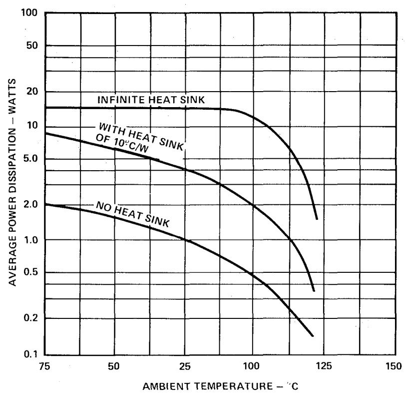
PARAMETER UNITS TEST CONDITIONS	7808C	7812	7812C	7815	7815C
	MIN TYP MAX	MIN TYP MAX	MIN TYP MAX	MIN TYP MAX	MIN TYP MAX
V_{OUT} (V) T_J=25°C P≤15W 5mA≤I_{OUT}≤1.0A	V_{IN}=14V 7.7 8.0 8.3 10.5V≤V_{IN}≤23V 7.6 8.4	V_{IN}=19V 11.5 12.0 12.5 15.5V≤V_{IN}≤27V 11.4 12.6	V_{IN}=19V 11.5 12.0 12.5 14.5V≤V_{IN}≤27V 11.4 12.6	V_{IN}=23V 14.4 15.0 15.6 18.5V≤V_{IN}≤30V 14.25 15.75	V_{IN}=23V 14.4 15.0 15.6 17.5V≤V_{IN}≤30V 14.25 15.75
LINE REGULATION mV T_J=25°C	10.5V≤V_{IN}≤25V 6 160 11V≤V_{IN}≤17V 2 80	14.5V≤V_{IN}≤30V 10 120 16V≤V_{IN}≤22V 3 60	14.5V≤V_{IN}≤30V 10 240 16V≤V_{IN}≤22V 3 120	17.5V≤V_{IN}≤30V 11 150 20V≤V_{IN}≤26V 3 75	17.5V≤V_{IN}≤30V 11 300 20V≤V_{IN}≤26V 3 150
LOAD REGULATION mV T_J=25°C 5mA≤I_{OUT}≤1.5A 250mA I_{OUT} 750mA	12 160 4 80	12 120 4 60	12 240 4 120	12 150 4 75	12 150 4 75
I_{CC} mA	4.3 8.0	4.3 6.0	4.3 8.0	4.4 6.0	4.4 8.0
with line T_J=25°C	10.5V≤V_{IN}≤25V 1.0	15≤V_{IN}≤30V 0.8	14.5V≤V_{IN}≤30V 1.0	18.5V≤V_{IN}≤30V 0.8	17.5V≤V_{IN}≤30V 1.0
with load 5mA≤I_{OUT}≤1.0A	0.5	0.5	0.5	0.5	0.5
OUTPUT NOISE VOLTAGE uV T_J=25°C 10Hz≤f≤100kHz	52	75	75	90	90
VOLTAGE DRIFT mV /1000HR	32	48	48	60	60
RIPPLE REJECTION dB f=120Hz	11.5V≤V_{IN}≤21.5V 56 72	15V≤V_{IN}≤25V 61 71	15V≤V_{IN}≤25V 61 71	18.5V≤V_{IN}≤28.5V 60 70	18.5V≤V_{IN}≤28.5V 60 70
DROPOUT VOLTAGE V T_J=25°C I_{OUT}=1.0A	2.0	2.0	2.0	2.0	2.0
OUTPUT RESISTANCE mΩ f=1kHz	16	18	18	19	19
I_{OS} mA T_J=25°C	450	350	350	230	230
PEAK OUTPUT CURRENT A T_J=25°C	2.2	2.2	2.2	2.1	2.1
V_{OUT} OUTPUT TEMPERATURE DRIFT mV/°C I_{OUT}=5mA	0°C≤T_J≤125°C −0.8	0°C≤T_J≤150°C −1.0	0°C≤T_J≤125°C −1.0	0°C≤T_J≤150°C −1.0	0°C≤T_J≤125°C −1.0

ELECTRICAL CHARACTERISTICS (CONT'D)

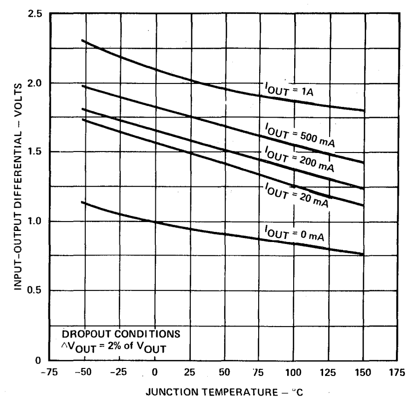
PARAMETER UNITS / TEST CONDITIONS	7818 MIN	7818 TYP	7818 MAX	7818C MIN	7818C TYP	7818C MAX	7824 MIN	7824 TYP	7824 MAX	7824C MIN	7824C TYP	7824C MAX
V_{OUT} (V)		$V_{IN}=27V$			$V_{IN}=27V$			$V_{IN}=33V$			$V_{IN}=33V$	
$T_J=25°C$	17.3	18.0	18.7	17.3	18.0	18.7	23.0	24.0	25.0	23.0	24.0	25.0
$P \leq 15W$		$22V \leq V_{IN} \leq 33V$			$21V \leq V_{IN} \leq 33V$			$28V \leq V_{IN} \leq 38V$			$28V \leq V_{IN} \leq 38V$	
$5mA \leq I_{OUT} \leq 1.0A$	17.1		18.9	17.1		18.9	22.8		25.2	22.8		25.2
LINE REGULATION mV		$21V \leq V_{IN} \leq 33V$			$21V \leq V_{IN} \leq 33V$			$27V \leq V_{IN} \leq 38V$			$27V \leq V_{IN} \leq 38V$	
		15	180		15	360		18	240		18	480
$T_J=25°C$		$24V \leq V_{IN} \leq 30V$			$24V \leq V_{IN} \leq 30V$			$30V \leq V_{IN} \leq 36V$			$30V \leq V_{IN} \leq 36V$	
		5	90		5	180		6	120		6	240
LOAD REGULATION mV, $T_J=25°C$												
$5mA \leq I_{OUT} \leq 1.5A$		12	180		12	360		12	240		12	480
250mA I_{OUT} 750mA		4	90		4	180		4	120		4	240
I_{CC} mA		4.5	6.0		4.5	8.0		4.6	6.0		4.6	8.0
with line		$22V \leq V_{IN} \leq 33V$			$21V \leq V_{IN} \leq 33V$			$28V \leq V_{IN} \leq 38V$			$27V \leq V_{IN} \leq 38V$	
$T_J=25°C$			0.8			1.0			0.8			1.0
with load $5mA \leq I_{OUT} \leq 1.0A$			0.5			0.5			0.5			0.5
OUTPUT NOISE VOLTAGE uV, $T_J=25°C$, $10Hz \leq f \leq 100kHz$		110			110			170			170	
VOLTAGE DRIFT mV/1000HR			72			72			96			96
RIPPLE REJECTION dB		$22V \leq V_{IN} \leq 32V$			$22V \leq V_{IN} \leq 32V$			$28V \leq V_{IN} \leq 38V$				
f=120Hz	59	69		59	69		56	66		56	66	
DROPOUT VOLTAGE V, $T_J=25°C$, $I_{OUT}=1.0A$		2.0			2.0			2.0			2.0	
OUTPUT RESISTANCE mΩ, f=1kHz		22			22			28			28	
I_{OS} mA, $T_J=25°C$		200			200			150			150	
PEAK OUTPUT CURRENT A, $T_J=25°C$		2.1			2.1			2.1			2.1	
V_{OUT} OUTPUT TEMPERATURE DRIFT mV/°C		$0°C \leq T_J \leq 150°C$			$0°C \leq T_J \leq 125°C$			$0°C \leq T_J \leq 150°C$			$0°C \leq T_J \leq 125°C$	
$I_{OUT}=5mA$		−1.0			−1.0			−1.5			−1.5	

TYPICAL CURVES (CONT'D)

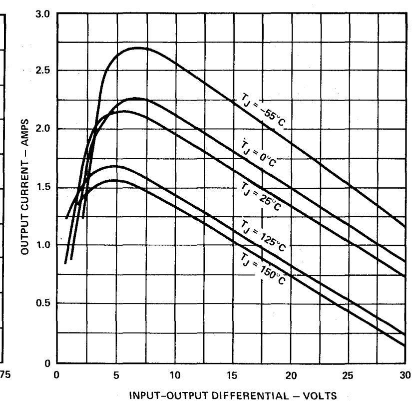
MAXIMUM AVERAGE POWER DISSIPATION AS A FUNCTION OF AMBIENT TEMPERATURE (TO-220, 7800C)



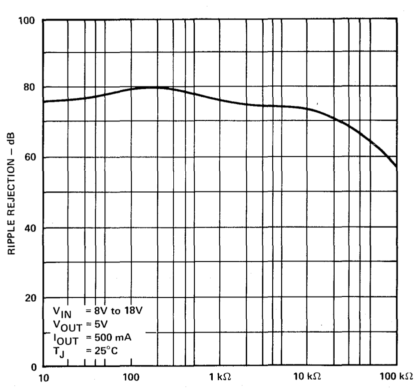
DROPOUT VOLTAGE AS A FUNCTION OF JUNCTION TEMPERATURE



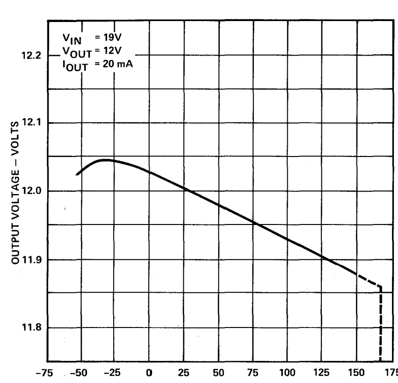
PEAK OUTPUT CURRENT AS A FUNCTION OF INPUT/OUTPUT DIFFERENTIAL VOLTAGE



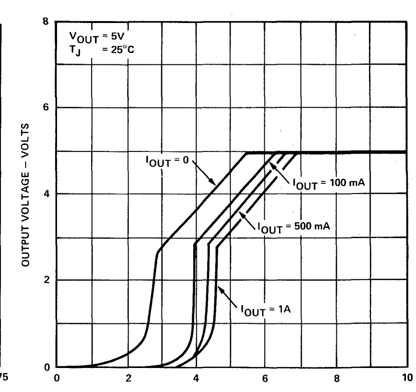
RIPPLE REJECTION AS A FUNCTION OF FREQUENCY



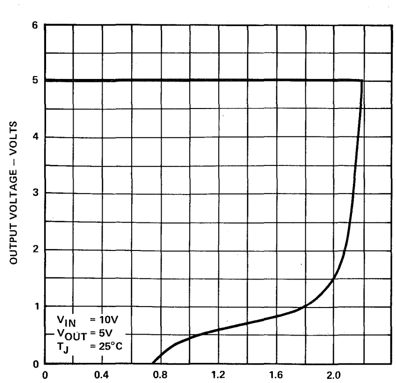
OUTPUT VOLTAGE AS A FUNCTION OF JUNCTION TEMPERATURE



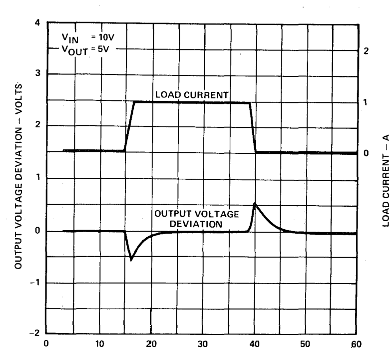
DROPOUT CHARACTERISTICS



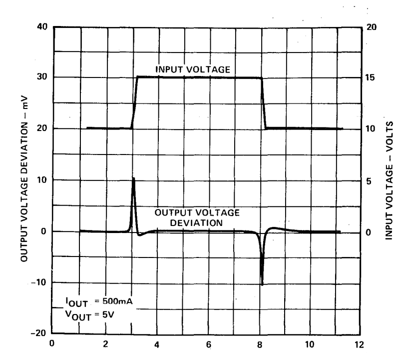
CURRENT LIMITING CHARACTERISTICS



LOAD TRANSIENT RESPONSE

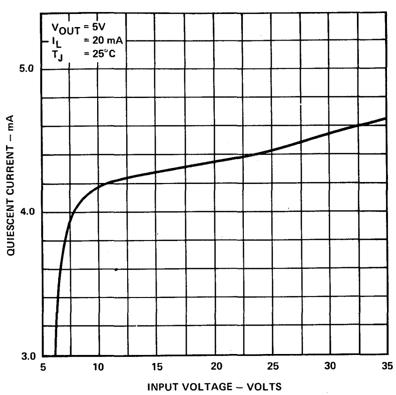


LINE TRANSIENT RESPONSE

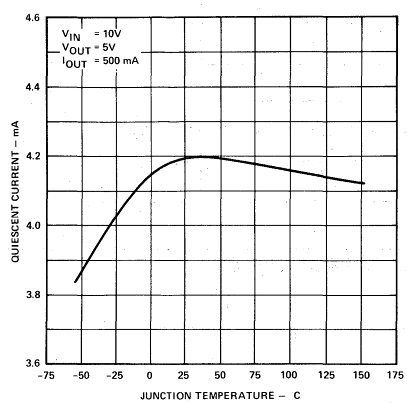


TYPICAL CURVES (CONT'D)

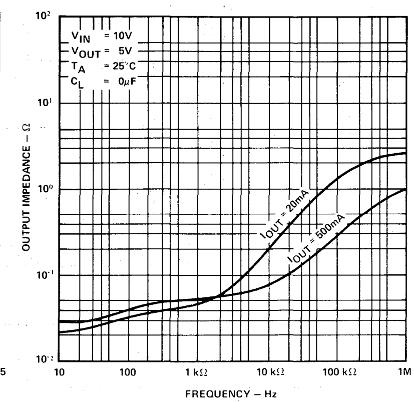
QUIESCENT CURRENT AS A FUNCTION OF INPUT VOLTAGE



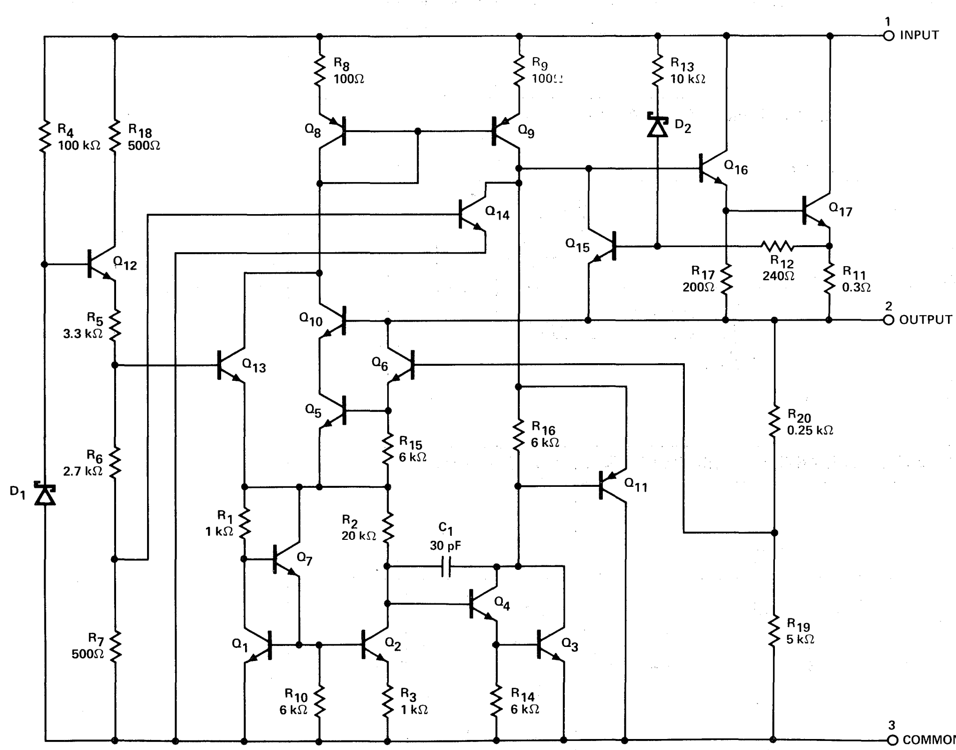
QUIESCENT CURRENT AS A FUNCTION OF TEMPERATURE



OUTPUT IMPEDANCE AS A FUNCTION OF FREQUENCY

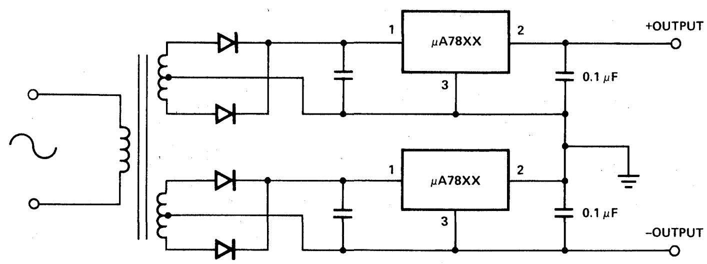


SCHEMATIC DIAGRAM

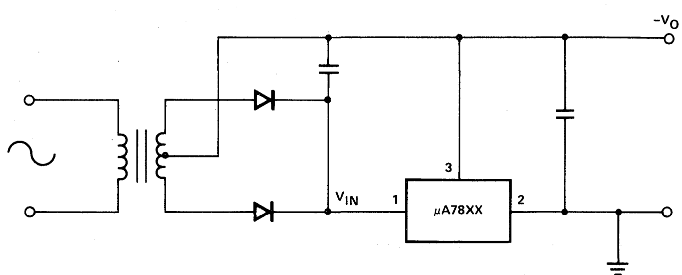


APPLICATIONS

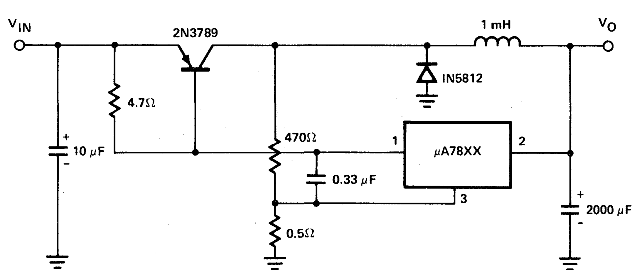
POSITIVE AND NEGATIVE REGULATOR



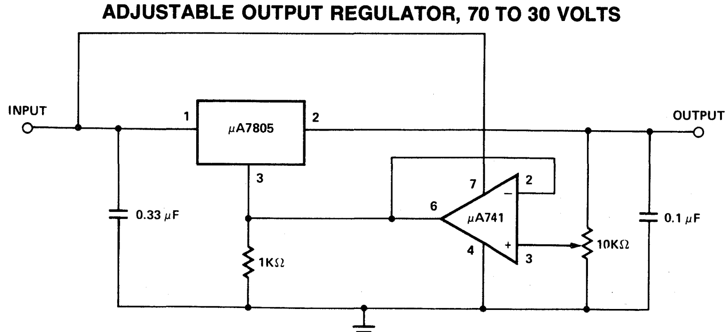
NEGATIVE OUTPUT VOLTAGE CIRCUIT



SWITCHING REGULATOR

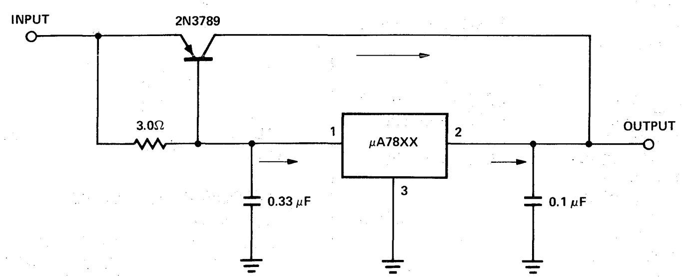


ADJUSTABLE OUTPUT REGULATOR, 70 TO 30 VOLTS

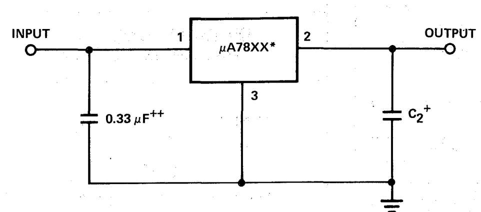


APPLICATIONS (CONT'D)

HIGH CURRENT VOLTAGE REGULATOR

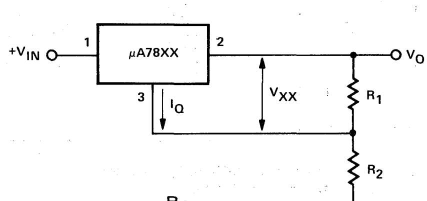


FIXED OUTPUT REGULATOR



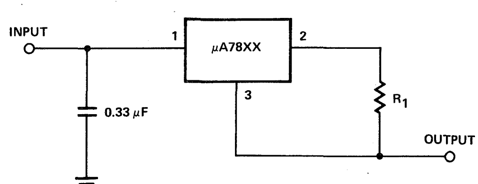
NOTES:
* To specify an output voltage, substitute voltage value for "XX".
+Although no output capacitor is needed for stability, it does improve transient response.
++Required if regulator is located an appreciable distance from power supply filter.

CIRCUIT FOR INCREASING OUTPUT VOLTAGE



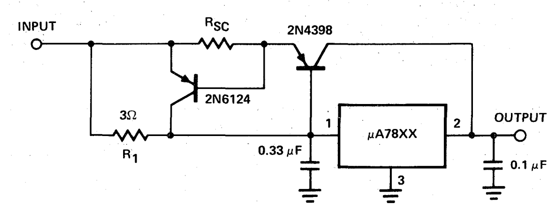
$$V_O = V_{XX}\left(1 + \frac{R_2}{R_1}\right) + I_Q R_2$$

CURRENT REGULATOR

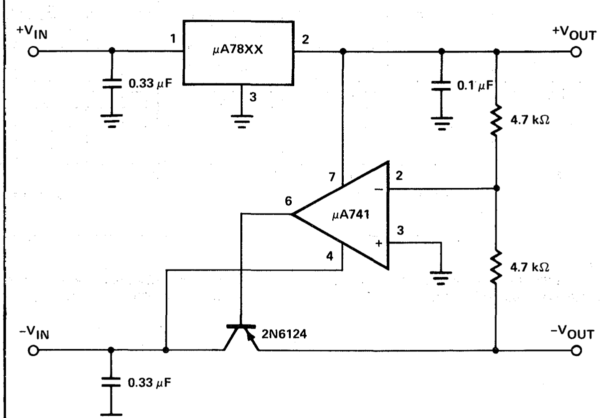


$$\text{Output Current} = \frac{V_{OUT}}{R1}$$

HIGH OUTPUT CURRENT, SHORT CIRCUIT PROTECTED



±TRACKING VOLTAGE REGULATOR



FEATURES

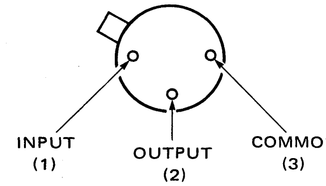
- OUTPUT CURRENT UP TO 100mA
- NO EXTERNAL COMPONENTS
- INTERNAL THERMAL OVERLOAD PROTECTION
- INTERNAL SHORT CIRCUIT CURRENT LIMITING
- AVAILABLE IN JEDEC TO-92 AND LOW PROFILE TO-39 PACKAGES
- OUTPUT VOLTAGES OF 2.6V, 5V, 6.2V, 12V AND 15V
- OUTPUT VOLTAGE TOLERANCES OF ±5% (78L00-AC) AND ±10% (78L00C) OVER THE TEMPERATURE RANGE

ABSOLUTE MAXIMUM RATINGS

Input Voltage	
2.6V, 5V and 6.2V	30V
12V and 15V	35V
Internal Power Dissipation	Internally Limited
Storage Temperature Range	
Metal Can (TO-39 Type)	−65°C to + 150°C
Molded TO-92	−55°C to + 150°C
Operating Junction Temperature Range	0°C to + 150°C
Lead Temperatures	
Metal Can (Soldering, 60 s time limit)	300°C
Molded TO-92 (Soldering, 10 s time limit)	260°C

PIN CONFIGURATION

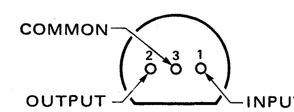
TO-39 TYPE METAL CAN PACKAGE OUTLINE DB



ORDER INFORMATION

OUTPUT VOLTAGE	PART NO.
5V	78L05A DB
5V	78L05 DB
12V	78L 12A DB
12V	78L 12DB
15V	78L 15A DB
15V	78L 15 DB

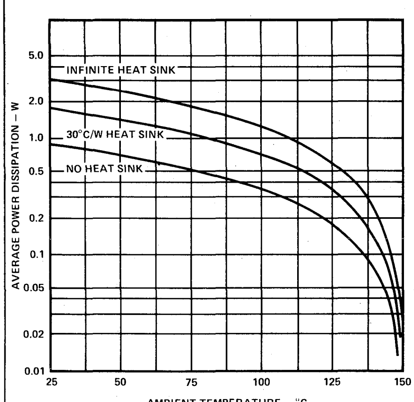
JEDEC (TO-92) PACKAGE PACKAGE OUTLINE S



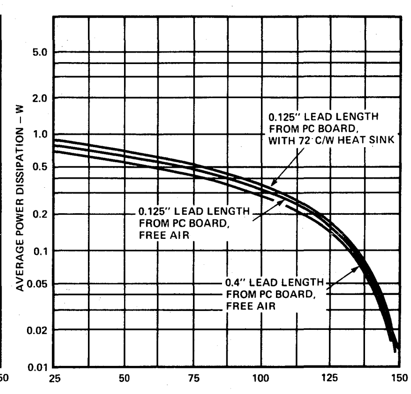
OUTPUT VOLTAGE	PART NO.
2.6V	78L02A S
2.6V	78L02 S
5V	78L05A S
5V	78L05 S
6.2V	78L06A S
6.2V	78L06 S
12V	78L12A S
12V	78L12 S
15V	78L15A S
15V	78L15 S

DESIGN CONSIDERATIONS

MAXIMUM AVERAGE POWER DISSIPATION AS A FUNCTION OF AMBIENT TEMPERATURE TO-39 TYPE PACKAGE



MAXIMUM AVERAGE POWER DISSIPATION AS A FUNCTION OF AMBIENT TEMPERATURE TO-92 TYPE PACKAGE



NOTE:
Typical thermal resistance of the TO-39 type metal can package without a heat sink is junction to case of 40°C/W and junction to ambient of 140°C/W. Typical thermal resistance of the TO-92 package is junction to ambient of 180°C/W with .400 inch leads from PC board and 160°C/W with .125 inch lead length.

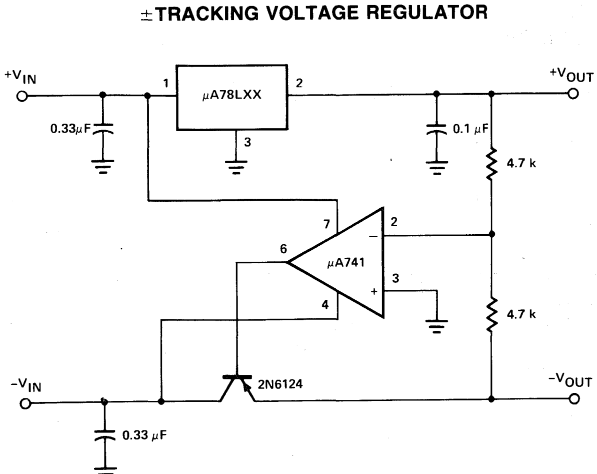
ELECTRICAL CHARACTERISTICS

IOUT = 40mA, 0°C <TJ<+125°C, CIN=0.33μF"COUT = 0.1μF (Unless Otherwise Specified)

PARAMETER	TEST CONDITIONS	78L02AC MIN	78L02AC TYP	78L02AC MAX	78L02C MIN	78L02C TYP	78L02C MAX	78L05AC MIN	78L05AC TYP	78L05AC MAX	UNITS
V_{OUT}	$T_J=25°C$	$V_{IN}=9.0V$						$V_{IN}=10V$			V
		2.5	2.6	2.7	2.4	2.6	2.8	4.8	5.0	5.2	
		$4.75V \le V_{IN} \le 20V$						$7V \le V_{IN} \le 20V$			
	$1mA \le I_{OUT} \le 70 mA$	2.45		2.75	2.45		2.75	4.75		5.25	
	$1mA \le I_{OUT} \le 40mA$	2.35		2.85	2.35		2.85	4.5		5.5	
LINE REGULATION	$T_J=25°C$	$4.75V \le V_{IN} \le 20V$						$7V \le V_{IN} \le 20V$			mV
			40	100		40	125		55	150	
		$5V \le V_{IN} \le 20V$						$8V \le V_{IN} \le 20V$			
			30	75		30	100		45	100	
LOAD REGULATION	$T_J=25°C$										mV
	$1mA \le I_{OUT} \le 100mA$		10	50		10	50		11	60	
	$1mA \le I_{OUT} \le 40mA$		4.0	25		4.0	25		5.0	30	
I_{CC}	$T_J=25°C$		3.6	6.0		3.6	6.0		3.8	6.0	mA
	$T_J=125°C$			5.5			5.5			5.5	
		$5V \le V_{IN} \le 20V$ (with line)						$8V \le V_{IN} \le 20V$ (with line)			
				2.5			2.5			1.5	
	$1mA \le I_{OUT} \le 40mA$ (with load)			0.1			0.2			0.1	
OUTPUT NOISE VOLTAGE	$T_J=25°C$ $10Hz \le f \le 100kHz$		30			30			40		μV
LONG TERM STABILITY			10			10			12		mV
RIPPLE REJECTION	$T_J=25°C$ $f=120H_Z$	$6V \le V_{IN} \le 16V$						$8V \le V_{IN} \le 18V$			dB
			43	51		42	51		41	49	
DROPOUT VOLTAGE	$T_A=25°C$		1.7			1.7			1.7		V

APPLICATIONS

±TRACKING VOLTAGE REGULATOR

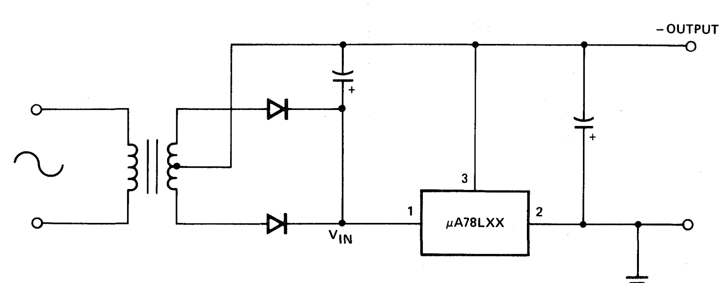


ELECTRICAL CHARACTERISTICS (CONT'D)

PARAMETER	TEST CONDITIONS	78L05C MIN	78L05C TYP	78L05C MAX	78L06AC MIN	78L06AC TYP	78L06AC MAX	78L06C MIN	78L06C TYP	78L06C MAX	UNITS
V_{OUT}	$T_J=25°C$	$V_{IN}\leq 10V$			$V_{IN}=12V$						V
		4.6	5.0	5.4	5.95	6.2	6.45	5.7	6.2	6.7	
		$7V\leq V_{IN}\leq 20V$			$8.5V\leq V_{IN}\leq 20V$						
	$1mA\leq I_{OUT}\leq 70mA$	4.75		5.25	5.90		6.5	5.90		6.5	
	$1mA\leq I_{OUT}\leq 40mA$	4.5		5.5	5.6		6.8	5.6		6.8	
LINE REGULATION	$T_J=25°C$	$7V\leq V_{IN}\leq 20V$			$8.5V\leq V_{IN}\leq 20V$						mV
			55	200		65	175		65	200	
		$8V\leq V_{IN}\leq 20V$			$9V\leq V_{IN}\leq 20V$						
			45	150		55	125		55	150	
LOAD REGULATION	$T_J=25°C$										mV
	$1mA\leq I_{OUT}\leq 100mA$		11	60		13	80		13	80	
	$1mA\leq I_{OUT}\leq 40mA$		5.0	30		6.0	40		6.0	40	
I_{CC}	$T_J=25°C$		3.8	6.0		3.9	6.0		3.9	6.0	mA
	$T_J=125°C$			5.5			5.5			5.5	
		$8\leq V_{IN}\leq 20V$			$9.0V\leq V_{IN}\leq 20V$ (with line)						
				1.5			1.5			1.5	
	$1mA\leq I_{OUT}\leq 40mA$ (with load)			0.2			0.1			0.2	
OUTPUT NOISE VOLTAGE	$T_J=25°C$ $10Hz\leq f\leq 100kHz$		40			50			50		µV
LONG TERM STABILITY			12			14			14		mV
RIPPLE REJECTION	$T_J=25°C$ $f=120H_z$	$8V\leq V_{IN}\leq 18V$			$10V\leq V_{IN}\leq 20V$						dB
		40	49		40	46		39	46		
DROPOUT VOLTAGE	$T_A=25°C$		1.7			1.7			1.7		V

APPLICATIONS (CONT'D)

NEGATIVE OUTPUT VOLTAGE CIRCUIT

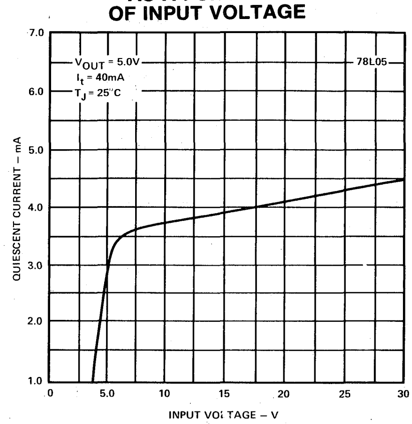


ELECTRICAL CHARACTERISTICS (CONT'D)

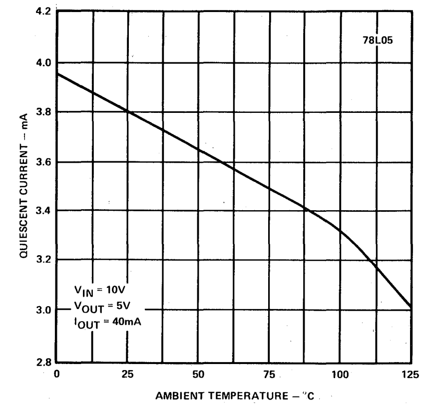
PARAMETER	TEST CONDITIONS	78L12AC MIN	78L12AC TYP	78L12AC MAX	78L12C MIN	78L12C TYP	78L12C MAX	78L15AC MIN	78L15AC TYP	78L15AC MAX	78L15C MIN	78L15C TYP	78L15C MAX	UNITS
V_{OUT}	T_J=25°C	V_{IN}=19V						V_{IN}=23V						V
		11.5	12	12.5	11.1	12	12.9	14.4	15	15.6	13.8	15	16.2	
		14.5V≤V_{IN}≤27V						17.5V≤V_{IN}≤30V						
	1mA≤I_{OUT}≤70mA	11.4		12.6	10.8		13.2	14.25		15.75	13.5		16.5	
	1mA≤I_{OUT}≤40mA	11.4		12.6	10.8		13.2	14.25		15.75	13.5		16.5	
LINE REGULATION	T_J=25°C	14.5V≤V_{IN}≤27V						17.5V≤V_{IN}≤30V						mV
			120	250		120	250		130	300		130	300	
		16V≤V_{IN}≤27V						20V≤V_{IN}≤30V						
			100	200		100	200		110	250		110	250	
LOAD REGULATION	T_J=25°C													mV
	1mA≤I_{OUT}≤100mA		20	100		20	100		25	150		25	150	
	1mA≤I_{OUT}≤40mA		10	50		10	50		12	75		12	75	
I_{CC}	T_J=25°C		4.2	6.5		4.2	6.5		4.4	6.5		4.4	6.5	mA
	T_J=125°C			6.0			6.0			6.0			6.0	
		16V≤V_{IN}≤27V (with line)						20V≤V_{IN}≤30V (with line)						
				1.5			1.5			1.5			1.5	
	1mA≤I_{OUT}≤40mA (with load)			0.1			0.2			0.1			0.2	
OUTPUT NOISE VOLTAGE	T_J=25°C 10Hz≤f≤100kHz		80			80			90			90		μV
LONG TERM STABILITY			24			24			30			30		mV
RIPPLE REJECTION	T_J=25°C f=120H_Z	15V≤V_{IN}≤23V						18.5V≤V_{IN}≤28.5V						dB
		37	42		36	42		34	39		33	39		
DROPOUT VOLTAGE	T_A=25°C		1.7			1.7			1.7			1.7		V

TYPICAL PERFORMANCE CURVES

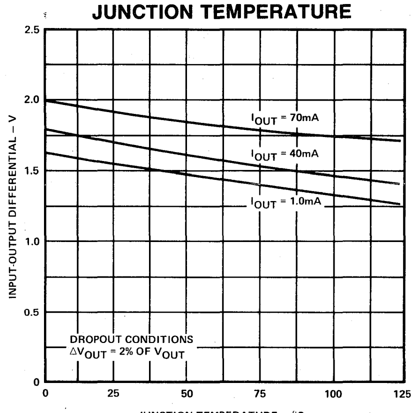
QUIESCENT CURRENT AS A FUNCTION OF INPUT VOLTAGE



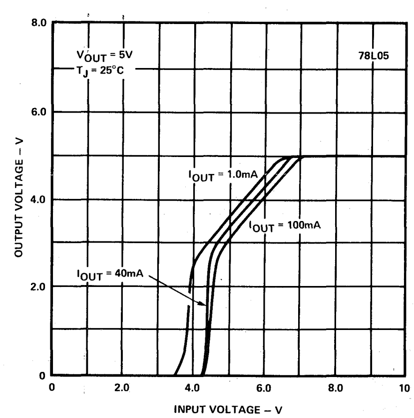
QUIESCENT CURRENT AS A FUNCTION OF TEMPERATURE



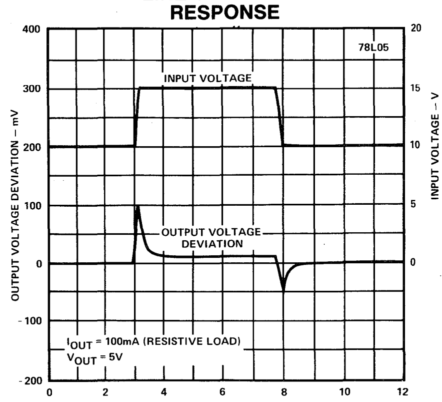
DROPOUT VOLTAGE AS A FUNCTION OF JUNCTION TEMPERATURE



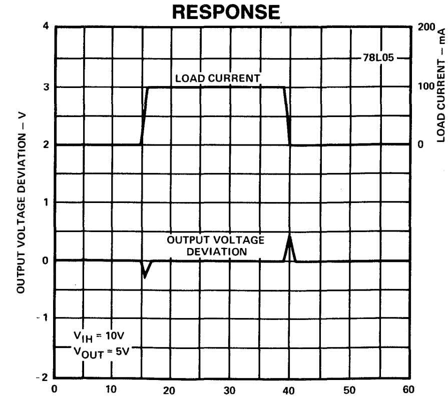
DROPOUT CHARACTERISTICS



LINE TRANSIENT RESPONSE

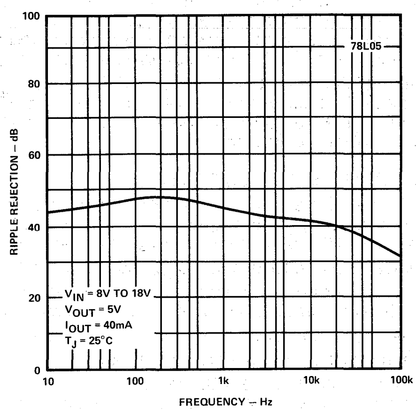


LOAD TRANSIENT RESPONSE



TYPICAL PERFORMANCE CURVES (CONT'D)

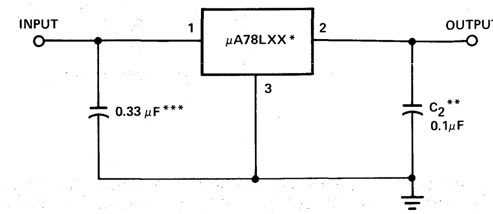
RIPPLE REJECTION AS A FUNCTION OF FREQUENCY



NOTE: Other μA78L00 Series Devices have similar curves.

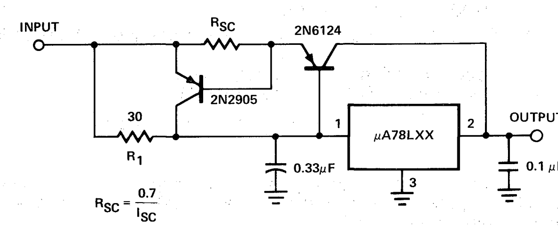
APPLICATIONS

FIXED OUTPUT REGULATOR



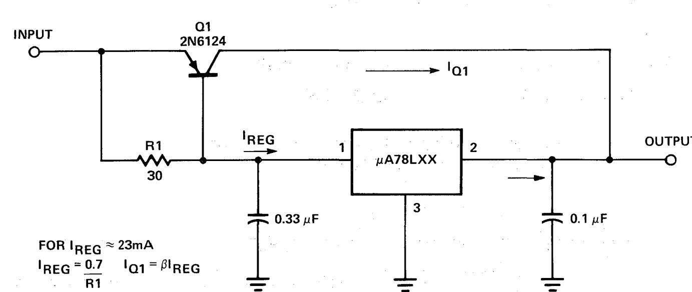
NOTES:
* TO SPECIFY AN OUTPUT VOLTAGE, SUBSTITUTE VOLTAGE FOR "XX".
** ALTHOUGH NO OUTPUT CAPACITOR IS NEEDED FOR STABILITY, IT DOES IMPROVE TRANSIENT RESPONSE.
*** REQUIRED IF REGULATOR IS LOCATED AN APPRECIABLE DISTANCE FROM POWER SUPPLY FILTER.

HIGH OUTPUT CURRENT, SHORT CIRCUIT PROTECTED



$R_{SC} = \frac{0.7}{I_{SC}}$

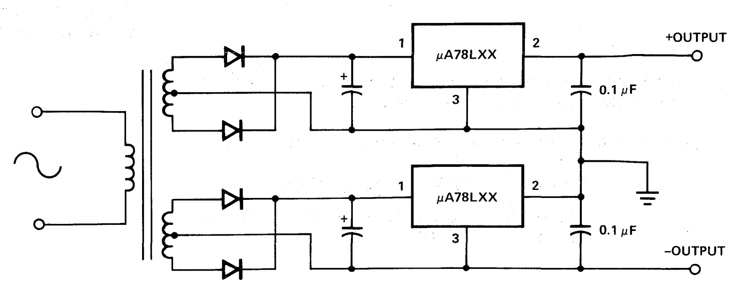
HIGH CURRENT VOLTAGE REGULATOR



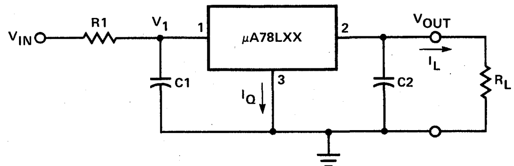
FOR $I_{REG} \approx 23mA$

$I_{REG} = \frac{0.7}{R1}$ $I_{Q1} = \beta I_{REG}$

POSITIVE AND NEGATIVE REGULATOR



HIGH DISSIPATION APPLICATIONS



When it is necessary to operate a μA78L00 regulator with a large input-output differential voltage, the addition of series resistor R1 will extend the output current range of the device by sharing the total power dissipation between R1 and the regulator.

R1 may be caluclated from

$$R1 = \frac{V_{IN(MIN)} - V_{OUT} - 2.0V}{I_{L(MAX)} + I_Q}$$

where IQ is the regulator quiescent current.

Regulator power dissipation at maximum input voltage and maximum load current is now

$P_{D(MAX)} = (V_1 - V_{OUT})\, I_{L(MAX)} + V_1 I_Q$

where

$V_1 = V_{IN(MAX)} - (I_{L(MAX)} + I_Q)\, R1$

The presence of R1 will affect load regulation according to the equation:

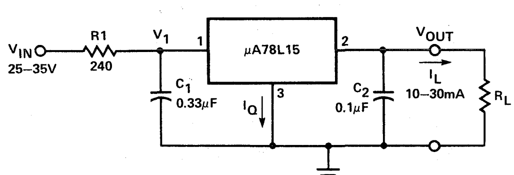
load regulation (at constant V_{IN}) = load regulation (at constant V_1)
+ (line regulation, mV per V) ×
(R1) × (ΔI_L).

As an example, consider a 15V regulator with a supply voltage of 30±5V, required to supply a maximum load current of 30mA. IQ is 4.3mA, and minimum load current is to be 10mA.

$$R1 = \frac{25 - 15 - 2}{30 + 4.3} = \frac{8}{34.3} = 240\Omega$$

$V_1 = 35 - (30 + 4.3)\,.24 = 35 - 8.2 = 26.8V$

$P_{D\,(MAX)} = (26.8 - 15)\,30 + 26.8\,(4.3)$
$= 354 + 115$
= 470mW, which will permit operation up to 70°C in most applications.



Line regulation of this circuit is typically 110mV for an input range of 25-35V at a constant load current, i.e. 11mV/V.

Load regulation = constant V_1 load regulation (typically 10mV, 10-30mA I_L)
+(11mV/V) × 0.24 × 20mA (typically 53mV)
= 63mV for a load current change of 20 mA at a constant V_{IN} of 30V.

THERMAL CONSIDERATIONS

The TO-92 molded package is capable of unusually high power dissipation due to the lead frame design. However, its thermal capabilities are generally overlooked because of a lack of understanding of the thermal paths from the semiconductor junction to ambient temperature. While thermal resistance is normally specified for the device mounted 1 cm above an infinite heat sink, very little has been mentioned of the options available to improve on the conservatively rated thermal capability.

An explanation of the thermal paths of the TO-92 and comparison of the thermal equivalent circuit of the TO-39 metal package with that of the TO-92 will allow the designer to determine the thermal stress he is applying in any given application.

THE METAL CAN THERMAL MODEL

In the TO-39 case, where the die is attached directly to the base of a metal package, the thermal equivalent circuit is often represented simply as a series connection of the junction-to-case thermal resistance, θ_{JC}, and the case-to-ambient thermal resistance, θ_{CA}, as shown in Figure 1.

In this model, the current source represents the thermal energy source; TJ is the junction temperature, assuming a constant surface temperature across the die; θ_{JC} is the junction-to-case thermal resistance, measured at a point on the case directly beneath the die location; θ_{CA} is the thermal resistance from the case to the ultimate heat sink, ambient temperature, as represented by the battery. The heat flow is analogous to electrical current, and temperature to voltage. The total thermal resistance from junction to ambient is then:

$$\theta_{JA} = \theta_{JC} + \theta_{CA}$$

The maximum power dissipation is a function of the maximum permissible junction temperature (which is a function of the package materials and construction) and the total thermal resistance from the junction to ambient temperature. Junction temperature is assumed to be the limiting factor.

Thus: maximum power dissipation $PD = \dfrac{T_{J(MAX)} - T_A}{\theta_{JC} + \theta_{CA}}$

Since $\theta_{JA} = \theta_{JC} + \theta_{CA}$

Then $\theta_{JA} = \dfrac{T_{J(MAX)} - T_A}{PD}$

Or $\theta_{JA}\, P_D = T_J - T_A$

$$P_D = \frac{T_J - T_A}{\theta_{JA}}$$

Therefore, using the V_{BE} method of junction temperature sensing, and attaching a thermocouple to the case at the location specified, the relative values of θ_{JC} and θ_{CA} can readily be determined.

The thermal ratings of the metal can package are normally presented with the case attached to an infinite heat sink at still air ambient temperature. This causes θ_{CA} to go to zero resulting in θ_{JC} representing the total θ_{JA}. The infinite heat sink is an unrealizable condition in the practical world, but serves to project a goal.

THE TO-92 PACKAGE

The TO-92 package thermal paths are considerably more complex than those of the TO-39 metal can package. In addition to the path through the molding compound to ambient temperature, there is another path through the leads in parallel with the case path, to ambient temperature, as shown in Figure 2.

The total thermal resistance in this model is then:

$$\theta_{JA} = \frac{(\theta_{JC} + \theta_{CA})\ (\theta_{JL} + \theta_{LA})}{\theta_{JC} + \theta_{CA} + \theta_{JL}\ \theta_{LA}} \qquad (3)$$

Where: θ_{JC} = thermal resistance of the case between the regulator die and a point on the case directly above the die location.

θ_{CA} = thermal resistance between the case and air at ambient temperature.

θ_{JL} = thermal resistance from transistor die through the collector lead to a point 1/16″ below the regulator case.

θ_{LA} = total thermal resistance of the collector-base-emitter leads to ambient temperature.

As one can see from Figure 1, the metal can package generally does not have the lead cooling path because of the high thermal resistances resulting from the construction of the header, case and leads. Normally, this material is kovar. Now, θ_{JC} and θ_{JL} are within the package and not variable by the user. However, θ_{CA} and θ_{LA} are outside the package and can be effectively used to control the total thermal resistance and, therefore, junction temperature.

Replacing θ_{JA} of equation (1) with θ_{JA} of equation (3) gives:

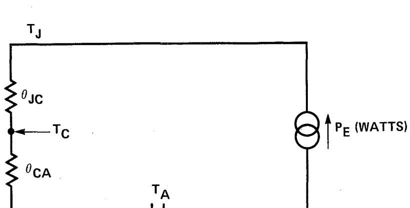
$$\theta JA = \frac{(\theta JC + \theta CA)\ (\theta JL \ \alpha\ \theta LA)}{\theta JC + \theta CA + \theta JL + \theta LA} = \frac{T_J - T_A}{P_D} \qquad (4)$$

The maximum TJ allowed in equation (4) is 150°C. The maximum power dissipation is determined by the net total thermal resistance θJA, the parallel equivalent networks of the case series path and lead series path, divided into the difference of the maximum junction temperature, 150°C, and ambient temperature generally specified as 25°C. In the case of the 78LXX, the maximum dissipation of a .4 inch condition is:

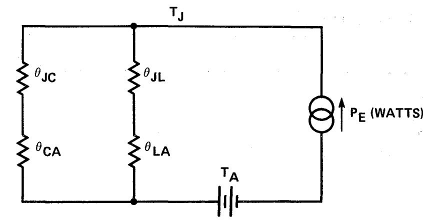
$$P_D = \frac{150 - 25}{\theta_{JA}}, \quad \theta_{JA} = 180°C/W$$

$$P_D = 0.7\ W$$

If lead length is reduced to .125 inch θ_{JA} becomes 160°C, and P_D (MAX) = 0.78 W.



THERMAL EQUIVALENT CIRCUIT TO-39 PACKAGE (DIE ATTACHED TO METAL PACKAGE BASE)
Figure 1



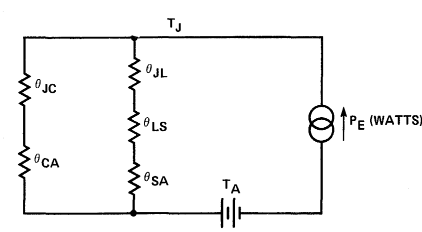
TO-92 THERMAL EQUIVALENT CIRCUIT
Figure 2

METHODS OF HEAT SINKING

With two external thermal resistances in each leg of a parallel network available to the circuit designer as variables, he can choose the method of heat sinking most applicable to his particular situation. To demonstrate, consider the effect of placing a small 72°C/W flag type heat sink, such as the Staver F1-7D-2, on the 78LXX molded case. The heat sink effectively replaces the θ_{CA} (Figure 2) and the new thermal resistance, θ_{JA}, is:

$$\theta_{JA} = 145°C/W \text{ (assuming .125 inch lead length)}$$

The net change of 15°C/W increases the allowable power dissipation to 0.86W with an inserted cost of 1-2 cents. A still further decrease in θ_{JA} could be achieved by using a sink rated at 46°C/W, such as the Staver FS-7A. Also, if the case sinking does not provide an adequate reduction in total θ_{JA}, the other external thermal resistance, θ_{LA}, may be reduced by shortening the lead length from package base to mounting medium. However, one point must be kept in mind. The lead thermal path includes a thermal resistance, θ_{SA}, from the leads at the mounting point to ambient, that is, the mounting medium, θ_{LA} is then equal to $\theta_{LS} + \theta_{SA}$. The new model is shown in Figure 3.



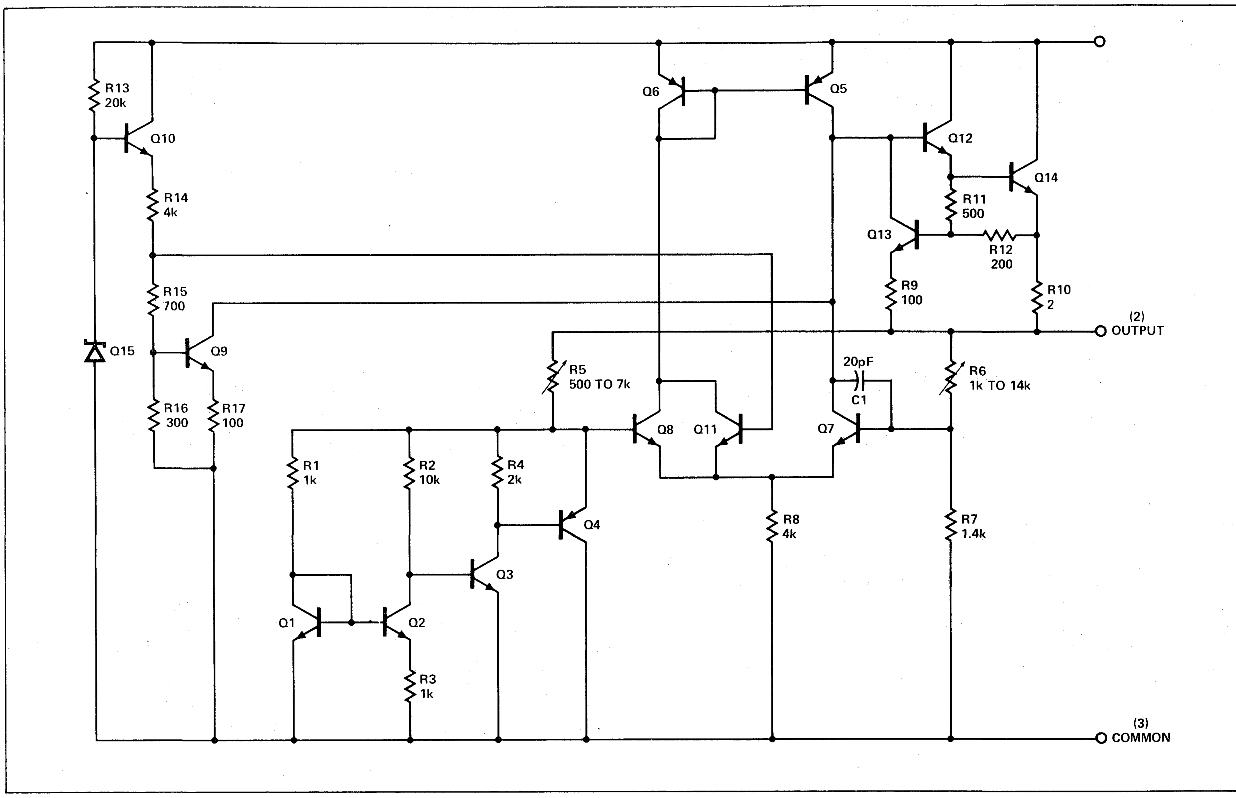
TO-92 THERMAL EQUIVALENT CIRCUIT (LEAD AT OTHER THAN AMBIENT TEMPERATURE)
Figure 3

In the case of a socket, θ_{SA} could be as high as 270°C/W, thus causing a net increase in θ_{JA} and a consequent decrease in the maximum dissipation capability. Shortening the lead length may return the net θ_{JA} to the original value, but lead sinking would not be accomplished.

In those cases where the regulator is inserted into a copper clad printed circuit board, it is advantageous to have a maximum area of copper at the entry points of the leads. While it would be desirable to rigorously define the effect of PC board copper, the real world variables are too great to allow anything more than a few general observations.

The best analogy for PC board copper is to compare it with parallel resistors. Beyond some point, additional resistors are not significantly effective; beyond some point, additional copper area is not effective.

EQUIVALENT CIRCUIT



THREE-TERMINAL POSITIVE VOLTAGE REGULATOR μA78M00 Series

FEATURES

- OUTPUT CURRENT UP TO 500MA
- NO EXTERNAL COMPONENTS
- INTERNAL THERMAL OVERLOAD PROTECTION
- INTERNAL SHORT CIRCUIT CURRENT LIMITING
- OUTPUT TRANSISTOR SAFE-AREA COMPENSATION
- AVAILABLE IN THE TO-220 AND THE TO-39 PACKAGE
- OUTPUT VOLTAGES OF 5, 6, 8, 12, 15, 20 AND 24 VOLTS

ABSOLUTE MAXIMUM RATINGS

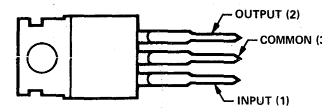
Input Voltage	
(5V through 15V)	35V
Internal Power Dissipation (20V, 24V)	40V
(Note 1)	Internally Limited
Storage Tempearture Range	
TO-39	−65°C to +150°C
TO-220	−55°C to +125°C
Operating Junction Temperature Range (Note 2)	
78M00	−55°C to +150°C
78M00C	0°C to +125°C
Lead Temperature	
TO-39 Package (Soldering, 60 second time limit)	300°C
TO-220 Package (Soldering, 10 second time limit)	230°C

NOTES:

1. Thermal resistance of the packages (without a heat sink) Junction to Case: TO-220 Package 2°C/W TO-39 Package 20°C/W
   Junction to Ambient: TO-220 Package 50°C/W TO-39 Package 170°C/W
2. Operating Ambient Temperature Range
   −55°C to + 125°C
   0°C to +85°C

PIN CONFIGURATION

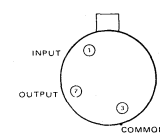
TO-220 PACKAGE PACKAGE OUTLINE U



ORDER INFORMATION

OUTPUT VOLTAGE	ORDER PART NO.
5V	78M05CU
6V	78M06CU
8V	78M08CU
12V	78M12CU
15V	78M15CU
20V	78M20CU
24V	78M24CU

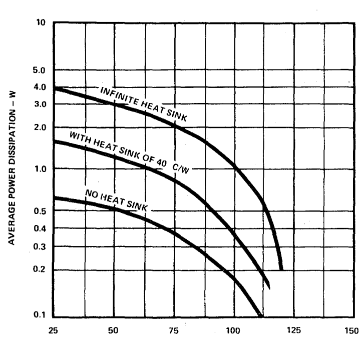
TO-39 TYPE METAL CAN PACKAGE OUTLINE DB



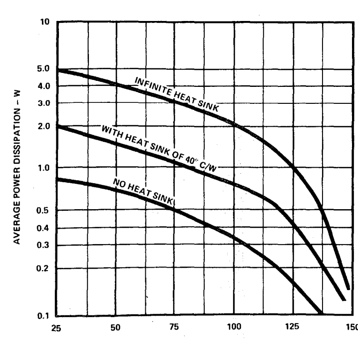
OUTPUT VOLTAGE	ORDER PART NO.
5V	78M05DB
6V	78M06DB
8V	78M08DB
12V	78M12DB
15V	78M15DB
20V	78M20DB
24V	78M24DB
5V	78M05CDB
6V	78M06CDB
8V	78M08CDB
12V	78M12CDB
15V	78M15CDB
20V	78M20CDB
24V	78M24CDB

TYPICAL CURVES

MAXIMUM AVERAGE POWER DISSIPATION AS A FUNCTION OF AMBIENT TEMPERATURE (TO-39, 78M00C)



MAXIMUM AVERAGE POWER DISSIPATION AS A FUNCTION OF AMBIENT TEMPERATURE (TO-39, 78M00)



ELECTRICAL CHARACTERISTICS I_{OUT} = 200mA, −55°C ≤T_J≤150°C (78M00), 0°C≤T_J≤125°C (78M00C), C_{IN}=0.33μF, C_{OUT}=0.1μF, (Unless Otherwise Specified)

PARAMETER / TEST CONDITIONS	UNITS	78M05 MIN	78M05 TYP	78M05 MAX	78M05C MIN	78M05C TYP	78M05C MAX	78M06 MIN	78M06 TYP	78M06 MAX	78M06C MIN	78M06C TYP	78M06C MAX	78M08 MIN	78M08 TYP	78M08 MAX
V_{OUT}	(V)	V_{IN}=10V						V_{IN}=IIV						V_{IN}=14V		
T_J=25°C		4.8	5.0	5.2	4.8	5.0	5.2	5.75	6.0	6.25	5.75	6.0	6.25	7.7	8.0	8.3
5mA≤I_{OUT}≤200mA		8V≤V_{IN}≤20V			7V≤V_{IN}≤25V			9V≤V_{IN}≤21V			8.0V≤V_{IN}≤25V			11.5V≤V_{IN}≤23V		
		4.7		5.3	4.75		5.25	5.7		6.3	5.7		6.3	7.6		8.4
LINE REGULATION	mV	7V≤V_{IN}≤25V						8V≤V_{IN}≤25V						10.5V≤V_{IN}≤25V		
T_J=25°C			3	50		3	100		5	60		5	100		6	60
		8V≤V_{IN}≤20V			8V≤V_{IN}≤25V			9V≤V_{IN}≤20V			9V≤V_{IN}≤25V			11V≤V_{IN}≤20V		
			1	25		1	50		1.5	30		1.5	50		2	30
LOAD REGULATION	mV															
T_J=25°C, 5mA≤I_{OUT}≤500mA			20	50		20	100		20	60		20	120		25	80
5mA≤I_{OUT}≤200mA			10	25		10	50		10	30		10	60		10	40
I_{CC}	mA		4.5	6.0		4.5	6.0		4.5	6.0		4.5	8.0		4.6	6.0
T_J=25°C		8V≤V_{IN}≤25V		0.8			0.8	9V≤V_{IN}≤25V		0.8			0.8	11.5≤V_{IN}≤25V		0.8
5mA≤I_{OUT}≤200mA				0.5			0.5			0.5			0.5			0.5
OUTPUT NOISE VOLTAGE, T_A=25°C, 10Hz≤f≤100kHz	μV		40			40			45			45			52	
VOLTAGE DRIFT	mV			20			20			24			24			32
RIPPLE REJECTION	dB	8V≤V_{IN}≤18V						9V≤V_{IN}≤19V						11.5V≤V_{IN}≤21.5V		
f=120Hz		68	80		62	80		59	80		59	80		56	80	
DROPOUT VOLTAGE, T_J=25°C	V		2.0			2.0			2.0			2.0			2.0	
IOS, T_J=25°C, V_{IN}=35V	mA		300			300			270			270			250	
PEAK OUTPUT CURRENT, T_J=25°C	mA		700			700			700			700			700	
V_{OUT} OUTPUT TEMPERATURE DRIFT, I_{OUT}=5mA	mV/°C		−1.0			−1.0			−0.5			−0.5			−0.5	

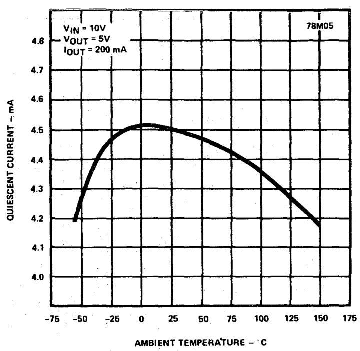
ELECTRICAL CHARACTERISTICS (CONT'D)

PARAMETER UNITS TEST CONDITIONS	78M08C MIN	78M08C TYP	78M08C MAX	78M12 MIN	78M12 TYP	78M12 MAX	78M12C MIN	78M12C TYP	78M12C MAX	78M15 MIN	78M15 TYP	78M15 MAX	78M15C MIN	78M15C TYP	78M15C MAX
V_{OUT} (V)	V_{IN} = 14V			V_{IN}=19V						V_{IN}=23V					
T_J=25°C	7.7	8.0	8.3	11.5	12.0	12.5	11.5	12.0	12.5	14.4	15.0	15.6	14.4	15.0	15.6
5mA≤I_{OUT}≤200mA	10.5V≤V_{IN}≤23V			15.5V≤V_{IN}≤27V			14.5V≤V_{IN}≤27V			18.5V≤V_{IN}≤30V			17.5V≤V_{IN}≤30V		
	7.6		8.4	11.4		12.6	11.4		12.6	14.25		15.75	14.25		15.75
LINE REGULATION mV	10.5≤V_{IN}≤25V			14.5V≤V_{IN}≤30V						17.5V≤V_{IN}≤30V					
		6	100		8	60		8	100		10	60		10	100
T_J=25°C	11V≤V_{IN}≤25V			16V≤V_{IN}≤25V			16V≤V_{IN}≤30V			20V≤V_{IN}≤30V					
		2	50		2	30		2	50		3	30		3	50
LOAD REGULATION mV T_J=25°C 5mA≤I_{OUT}≤500mA		25	160		25	120		25	240		25	150		25	150
5mA≤I_{OUT}≤200mA		10	80		10	60		10	120		10	75		10	75
I_{CC} mA T_J=25°C		4.6	8.0		4.8	6.0		4.8	8.0		4.8	6.0		4.8	8.0
	10.5V≤V_{IN}≤25V		0.8	15≤V_{IN}≤30V		0.8	14.5V≤V_{IN}≤30V		0.8	18.5V≤V_{IN}≤30V		0.8	17.5V≤V_{IN}≤30V		0.8
5mA≤I_{OUT}≤200mA			0.5			0.5			0.5			0.5			0.5
OUTPUT NOISE VOLTAGE μV T_A=25°C 10Hz≤f≤100kHz		52			75			75			90			90	
VOLTAGE DRIFT mV			32			48			48			60			60
RIPPLE REJECTION dB f=120Hz	11.5≤V_{IN}≤21.5V			15V≤V_{IN}≤25V						18.5V≤V_{IN}≤28.5V					
	56	80		55	80		55	80		54	70		54	70	
DROPOUT VOLTAGE V T_J=25°C		2.0			2.0			2.0			2.0			2.0	
IOS mA T_J=25°C V_{IN}=35V		250			240			240			240			240	
PEAK OUTPUT CURRENT mA T_J=25°C		700			700			700			700			700	
V_{OUT} OUTPUT TEMPERATURE DRIFT mV/°C I_{OUT}=5mA		−0.5			−1.0			−1.0			−1.0			−1.0	

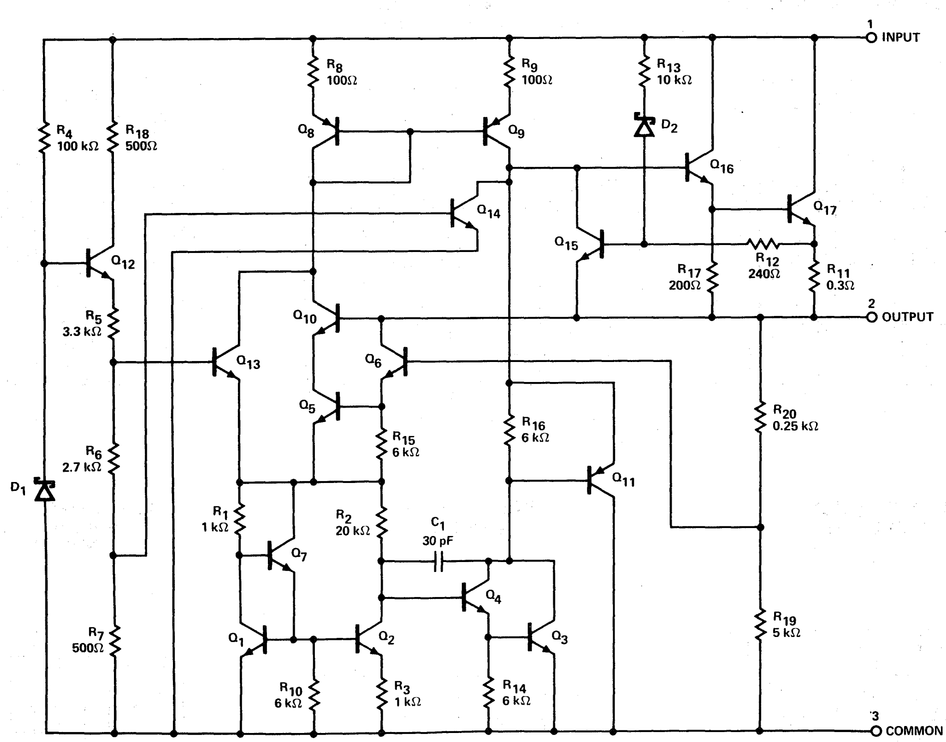
PARAMETER UNITS TEST CONDITIONS	78M20			78M20C			78M24			78M24C		
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
V_{OUT} (V)	$V_{IN}=29V$						$V_{IN}=33V$					
$T_J=25°C$	19.2	20	20.8	19.2	20	20.8	23.0	24.0	25.0	23.0	24.0	25.0
$5mA \leq I_{OUT} \leq 200mA$	$24V \leq V_{IN} \leq 35V$			$23V \leq V_{IN} \leq 35V$			$28V \leq V_{IN} \leq 38V$			$27V \leq V_{IN} \leq 38V$		
	19		21	19		21	22.8		25.2	22.8		25.2
LINE REGULATION mV	$23V \leq V_{IN} \leq 35V$						$27V \leq V_{IN} \leq 38V$					
$T_J=25°C$		10	60		10	100		10	40		10	100
	$24V \leq V_{IN} \leq 35V$						$30V \leq V_{IN} \leq 36V$			$30V \leq V_{IN} \leq 38V$		
		15	30		5	50		5	30		5	50
LOAD REGULATION mV $T_J=25°C$												
$5mA \leq I_{OUT} \leq 500mA$		30	200		30	400		30	240		30	480
$5mA \leq I_{OUT} \leq 200mA$		10	100		10	200		10	120		10	240
I_{CC} mA $T_J=25°C$		4.9	6.0		4.9	6.5		5	6.0		5	7
	$24V \leq V_{IN} \leq 35V$			$23V \leq V_{IN} \leq 35V$			$28V \leq V_{IN} \leq 38V$			$27V \leq V_{IN} \leq 38V$		
			0.8			0.8			0.8			0.8
$5mA \leq I_{OUT} \leq 200mA$			0.5			0.5			0.5			0.5
OUTPUT NOISE VOLTAGE μV $T_A=25°C$ $10Hz \leq f \leq 100kHz$		110			110			170			170	
VOLTAGE DRIFT mV			80			80			96			96
RIPPLE REJECTION dB	$24V \leq V_{IN} \leq 34V$						$28V \leq V_{IN} \leq 38V$					
$f=120Hz$	53	70		53	70		50	70		50	70	
DROPOUT VOLTAGE V $T_J=25°C$		2.0			2.0			2.0			2.0	
IOS mA $T_J=25°C$ $V_{IN}=35V$		240			240			240			240	
PEAK OUTPUT CURRENT mA $T_J=25°C$		700			700			700			700	
V_{OUT} OUTPUT TEMPERATURE DRIFT mV/°C $I_{OUT}=5mA$		−1.1			−1.1			−1.2			−1.2	

TYPICAL CURVES (CONT'D)

QUIESCENT CURRENT AS A FUNCTION OF TEMPERATURE

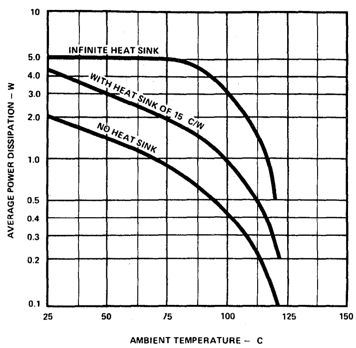


SCHEMATIC DIAGRAM

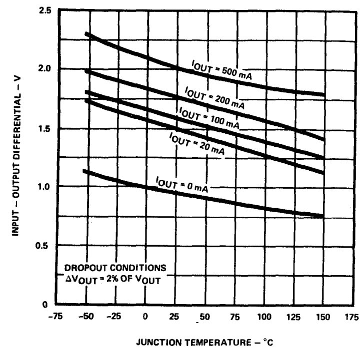


TYPICAL CURVES (CONT'D)

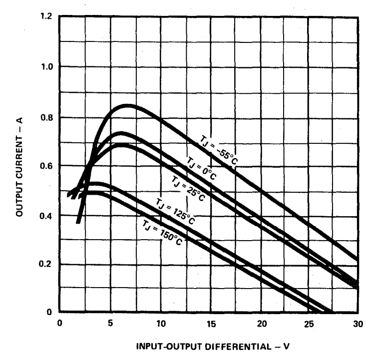
MAXIMUM AVERAGE POWER DISSIPATION AS A FUNCTION OF AMBIENT TEMPERAMENT (TO-220, 78M00C)



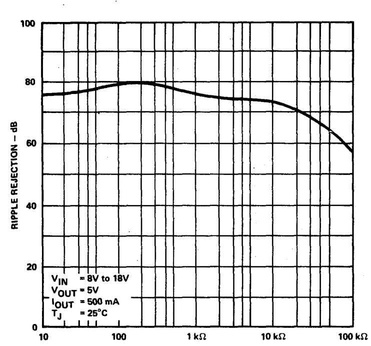
DROPOUT VOLTAGE AS A FUNCTION OF JUNCTION TEMPERATURE



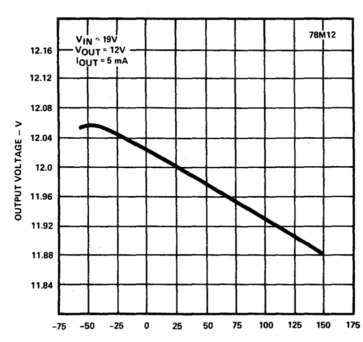
PEAK OUTPUT CURRENT AS A FUNCTION OF INPUT/OUTPUT DIFFERENTIAL VOLTAGE



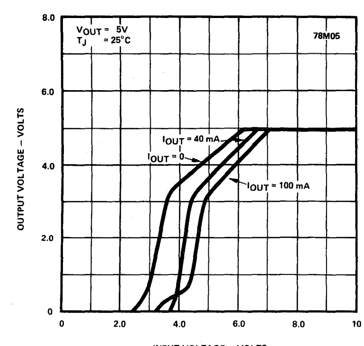
RIPPLE REJECTION AS A FUNCTION OF FREQUENCY



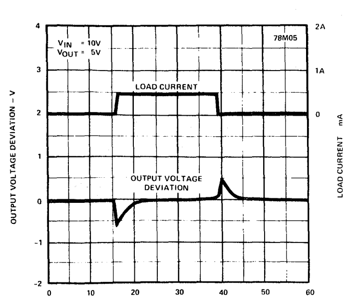
OUTPUT VOLTAGE AS A FUNCTION OF JUNCTION TEMPERATURE



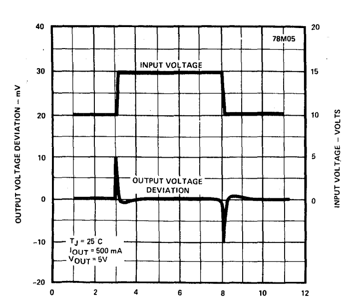
DROPOUT CHARACTERISTICS



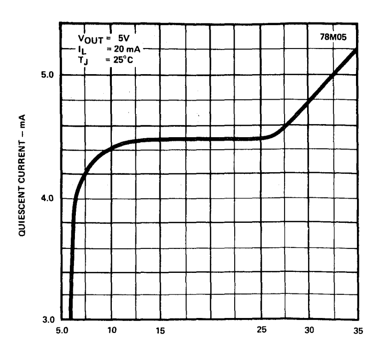
LOAD TRANSIENT RESPONSE



LINE TRANSIENT RESPONSE

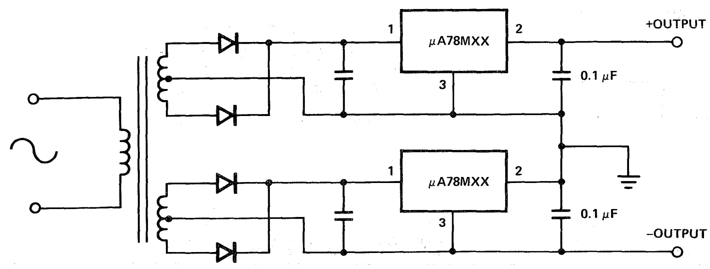


QUIESCENT CURRENT AS A FUNCTION OF INPUT VOLTAGE

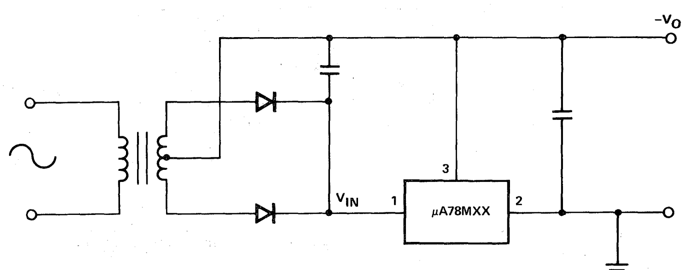


APPLICATIONS

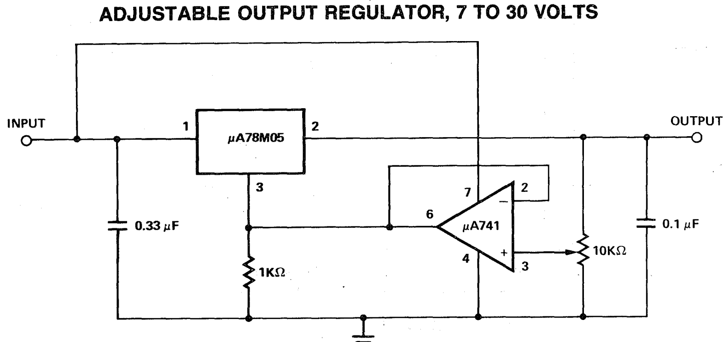
POSITIVE AND NEGATIVE REGULATOR



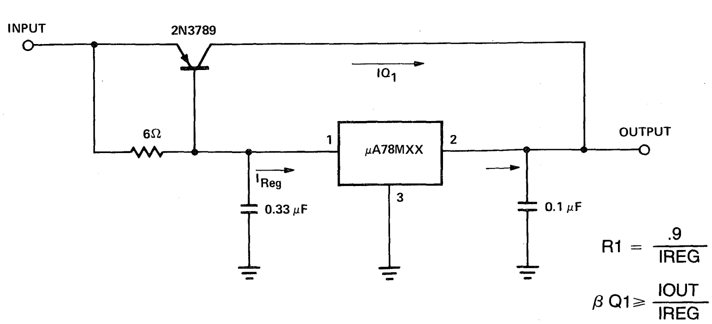
NEGATIVE OUTPUT VOLTAGE CIRCUIT



ADJUSTABLE OUTPUT REGULATOR, 7 TO 30 VOLTS

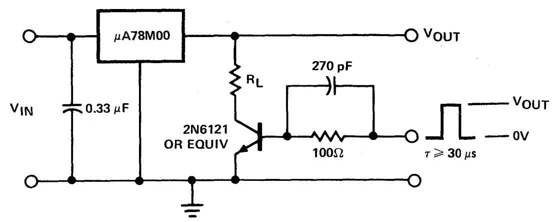


HIGH CURRENT VOLTAGE REGULATOR

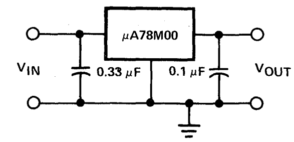


APPLICATIONS (CONT'D)

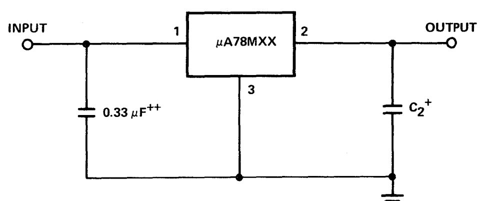
TEST CIRCUITS



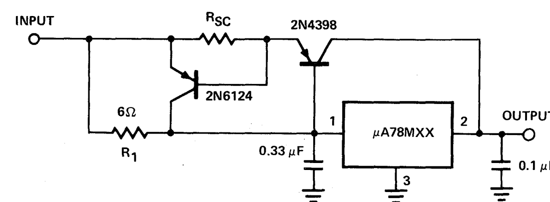
LOAD REGULATION TEST CIRCUIT



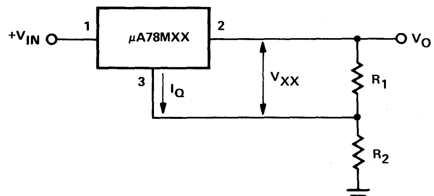
DC PARAMETER TEST CIRCUIT



NOTES:
* To specify an output voltage, substitute voltage value for "XX".
+ Although no output capacitor is needed for stability, it does improve transient response.
++ Required if regulator is located an appreciable distance from power supply filter.

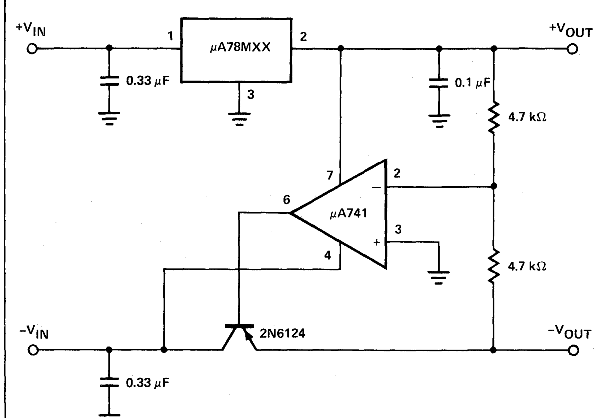


CIRCUIT FOR INCREASING OUTPUT VOLTAGE

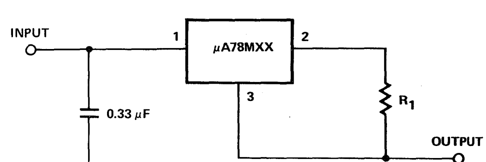


$$V_O = V_{XX}\left(1 + \frac{R_2}{R_1}\right) + I_Q R_2$$

±TRACKING VOLTAGE REGULATOR



CURRENT REGULATOR



$$\text{Output Current} = \frac{V_{OUT}}{R1}$$

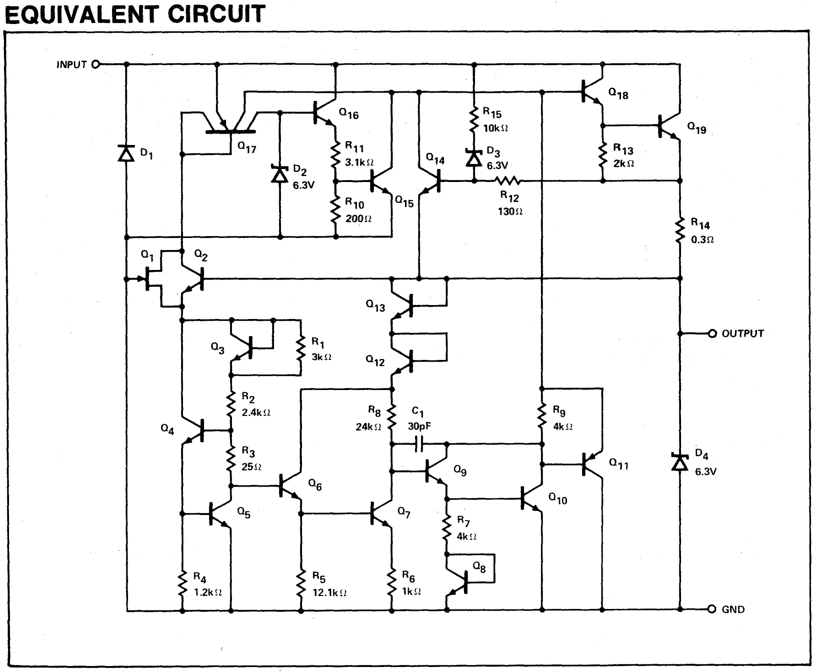
FEATURES

- OUTPUT CURRENTS IN EXCESS OF 1 amp
- INTERNAL THERMAL OVERLOAD PROTECTION
- INTERNAL CURRENT LIMITING
- NO EXTERNAL COMPONENTS REQUIRED

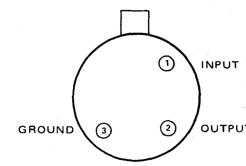
ABSOLUTE MAXIMUM RATINGS

Input Voltage	35V
Power Dissipation	Internally Limited
Operating Junction Temperature Range	
LM109	−55°C to 150°C
LM309	0°C to 125°C
Storage Temperature Range	−65°C to 150°C
Lead Temperature (Soldering, 10 sec)	300°C

EQUIVALENT CIRCUIT

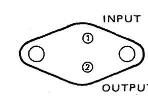


DB PACKAGE



ORDER PART NOS. LM109DB/LM209DB/LM309DB

DA PACKAGE



CASE IS CONNECTED TO GROUND.

ORDER PART NO. LM109DA/LM209DA/LM309DA

ELECTRICAL CHARACTERISTICS (Note 1)

PARAMETER	CONDITIONS	LM109			LM309			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Output Voltage	$T_j = 25°C$	4.7	5.05	5.3	4.8	5.05	5.2	V
Line Regulation	$T_j = 25°C$							
	$7V \leq V_{IN} \leq 25V$		4	50		4	50	mV
Load Regulation	$T_j = 25°C$							
TO-5	$5mA \leq I_{OUT} \leq 0.5A$		20	50		20	50	mV
TO-3	$5mA \leq I_{OUT} \leq 1.5A$		50	100		50	100	mV
Output Voltage	$8V \leq V_{IN} \leq 20V$							
	$5mA \leq I_{OUT} \leq I_{max}$							
	$P < P_{max}$	4.6		5.4	4.75		5.25	V
Quiescent Current	$7V \leq V_{IN} \leq 25V$		5.2	10		5.2	10	mA
Quiescent Current Change	$8V \leq V_{IN} \leq 25V$			0.5			0.5	mA
	$5mA \leq I_{OUT} \leq I_{max}$			0.8			0.8	mA
Output Noise Voltage	$T_A = 25°C$							
	$10Hz \leq f \leq 100 kHz$		40			40		μV
Long Term Stability				10			20	mV
Thermal Resistance								
Junction to Case (Note 2)								
TO-5			15			15		°C/W
TO-3			3			3		°C/W

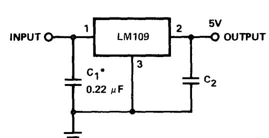
NOTES:

1. Unless otherwise specified, these specifications apply for $-55°C \leq T_j \leq 150°C$ for the LM109 or $0°C \leq T_j \leq 125°C$ for the LM309, $V_{IN} = 10V$ and $I_{OUT} = 0.1A$ for the TO-5 package or $I_{OUT} = 0.5A$ for the TO-3 pacakge. For the TO-5 package, $I_{max} = 0.2A$ and $P_{max} = 2.0W$. For the TO-3 package, $I_{max} = 1.0A$ and $P_{max} = 20W$.

2. Without a heat sink, the thermal resistance of the TO-5 package is about 150°C/W, while that of the TO-3 package is approximately 35°C/W. With a heat sink, the effective thermal resistance can only approach the values specified, depending on the efficiency of the sink.

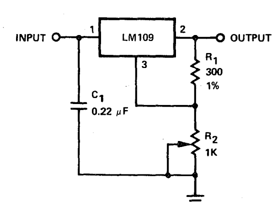
TYPICAL APPLICATIONS

FIXED 5V REGULATOR

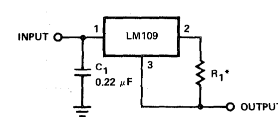


NOTES:
*Required if regulator is located an appreciable distance from power supply filter.
†Although no output capacitor is needed for stability, it does improve transient response.

ADJUSTABLE OUTPUT REGULATOR

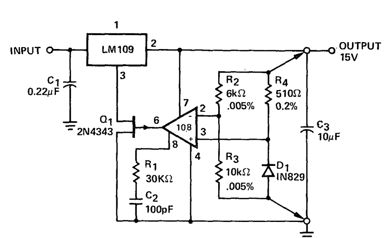


CURRENT REGULATOR



NOTES:
*Determines output current.

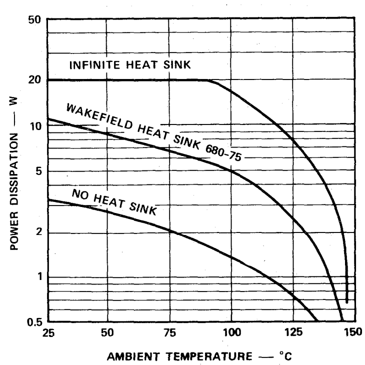
PRECISION VOLTAGE REGULATOR



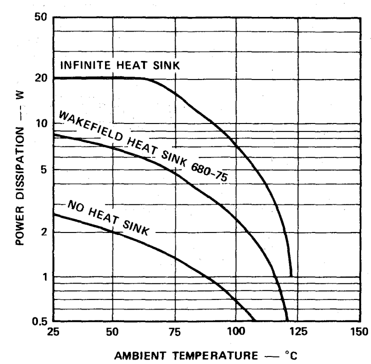
NOTES:
*Regulation better than 0.01% load, line and temperature, can be obtained.
†Determines zener current. May be adjusted to minimize thermal drift.
‡Solid tantalum.

TYPICAL CHARACTERISTIC CURVES

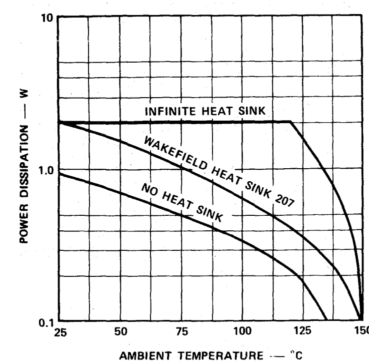
MAXIMUM AVERAGE POWER DISSIPATION LM109/LM209 (TO-3)



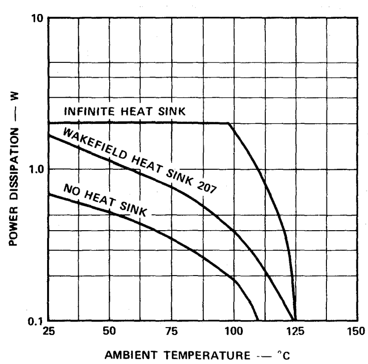
MAXIMUM AVERAGE POWER DISSIPATION LM309 (TO-3)



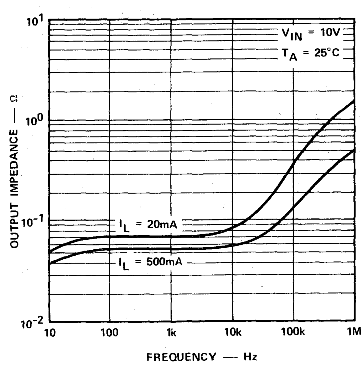
MAXIMUM AVERAGE POWER DISSIPATION LM109/LM209 (TO-5)



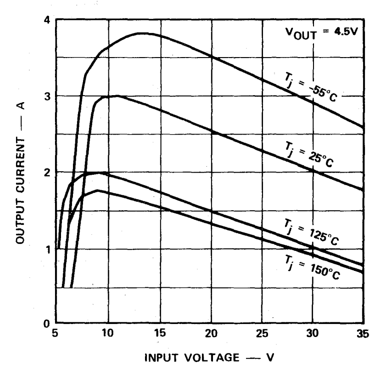
MAXIMUM AVERAGE POWER DISSIPATION LM309 (TO-5)



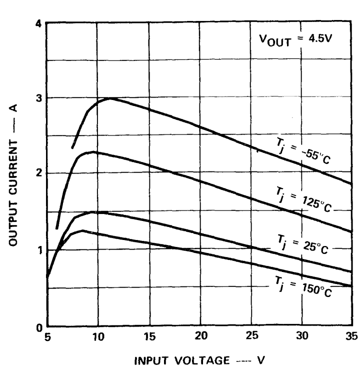
OUTPUT IMPEDANCE



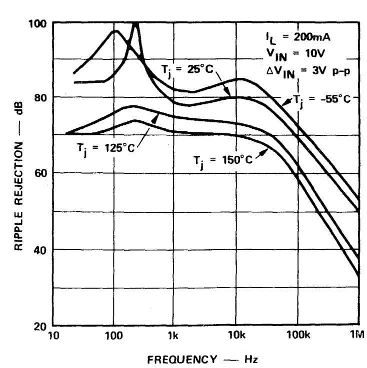
PEAK OUTPUT CURRENT DA PACKAGE (TO-3)



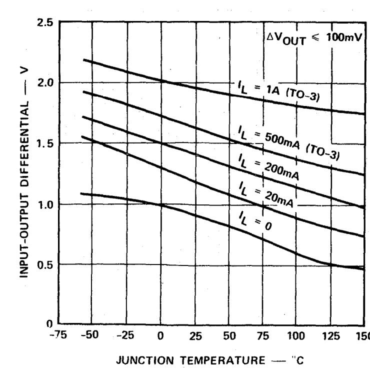
PEAK OUTPUT CURRENT DB PACKAGE (TO-5)



RIPPLE REJECTION

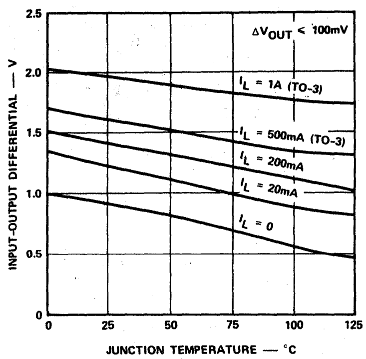


DROPOUT VOLTAGE

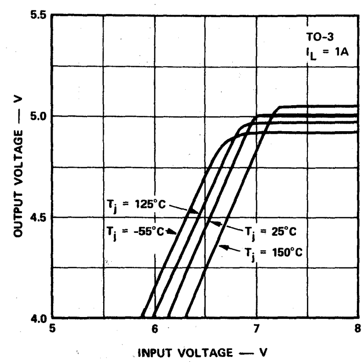


TYPICAL CHARACTERISTIC CURVES (CONT'D)

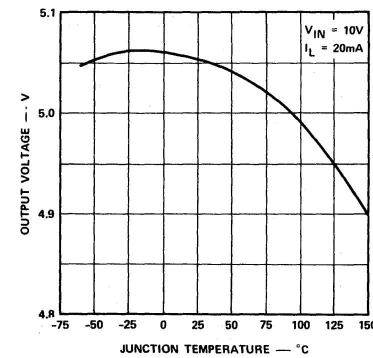
DROPOUT VOLTAGE



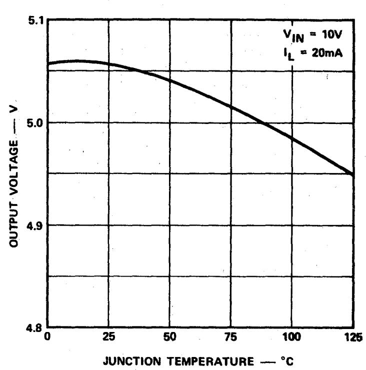
DROPOUT CHARACTERISTIC



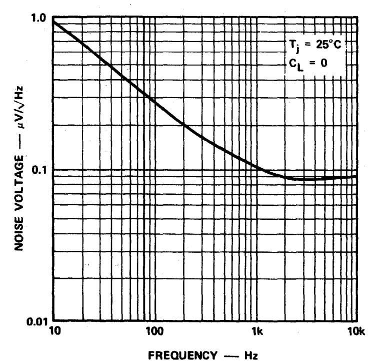
OUTPUT VOLTAGE



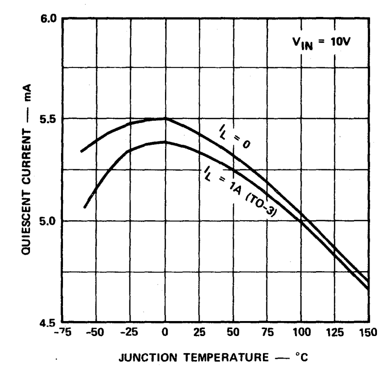
OUTPUT VOLTAGE



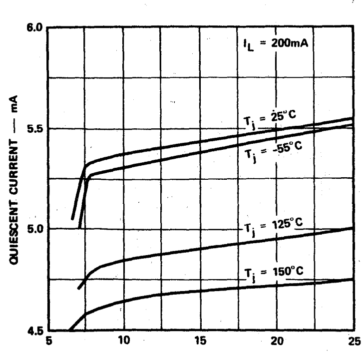
OUTPUT NOISE VOLTAGE



QUIESCENT CURRENT



QUIESCENT CURRENT



FEATURES

- OUTPUT CURRENT IN EXCESS OF 1A
- INTERNAL THERMAL OVERLOAD PROTECTION
- NO EXTERNAL COMPONENTS REQUIRED
- OUTPUT TRANSISTOR SAFE AREA PROTECTION
- INTERNAL SHORT CIRCUIT CURRENT LIMIT
- AVAILABLE IN PLASTIC TO-220 AND METAL TO-3 PACKAGES

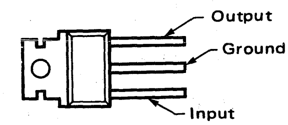
ABSOLUTE MAXIMUM RATINGS

Input Voltage	
(V_0 = 5V through 18V)	35V
(V_0 = 24V)	40V
Internal Power Dissipation (Note 1)	Internally Limited
Operating Temperature Range	0°C to 70°C
Maximum Junction Temperature	
TO-3 Package	150°C
TO-220 Package	150°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature	
TO-3 Package (Soldering, 10 sec)	300° C
TO-220 Package (Soldering, 10 sec)	230°C

NOTE:
1. Thermal resistance without a heat sink for junction to case temperature is 4°C/W for the TO-3 package and 6°C/W for the TO-220 package. Thermal resistance for case to ambient temperature is 35°C/W for the TO-3 package and 50°C/W for the TO-220 package.

PIN CONFIGURATION

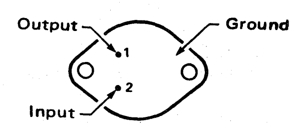
U PACKAGE
TO-220



ORDER NUMBERS:

LM340U5	LM340U15
LM340U6	LM340U18
LM340U8	LM340U24
LM340U12	

DA PACKAGE
TO-3



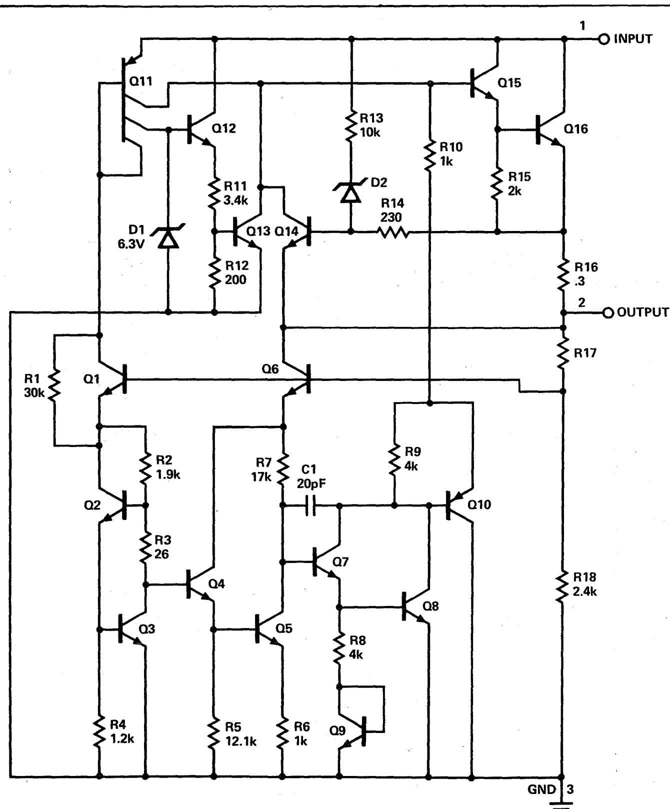
ORDER NUMBERS:

LM340DA5	LM340DA15
LM340DA6	LM340DA18
LM340DA8	LM340DA24

VOLTAGE RANGE

LM340-5	5V	LM340-15	15V
LM340-6	6V	LM340-18	18V
LM340-8	8V	LM340-24	24V
LM340-12	12V		

EQUIVALENT SCHEMATIC



NOTE: ALL RESISTOR VALUES ARE IN OHMS.

TYPICAL CIRCUIT

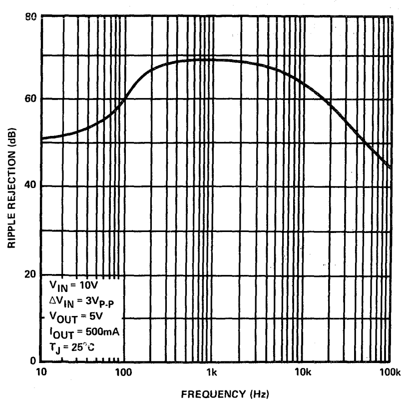
ELECTRICAL CHARACTERISTICS I_{OUT} = 500mA, 0°C ≤ TA ≤ 70°C (Unless Otherwise Noted)

PARAMETER	TEST CONDITIONS	LM340-5 MIN	LM340-5 TYP	LM340-5 MAX	LM340-6 MIN	LM340-6 TYP	LM340-6 MAX	LM340-8 MIN	LM340-8 TYP	LM340-8 MAX	UNITS
V_{OUT}	T_J=25°C	V_{IN}=10V			V_{IN}=IIV			V_{IN}=14V			V
		4.8	5	5.2	5.75	6	6.25	7.7	8	8.3	
	P_D=≤15W 5mA≤I_{OUT}≤1.0A	7V≤V_{IN}≤20V			8V≤V_{IN}≤21V			10.5V≤V_{IN}≤23V			
		4.75		5.25	5.7		6.3	7.6		8.4	
LINE REGULATION	T_J=25°C	7V≤V_{IN}≤25V			8V≤V_{IN}≤25V			10.5V≤V_{IN}≤25V			mV
	I_{OUT}=100mA			50			60			80	
	I_{OUT}=500mA			100			120			160	
LOAD REGULATION	T_J=25°C 5mA≤I_{OUT}≤1.5A			100			120			160	mV
I_{CC}	T_J=25°C		4.2	10		4.2	10		4.2	10	mA
		7V≤V_{IN}≤25V			8V≤V_{IN}≤25V			10.5V≤V_{IN}≤25V			
				1.3			1.3			1	
	5mA≤I_{OUT}≤1.5A			.5			.5			.5	
OUTPUT NOISE VOLTAGE	T_A=25°C 10Hz≤f≤100kHz		40			45			52		μV
VOLTAGE DRIFT	mV/1000 Hrs.			20			24			32	mV
RIPPLE REJECTION	I_{OUT}=20mA f=120Hz		60			57			55		dB
DROPOUT VOLTAGE	T_J=25°C I_{OUT}=1.0A		2			2			2		V

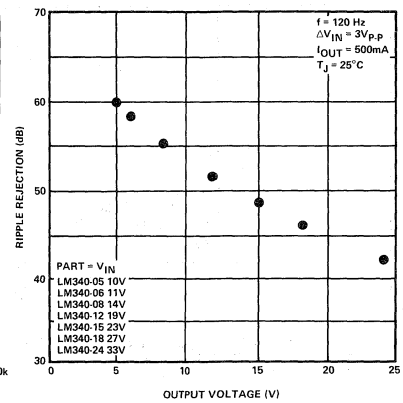
PARAMETER	TEST CONDITIONS	LM340-12 MIN	LM340-12 TYP	LM340-12 MAX	LM340-15 MIN	LM340-15 TYP	LM340-15 MAX	LM340-18 MIN	LM340-18 TYP	LM340-18 MAX	LM340-24 MIN	LM340-24 TYP	LM340-24 MAX	UNITS
V_{OUT}	T_J=25°C	V_{IN}=19V			V_{IN}=23V			V_{IN}=27V			V_{IN}=33V			V
		11.5	12	12.5	14.4	15	15.6	17.3	18	18.7	23	24	25	
	P_D=≤15W 5mA≤I_{OUT}≤1.0A	14.5V≤V_{IN}≤27V			17.5V≤V_{IN}≤30V			21V≤V_{IN}≤33V			27V≤V_{IN}≤38V			
		11.4		12.6	14.25		15.75	17.1		18.9	22.8		25.2	
LINE REGULATION	T_J=25°C	14.5V≤V_{IN}≤30V			17.5V≤V_{IN}≤30V			21V≤V_{IN}≤33V			27V≤V_{IN}≤38V			mV
	I_{OUT}=100mA			120			150			180			240	
	I_{OUT}=500mA			240			300			360			480	
LOAD REGULATION	T_J=25°C 5mA≤I_{OUT}≤1.5A			240			300			360			480	mV
I_{CC}	T_J=25°C		4.2	10		4.2	10		4.2	10		4.2	10	mA
		14.5V≤V_{IN}≤30V			17.5V≤V_{IN}≤30V			21V≤V_{IN}≤33V			27V≤V_{IN}≤38V			
				1			1			1			1	
	5mA≤I_{OUT}≤1.5A			.4			.5			.5			.5	
OUTPUT NOISE VOLTAGE	T_A=25°C 10Hz≤f≤100kHz		75			90			110			170		μV
VOLTAGE DRIFT	mV/1000 Hrs.			48			60			72			96	mV
RIPPLE REJECTION	I_{OUT}=20mA f=120Hz		52			50			48			44		dB
DROPOUT VOLTAGE	T_J=25°C I_{OUT}=1.0A		2			2			2			2		V

TYPICAL PERFORMANCE CHARACTERISTICS

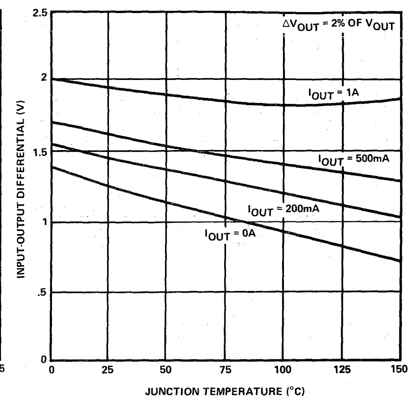
RIPPLE REJECTION



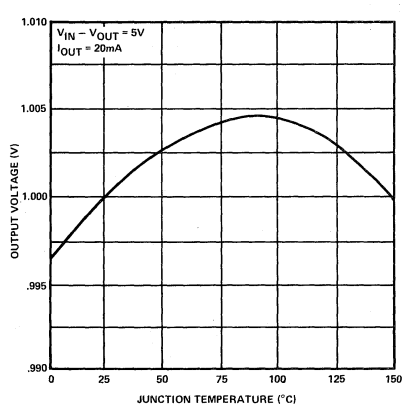
RIPPLE REJECTION



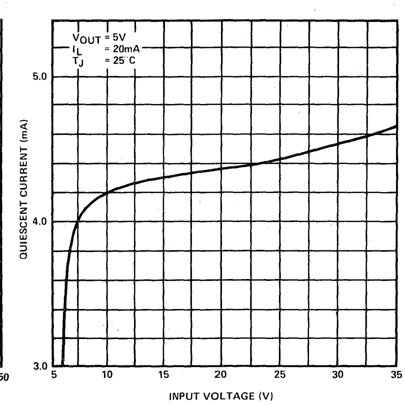
DROPOUT VOLTAGE



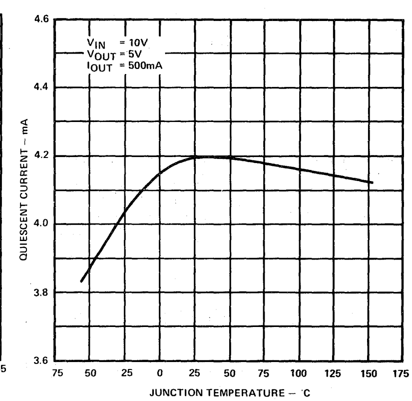
OUTPUT VOLTAGE (NORMALIZED TO 1V AT 25°C TJ)



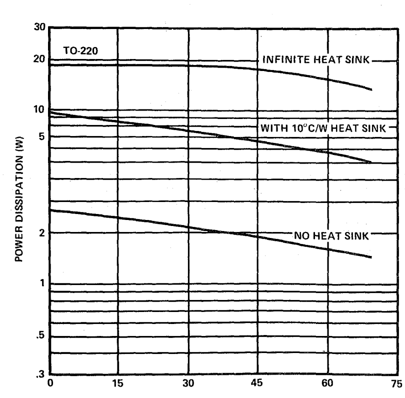
QUIESCENT CURRENT AS A FUNCTION OF INPUT VOLTAGE



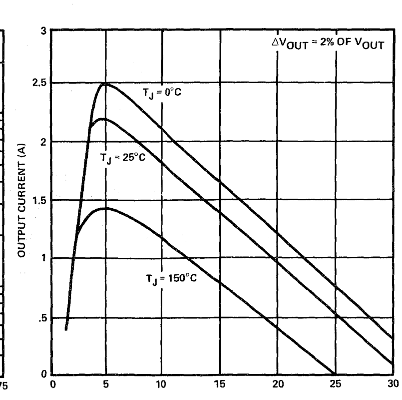
QUIESCENT CURRENT AS A FUNCTION OF TEMPERATURE



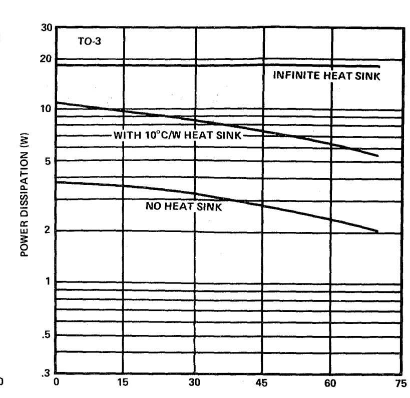
MAXIMUM AVERAGE POWER DISSIPATION



PEAK OUTPUT CURRENT

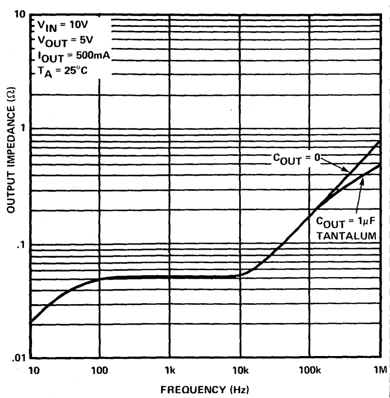


MAXIMUM AVERAGE POWER DISSIPATION



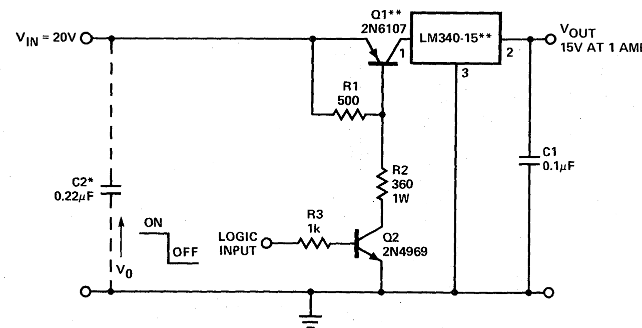
TYPICAL PERFORMANCE CHARACTERISTICS

OUTPUT IMPEDANCE



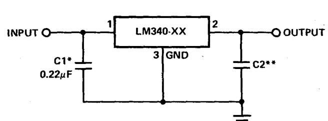
TYPICAL APPLICATIONS

ELECTRONIC SHUTDOWN CIRCUIT



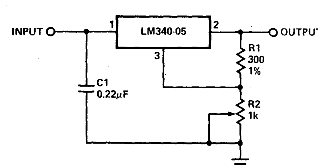
*REQUIRED IF THE REGULATOR IS LOCATED FAR FROM THE POWER SUPPLY FILTER.
**HEAT SINK Q1 AND THE LM340.

FIXED OUTPUT REGULATOR



*REQUIRED IF THE REGULATOR IS LOCATED FAR FROM THE POWER SUPPLY FILTER.
**ALTHOUGH NO OUTPUT CAPACITOR IS NEEDED FOR STABILITY, IT DOES HELP TRANSIENT RESPONSE. (IF NEEDED USE 0.1μF, CERAMIC, DISC.)

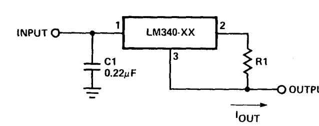
ADJUSTABLE OUTPUT REGULATOR



$V_{OUT} = 5V + (16.7mA + 1_O)R_2$

Δ_{IO} = 1.5mA OVER LINE AND LOAD CHANGES

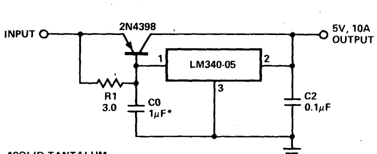
CURRENT REGULATOR



$I_{OUT} = \frac{V_{2-3}}{R1} + I_O$

Δ_{IO} = 1.5mA OVER LINE AND LOAD CHANGES

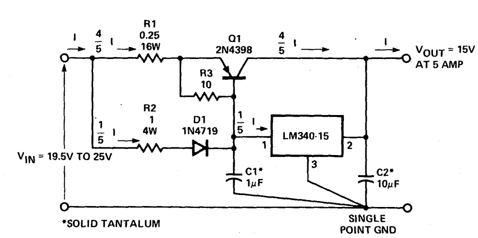
HIGH CURRENT VOLTAGE REGULATOR



*SOLID TANTALUM

TA = 25°C
@V_{IN} 10V, 0A<I_L<10A
LOAD REGULATION = 2mV
@I_L = 10A, 9V<V_{IN}<12V
LINE REGULATION = 20mV

15V AMP REGULATOR WITH SHORT CIRCUIT CURRENT LIMIT



*SOLID TANTALUM

NOTES:
1. CURRENT SHARING BETWEEN THE LM340 AND Q1 ALLOWS THE EXTENSION OF SHORT CIRCUIT CURRENT LIMIT, SAFE OPERATING AREA PROTECTION, AND (ASSUMING Q1'S HEAT SINK HAS FOUR OR MORE TIMES THE CAPACITY OF THE LM340 HEAT SINK) THERMAL SHUTDOWN PROTECTION.
2. $I_{SHORT\ CIRCUIT}$ IS APPROXIMATELY 5.5 AMP.
3. $I_{OUT\ MAX}$ AT V_{OUT} = 15V IS APPROXIMATELY 9.5 AMP.

SE553-BA,F • NE553-BA,F • SE554-BA,F • NE534-BA,F

FEATURES

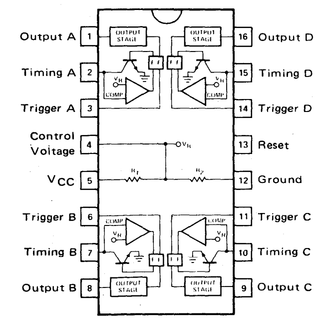
- 100mA OUTPUT CURRENT PER SECTION
- EDGE-TRIGGERED (NO COUPLING CAPACITOR)
- OUTPUT INDEPENDENT OF TRIGGER CONDITIONS
- WIDE SUPPLY VOLTAGE RANGE 4.5V TO 16V
- TIMER INTERVALS FROM MICROSECONDS TO HOURS

APPLICATIONS

SEQUENTIAL TIMING
TIME DELAY GENERATION
PRECISION TIMING
INDUSTRIAL CONTROLS
QUAD ONE-SHOT

PIN CONFIGURATION

BA, F PACKAGE



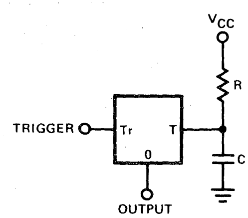
ELECTRICAL CHARACTERISTICS

$T_A = 25°C$, $V_{CC} = +5V$ to $+15V$ (Unless Otherwise Noted).

PARAMETER	TEST CONDITIONS	LIMITS			UNIT
		MIN	TYP	MAX	
Supply Voltage		4.5		16	V
Supply Current	$V_{CC} = 5V$, $R_L = \infty$		18	27	mA
	$V_{CC} = 15V$, $R_L = \infty$		22	32	mA
Timing Accuracy	R = 2k to 100k C = 1μF				
Initial Accuracy			1	4	%
Drift With Temperature			150		ppm/°C
Drift With Supply Voltage			0.03	0.1	%/V
Match Between Sections			0.2	0.5	%
Trigger Voltage		0.8	1.6	2.4	V
Trigger Current					
Logical "1"			10	100	nA
Logical "0"			50	100	μA
Threshold Voltage			0.63		xV_{CC}
Threshold Leakage			10	100	nA
Output Voltage (553)	$I_L = 10mA$		0.1	0.2	V
	$I_L = 100mA$		1.0	1.5	V
Output Voltage (554)	$I_L = 10mA$ $V_{CC} = 15V$	13	14		V
	$I_L = 100mA$ $V_{CC} = 15V$	12.5	13.5		V
Output Leakage			10	100	nA
Propagation Delay			1.0		μs
Risetime of Output	$I_L = 100mA$		100		ns
Falltime of Output	$I_L = 100mA$		100		ns

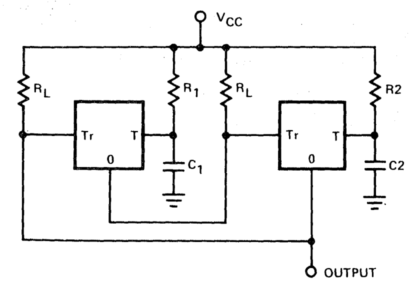
TYPICAL APPLICATIONS

MONOSTABLE OPERATION (ONE SHOT)

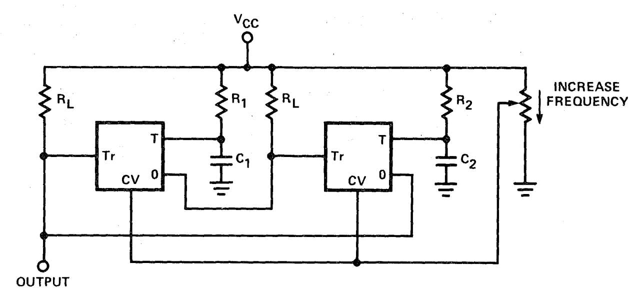


T = RC

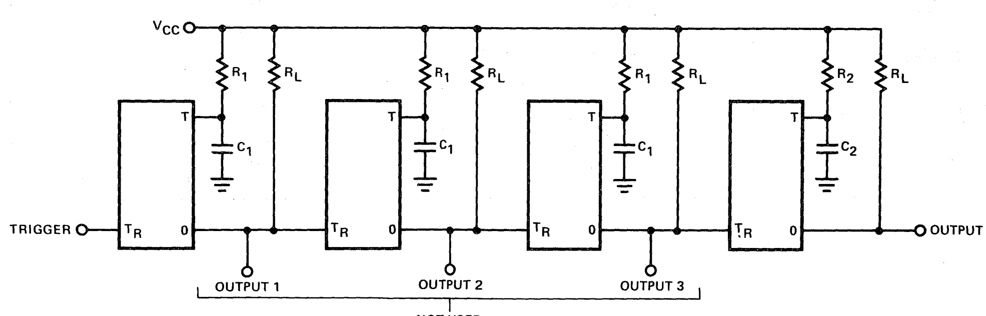
ASTABLE OPERATION (OSCILLATOR)

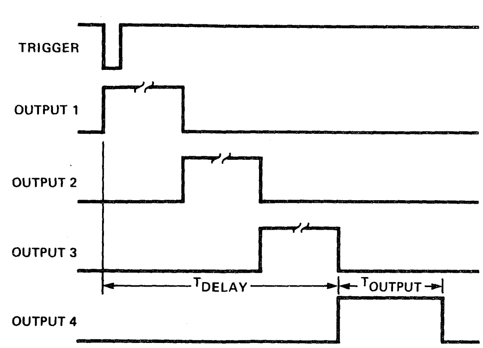


VARIABLE FREQUENCY OSCILLATOR WITH FIXED DUTY CYCLE



LONG-TIME DELAY

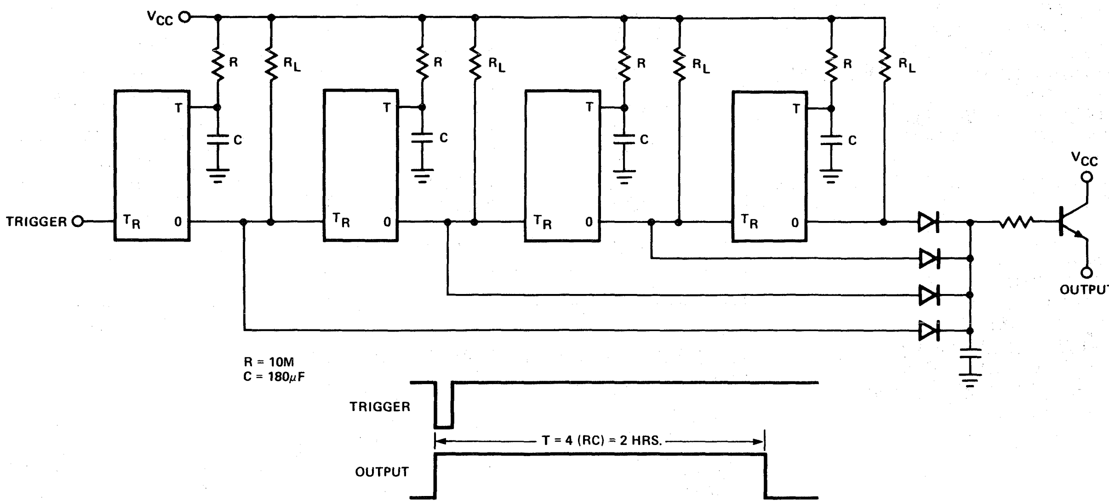




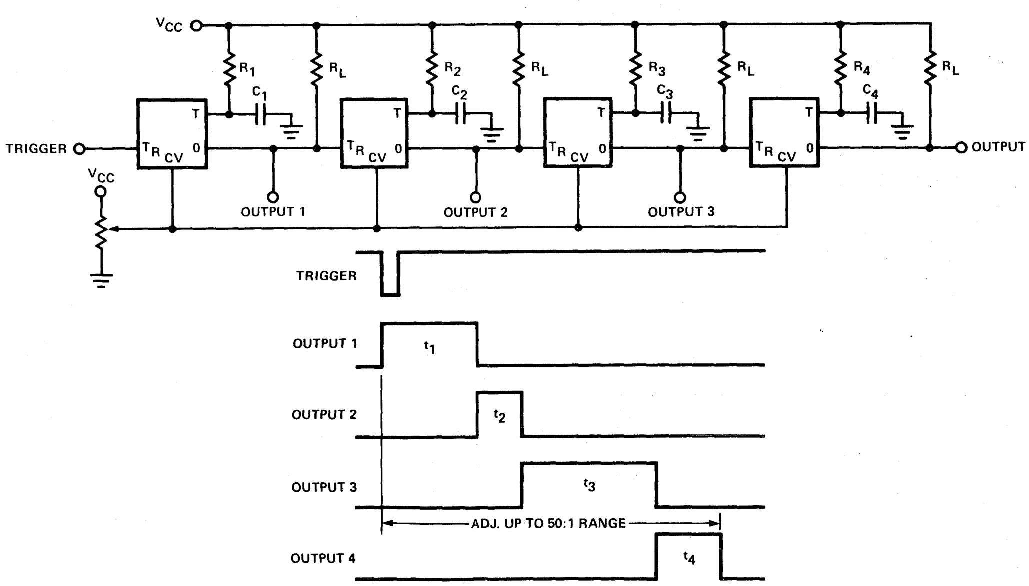
$T_{DELAY} = 3\,(R_1C_1)$
$T_{OUT} = R_2C_2$

TYPICAL APPLICATIONS (CONT'D)

TWO HOUR TIMER



SEQUENTIAL TIMER WITH VOLTAGE CONTROLLED CYCLE TIME (50:1 RANGE)



NOTE: t_1, t_2, t_3, t_4 REMAIN PROPORTIONAL OVER ENTIRE ADJ. RANGE.

SE555-F, T, V·NE555-F, T, V

FEATURES

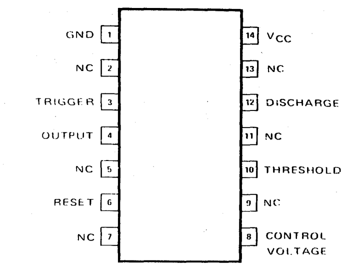
- TIMING FROM MICROSECONDS THROUGH HOURS
- OPERATES IN BOTH ASTABLE AND MONOSTABLE MODES
- ADJUSTABLE DUTY CYCLE
- HIGH CURRENT OUTPUT CAN SOURCE OR SINK 200mA
- OUTPUT CAN DRIVE TTL
- TEMPERATURE STABILITY OF 0.005% PER °C
- NORMALLY ON AND NORMALLY OFF OUTPUT

APPLICATIONS

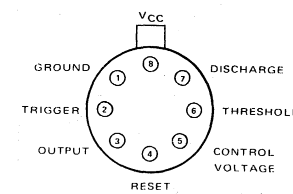
PRECISION TIMING
PULSE GENERATION
SEQUENTIAL TIMING
TIME DELAY GENERATION
PULSE WIDTH MODULATION
PULSE POSITION MODULATION
MISSING PULSE DETECTOR

PIN CONFIGURATION

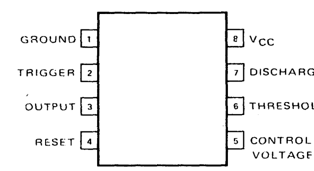
F PACKAGE



T PACKAGE



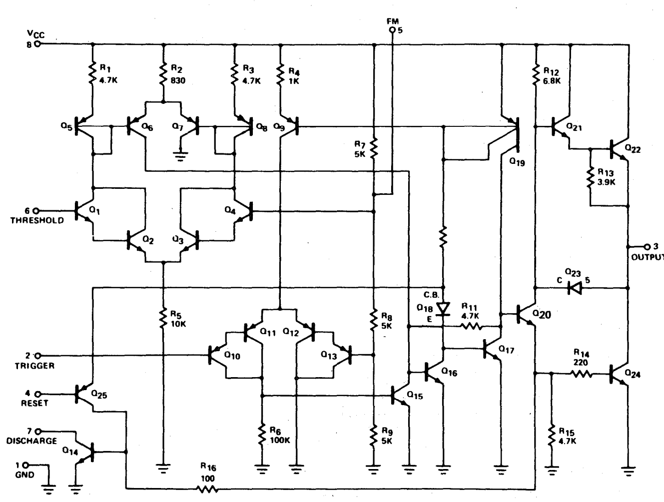
V PACKAGE



ABSOLUTE MAXIMUM RATINGS

Supply Voltage	
SE555	+18V
NE555	+16V
Power Dissipation	600 mW
Operating Temperature Range	
NE555	0°C to +70°C
SE555	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 seconds)	+300°C

EQUIVALENT CIRCUIT



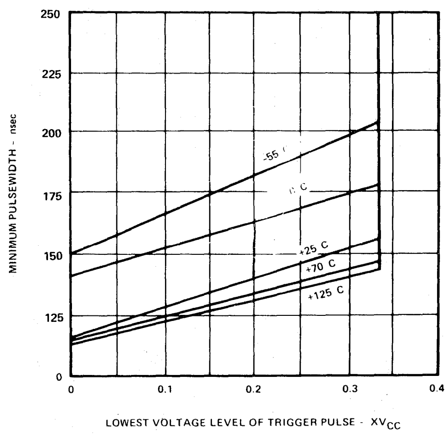
ELECTRICAL CHARACTERISTICS TA = 25°C, VCC = +5V to +15 unless otherwise specified

PARAMETER	TEST CONDITIONS	SE 555			NE 555			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Supply Voltage		4.5		18	4.5		16	V
Supply Current	VCC = 5V $R_L = \infty$		3	5		3	6	mA
	VCC = 15V $R_L = \infty$		10	12		10	15	mA
	Low State, Note 1							
Timing Error (Monostable)	R_A = 2KΩ to 100 KΩ							
Initial Accuracy	C = 0.1µF Note 2		0.5	2		1		%
Drift with Temperature			30	100		50		ppm/°C
Drift with Supply Voltage			0.05	0.2		0.1		%/Volt
Timing Error (Astable)	R_A, R_B = 2KΩ to 100 KΩ							
Initial Accuracy	C = 0.1µF Note 2		1.5			2.25		%
Drift with Temperature			90			150		ppm/°C
Drift with Supply Voltage			0.15			0.3		%/Volt
Threshold Voltage			2/3			2/3		X VCC
Trigger Voltage	VCC = 15V	4.8	5	5.2		5		V
	VCC = 5V	1.45	1.67	1.9		1.67		V
Trigger Current			2.0			2.0		µA
Reset Voltage (Note 4)		0.4	0.7	1.0	0.4	0.7	1.0	V
Reset Current			0.1			0.1		mA
Threshold Current	Note 3		0.1	.25		0.1	.25	µA
Control Voltage Level	VCC = 15V	9.6	10	10.4	9	10	11	V
	VCC = 5V	2.9	3.33	3.8	2.6	3.33	4	V
Output Voltage (low)	VCC = 15V							
	ISINK = 10mA		0.1	0.15		0.1	.25	V
	ISINK = 50mA		0.4	0.5		0.4	.75	V
	ISINK = 100mA		2.0	2.2		2.0	2.5	V
	ISINK = 200mA		2.5			2.5		
	VCC = 5V							
	ISINK = 8mA		0.1	0.25				V
	ISINK = 5mA					.25	.35	
Output Voltage (High)								
	ISOURCE = 200mA		12.5			12.5		
	VCC = 15V							
	ISOURCE = 100mA							
	VCC = 15V	13.0	13.3		12.75	13.3		V
	VCC = 5V	3.0	3.3		2.75	3.3		V
Rise Time of Output			100			100		nsec
Fall Time of Output			100			100		nsec
Discharge Leakage Current			20	100		20	100	NA

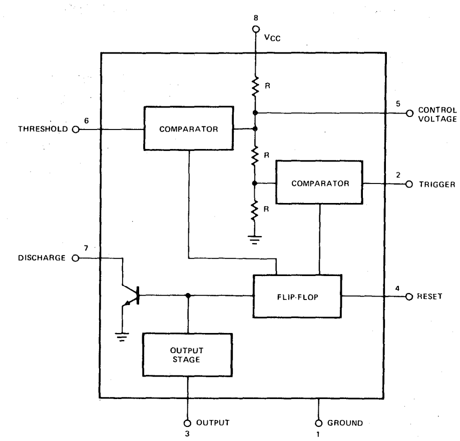
NOTES
1. Supply Current when output high typically 1mA less.
2. Tested at VCC = 5V and VCC = 15V
3. This will determine the maximum value of RA + RBF for 15V operation, the max total R = 20 megohm, and for 5V operation, the max. total R = 6.8 megohm.
4. Specified with trigger input high.

TYPICAL CHARACTERISTICS

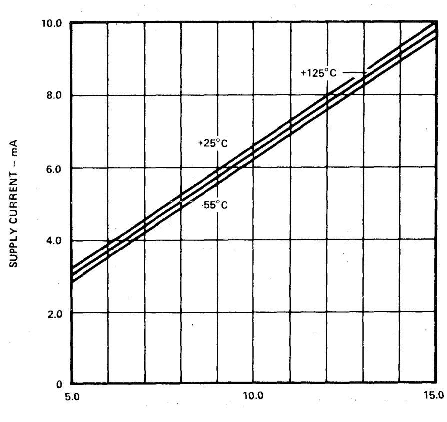
MINIMUM PULSE WIDTH REQUIRED FOR TRIGGERING



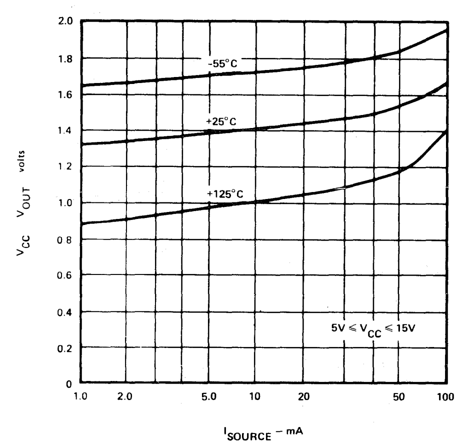
BLOCK DIAGRAM



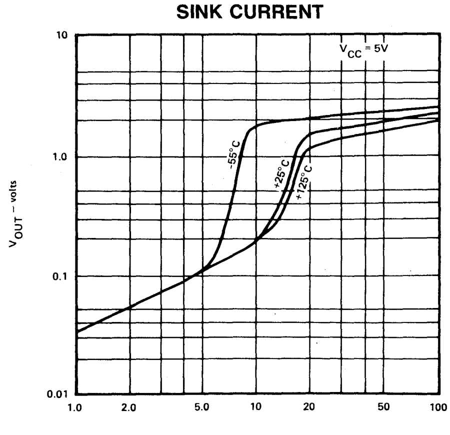
SUPPLY CURRENT vs SUPPLY VOLTAGE



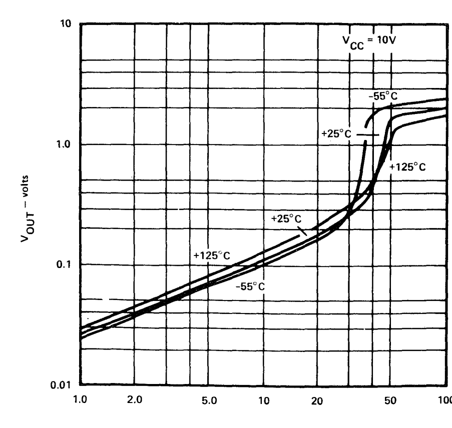
HIGH OUTPUT VOLTAGE DROP vs OUTPUT SOURCE CURRENT



LOW OUTPUT VOLTAGE vs OUTPUT SINK CURRENT

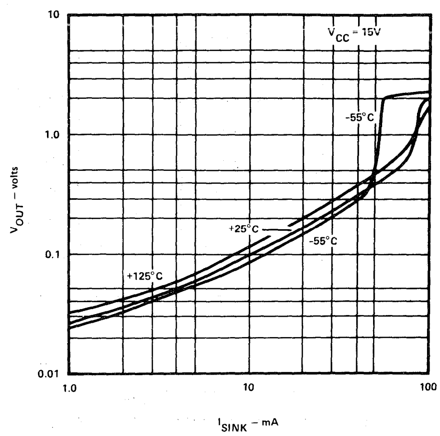


LOW OUTPUT VOLTAGE vs OUTPUT SINK CURRENT

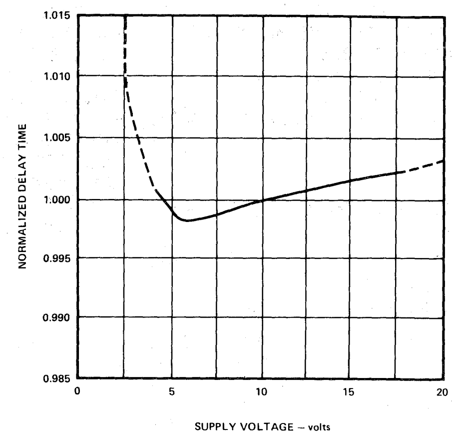


TYPICAL CHARACTERISTICS (CONT'D)

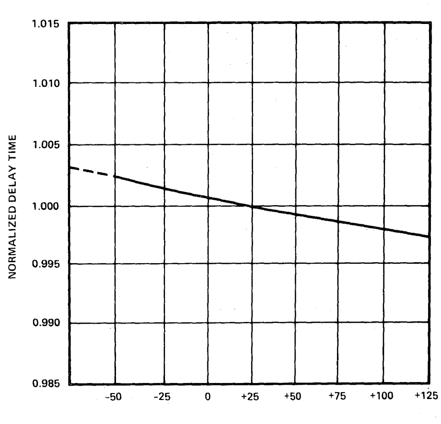
LOW OUTPUT VOLTAGE vs OUTPUT SINK CURRENT



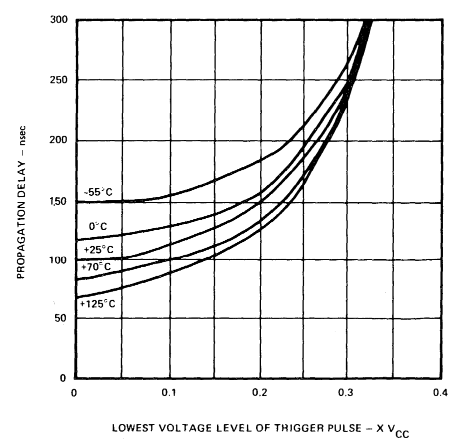
DELAY TIME vs SUPPLY VOLTAGE



DELAY TIME vs TEMPERATURE



PROPAGATION DELAY vs VOLTAGE LEVEL OF TRIGGER PULSE



FEATURES

- TIMING FROM MICROSECONDS TO HOURS
- REPLACES TWO 555 TIMERS
- OPERATES IN BOTH ASTABLE, MONOSTABLE, TIME DELAY MODES
- HIGH OUTPUT CURRENT
- ADJUSTABLE DUTY CYCLE
- TTL COMPATIBLE
- TEMPERATURE STABILITY OF 0.005% PER °C

ABSOLUTE MAXIMUM RATIONS

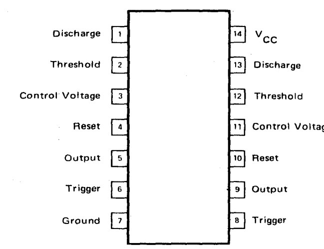
Supply Voltage	
SE556	+18V
NE556	+16V
Power Dissipation	600mW
Operating Temperature Range	
NE556	0°C to +70°C
SE556	−55°C to +125°C
SE556C	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 sec)	+300°C

APPLICATIONS

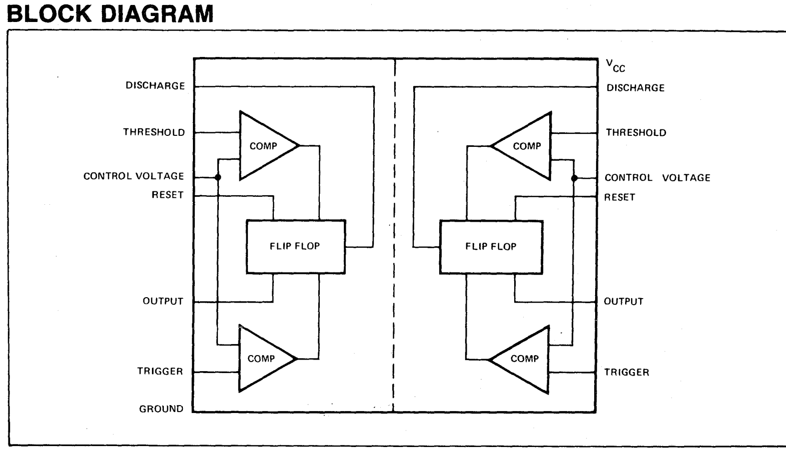
PRECISION TIMING
SEQUENTIAL TIMING
PULSE SHAPING
PULSE GENERATOR
MISSING PULSE DETECTOR
TONE BURST GENERATOR
PULSE WIDTH MODULATION
TIME DELAY GENERATOR
FREQUENCY DIVISION
INDUSTRIAL CONTROLS
PULSE POSITION MODULATION
APPLIANCE TIMING
TRAFFIC LIGHT CONTROL
TOUCH TONE ENCODER

PIN CONFIGURATION

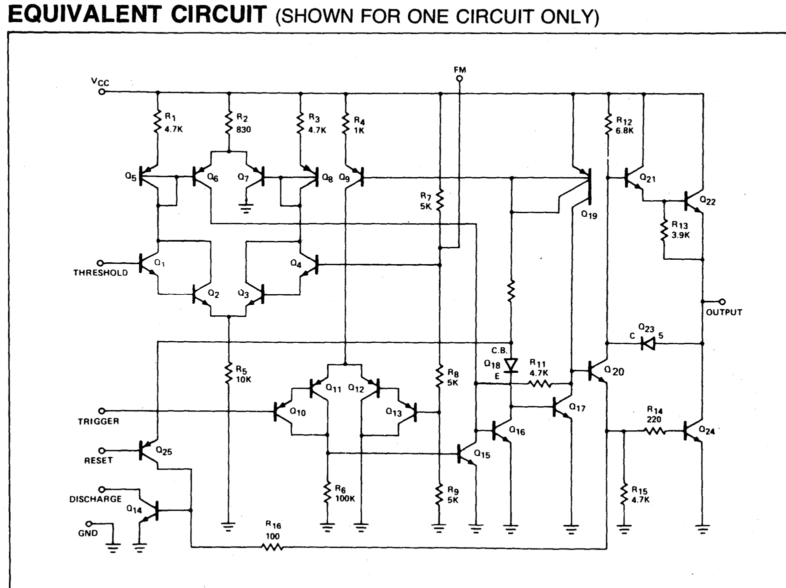
A PACKAGE



BLOCK DIAGRAM



EQUIVALENT CIRCUIT (SHOWN FOR ONE CIRCUIT ONLY)



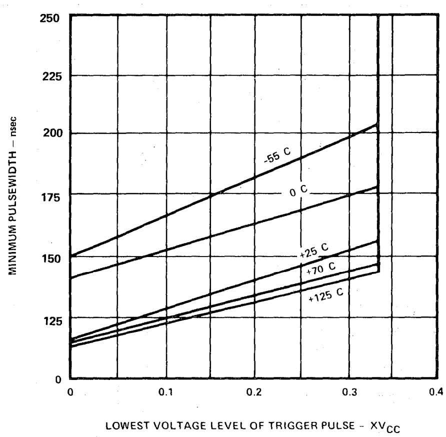
ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = +5V to +15 unless otherwise specified

PARAMETER	TEST CONDITIONS	SE556			NE556			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Supply Voltage		4.5		18	4.5		16	V
Supply Current	V_{CC}=5V $R_L=\infty$		6	10		6	12	mA
	V_{CC}= 15V $R_L=\infty$		20	24		20	30	mA
	Low State, Note 1							
Timing Error (Monostable)	RA=2KΩ to 100KΩ							
Initial Accuracy	C=0.1µF Note 2		0.5	1.5		0.75		%
Drift with Temperature			30	100		50		ppm/°C
Drift with Supply Voltage			0.05	0.2		0.1		%/Volt
Timing Error (Astable)	R_A, R_B=2KΩ to 100KΩ							
Initial Accuracy	C= 0.1µF Note 2		1.5			2.25		%
Drift with Temperature			90			150		ppm/°C
Drift with Supply Voltage			0.15			0.3		%/Volt
Threshold Voltage			2/3			2/3		X V_{CC}
Threshold Current	Note 3		30	250		30	250	nA
Trigger Voltage	V_{CC}= 15V	4.8	5	5.2		5		V
	V_{CC}= 5V	1.45	1.67	1.9		1.67		V
Trigger Current			2.0			2.0		µA
Reset Voltage (Note 5)		0.4	0.7	1.0	0.4	0.7	1.0	V
Reset Current			0.1			0.1		mA
Control Voltage Level	V_{CC} = 15V	9.6	10	10.4	9.0	10	11	V
	V_{CC} = 5V	2.9	3.33	3.8	2.6	3.33	4	V
Output Voltage (low)	V_{CC} = 15V							
	I_{SINK} = 10mA		0.1	0.15		0.1	.25	V
	I_{SINK} = 50mA		0.4	0.5		0.4	.75	V
	I_{SINK} = 100mA		2.0	2.25		2.0	2.75	V
	I_{SINK} = 200mA		2.5			2.5		
	V_{CC} = 5V							
	I_{SINK} = 8mA		0.1	0.25				V
	I_{SINK} = 5mA					.25	.35	
Output Voltage (high)								
	I_{SOURCE} = 200mA		12.5			12.5		
	V_{CC} = 15V							
	I_{SOURCE} = 100mA							
	V_{CC} = 15V	13.0	13.3		12.75	13.3		V
	V_{CC} = 5V	3.0	3.3		2.75	3.3		V
Rise Time of Output			100			100		nsec
Fall Time of Output			100			100		nsec
Discharge Leakage Current			20	100		20	100	nA
Matching Characteristics (Note 4)								
Initial Timing Accuracy			0.05	0.1		0.1	0.2	%
Timing Drift with Temperature			±10			±10		ppm/°C
Drift with Supply Voltage			0.1	0.2		0.2	0.5	%/Volt

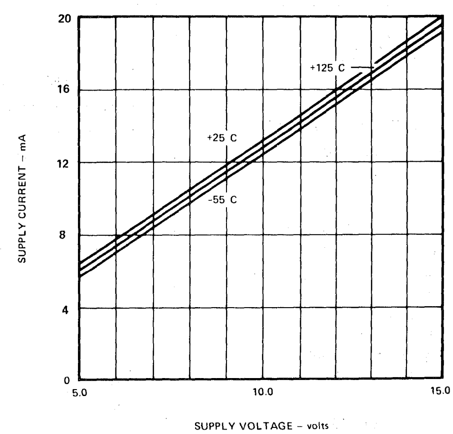
NOTES:
1. Supply current when output is high is typically 1.0ma less.
2. Tested at VCC = 5V and VCC = 15V.
3. This will determine the maximum value of RA + RB for 15V operation, the maximum total R = 20 meg-ohms, and for 5V operation, the max. total R = 6.8 meg-ohm.
4. Matching characteristics refer to the difference between performance characteristics of each timer section.
5. Specified with trigger input high.

TYPICAL CHARACTERISTICS

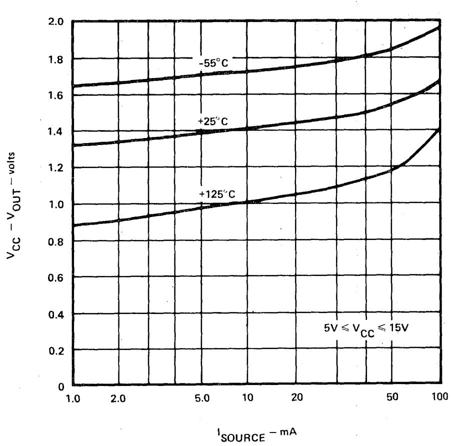
MINIMUM PULSE WIDTH REQUIRED FOR TRIGGERING



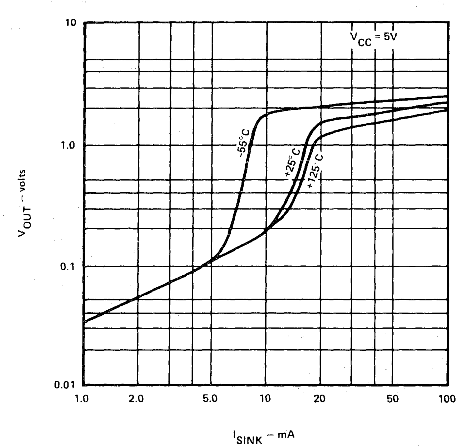
SUPPLY CURRENT vs SUPPLY VOLTAGE



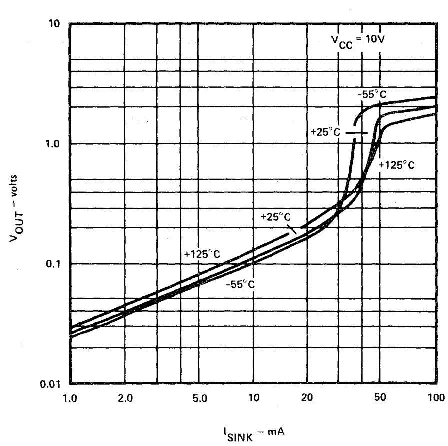
HIGH OUTPUT VOLTAGE DROP vs OUTPUT SOURCE CURRENT



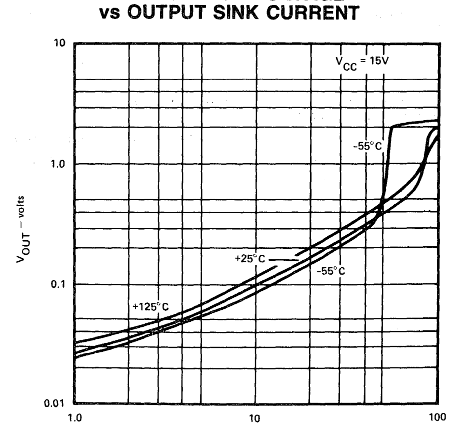
LOW OUTPUT VOLTAGE vs OUTPUT SINK CURRENT



LOW OUTPUT VOLTAGE vs OUTPUT SINK CURRENT

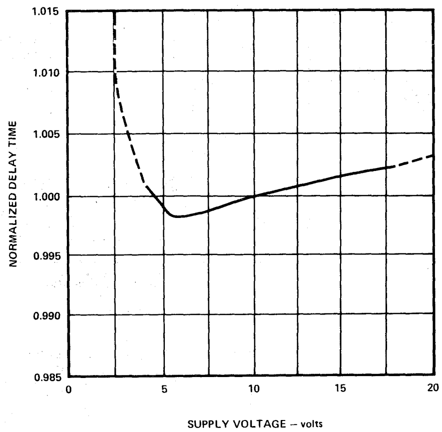


LOW OUTPUT VOLTAGE vs OUTPUT SINK CURRENT

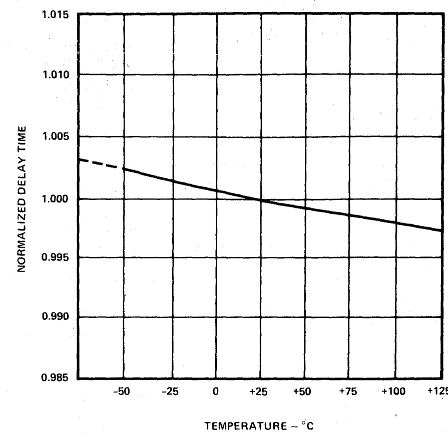


TYPICAL CHARACTERISTICS (CONT'D)

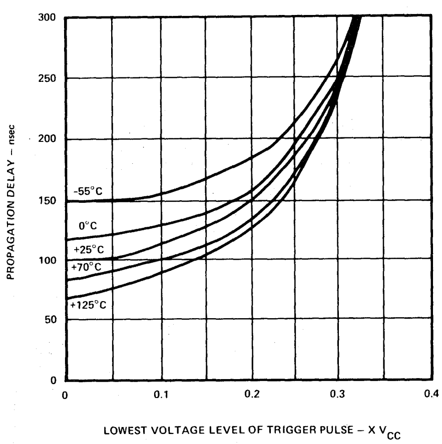
DELAY TIME vs SUPPLY VOLTAGE



DELAY TIME vs TEMPERATURE



PROPAGATION DELAY vs VOLTAGE LEVEL OF TRIGGER PULSE



ANALOG

SE501-AIK · NE501-AIK

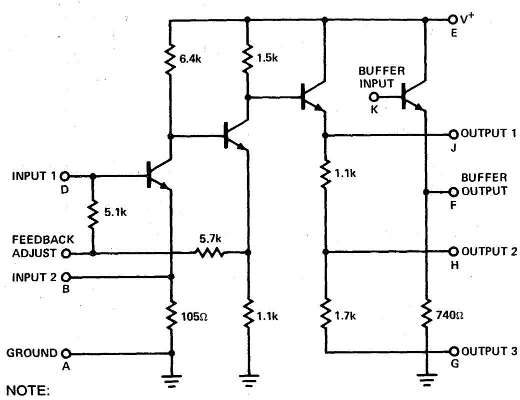
FEATURES

- ADJUSTABLE GAIN AND IMPEDANCE CHARACTERISTICS
- UNITY GAIN FREQUENCY — 150 MHz
- NOISE FIGURE — 5.0dB
- POWER DISSIPATION — 20mW

ABSOLUTE MAXIMUM RATINGS

Voltage Applied VG,H,E,C	+8.0V
Voltage Applied VB	±3.0V
Voltage Applied VK,D	+4.0V
Current Rating IF,J	±30mA
Storage Temperature	−65° to + 150°C
Operating Temperature	
NE501	0°C to +70°C
SE501	−55°C to +125°C

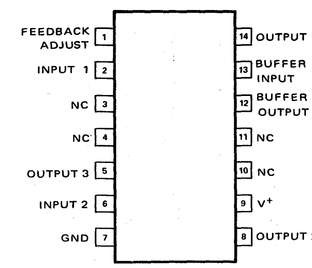
CIRCUIT SCHEMATIC



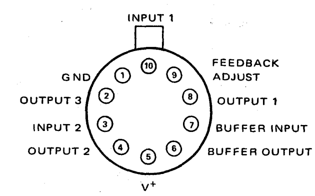
NOTE:
Component values are typical.

CONFIGURATION

A PACKAGE



K PACKAGE



ELECTRICAL CHARACTERISTICS

PARAMETER	TEST CONDITIONS	NE501			SE501			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Voltage Gain	f = 50 kHz; Notes 1, 2, 6	22.5	24	26.5	23	24	26	dB
Bandwidth (−3dB)	Notes 1, 2, 6	11			14			MHz
Unity Gain Frequency	A_{VO} = OdB; Notes 2, 6	100	150		100	150		MHz
Voltage Gain Stability	f = 50 kHz; T = 0°C; Notes 2, 6	−1.0						dB
	f = 50 kHz; T = +70°C; Notes 2,6			+0.6				dB
	f = 50 kHz; T = −50°C; Notes 2, 6				−1.0			dB
	f = 50 kHz; T = +125°C; Notes 2, 6						+0.6	dB
Output Voltage	Notes 1, 2, 6, 9	0.71	1.0		0.71	1.0		V_{RMS}
Input Impedance	Notes 1, 6; f = 50 kHz; $V_J = V_K$	470		1200	540		1100	Ω
Output Impedance	Notes 1, 2; f = 50 kHz; V_D = AC ground		12	18		12	18	Ω
Output Impedance	Notes 1, 5; f = 50 kHz; V_D = AC ground		25	65		25	50	Ω
Power Dissipation				24			21	mW
Power Dissipation	$V_K = V_J$			60			53	mW
Pulse Response								
Delay Time	Notes 2, 6, 7			15			15	ns
Rise Time	Notes 2, 6, 7		12	20		12	16	ns
Noise Figure	f = 100 kHz; BW = 100 Hz; Zs = 500Ω		5.0	8.0				dB
	f_C = 100 kHz, BW = 100 Hz; Zs = 500Ω $V_J = V_K$					5.0	7.0	dB

(Notes: 3, 4, 5 8) Standard Conditions: V_E = +6.0 V, V_A = 0V, $V_G = V_B$, T = +25°C (except as noted)

NOTES:
1. Variations in this parameter depend on optional alternate connections as indicated in accompanying curves.
2. Measured at Pin F, with Pins J and K connected.
3. Pins not specifically referenced are left electrically open. All voltages are referenced to Pin A. Letter subscripts denote pins on circuit schematic.
4. Positive current flow is defined as into the terminal referenced.
5. Measured at Pin J.
6. Load Resistance = 600Ω, capacitively coupled.
7. Delay time is defined as the time interval between the 50% points of e_D and e_F. Rise time = 20% to 80% points of e_F. Input Pulse Characteristics: Amplitude = 25mV; PW = 100 ns.
8. See Signetics SURE Program Bulletin No. 5001 for definition of Acceptance test Sub-Groups Sub-Group A-7 is used for the electrical end points for Linear Products.
9. Total harmonic distortion less than 5% at e_o = 0.71 V_{RMS}.

FEATURES

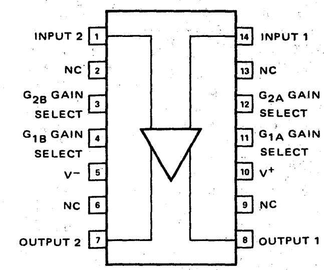
- 120 MHz BANDWIDTH
- ADJUSTABLE GAINS FROM 0 TO 400
- ADJUSTABLE PASS BAND
- NO FREQUENCY COMPENSATION REQUIRED

ABSOLUTE MAXIMUM RATINGS

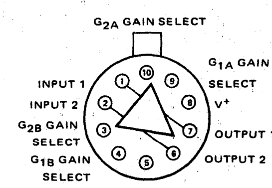
Supply Voltage	±8V
Differential Input Voltage	±5V
Common Mode Input Voltage	±6V
Output Current	10mA
Operating Temperature Range	
SE592K	−55°C to +125°C
NE592K	0°C to+ 70°C
Storage Temperature Range	−65°C to +150°C

PIN CONFIGURATION

A PACKAGE



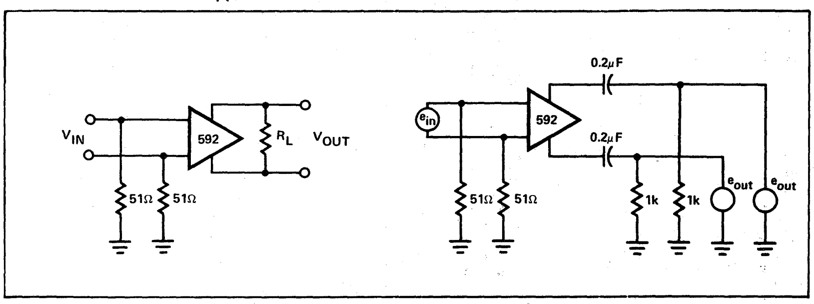
K PACKAGE



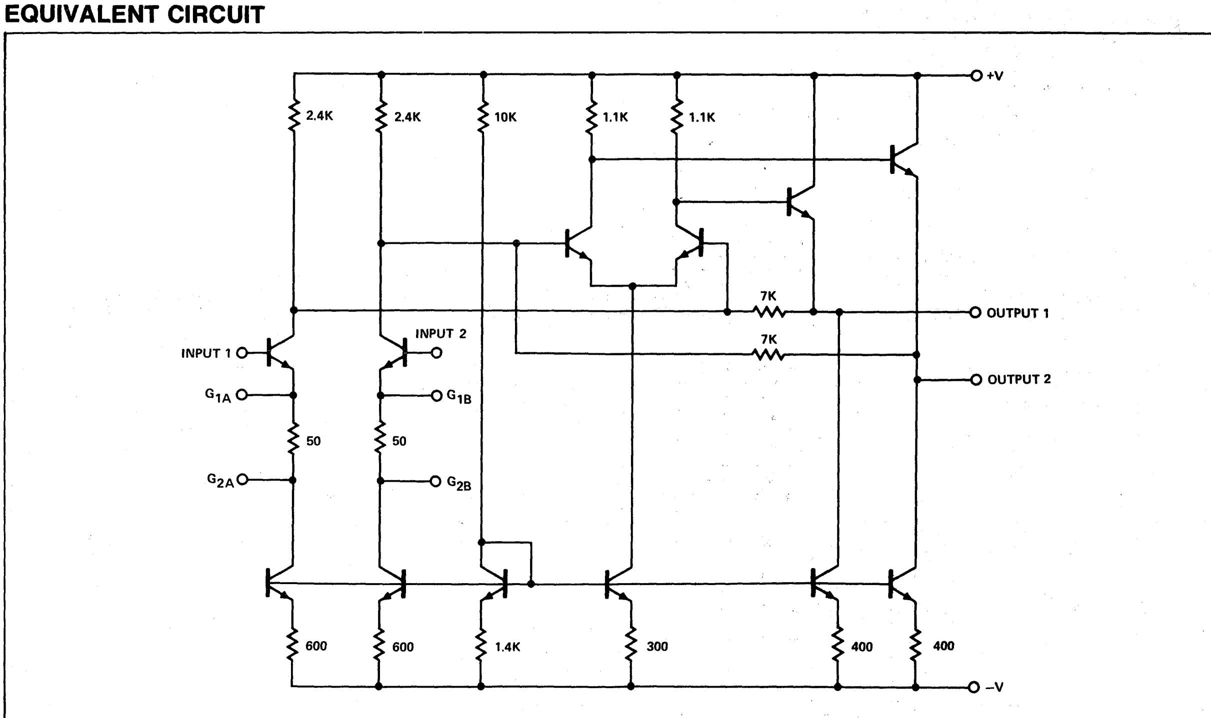
NOTE:
Pin 5 connected to case.

Thermal Resistance (θ_{J-A}, Junction to Ambient for each package):	
A Package	0.16°C/mW
K Package	0.145°C/mW
Power Dissipation	500mW

TEST CIRCUITS (T_A = 25°C unless otherwise specified)



EQUIVALENT CIRCUIT



ANALOG

ELECTRICAL CHARACTERISTICS Standard Conditions (T_A = +25°C, V_S = ±6V, V_{CM}=0 unless otherwise specified)

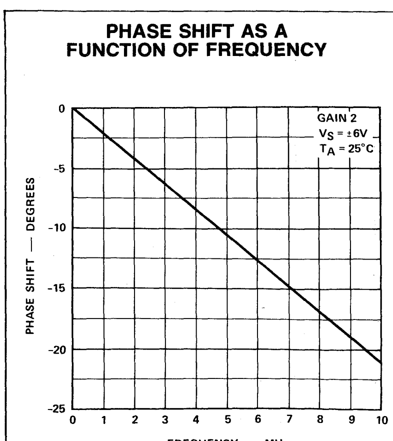
PARAMETER	TEST CONDITIONS	NE 592 MIN	NE 592 TYP	NE 592 MAX	SE 592 MIN	SE 592 TYP	SE 592 MAX	UNITS
Differential Voltage Gain								
Gain 1	Note 1 R_L = 2KΩ, V_{OUT} = 3V p-p	250	400	600	300	400	500	
Gain 2	Note 2	80	100	120	90	100	110	
Bandwidth								
Gain 1	Note 1		40			40		MHz
Gain 2	Note 2		90			90		MHz
Rise Time								
Gain 1	Note 1 V_{OUT} = 1V p-p		10.5			10.5		ns
Gain 2	Note 2		4.5	12		4.5	10	ns
Propagation Delay								
Gain 1	Note 1 V_{OUT} = 1V i-p		7.5			7.5		ns
Gain 2	Note 2		6.0	10		6.0	10	ns
Input Resistance								
Gain 1	Note 1		4.0			4.0		KΩ
Gain 2	Note 2	10	30		20	30		KΩ
Input Capacitance	Gain 2, Note 2		2.0			2.0		pF
Input Offset Current			0.4	5.0		0.4	3.0	μA
Input Bias Current			9.0	30		9.0	20	μA
Input Noise Voltage	BW 1 kHz to 10 kHz		12			12		μV rms
Input Voltage Range				±1.0			±1.0	V
Common Mode Rejection Ratio								
Gain 2	VCM ±1V,F < 100 kHz	60	86		60	86		dB
Gain 2	VCM ±1V,F = 5 MHz		60			60		dB
Supply Voltage Rejection Ratio								
Gain 2	ΔVS = ±0.5V	50	70		50	70		dB
Output Offset Voltage								
Gain 3	R_L = ∞, Note 3		0.35	0.75		0.35	0.75	V
Output Common Mode Voltage	R_L = ∞	2.4	2.9	3.4	2.4	2.9	3.4	V
Output Voltage Swing	R_L = 2K	3.0	4.0		3.0	4.0		
Output Resistance			20			20		Ω
Power Supply Current	R_L = ∞		18	24		18	24	mA

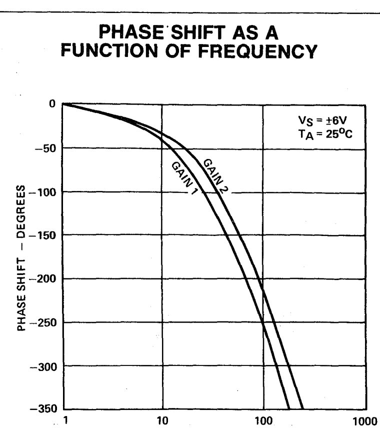
Recommended Operating Supply Voltages (V_S = ±6.0V)

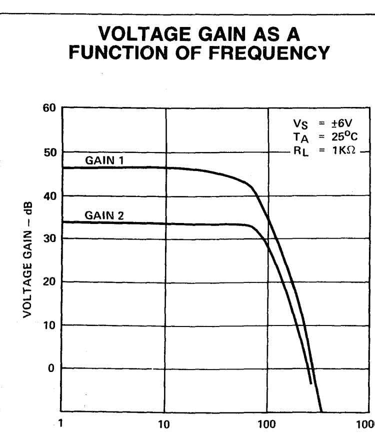
NOTES:

1. Gain select pins G_{1A} and G_{1B} connected together.
2. Gain select pins G_{2A} and G_{2B} connected together.
3. All gain select pins open.

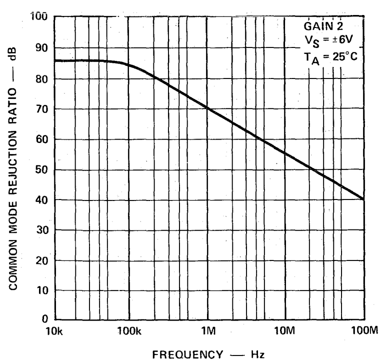
TYPICAL CHARACTERISTICS



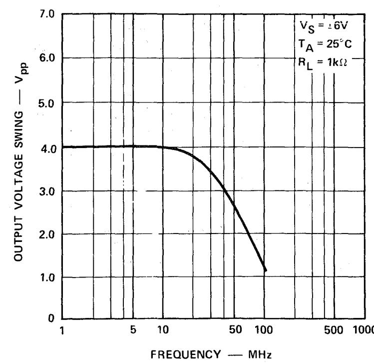




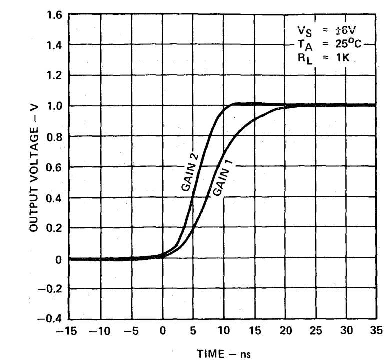
COMMON MODE REJECTION RATIO AS A FUNCTION OF FREQUENCY



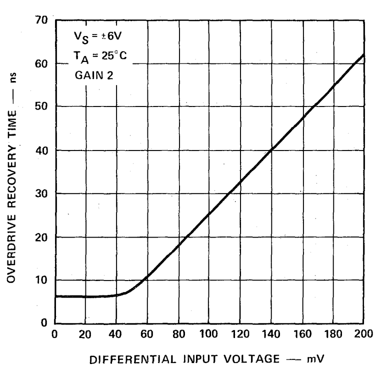
OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY



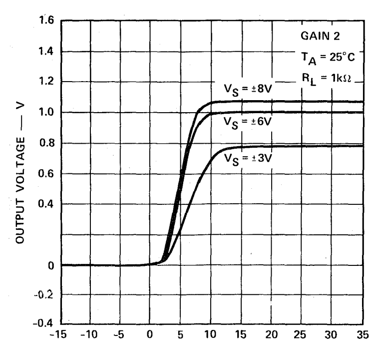
PULSE RESPONSE



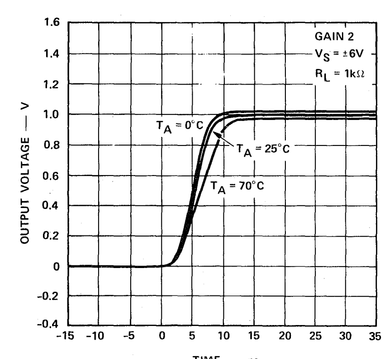
DIFFERENTIAL OVERDRIVE RECOVERY TIME



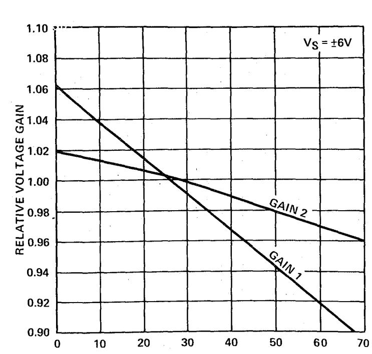
PULSE RESPONSE AS A FUNCTION OF SUPPLY VOLTAGE



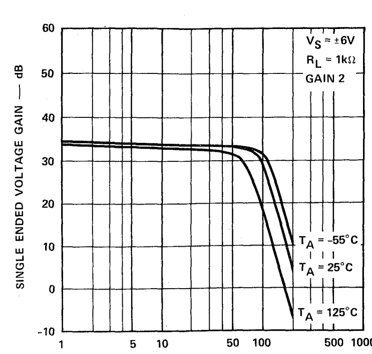
PULSE RESPONSE AS A FUNCTION OF TEMPERATURE



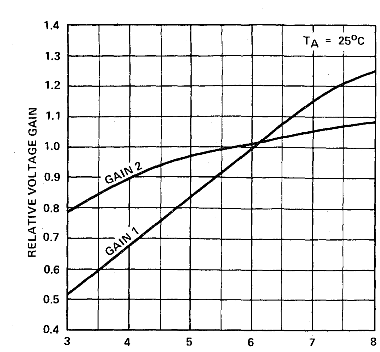
VOLTAGE GAIN AS A FUNCTION OF TEMPERATURE



GAIN VS FREQUENCY AS A FUNCTION OF TEMPERATURE

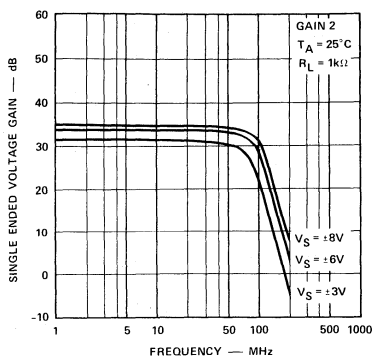


VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE

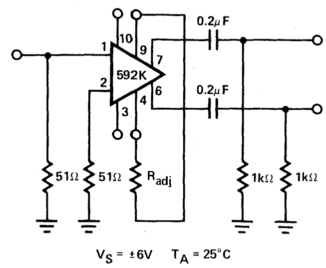


TYPICAL CHARACTERISTICS (Cont'd)

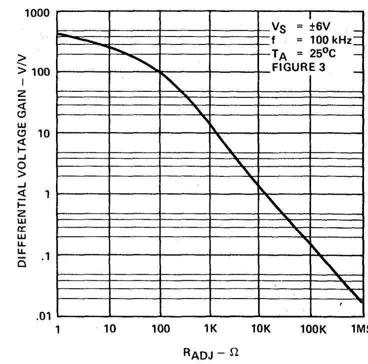
GAIN VS FREQUENCY AS A FUNCTION OF SUPPLY VOLTAGE



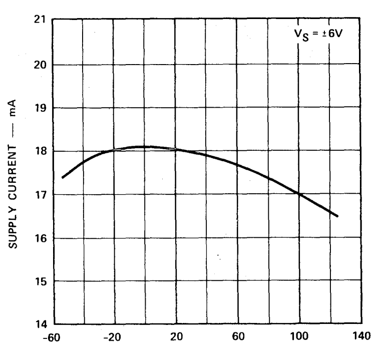
VOLTAGE GAIN ADJUST CIRCUIT



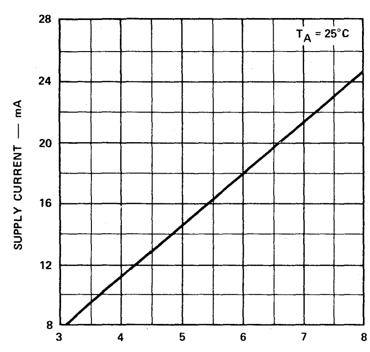
VOLTAGE GAIN AS A FUNCTION OF RADJ (FIGURE 3)



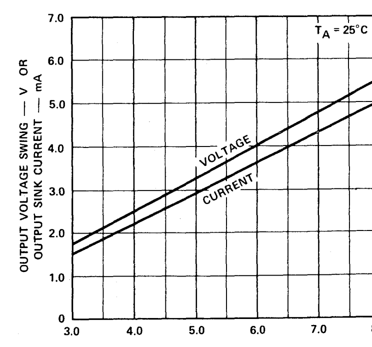
SUPPLY CURRENT AS A FUNCTION OF TEMPERATURE



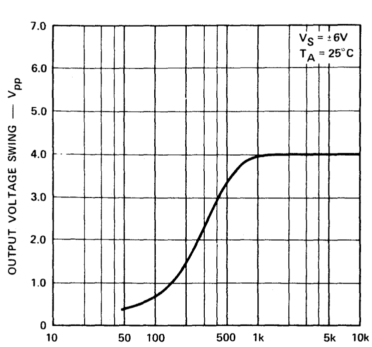
SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



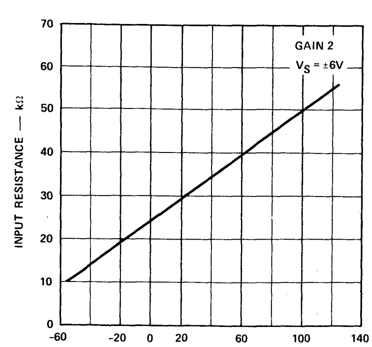
OUTPUT VOLTAGE AND CURRENT SWING AS A FUNCTION OF SUPPLY VOLTAGE



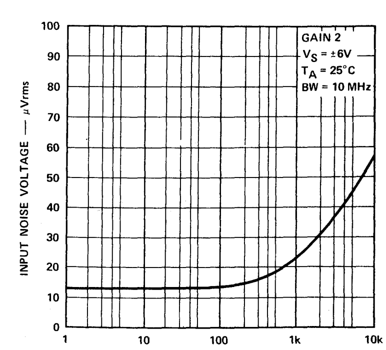
OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE



INPUT RESISTANCT AS A FUNCTION OF TEMPERATURE

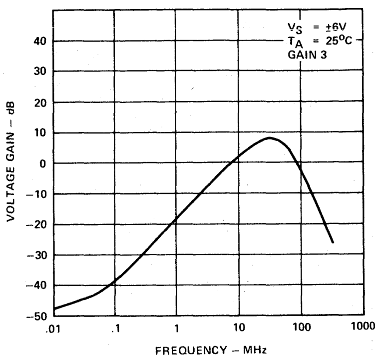


INPUT NOISE VOLTAGE AS A FUNCTION OF SOURCE RESISTANCE



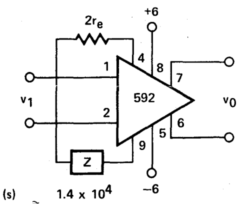
TYPICAL CHARACTERISTICS (Cont'd)

VOLTAGE GAIN AS A FUNCTION OF FREQUENCY (ALL GAIN SELECT PINS OPEN)



TYPICAL APPLICATIONS

FILTER NETWORKS



$$\frac{v_0(s)}{v_1(s)} \cong \frac{1.4 \times 10^4}{Z(s) + 2r_e}$$

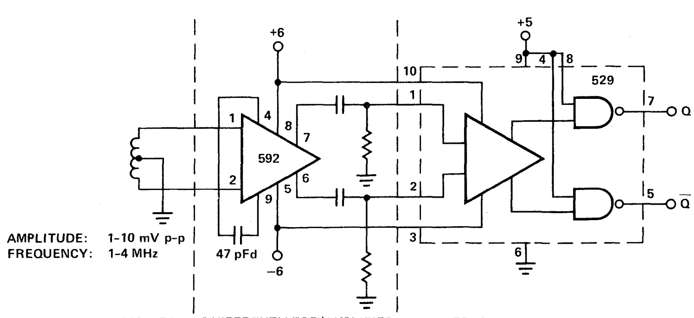
$$\cong \frac{1.4 \times 10^4}{Z(s) + 32}$$

BASIC CONFIGURATION

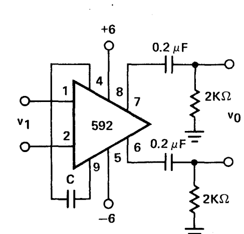
Z NETWORK	FILTER TYPE	$\frac{v_0(s)}{v_1(s)}$ TRANSFER FUNCTION
R L	LOW PASS	$\frac{1.4 \times 10^4}{L}\left[\frac{1}{s + R/L}\right]$
R C	HIGH PASS	$\frac{1.4 \times 10^4}{R}\left[\frac{s}{s + 1/RC}\right]$
R L C	BAND PASS	$\frac{1.4 \times 10^4}{L}\left[\frac{s}{s^2 + R/L\, s + 1/LC}\right]$
R L C	BAND REJECT	$\frac{1.4 \times 10^4}{R}\left[\frac{s^2 + 1/LC}{s^2 + 1/LC + s/RC}\right]$

NOTE:
In the networks above, the R value used is assumed to include $2\,r_e$, or approximately 32 OHMS.

DISC/TAPE PHASE MODULATED READBACK SYSTEMS



DIFFERENTIATION WITH HIGH COMMON MODE NOISE REJECTION



FOR FREQUENCY $F_1 << 1/2\pi(32)\,C$

$v_0 \cong 1.4 \times 10^4 C \frac{dv_i}{dT}$

FEATURES

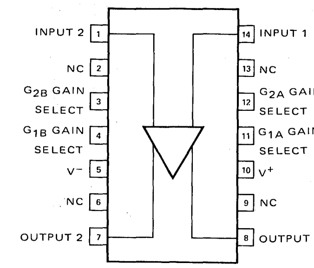
- **120 MHz BANDWIDTH**
- **250kΩ INPUT RESISTANCE**
- **SELECTABLE GAINS OF 10,100 and 400**
- **NO FREQUENCY COMPENSATION REQUIRED**

ABSOLUTE MAXIMUM RATINGS

Differential Input Voltage	±5V
Common Mode Input Voltage	±6V
V_{CC}	±8V
Output Current	10mA
Junction Temperature	+150°C
Storage Temperature Range	−65°C to +150°C
Operation Temperature Range	
μA733C	0°C to +75°C
μA733	−55°C to +125°C

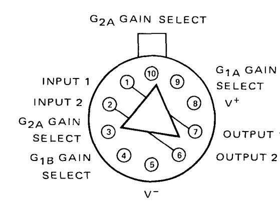
PIN CONFIGURATION

A, I PACKAGE



ORDER PART NOS.
μA733A/ μA733I/
μA733CA/ μA733CI

K PACKAGE

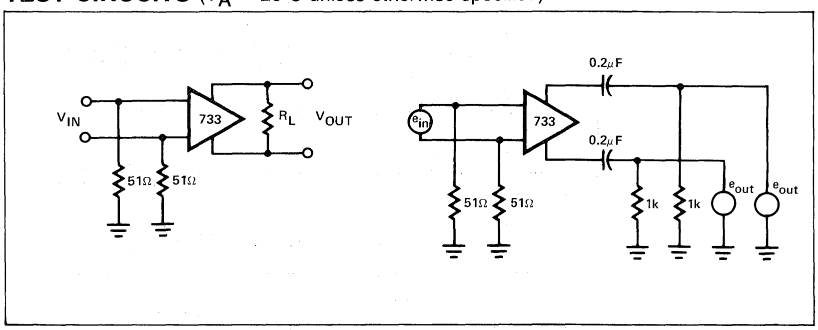


NOTE: Pin 5 connected to case.
ORDER PART NOS.
μA733K/μA733CK

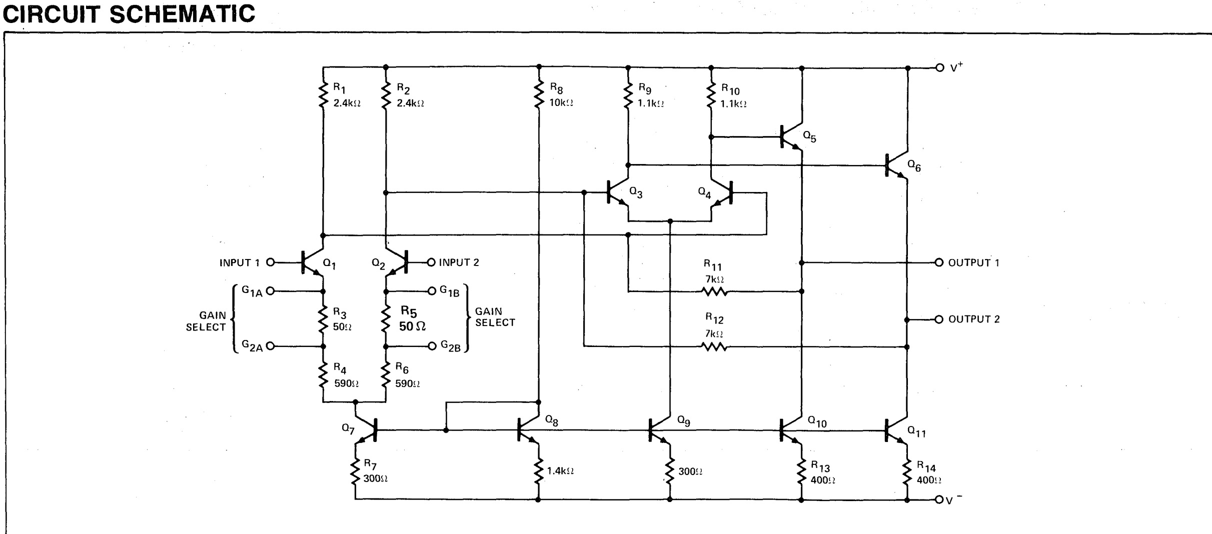
Thermal Resistance (θ_{J-A}, Junction to Ambient for each package):

A Package	0.16°C/mW
I Package	0.10°C/mW
K Package	0.145°C/mW
Power Dissipation	500mW

TEST CIRCUITS (T_A = 25°C unless otherwise specified)



CIRCUIT SCHEMATIC



ELECTRICAL CHARACTERISTICS

Standard Conditions (T_A = +25°C, V_S = ±V, V_{CM} = 0 unless otherwise specified)

PARAMETERS	TEST CONDITIONS		μA733C MIN	μA733C TYP	μA733C MAX	μA733 MIN	μA733 TYP	μA733 MAX	UNITS
Differential Voltage Gain									
Gain 1		Note 1	250	400	600	300	400	500	
Gain 2	R_I = 2kΩ, V_{out} = 3V p-p	Note 2	80	100	120	90	100	110	
Gain 3		Note 3	8.0	10	12	9.0	10	11	
Bandwidth									
Gain 1		Note 1		40			40		MHz
Gain 2		Note 2		90			90		MHz
Gain 3		Note 3		120			120		MHz
Rise Time									
Gain 1		Note 1		10.5			10.5		ns
Gain 2	V_{out} = 1V p-p	Note 2		4.5	12		4.5	10	ns
Gain 3		Note 3		2.5			2.5		ns
Propagation Delay									
Gain 1		Note 1		7.5			7.5		ns
Gain 2	V_{out} = 1V p-p	Note 2		6.0	10		6.0	10	ns
Gain 3		Note 3		3.6			3.6		ns
Input Resistance									
Gain 1		Note 1		4.0			4.0		kΩ
Gain 2		Note 2	10	30		20	30		kΩ
Gain 3		Note 3		250			250		kΩ
Input Capacitance	Gain 2	Note 2		2.0			2.0		pF
Input Offset Current				0.4	5.0		0.4	3.0	μA
Input Bias Current				9.0	30		9.0	20	μA
Input Noise Voltage	BW = 1k Hz to 10 MHz			12			12		μV_{rms}
Input Voltage Range			±1.0			±1.0			V
Common Mode Rejection Ratio									
Gain 2	V_{CM} = ±V, f≤100 kHz		60	86		60	86		dB
Gain 2	V_{CM} = ±1V, F = 5 MHz			60			60		dB
Supply Voltage Rejection Ratio									
Gain 2	ΔV_S = ±0.5 V		50	70		50	70		dB
Output Offset Voltage									
Gain 1	R_L = ∞	Note 1		0.6	1.5		0.6	1.5	V
Gain 2 and 3		Notes 2,3		0.35	1.5		0.35	1.0	V
Output Common Mode Voltage	R_L = ∞		2.4	2.9	3.4	2.4	2.9	3.4	V
Output Voltage Swing	R_L = 2k		3.0	4.0		3.0	4.0		
Output Sink Current			2.5	3.6		2.5	3.6		mA
Output Resistance				20			20		Ω
Power Supply Current	R_L = ∞			18	24		18	24	mA

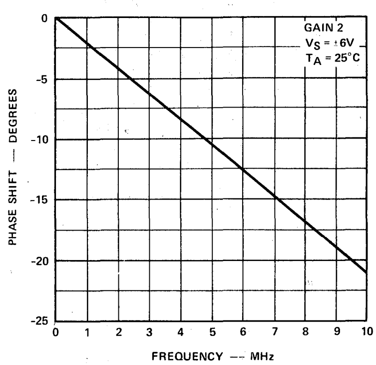
Recommended Operating Supply Voltages (V_S = ±6.0 V)

NOTES:

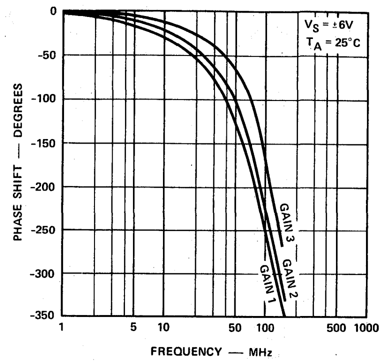
1. Gain select pins G_{1A} and G_{1B} connected together.
2. Gain select pins G_{2A} and G_{2B} connected together.
3. All gain select pins open.

TYPICAL CHARACTERISTIC CURVES

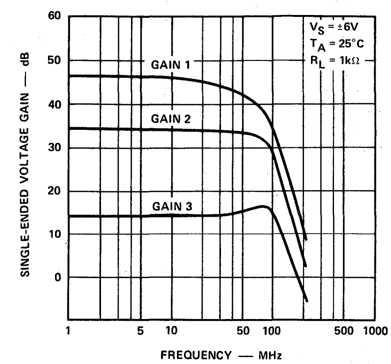
PHASE SHIFT AS A FUNCTION OF FREQUENCY



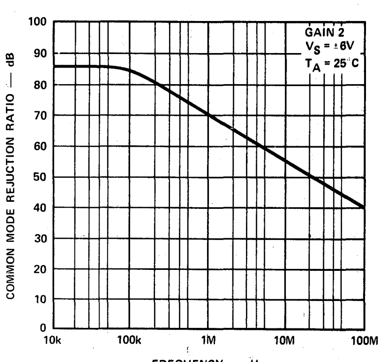
PHASE SHIFT AS A FUNCTION OF FREQUENCY



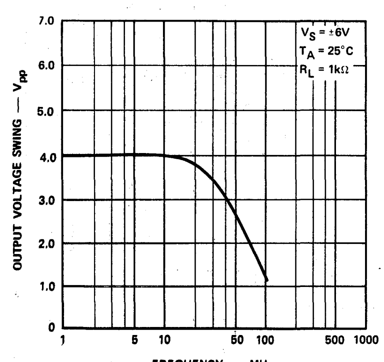
VOLTAGE GAIN AS A FUNCTION OF FREQUENCY



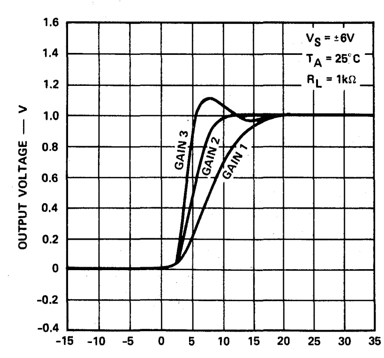
COMMON MODE REJECTION RATIO AS A FUNCTION OF FREQUENCY



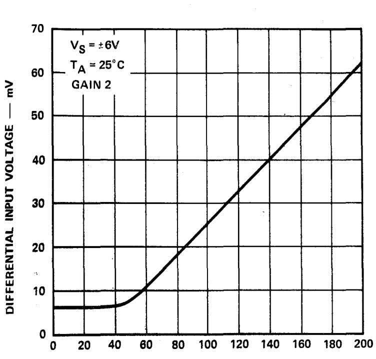
OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY



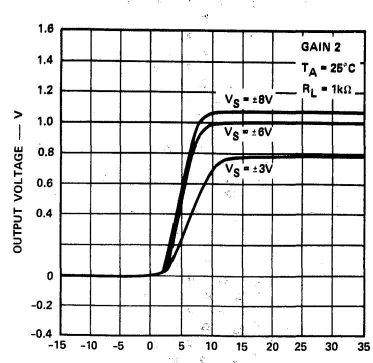
PULSE RESPONSE



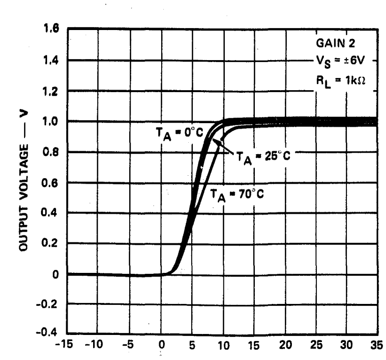
DIFFERENTIAL OVERDRIVE RECOVERY TIME



PULSE RESPONSE AS A FUNCTION OF SUPPLY VOLTAGE

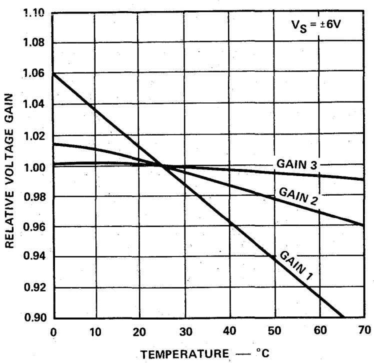


PULSE RESPONSE AS A FUNCTION OF TEMPERATURE

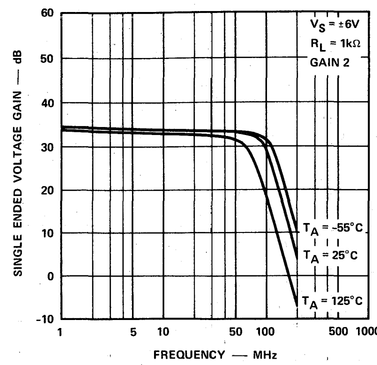


TYPICAL CHARACTERISTIC CURVES (CONT'D)

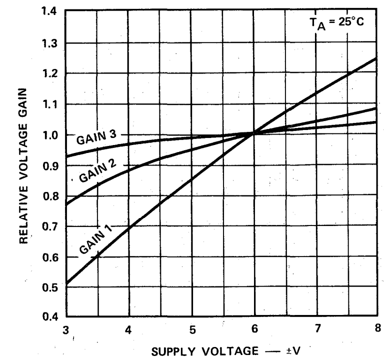
VOLTAGE GAIN AS A FUNCTION OF TEMPERATURE



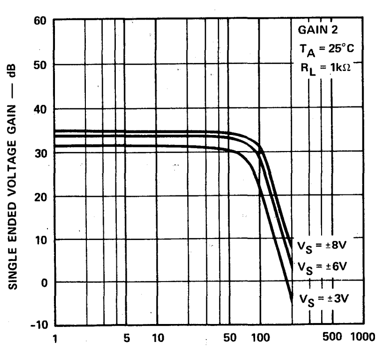
GAIN VS FREQUENCY AS A FUNCTION OF TEMPERATURE



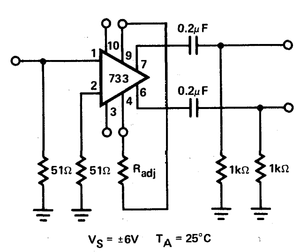
VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE



GAIN VS FREQUENCY AS A FUNCTION OF SUPPLY VOLTAGE



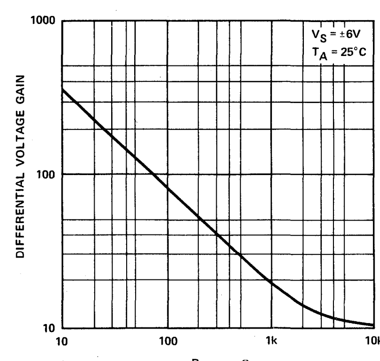
VOLTAGE GAIN ADJUST CIRCUIT



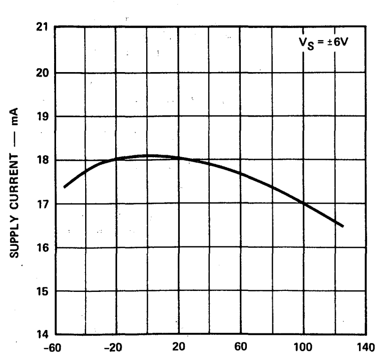
(Pin numbers apply to K Package)

FIGURE 3

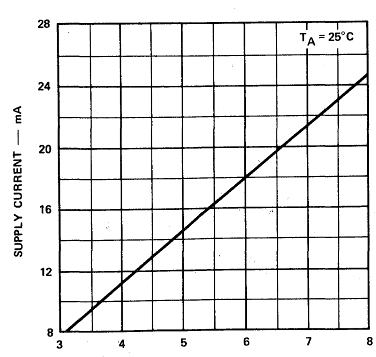
VOLTAGE GAIN AS A FUNCTION OF RADJ (FIGURE 3)



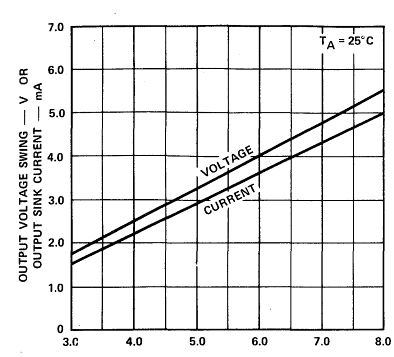
SUPPLY CURRENT AS A FUNCTION OF TEMPERATURE



SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



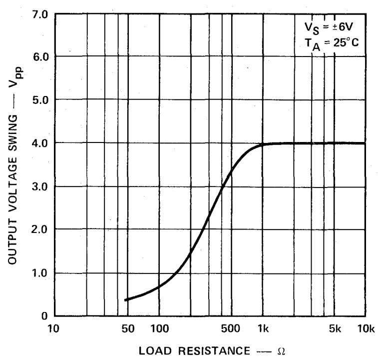
OUTPUT VOLTAGE AND CURRENT SWING AS A FUNCTION OF SUPPLY VOLTAGE



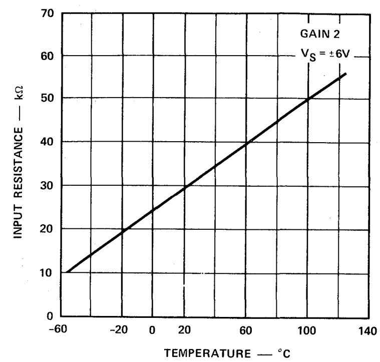
ANALOG

TYPICAL CHARACTERISTIC CURVES (CONT'D)

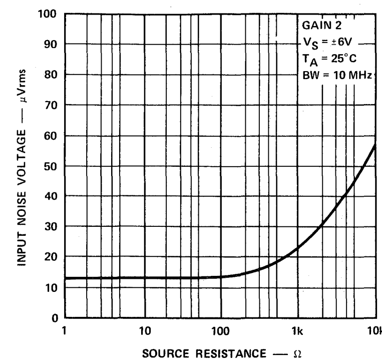
OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE



INPUT RESISTANCE AS A FUNCTION OF TEMPERATURE



INPUT NOISE VOLTAGE AS A FUNCTION OF SOURCE RESISTANCE



FEATURES

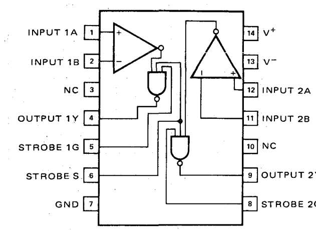
- 12 ns MAXIMUM GUARANTEED PROPAGATION DELAY
- 20 μA MAXIMUM INPUT BIAS CURRENT
- TTL COMPATIBLE STROBES AND OUTPUTS
- LARGE COMMON MODE INPUT VOLTAGE RANGE
- OPERATES FROM STANDARD SUPPLY VOLTAGES

APPLICATIONS

- MOS MEMORY SENSE AMP
- A/D CONVERSION
- HIGH SPEED LINE RECEIVER

PIN CONFIGURATION

A,F PACKAGE



ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $R_L = 280\Omega$, $C_L = 15pF$

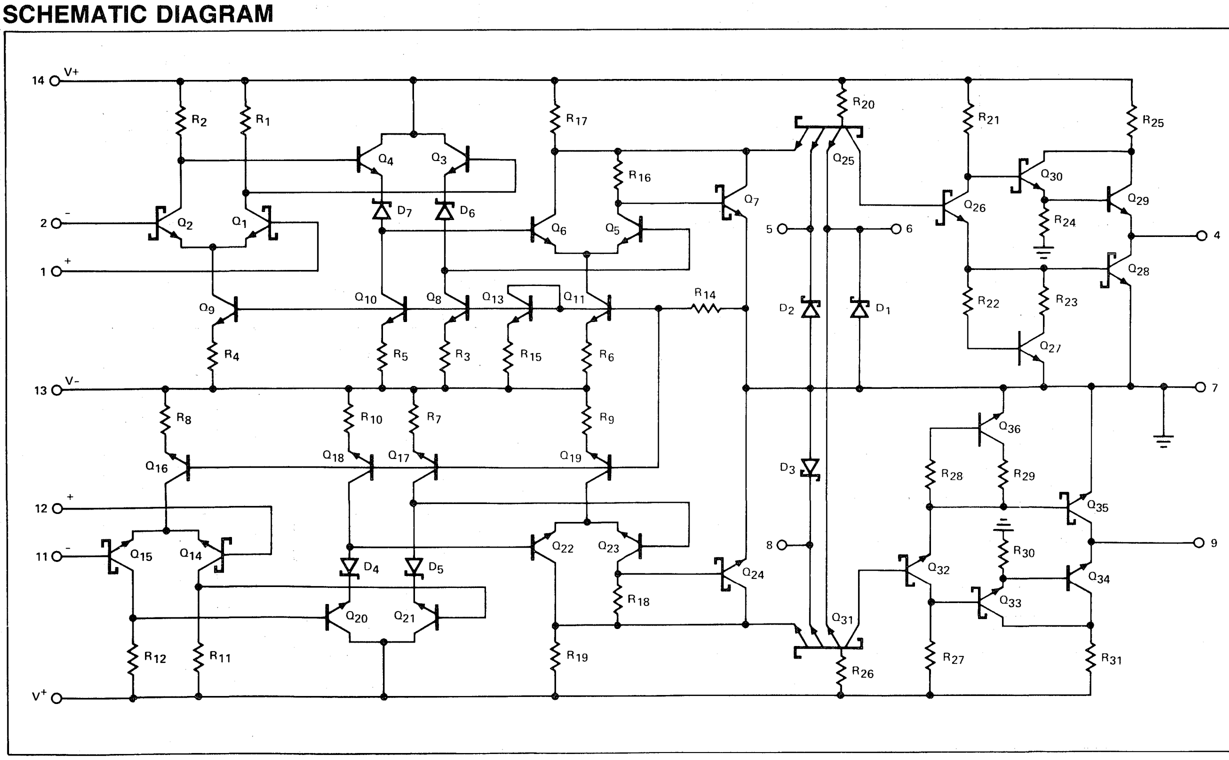
Parameter	From Input	To Output	Limits Min	Limits Typ	Limits Max	Unit
Input Resistance				4		KΩ
Input Capacitance				3	6	pF
Large Signal Switching Speed						
Propagation Delay						
t_{PLH} (D)[1]	Amp	Output		8	12	ns
t_{PHL} (D)[1]	Amp	Output		6	9	ns
t_{PLH} (S)[2]	Strobe	Output		4.5	6	ns
t_{PHL} (S)[2]	Strobe	Output		3.0	4.5	ns
Maximum Operating Frequency			40	55		MHz
Small Signal Switching Characteristics						
Propagation Delay						
t_{PLH} (D)[3]	Amp	Output		12	18	ns
t_{PHL} (D)[3]	Amp	Output		10	15	ns

NOTES:
1. Response time measured from 0 volt point of ±100 mV p-p 10MHz square wave to the 1.5V point of the output.
2. Response time measured from 1.5V point of input to 1.5V point of the output.
3. Response time measured from the start of a 100mv input step with 5 mv over drive to the 1.5v point of the output.

ABSOLUTE MAXIMUM RATINGS

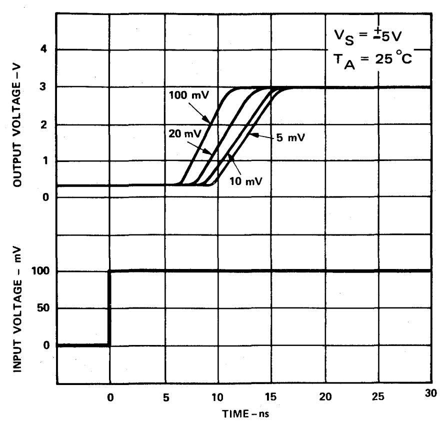
Positive Supply Voltage (V+)	+7 Volts
Negative Supply Voltage (V−)	−7 Volts
Differential input voltage	±6 Volts
Common mode input voltage	±5 Volts
Strobe/Gate input voltage	+5.25 Volts
Power Dissipation	600 mw
Operating Temperature Range	0°C to 70°C
Storage temperature range	−65°C to +150°C
Lead temperature (Soldering 60 seconds)	+300°C

SCHEMATIC DIAGRAM

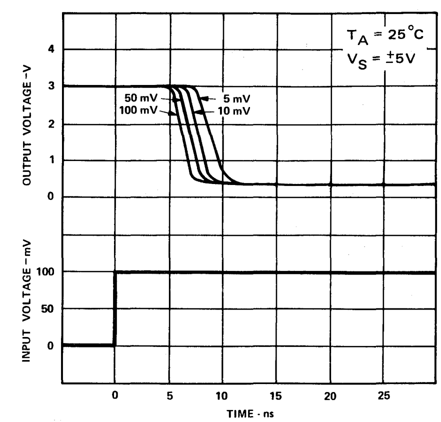


TYPICAL PERFORMANCE CHARACTERISTICS

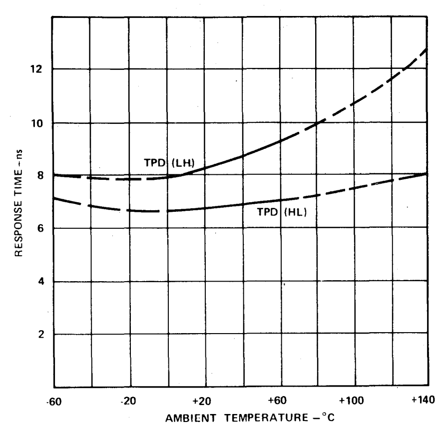
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



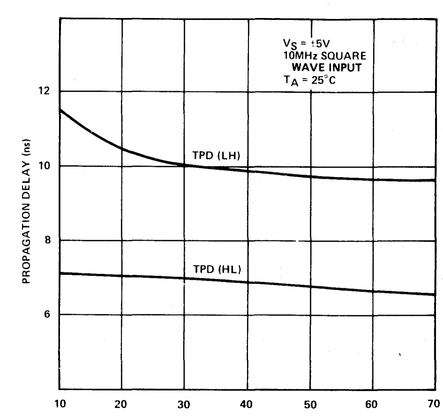
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



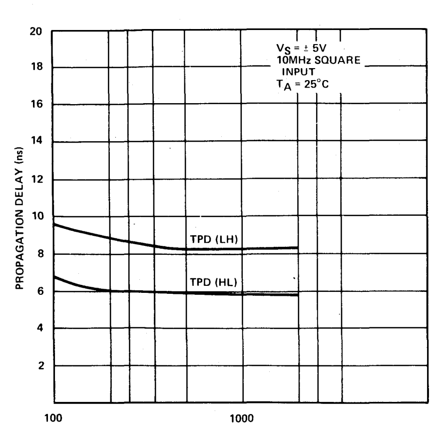
RESPONSE TIME VS TEMPERATURE



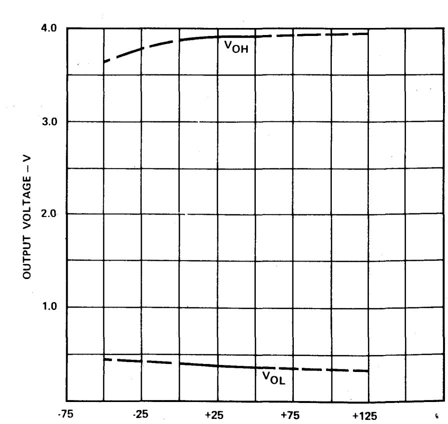
PROPAGATION DELAY FOR VARIOUS INPUT VOLTAGES



PROPAGATION DELAY FOR VARIOUS INPUT VOLTAGES

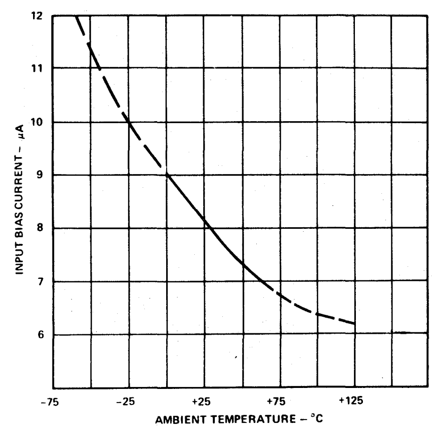


OUTPUT VOLTAGE VS. AMBIENT TEMPERATURE

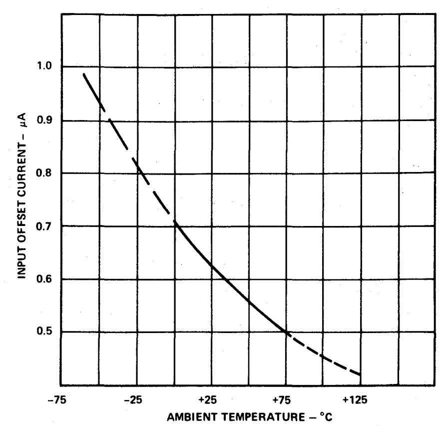


TYPICAL PERFORMANCE CHARACTERISTICS (CONT'D)

INPUT BIAS CURRENT VS. AMBIENT TEMPERATURE



INPUT OFFSET CURRENT VS. AMBIENT TEMPERATURE



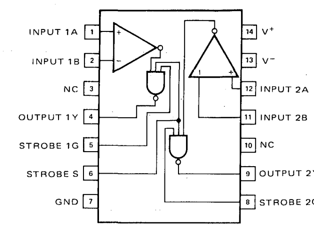
ANALOG

FEATURES
- 15 ns MAXIMUM GUARANTEED PROPAGATION DELAY
- 20 μA MAXIMUM INPUT BIAS CURRENT
- TTL COMPATIBLE STROBES AND OUTPUTS
- OPEN COLLECTOR OUTPUT FOR "WIRE-OR'D" APPLICATIONS
- LARGE COMMON MODE INPUT VOLTAGE RANGE
- OPERATES FROM STANDARD SUPPLY VOLTAGES

APPLICATIONS
- MOS MEMORY SENSE AMP
- A/D CONVERSION
- HIGH SPEED LINE RECEIVER

PIN CONFIGURATION

A, F PACKAGE



ELECTRICAL CHARACTERISTICS $T_A=25°C$, $R_L=280\Omega$, $C_L=15pF$

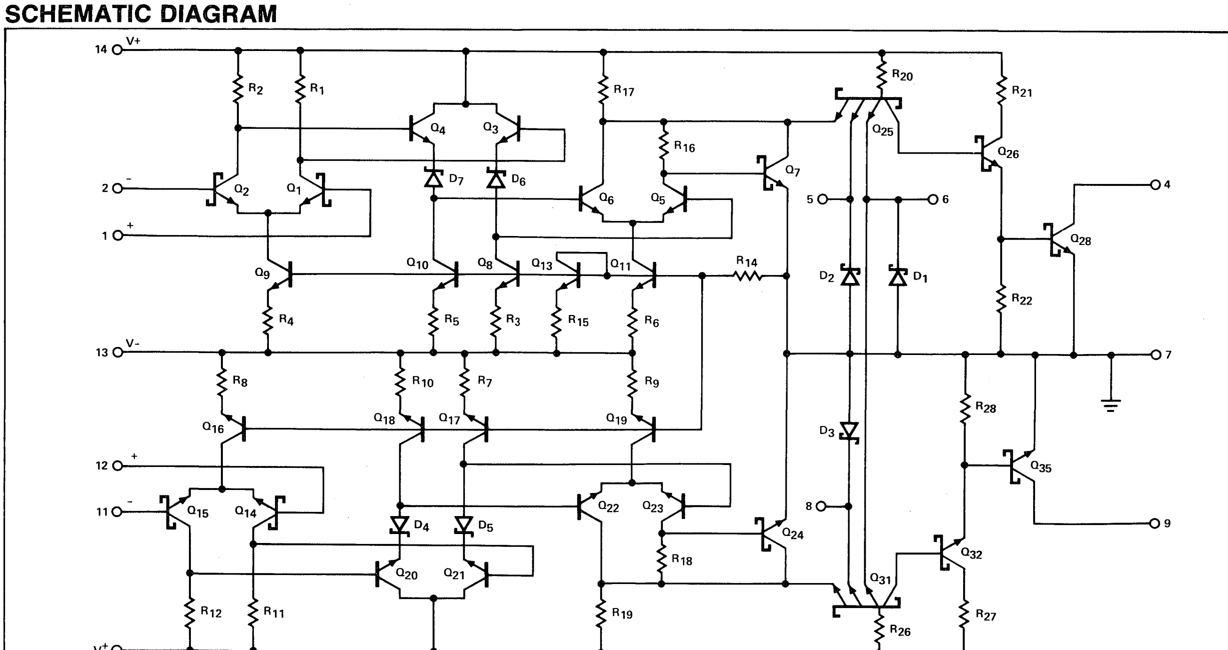
PARAMETER	FROM INPUT	TO OUTPUT	Limits MIN	TYP	MAX	UNITS
Input Resistance				4		KΩ
Input Capacitance				3	6	pF
Large Signal Switching Speed						
Propagation Delay						
tPLH (D)1	Amp	Output		10	15	ns
tPHL (D)1	Amp	Output		8	12	ns
tPHL (S)2	Strobe	Output		6	10	ns
tPHL (S)2	Strobe	Output		5	8	ns
Maximum Operating Frequency			25	35		MHz
Small Signal Switching Characteristics						
Propagation						
tPLH (D)3	Amp	Output		17	25	ns
tPHL (D)3	Amp	Output		11	17	ns

NOTES:
1. Response time measured from 0V of ±100 mV p-p 10MHz square wave to the 1.5V point of the output.
2. Response time measured from 1.5V point of input to 1.5V point of the output.
3. Response time measured from the start of a 100mv input step with 5mv over drive to the 1.5v point of the output.

ABSOLUTE MAXIMUM RATINGS

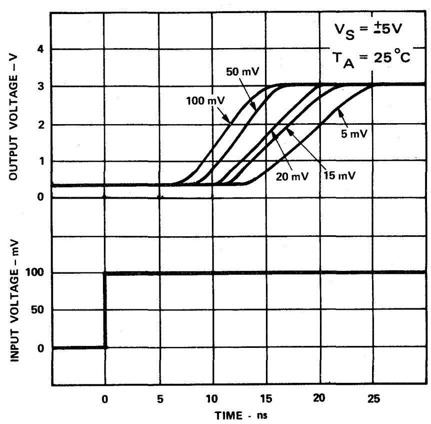
Positive Supply Voltage (V+)	+7 Volts
Negative Supply Voltage (V−)	−7 Volts
Differential input voltage	±6 Volts
Common mode input voltage	±5 Volts
Strobe/Gate input voltage	+5.25 Volts
Power Dissipation	600 mw
Operating Temperature Range	0°C to 70°C
Storage temperature range	−65°C to +150°C
Lead temperature (Soldering 60 seconds)	+300°C

SCHEMATIC DIAGRAM

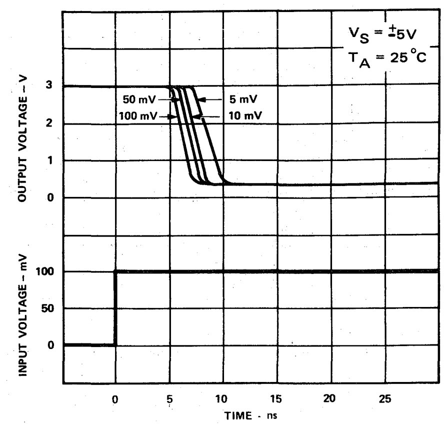


TYPICAL PERFORMANCE CHARACTERISTICS

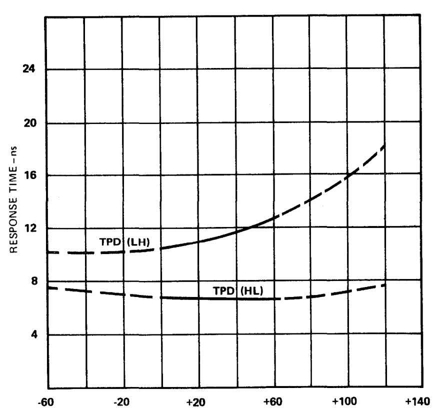
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



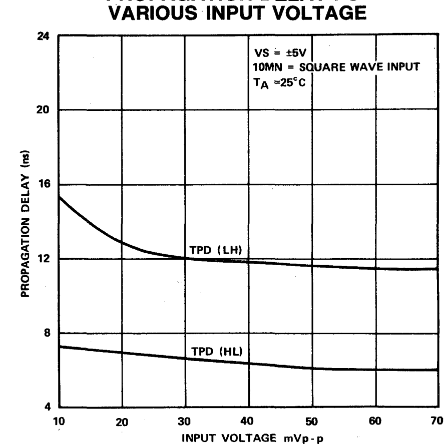
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



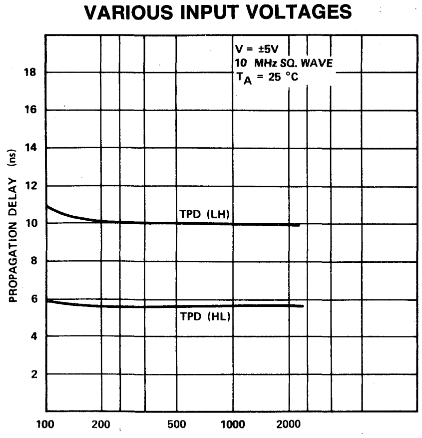
RESPONSE TIME VS TEMPERATURE



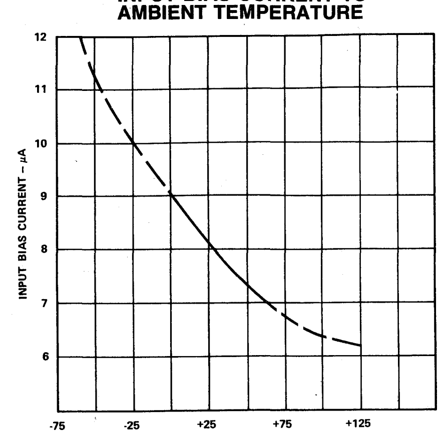
PROPAGATION DELAY FOR VARIOUS INPUT VOLTAGE



PROPAGATION DELAY FOR VARIOUS INPUT VOLTAGES

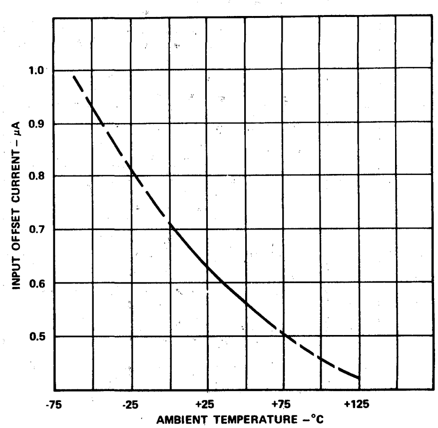


INPUT BIAS CURRENT VS AMBIENT TEMPERATURE



TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

INPUT OFFSET CURRENT VS AMBIENT TEMPERATURE



SE526-A, K·NE526-A, K

FEATURES

- **PROPAGATION DELAY** **30ns**
- **INPUT COMMON MODE RANGE** **+4.5V −3.5V**
- **DIFFERENTIAL OVERDRIVE RECOVERY** **20ns**
- **OUTPUT COMPATIBLE WITH STANDARD LOGIC FORMS**
- **OPERATES FROM STANDARD ±5V SUPPLIES**

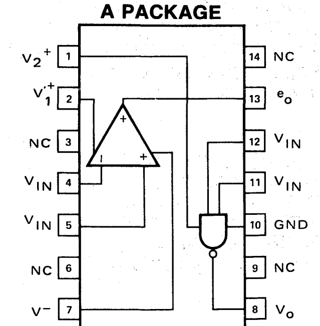
ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+7.0V
Gate Input Voltage	+6.0V
Differential Input Voltage	+5.0V
Common Mode Input Voltage	+5.0V
Gate Output Current	+100 mA
Storage Temperature	−65°C to +150°C
Operating Temperature	
SE526	−55°C to +125°C
NE526	0°C to +75°C

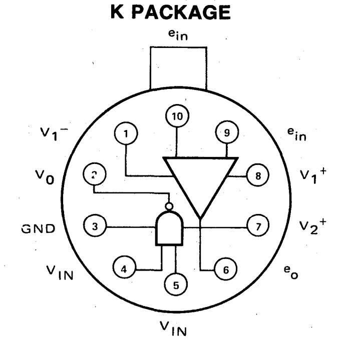
Absolute Maximum Ratings are limiting values above which serviceablity may be impaired.

CONFIGURATION

A PACKAGE



K PACKAGE

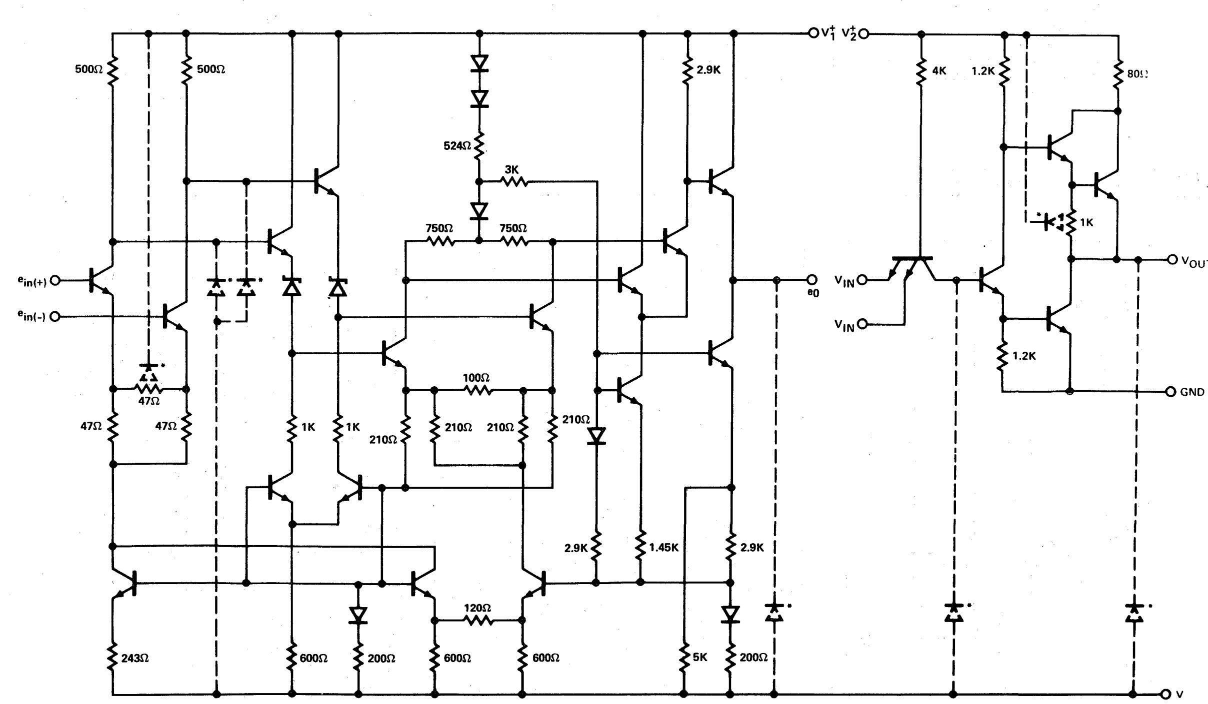


ELECTRICAL CHARACTERISTICS $T_A = 25°C$

PARAMETER	LIMITS			UNIT
	MIN	TYP	MAX	
BV_i Gate Input Latch Voltage Rating			6	V
Switching Times[1]				
T_{on} Gate Turn-on Delay		15	17	ns
T_{off} Gate Turn-off Delay		15	17	ns
Propagation Delay				
t_{PLH}		40	48	ns
t_{PHL}		30	42	ns
tdm Differential Overload Recovery[2]		30	40	ns

NOTES:
1. Load capacitance includes test fixture and probe capacitance.
2. Differential input voltage = 500mV for this test.

EQUIVALENT CIRCUIT



NOTES:
COMPONENT VALUES ARE TYPICAL
*ISOLATION DIODES

SE527-A,K · NE527-A,K

FEATURES

- 15 nsec PROPAGATION DELAY
- COMPLEMENTARY OUTPUT GATES
- TTL OR ECL COMPATIBLE OUTPUTS
- WIDE COMMON MODE AND DIFFERENTIAL VOLTAGE RANGE

APPLICATIONS

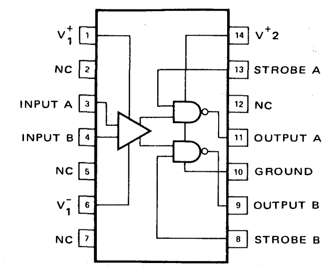
A/D CONVERSION
ECL TO TTL INTERFACE
TTL TO ECL INTERFACE
MEMORY SENSING
OPTICAL DATA COUPLING

ABSOLUTE MAXIMUM RATINGS

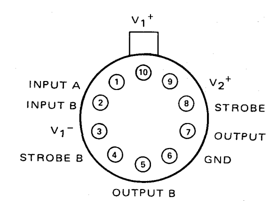
Positive Supply Voltage (V1+)	+15 volts
Negative Supply Voltage (V1−)	−15 volts
Gate Supply Voltage (V2+)	+7 volts
Output Voltage	+15 volts
Differential Input Voltage	±5 volts
Input Common Mode Voltage	±6 volts
Power Dissipation	600mW
Operating Temperature Range	
NE527	0°C to +70°C
SE527	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 seconds)	+300°C

PIN CONFIGURATION

A PACKAGE



K PACKAGE

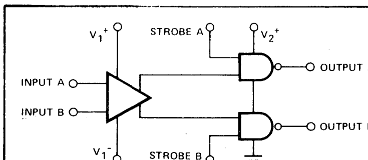


ELECTRICAL CHARACTERISTICS (T_A + 25°C)

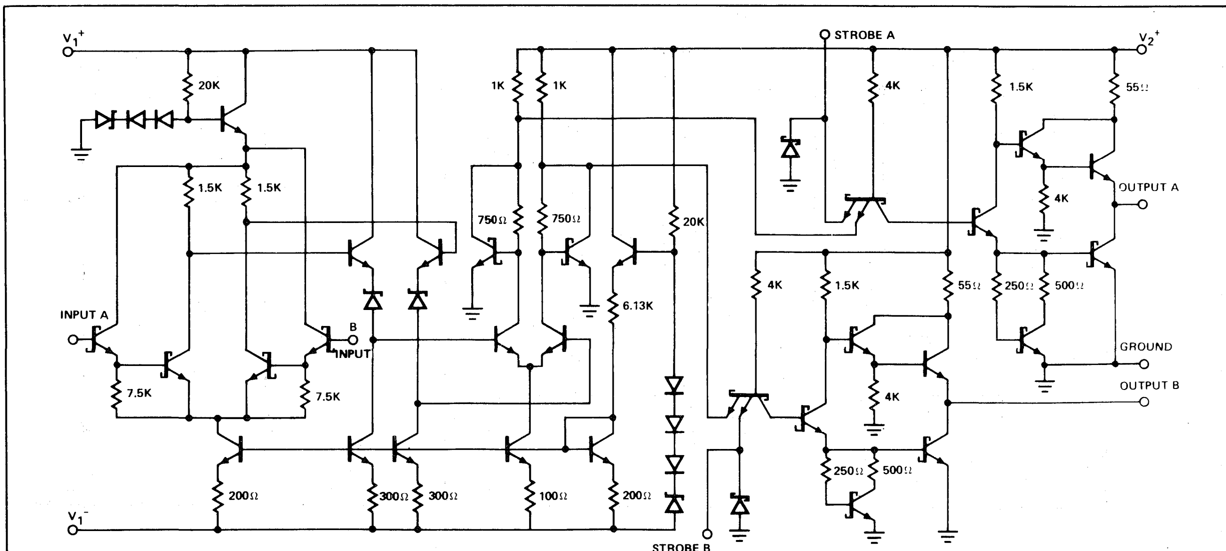
PARAMETER	TEST CONDITIONS	LIMITS MIN	TYP	MAX	UNIT
Input Impedance	f = 1kHz		500		KΩ
Transient Response	V_{in}=50mV overdrive				
Propagation Delay Time					
t_{PLH}			16	26	ns
t_{PHL}			14	24	ns
Delay between Output A and B			2	5	ns
Strobe Delay Time					
t_{on} Turn-on time			6		ns
t_{off} Turn-off time			6		ns

Parameters are guaranteed over the temperature range unless otherwise noted.

BLOCK DIAGRAM



EQUIVALENT CIRCUIT



SE527-A, K · NE527-A, K

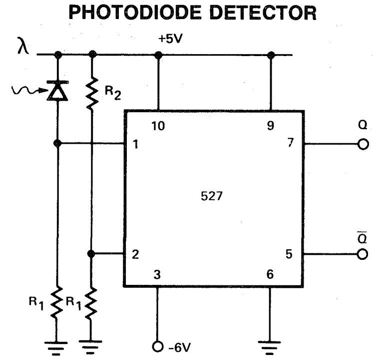
APPLICATIONS

One of the main features of the device is that supply voltages (V1 + , V1 −) need not be balanced, as indicated in the following diagrams. For proper operation, however, negative supply (V1−) should always be at least six volts more negative than the ground terminal (pin 6). Input Common Mode range should be limited to values of two volts less than the supply voltages (V1+ and V1−) up to a maximum of ±6 volts as supply voltages are increased.

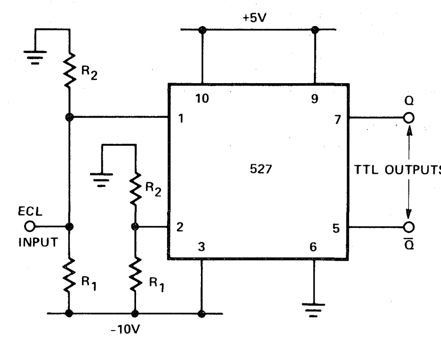
It is also important to note that Output A is in phase with Input A and Output B is in phase with Input B.

TYPICAL APPLICATIONS

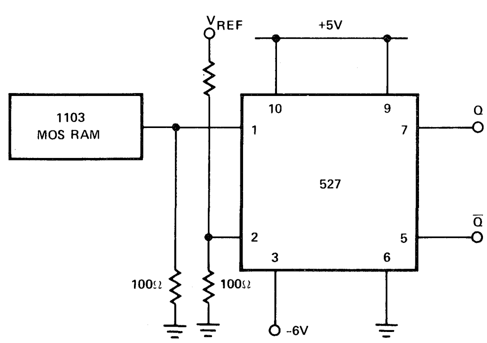
PHOTODIODE DETECTOR



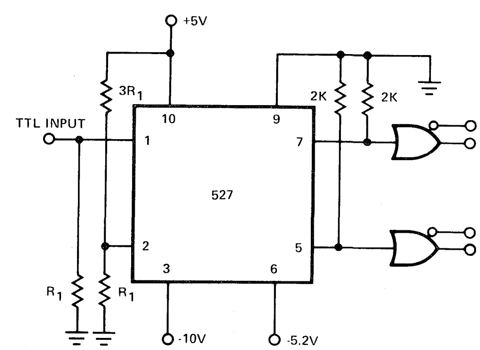
ECL TO TTL INTERFACE



MOS MEMORY SENSE AMP

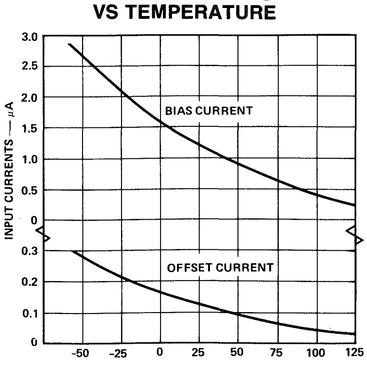


TTL TO ECL INTERFACE

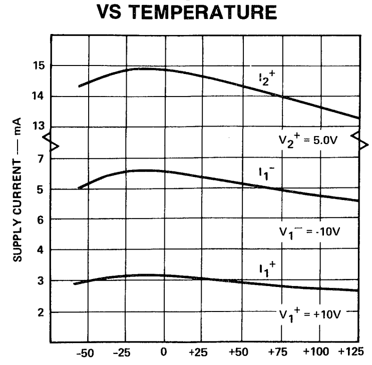


TYPICAL PERFORMANCE CURVES

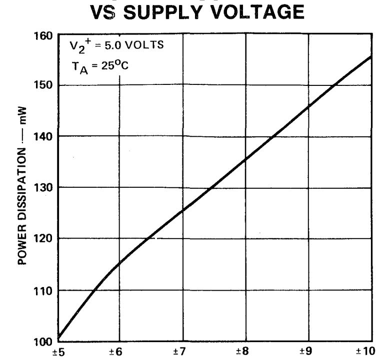
INPUT CURRENTS VS TEMPERATURE



SUPPLY CURRENT VS TEMPERATURE



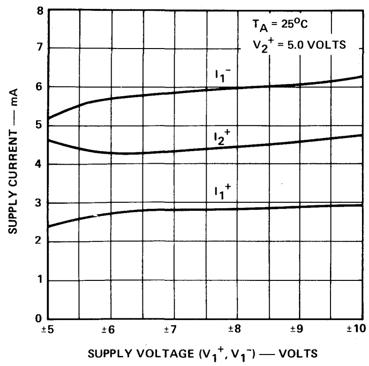
POWER DISSIPATION VS SUPPLY VOLTAGE



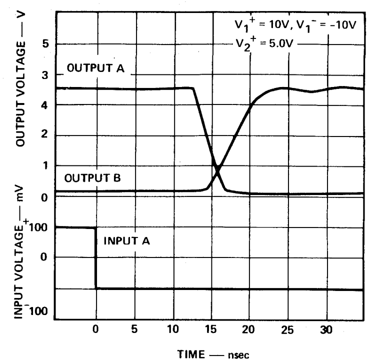
ANALOG

TYPICAL PERFORMANCE CURVES (Cont'd)

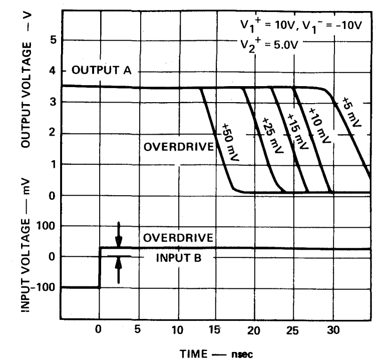
SUPPLY CURRENT VS SUPPLY VOLTAGE



OUTPUT PROPAGATION DELAYS



RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



SE529-A,K · NE529-A,K

FEATURES
- 10 nsec PROPAGATION DELAY
- COMPLEMENTARY OUTPUT GATES
- TTL OR ECL COMPATIBLE OUTPUTS
- WIDE COMMON MODE AND DIFFERENTIAL VOLTAGE RANGE

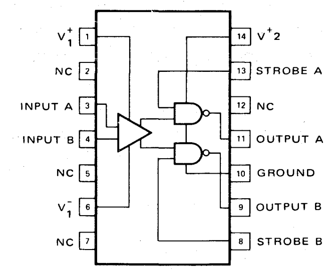
APPLICATIONS
A/D CONVERSION
ECL TO TTL INTERFACE
TTL TO ECL INTERFACE
MEMORY SENSING
OPTICAL DATA COUPLING

ABSOLUTE MAXIMUM RATINGS

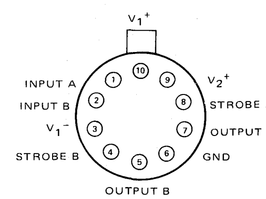
Positive Supply Voltage (V1+)	+15 volts
Negative Supply Voltage (V1−)	−15 volts
Gate Supply Voltage (V2+)	+7 volts
Output Voltage	+15 volts
Differential Input Voltage	±5 volts
Input Common Mode Voltage	±6 volts
Power Dissipation	600mW
Operating Temperature Range	
NE 529	0°C to +70°C
SE 529	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering 60 seconds)	+300°C

PIN CONFIGURATION

A PACKAGE



K PACKAGE

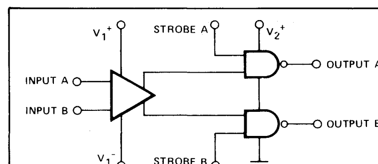


ELECTRICAL CHARACTERISTICS $T_A = 25°C$

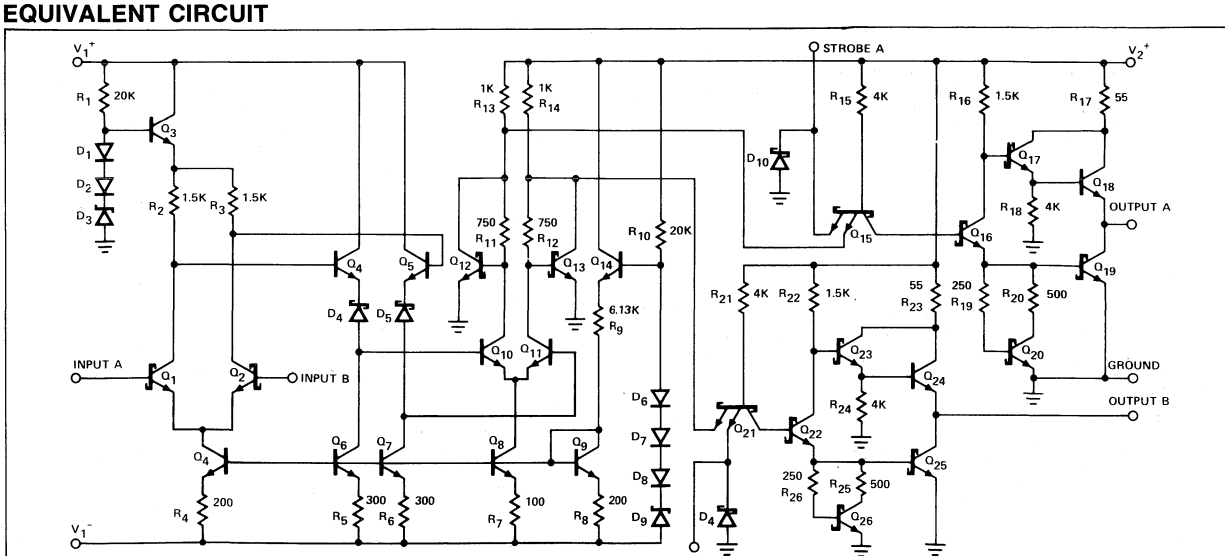
PARAMETER	TEST CONDITIONS	LIMITS MIN	TYP	MAX	UNIT
Input Impedance	F = 1kHz		10		KΩ
Transient Response	V_{in} = 50mV overdrive				
Propagation Delay Time					
t_{PLH}			12	22	ns
t_{PHL}			10	20	ns
Delay between Output A and B			2	5	ns
Strobe Delay Time					
t_{on} Turn-on Time			6		ns
t_{off} Turn-off Time			6		ns

Parameters are guaranteed over the temperature range unless otherwise noted.

BLOCK DIAGRAM



EQUIVALENT CIRCUIT



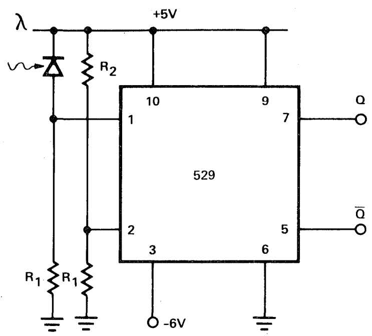
APPLICATIONS

One of the main features of the device is that supply voltages (V1+, V1−) need not be balanced, as indicated in the following diagrams. For proper operation, however, negative supply (V1−) should always be at least five volts more negative than the ground terminal (pin 6). Input Common Mode range should be limited to values of two volts less than the supply voltages (V1+ and V1−) up to a maximum of ±6 volts as supply voltages are increased.

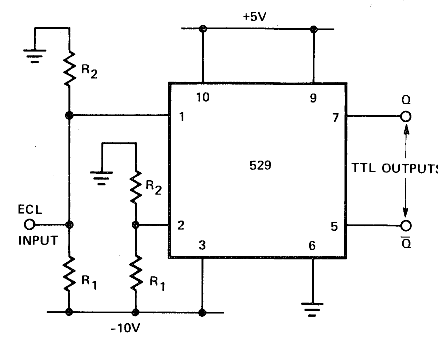
It is also important to note that Output A is in phase with Input A and Output B is in phase with Input B.

TYPICAL APPLICATIONS

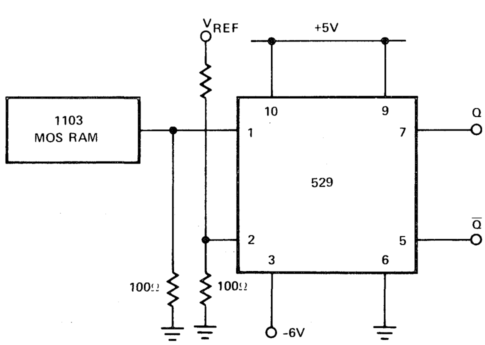
PHOTODIODE DETECTOR



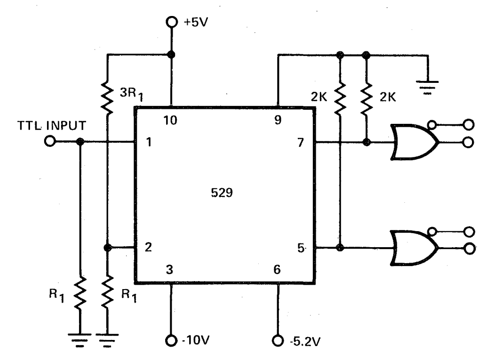
ECL TO TTL INTERFACE



MOS MEMORY SENSE AMP

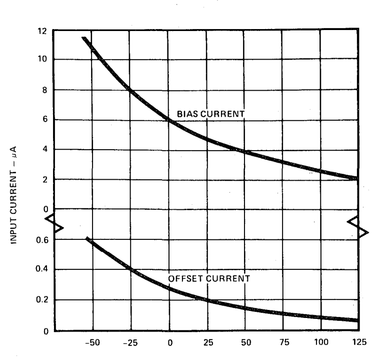


TTL TO ECL INTERFACE

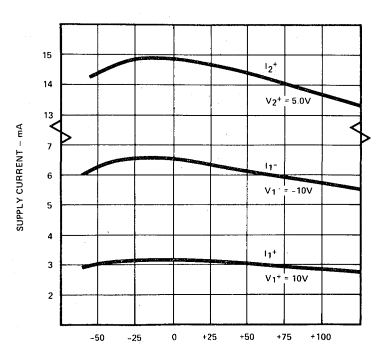


TYPICAL PERFORMANCE CURVES

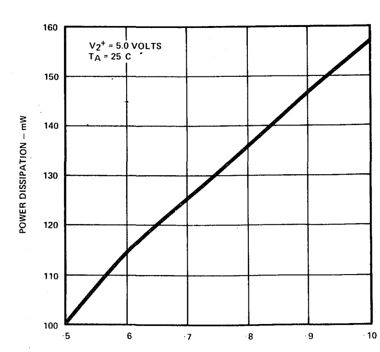
INPUT CURRENTS VS TEMPERATURE



SUPPLY CURRENT VS TEMPERATURE



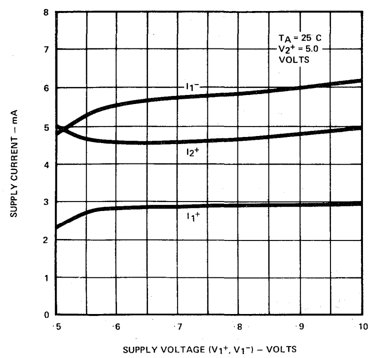
POWER DISSIPATION VS SUPPLY VOLTAGE



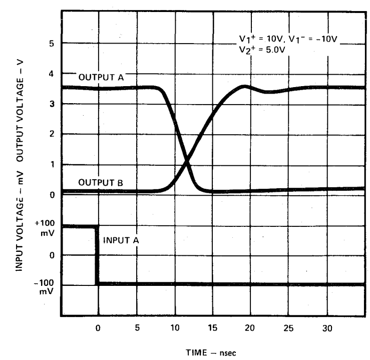
SE529-A, K · NE529-A, K

TYPICAL PERFORMANCE CURVES (CONT'D)

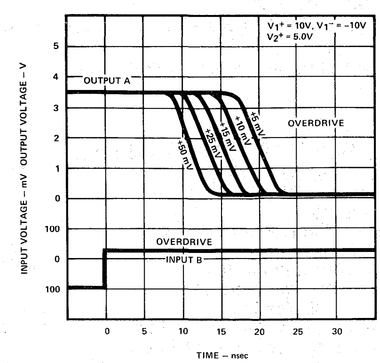
SUPPLY CURRENT VS SUPPLY VOLTAGE



OUTPUT PROPAGATION DELAYS



RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



ANALOG

LM111-F,T · LM211-F,T

FEATURES

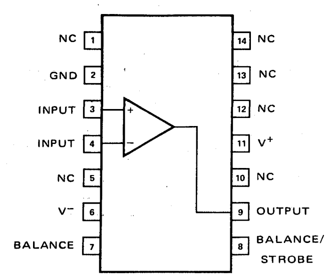
- OPERATES FROM SINGLE 5V SUPPLY
- MAXIMUM INPUT CURRENT: 150nA
- MAXIMUM OFFSET CURRENT: 20nA
- DIFFERENTIAL INPUT VOLTAGE RANGE: ±30V
- POWER CONSUMPTION: 135mW AT ±15V
- HIGH SENSITIVITY — 200V/mV

ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage	36V
Output to Negative Supply Voltage	50V
Ground to Negative Supply Voltage	30V
Differential Input Voltage	±30V
Input Voltage (Note 1)	±15V
Power Dissipation	500mW
Output Short Circuit Duration	10 sec
Operating Temperature Range	
LM111	−55°C to 125°C
LM211	−25°C to 85°C
Storage Temperature Range	−65° to 150°C
Lead Temperature (Soldering, 10 sec)	300°C

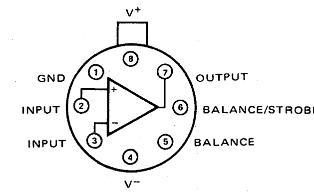
PIN CONFIGURATION

F PACKAGE



ORDER NOS. LM11H or LM211H

T PACKAGE



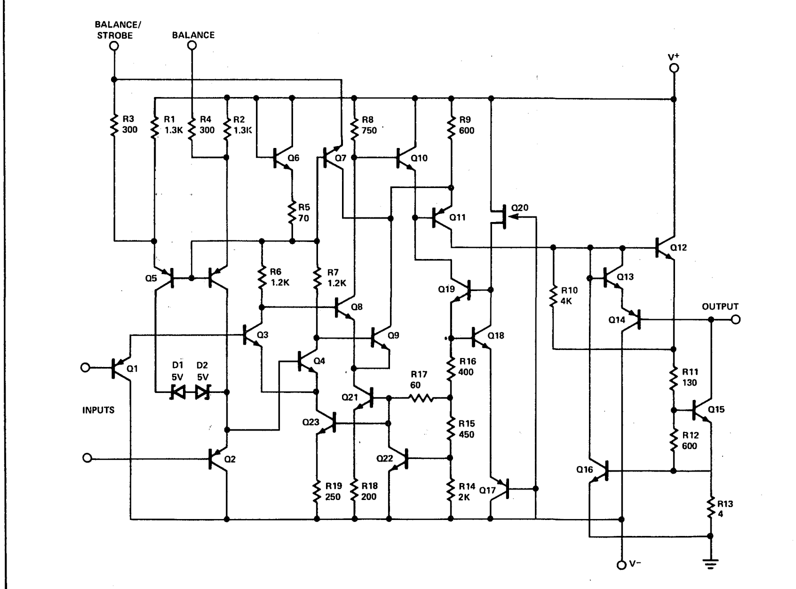
ORDER NOS. LM111D or LM211D

ELECTRICAL CHARACTERISTICS (TA = 25°C)

	LIMITS	
PARAMETER	MIN TYP MAX	UNIT
Response Time	200	ns

The response time specified is for a 100mV input step with 5mV overdrive.

CIRCUIT SCHEMATIC



FEATURES

- WIDE OPERATING SUPPLY RANGE — ±15V TO A SINGLE +5V
- LOW INPUT CURRENTS — 6nA
- HIGH SENSITIVITY — 10μV
- WIDE DIFFERENTIAL INPUT RANGE — ±30V
- HIGH OUTPUT DRIVE — 50mA, 50V

ELECTRICAL CHARACTERISTICS (tA = 25°C)

PARAMETER	LIMITS			UNIT
	MIN	TYP	MAX	
Response Time		200		ns

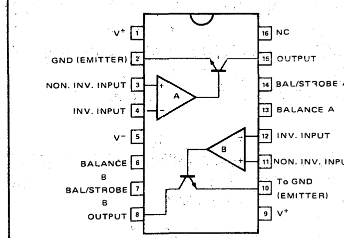
The response time specified is for a 100mV input step with 5mV overdrive

ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage (V+−V⁻)	36V
Output to Negative Supply Voltage (VOUT—V⁻)	
Ground to Negative Supply	50V
Voltage (GND—V⁻)	30V
Differential Input Voltage	±30V
Input Voltage (Note 1)	±15V
Power Dissipation (Note 2)	500mW
Output Short Circuit Duration	10 sec
Operating Temperature Range	
LH2111	−55°C to 125°C
LH2211	−25°C to 85°C
LH2311	0°C to 70°C
Storage Temperature Range	−65°C to 150°C
Lead Temperature (Soldering, 10 sec)	300°C

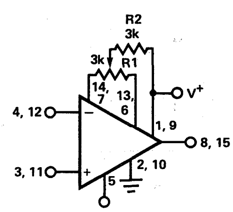
PIN CONFIGURATION

F PACKAGE

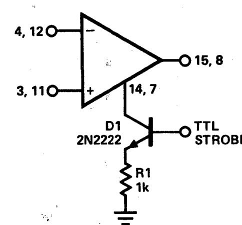


AUXILIARY CIRCUITS

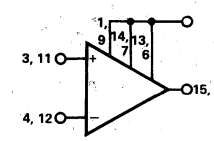
OFFSET BALANCING



STROBING

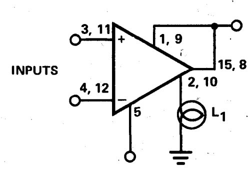


INCREASING INPUT STAGE CURRENTS

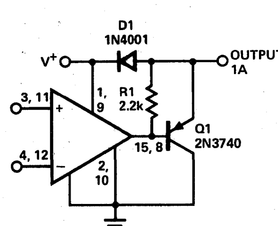


Increases Typical Common mode slew from 7.0V/ S to 18/ S

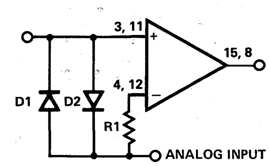
DRIVING GROUND-REFERRED LOAD



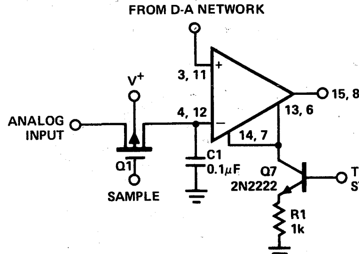
COMPARATOR AND SOLENOID DRIVER



USING CLAMP DIODES TO IMPROVE RESPONSES

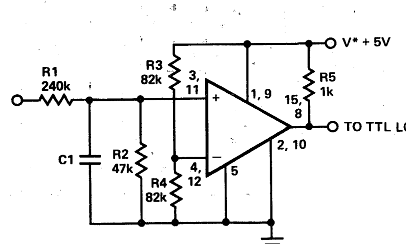


STROBING OFF BOTH INPUT AND OUTPUT STAGES



*TYPICAL INPUT CURRENT IS 50μA WITH INPUTS STROBED OFF.

TTL INTERFACE WITH HIGH LEVEL LOGIC



ANALOG

FEATURES
- OPERATES FROM SINGLE 5V SUPPLY
- MAXIMUM INPUT CURRENT: 250 nA
- MAXIMUM OFFSET CURRENT: 50 nA
- DIFFERENTIAL INPUT VOLTAGE RANGE: ±30V
- POWER CONSUMPTION: 135 mW AT ±15V
- HIGH SENSITIVITY — 200 V/mV

ABSOLUTE MAXIMUM RATINGS

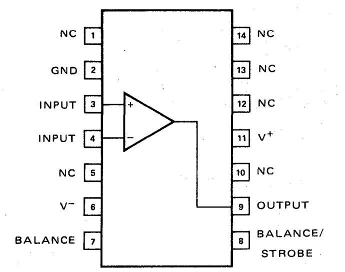
Total Supply Voltage	36V
Output to Negative Supply Voltage	40V
Ground to Negative Supply Voltage	30V
Differential Input Voltage	±30V
Input Voltage (Note 1)	±15V
Power Dissipation	500 mW
Output Short Circuit Duration	10 sec
Operating Temperature Range	0°C to 70°C
Storage Temperature Range	−65°C to 150°C
Lead Temperature (Soldering, 10 sec)	300°C

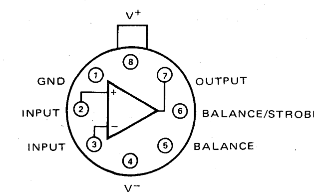
ELECTRICAL CHARACTERISTICS
$T_A = 25°C$

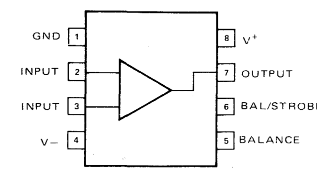
PARAMETER	LIMITS			UNIT
	MIN	TYP	MAX	
Response Time		200		ns

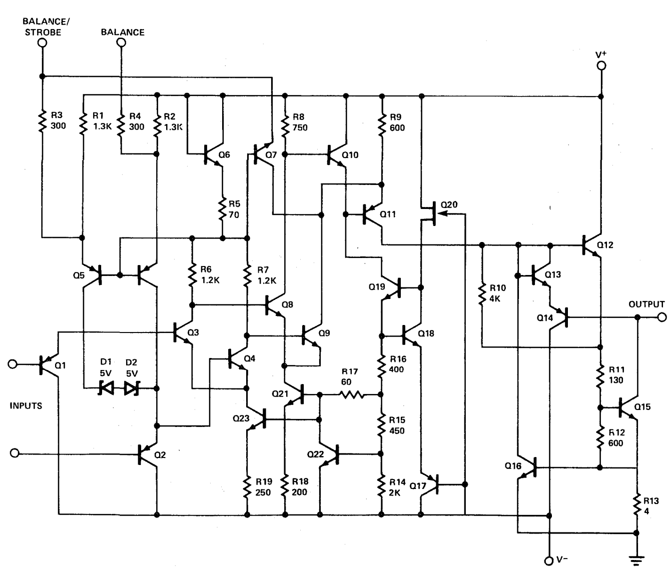
The response time specified is for a 100mV input step with 5mV overdrive.

PIN CONFIGURATION

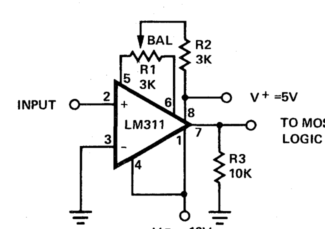
A F PACKAGE


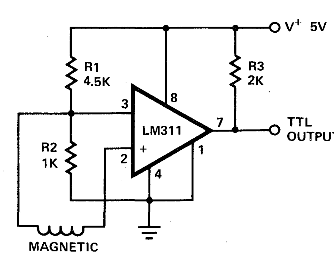
T PACKAGE


V PACKAGE


CIRCUIT SCHEMATIC


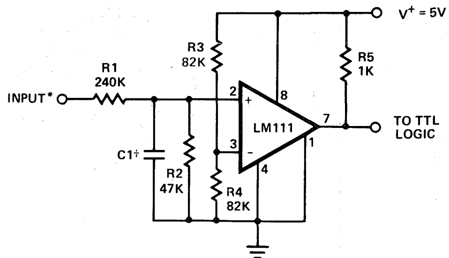
TYPICAL APPLICATIONS

ZERO CROSSING DETECTOR DRIVING MOS LOGIC


DETECTOR FOR MAGNETIC TRANSDUCER


TYPICAL APPLICATIONS (CONT'D)

TTL INTERFACE WITH HIGH LEVEL LOGIC



*Values shown are for a 0 to 30V logic swing and a 15V threshold.
†May be added to control speed and reduce susceptability to noise spikes.

FEATURES

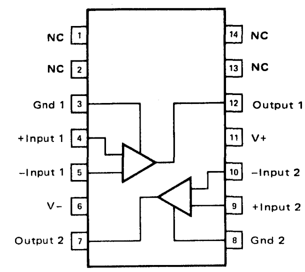
- TWO INDEPENDENT COMPARATORS
- OPERATES FROM A SINGLE 5V SUPPLY
- TYPICALLY 80ns RESPONSE TIME AT ±15V
- MINIMUM FAN-OUT OF 3 (EACH SIDE)
- MAXIMUM INPUT CURRENT OF 1μA OVER TEMPERATURE
- INPUTS AND OUTPUTS CAN BE ISOLATED FROM SYSTEM GROUND
- HIGH COMMON MODE SLEW RATE

ABSOLUTE MAXIMUM RATINGS

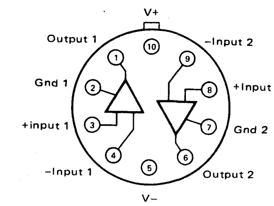
Total Supply Voltage	36V
Output to Negative Supply Voltage	36V
Ground to Negative Supply Voltage	25V
Ground to Positive Supply Voltage	18V
Differential Input Voltage	±5V
Input Voltage	±15V
Power Dissipation	500mW
Output Short Circuit Duration	10 sec
Operating Temperature Range	
LM119	−55°C to 125°C
LM219	−25°C to 85°C
Storage Temperature Range	−65°C to 150°C
Lead Temperature (Soldering, 10 sec)	300°C

PIN CONFIGURATION

F PACKAGE



K PACKAGE



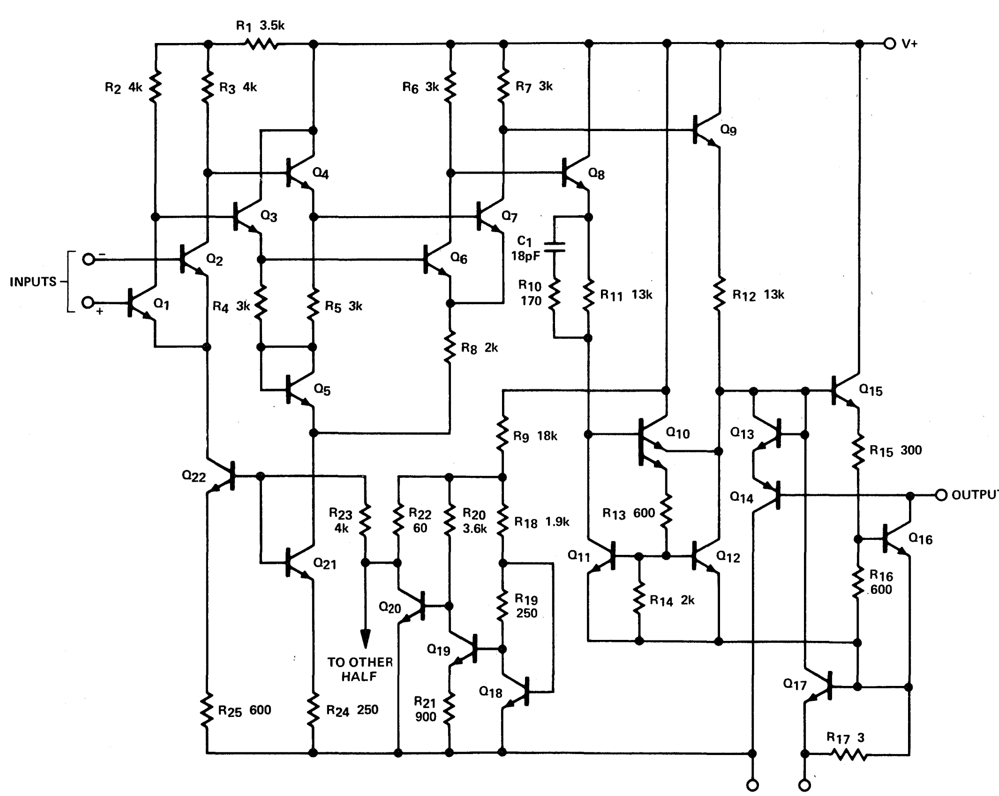
ELECTRICAL CHARACTERISTICS

$T_A = 25°C, V_S = \pm 15V$

PARAMETER	LIMITS			UNIT
	MIN	TYP	MAX	
Response Time		80		ns

The response time specified is for a 100mV input step with 5mV overdrive.

CIRCUIT SCHEMATIC



FEATURES

- TWO INDEPENDENT COMPARATORS
- OPERATES FROM A SINGLE 5V SUPPLY
- TYPICALLY 80ns RESPONSE TIME AT ±15V
- MINIMUM FAN-OUT OF 2 (EACH SIDE)
- MAXIMUM INPUT CURRENT OF 1μA
- INPUTS AND OUTPUTS CAN BE ISOLATED FROM SYSTEM GROUND
- HIGH COMMON MODE SLEW RATE

ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage	36V
Output to Negative Supply Voltage	36V
Ground to Negative Supply Voltage	25V
Ground to Positive Supply Voltage	18V
Differential Input Voltage	±5V
Input Voltage (Note 1)	±15V
Power Dissipation	500mW
Output Short Circuit Duration	10 sec
Operating Temperature Range LM319	0°C to 70°C
Storage Temperature Range	−65°C to 150°C
Lead Temperature (Soldering, 10 sec)	300°C

NOTE:
1. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

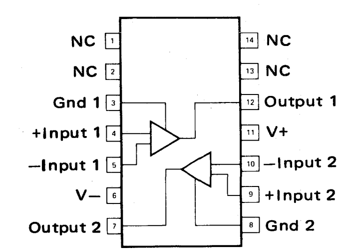
ELECTRICAL CHARACTERISTICS
$T_A = 25°C$, $V_S = \pm15V$

PARAMETER	LIMITS			UNIT
	MIN	TYP	MAX	
Response Time		80		ns

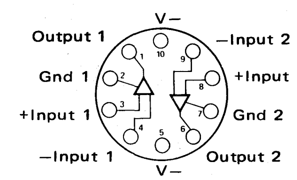
The response time specified is for a 100mV input step with 5mV overdrive.

PIN CONFIGURATION

A,F PACKAGE

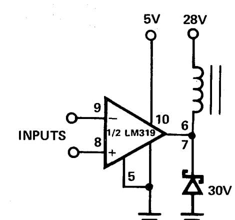


K PACKAGE

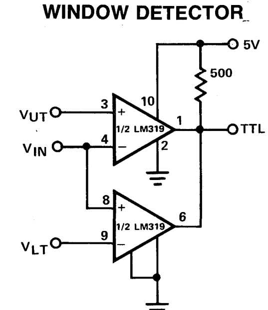


TYPICAL APPLICATIONS

RELAY DRIVER

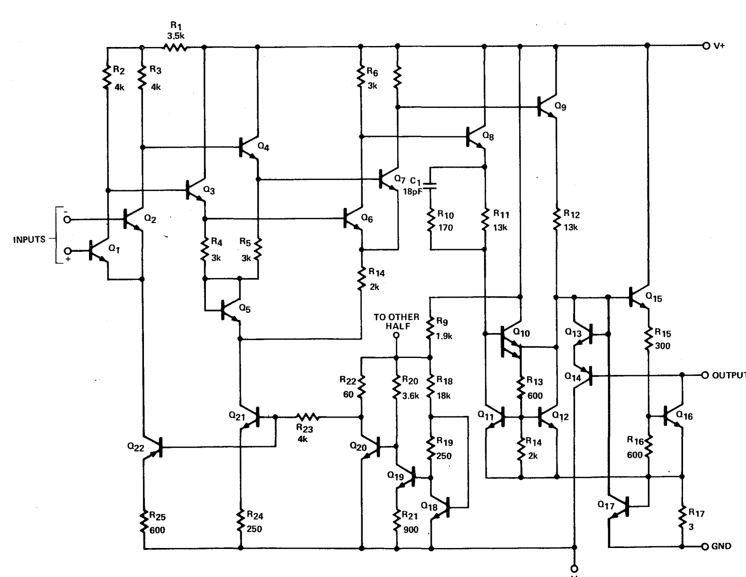


WINDOW DETECTOR



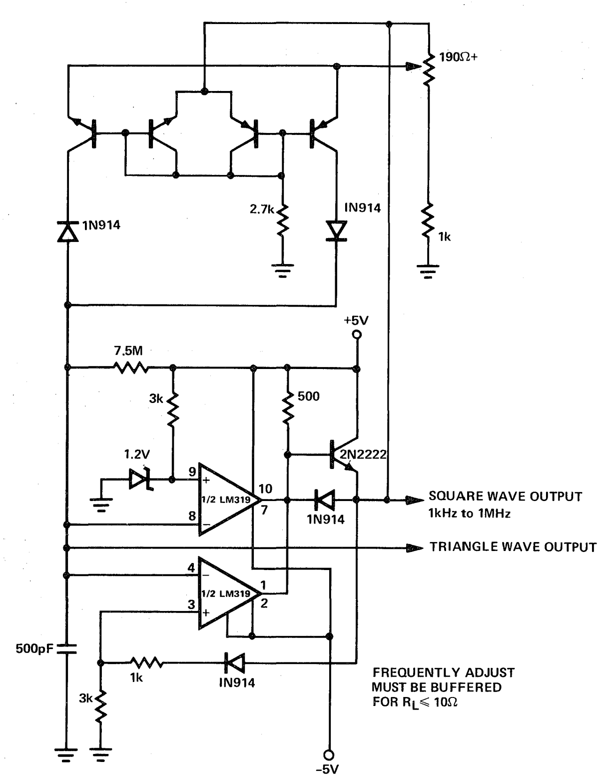
VOUT = 5V FOR VLT<VIN<VUT
VOUT = 0 FOR VIN<VLT OR VIN >VUT

CIRCUIT SCHEMATIC



TYPICAL APPLICATIONS (Cont'd)

WIDE RANGE VARIABLE OSCILLATOR



FEATURES

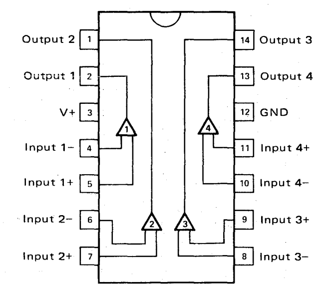
- WIDE SINGLE SUPPLY VOLTAGE RANGE 2 V_{DC} TO 36 V_{DC} OR DUAL SUPPLIES ±1 V_{DC} TO ±18 V_{DC}
- VERY LOW SUPPLY CURRENT DRAIN (0.8mA) INDEPENDENT OF SUPPLY VOLTAGE (1mW/COMPARATOR AT +5 V_{DC})
- LOW INPUT BIASING CURRENT — 35nA
- LOW INPUT OFFSET CURRENT — 3nA
  OFFSET VOLTAGE — 3mV
- INPUT COMMON-MODE VOLTAGE RANGE INCLUDES GROUND
- DIFFERENTIAL INPUT VOLTAGE RANGE EQUAL TO THE POWER SUPPLY VOLTAGE
- LOW OUTPUT SATURATION VOLTAGE 1mV AT 5μA, 70mV AT 1mA
- OUTPUT VOLTAGE COMPATIBLE WITH TTL (FANOUT OF 2), DTL, ECL, MOS AND CMOS LOGIC SYSTEMS

ABSOLUTE MAXIMUM RATINGS

Supply voltage	36Vdc or ±18Vdc
Differential input voltage	36Vdc
Input voltage	−0.3Vdc to +36Vdc
Power dissipation	
Molded DIP (LM 139A, LM 239A, LM 339A	570mW
CERDIP (LM 139F, LM 239F, LM 339F)	900 mW
Output short — Circuit to ground	Continuous
Input current (Vin ≤ −0.3Vdc)	50 mA
Operating temperature range	
LM339	0°C to +70°C
LM239	−25°C to +85°C
LM139	−55°C to +125°C
Storage temperature range	−65°C to +150°C
Lead temperature (Soldering 10 sec)	300°C

PIN CONFIGURATION

A, F PACKAGE



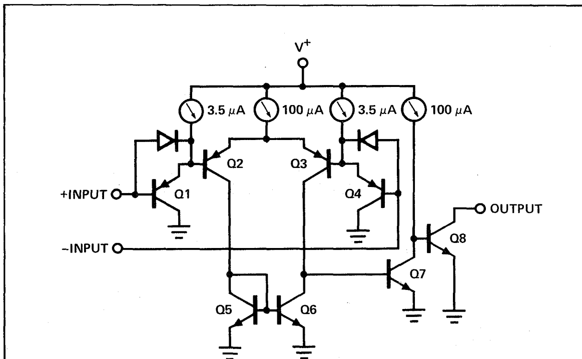
ELECTRICAL CHARACTERISTICS

V_{RL} = 5VDC, R_L = 5.1KΩ, V+ = 5V

PARAMETER	TEST CONDITIONS	LIMITS MIN	TYP	MAX	UNIT
Large Signal Response Time	VIN = TTL Logic Swing, VREF = +1.4VDC		300		ns
Response Time1	TA = 25°C		1.3	μs	

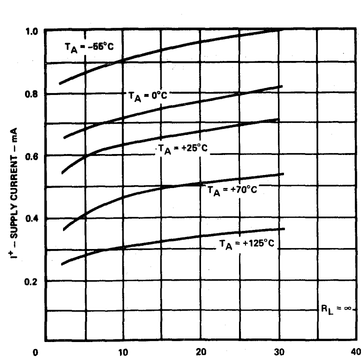
NOTE 1:
The response time specified is for a 100mV input step with 5mV overdrive. For larger overdrive signals 300ns can be obtained, see typical performance characteristics section.

SCHEMATIC DIAGRAM

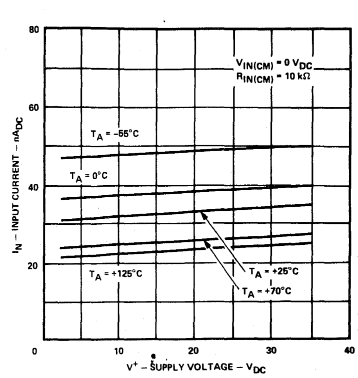


TYPICAL PERFORMANCE CHARACTERISTICS

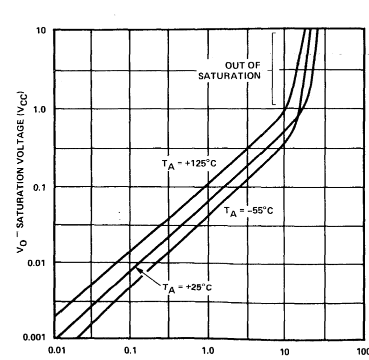
SUPPLY CURRENT



INPUT CURRENT

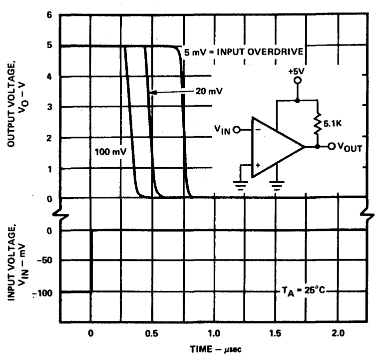


OUTPUT SATURATION VOLTAGE

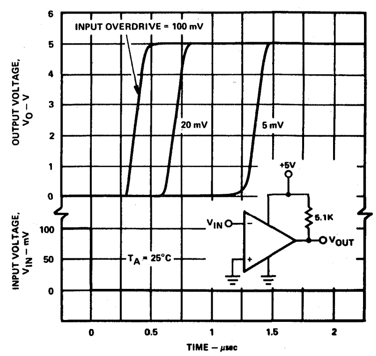


TYPICAL PERFORMANCE CHARACTERISTICS (CONT'D)

RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES— NEGATIVE TRANSITION

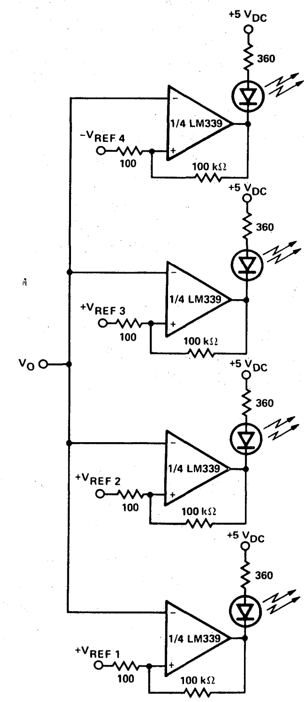


RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES— POSITIVE TRANSITION

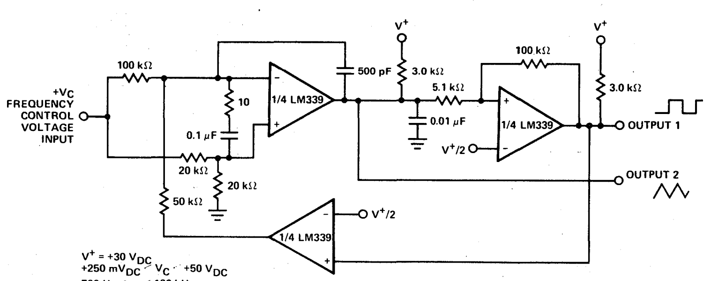


TYPICAL APPLICATIONS

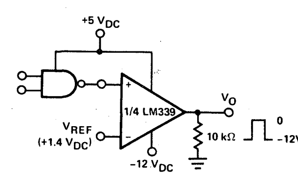
VISIBLE VOLTAGE INDICATOR



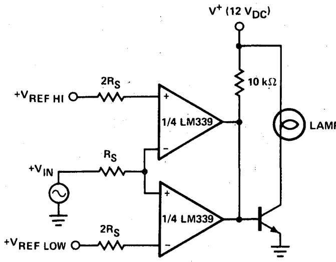
TWO-DECADE HIGH-FREQUENCY V_{CO}



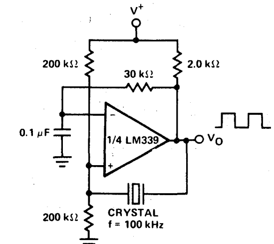
TTL TO MOS LOGIC CONVERTER



LIMIT COMPARATOR



CRYSTAL CONTROLLED OSCILLATOR



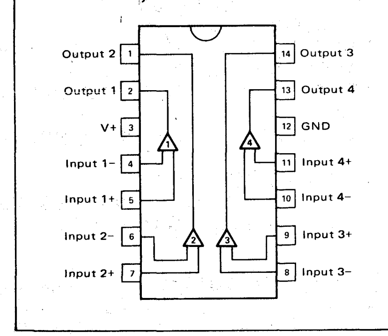
FEATURES

- WIDE SINGLE SUPPLY VOLTAGE RANGE 2 V_{DC} TO 36 V_{DC} OR DUAL SUPPLIES ± 1 V_{DC} TO ± 18 V_{DC}
- VERY LOW SUPPLY CURRENT DRAIN (0.8mA)—INDEPENDENT OF SUPPLY VOLTAGE (2mW/COMPARATOR AT +5 V_{DC})
- LOW INPUT BIASING CURRENT — 35nA
- LOW INPUT OFFSET CURRENT— 3.0nA AND MAXIMUM OFFSET VOLTAGE — 2mV
- INPUT COMMON-MODE VOLTAGE RANGE INCLUDES GROUND
- DIFFERENTIAL INPUT VOLTAGE RANGE EQUAL TO THE POWER SUPPLY VOLTAGE
- LOW OUTPUT SATURATION VOLTAGE — 1mV AT 5μA, 70mV AT 1mA
- OUTPUT VOLTAGE COMPATIBLE WITH TTL, DTL, ECL, MOS AND CMOS LOGIC SYSTEMS

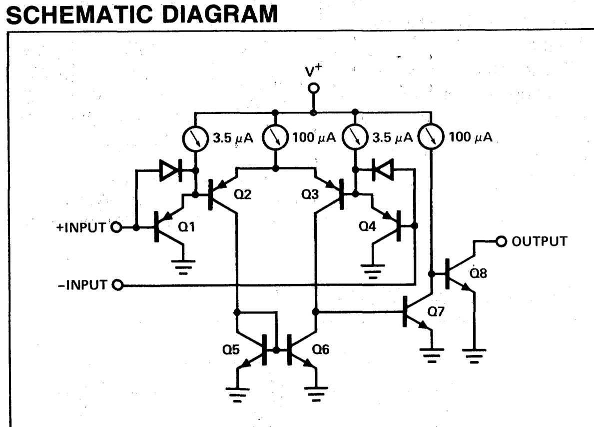
ABSOLUTE MAXIMUM RATINGS

Supply Voltage V+	36V_{DC} or ± 18 V_{DC}
Differential Input Voltage	36 V_{DC}
Input Voltage	-0.3 V_{DC} to $+36$ V_{DC}
Power Dissipation	
Molded DIP	570 mW
(LM 139AA, LM 239AA, LM 339AA) CERDIP (LM 139AF, LM 239AF, LM 339AF)	900 mW
Output Short-Circuit to GND	Continuous
Operating Temperature Range	
LM339A	0°C to +70°C
LM239A	−25°C to +85°C
LM139A	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

PIN CONFIGURATION



SCHEMATIC DIAGRAM



ELECTRICAL CHARACTERISTICS

$V_{RL} = 5V$, $R_L = 5.1K\Omega$, $V+ = 5V$

PARAMETER	TEST CONDITIONS	LIMITS			UNIT
		MIN	TYP	MAX	
Large Signal Response Time	VIN = TTL Logic Swing, VREF = +1.4VDC		300		ns
Response Time1	TA = 25°C		1.3	μs	

NOTE 1:
The response time specified is for a 100mV input step with 5mV overdrive. For larger overdrive signals 300ns can be obtained, see typical performance characteristics section.

ANALOG

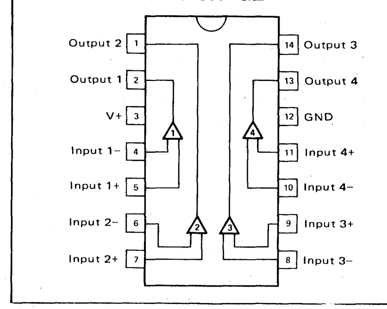
MC3302-A

FEATURES

- WIDE OPERATING TEMPERATURE RANGE — −40 TO +85°C
- TTL COMPATIBLE
- INPUT COMMON-MODE VOLTAGE RANGE INCLUDES GROUND
- DIFFERENTIAL INPUT VOLTAGE = $\pm V_{CC}$
- SINGLE SUPPLY VOLTAGE RANGE — +2 TO +28 V_{DC}
- LOW CURRENT DRAIN
- OUTPUTS CAN BE CONNECTED TO GIVE THE IMPLIED AND FUNCTION

PIN CONFIGURATION

A PACKAGE



MAXIMUM RATINGS T_A = +25°C (Unless Otherwise Noted).

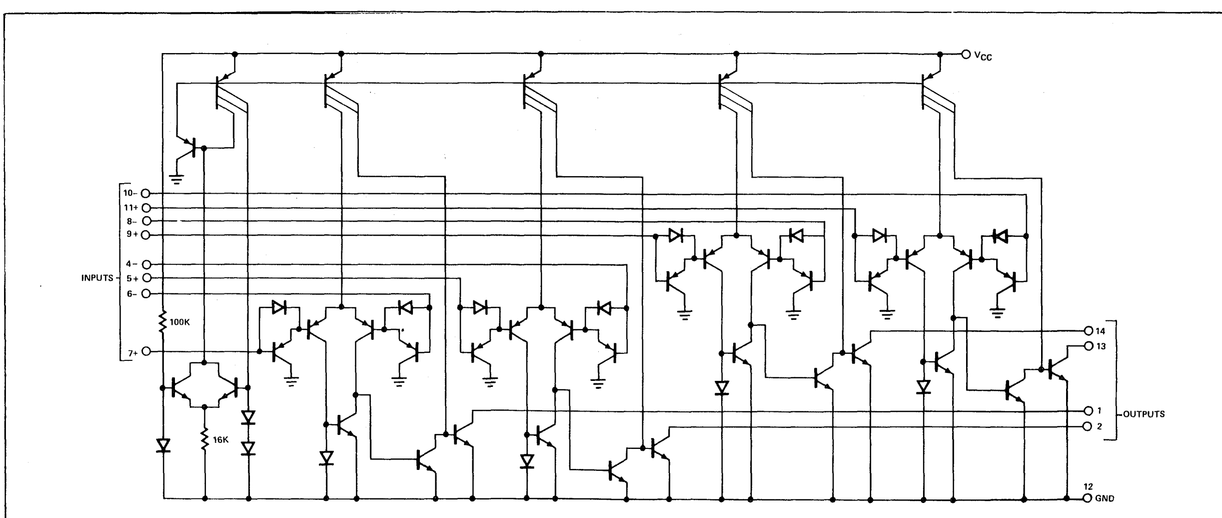
RATING	SYMBOL	VALUE	UNIT
Power supply range	V_{CC}	+2.0 to +28	Vdc
Output supply current[1]	I_O	20	mA
Differential input voltage	V_{IDR}	$\pm V_{CC}$	Vdc
Common-mode input voltage range[2]	V_{ICR}	-0.3 to $+V_{CC}$	Vdc
Power dissipation (package limitation)	P_D	625	mW
Derate above TA = +25°C		5.0	mW/°C
Operating temperature range	T_A	−40 to +85	°C
Storage temperature range	T_{stg}	−65 to +150	°C

NOTES:
1. Requires an external resistor, R_L, to limit current below maximum rating.
2. If either (+) or (−) inputs of any comparator go more than several tenths of a volt below ground, a parasitic transistor turns "on" causing high input current and possible faulty outputs.

ELECTRICAL CHARACTERISTICS (R_L = 15KΩ)

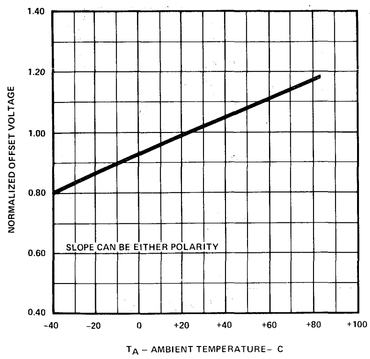
PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT
gm Transconductance		2		mhos
CMRR Common-mode Rejection Ratio		60		dB
Propagation Delay Time				
t_{PLH}		2		μs
t_{PHL}		2		μs
t_{SR-} Slew Rate		200		V/μs
t_{SR+} Slew Rate		50		V/μs

SCHEMATIC DIAGRAM

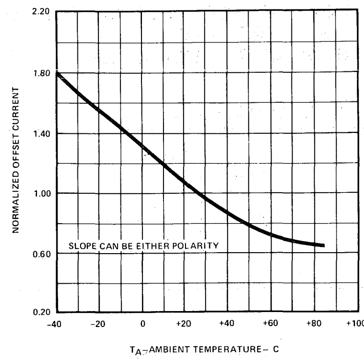


TYPICAL CHARACTERISTICS V_{CC} = +15 Vdc, T_A = +25°C (each compactor) Unless Otherwise Noted.

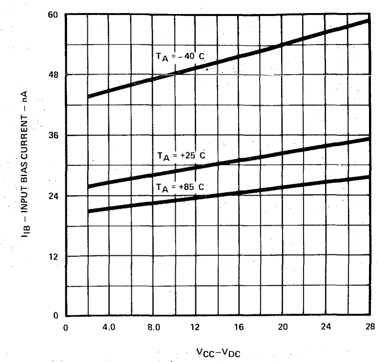
INPUT OFFSET VOLTAGE



OFFSET BIAS CURRENT



INPUT BIAS CURRENT



ANALOG

DIFFERENTIAL VOLTAGE COMPARATOR µA710

µA710-A,T · µ710C-A,T

ABSOLUTE MAXIMUM RATINGS

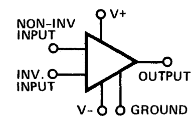
Positive Supply Voltage	+14.0V
Negative Supply Voltage	−7.0V
Peak Output Current	10mA
Differential Input Voltage	±5.0V
Input Voltage	±7.0V
Internal Power Dissipation (Note 4)	
TO-99	300mW
TO-91	200mW
Operating Temperature Range	
µA710	−55°C to +125°C
µA710C	0°C to +75°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 sec)	300°C

Maximum Ratings are limiting values above which serviceability may be impaired.

FEATURES

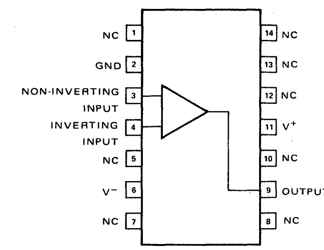
- **FAST RESPONSE — 40 ns**
- **HIGH SENSITIVITY — 1.7V/mv**
- **LOW OFFSET VOLTAGE TEMPERATURE COEFFICIENT — 3.5µV/°C**
- **HIGH INPUT VOLTAGE RANGE — ±5.0V**

LOGIC DIAGRAM

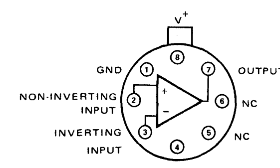


PIN CONFIGURATION

A PACKAGE



T PACKAGE

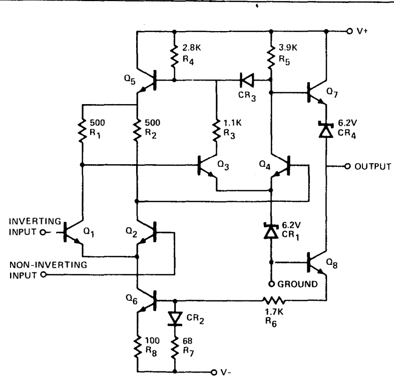


ELECTRICAL CHARACTERISTICS µA710 $-55°C \leq T_A \leq +125°C$
µA710C $0°C \leq T_A \leq +75°C$

PARAMETER	TEST CONDITIONS	LIMITS µA710 MIN	TYP	MAX	µA710C MIN	TYP	MAX	UNIT
Output Resistance			200			200		Ω
Response Time1			40			40		ns
V_{OS} Drift	R_S = 50Ω, T_A = +25°C to +125°C		3.5	10				µV/°C
	R_S = 50Ω, T_A = +25°C to −55°C		2.7	10				µV/°C
	R_S = 50Ω, T_A = 0°C to +75°C					5	20	µV/°C
I_{OS} Drift	T_A = +25°C to +125°C		5	25				nA/°C
	T_A = +25°C to −55°C		15	75				nA/°C
	T_A = +25°C to +75°C					15	50	µA/°C
	T_A = +25°C to 0°C					24	100	µA/°C
CMRR Common-mode Rejection Ratio	$R_S \leq$ 200 Ω	80	100		70	98		dB

NOTE 1: The response time specified is measured with a 100mV input step and a 5mV overdrive.

CIRCUIT SCHEMATIC



μA711 μA711-A,K · μA711C-A,K

ABSOLUTE MAXIMUM RATINGS

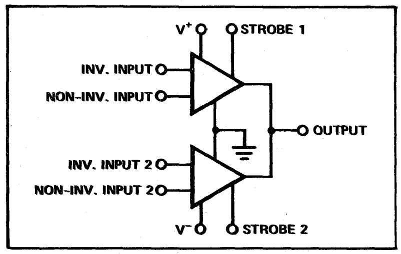
Positive Supply Voltage	+14.0V
Negative Supply Voltage	−7.0V
Peak Output Current	50mA
Differential Input Voltage	±5.0V
Internal Power Dissipation (Note 4) TO-99	300mW
Operating Temperature Range μA711	−55°C to +125°C
μA711C	0°C to +75°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 sec)	300°

Maximum ratings are limiting values above which serviceability may be impaired.

FEATURES

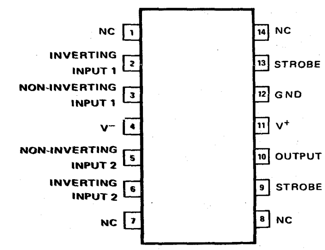
- **FAST RESPONSE — 40ns**
- **HIGH SENSITIVITY — 1.5V/mV**
- **LOW OFFSET VOLTAGE TEMPERATURE COEFFICIENT — 5μV/°C**
- **HIGH INPUT VOLTAGE RANGE — ±5.0V**

LOGIC DIAGRAM

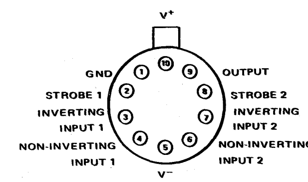


PIN CONFIGURATION

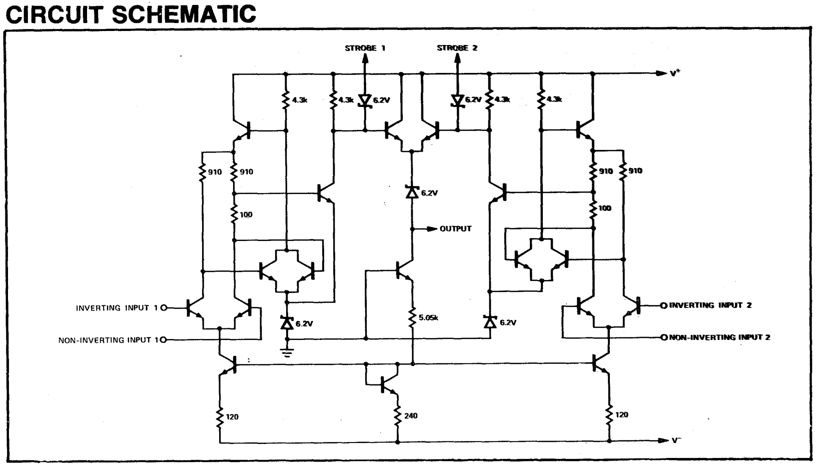
A PACKAGE



K PACKAGE



CIRCUIT SCHEMATIC



ELECTRICAL CHARACTERISTICS

$V_{strobe} = 100mV$

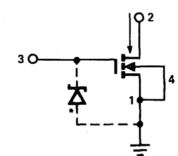
PARAMETER	LIMITS		UNIT
	TYP	MAX	
Response Time[1]	40		ns
Strobe Release Time	12		ns
Output Resistance	200		Ω
Strobe Current	1.2	2.5	mA
V_{OS} Drift	5		μV/°C

Note 1: The response time specified is for a 100mV input step, with a 5mV overdrive.

FEATURES

- Ion-implanted for greater control and reliability
- Wide dynamic range
- Positive bias only
- High gain through UHF range - 10dB at 1GHz
- Low noise through UHF range:
  - SD200 - 4.5dB
  - SD201 - 5.0dB
- Low input capacitance - 2.4pF
- Low feedback capacitance - 0.20pF
- High drain-to-source voltage - +30V
- High forward transconductance - 15,000umhos

COMMON SOURCE BIAS SCHEME

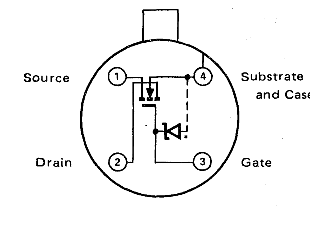


+VDS = 0 +20 Volts
+VGS = 0 +4 Volts
+IDS = 0 +20mA

DIODE PROTECTION ON SD201 ONLY.

PIN CONFIGURATION

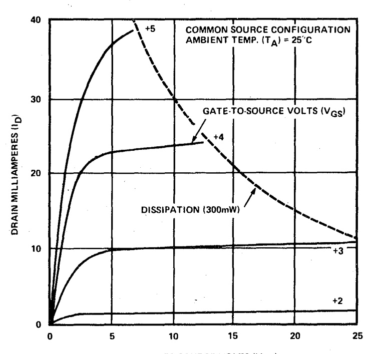
DE PACKAGE



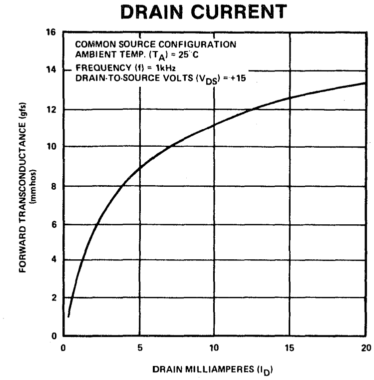
*DIODE PROTECTION ON SD201 ONLY.

CHARACTERISTIC CURVES

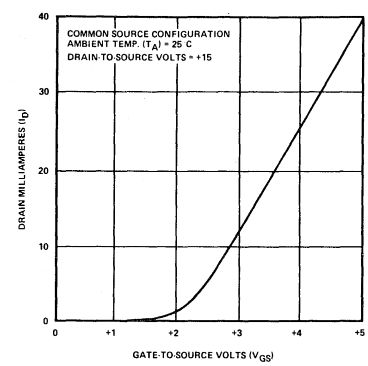
DRAIN CURRENT VS DRAIN-TO-SOURCE VOLTAGE



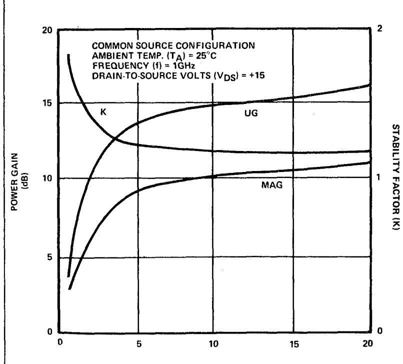
1kHz FORWARD TRANSCONDUCTANCE VS DRAIN CURRENT



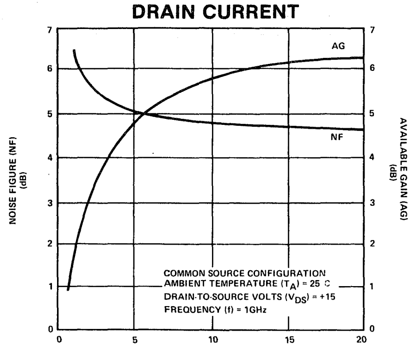
DRAIN CURRENT VS GATE-TO-SOURCE VOLTAGE



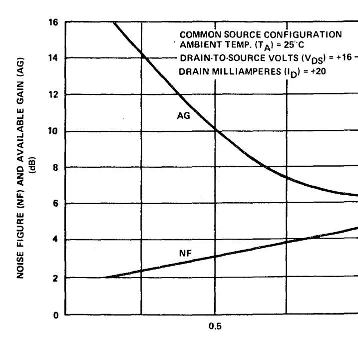
POWER GAIN VS DRAIN CURRENT



NOISE FIGURE AND AVAILABLE GAIN VS DRAIN CURRENT



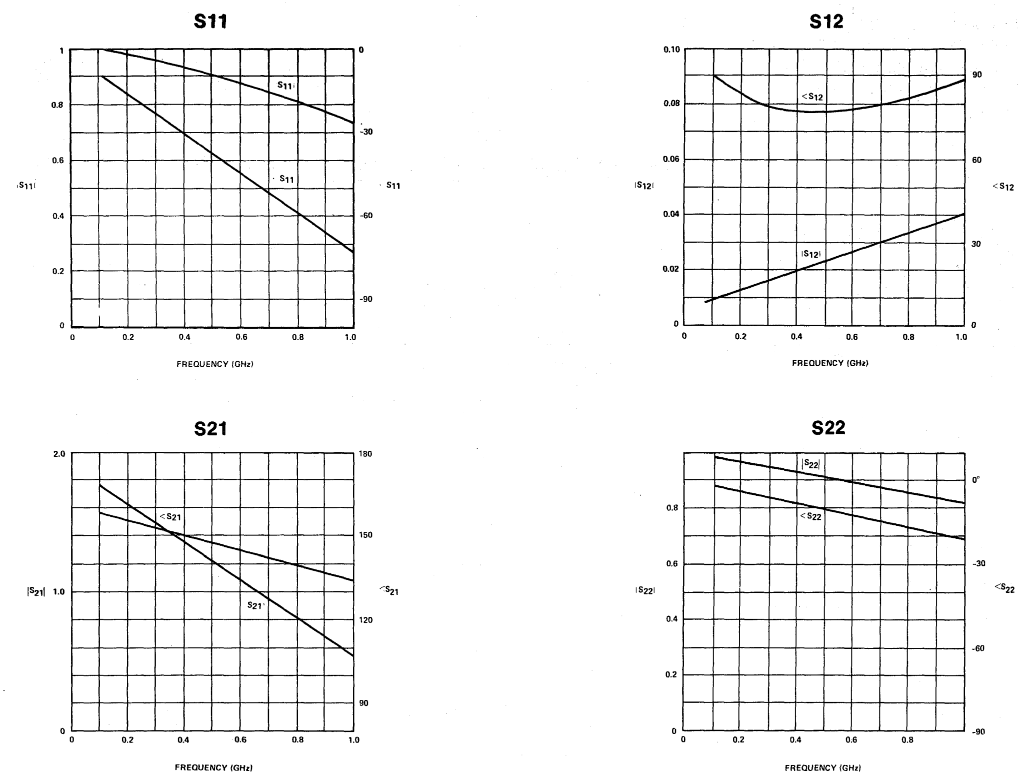
OPTIMUM NOISE FIGURE AND AVAILABLE GAIN VS FREQUENCY



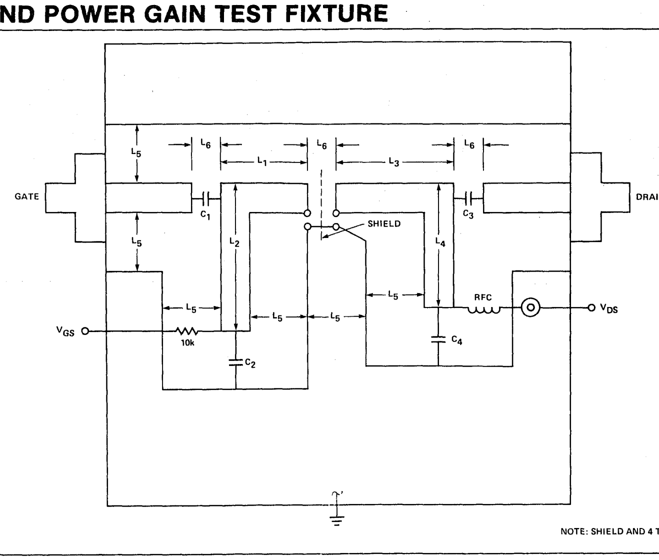
CHARACTERISTIC CURVES (Continued)

"S" PARAMETERS

COMMON SOURCE CONFIGURATION
AMBIENT TEMPERATURE (TA) = 25°C
DRAIN MILLIAMPERES (ID) = 20
DRAIN-TO-SOURCE VOLTS (VDS) = +15



1GHz NOISE FIGURE AND POWER GAIN TEST FIXTURE



DIALECTRIC IS 1/16" TEFLON-FIBERGLASS (3M-K6098-11)
ALL MICROSTRIP WIDTH = 0.175"

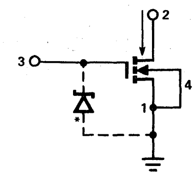
L_1 = 0.48"	$C_1 = C_2 = C_3$ = 0.8-10pF Johanson 5201
L_2 = 1.52"	
L_3 = 0.64"	C_4 = 1.20pF Johanson 5501
L_4 = 1.36"	
L_5 = 5/16"	RFC = 10 TURNS 26 AWG 1/4" DIA.
L_6 = 1/8"	1000pF BYPASS CORY FT4-01-2
	LAUNCHERS – OSM248-2

NOTE: SHIELD AND 4 TUNABLE CAPACITORS ON GROUND PLANE SIDE OF AMPLIFIER.

FEATURES

- Ion-implanted for greater control and reliability
- Wide dynamic range
- Positive bias only
- High gain through UHF range - 10dB at 1.5GHz
- Low noise through UHF range - 3.2dB at 1.0GHz
- Low input capacitance - 3.0pF
- Low feedback capacitance - 0.20pF
- High drain-to-source voltage - +25V
- High forward transconductance - 20,000umhos

COMMON SOURCE BIAS SCHEME

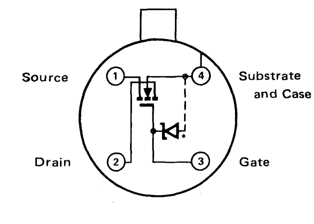


+VDS = 0 +20 Volts
+VGS = 0 +4 Volts
+IDS = 0 +20mA

*DIODE PROTECTION ON SD 203 ONLY.

PIN CONFIGURATION

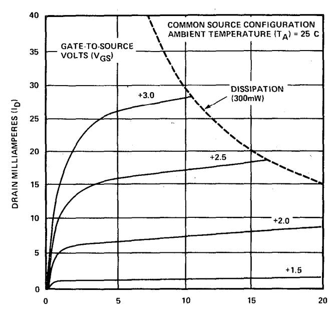
PACKAGE



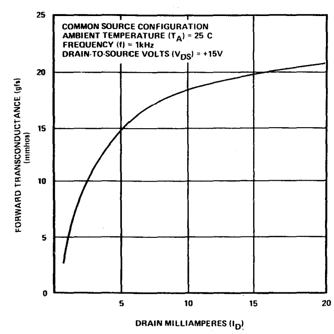
*DIODE PROTECTION ON SD203 ONLY.

CHARACTERISTIC CURVES

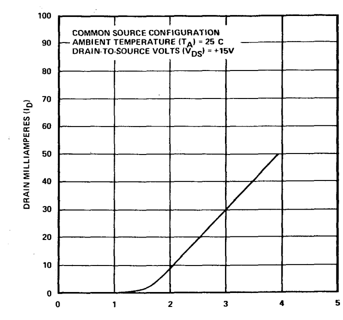
DRAIN CURRENT VS DRAIN-TO-SOURCE VOLTAGE



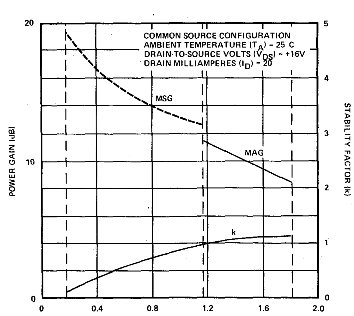
1kHz FORWARD TRANSCONDUCTANCE VS DRAIN CURRENT



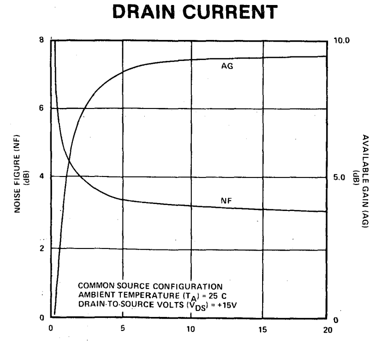
DRAIN CURRENT VS GATE-TO-SOURCE VOLTAGE



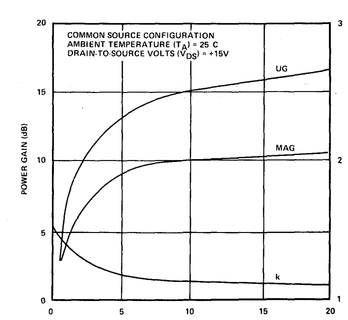
POWER GAIN VS FREQUENCY



1.0GHz NOISE FIGURE AND AVAILABLE GAIN VS DRAIN CURRENT

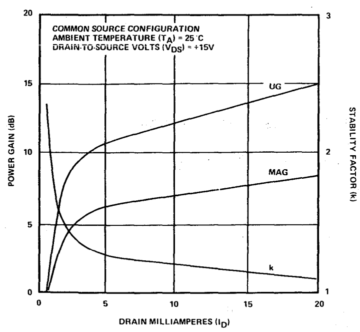


1.5GHz POWER GAIN VS DRAIN CURRENT



CHARACTERISTIC CURVES (Continued)

1.8GHz POWER GAIN VS DRAIN CURRENT

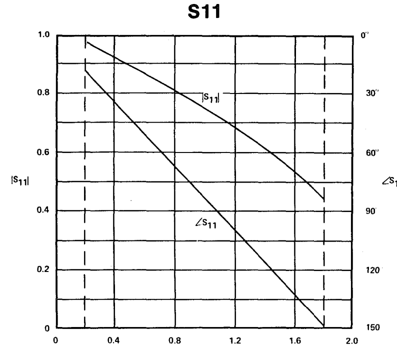


"S" PARAMETERS

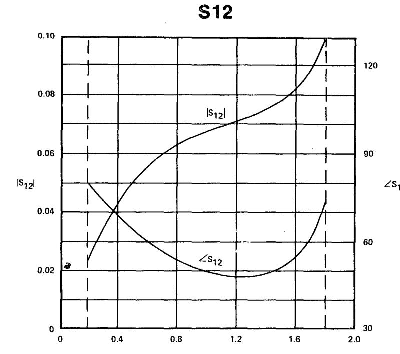
COMMON SOURCE CONFIGURATION
AMBIENT TEMPERATURE (T_A) = 25°C

DRAIN MILLIAMPERES (I_D) = 20
DRAIN-TO-SOURCE VOLTS (V_{DS}) =+15

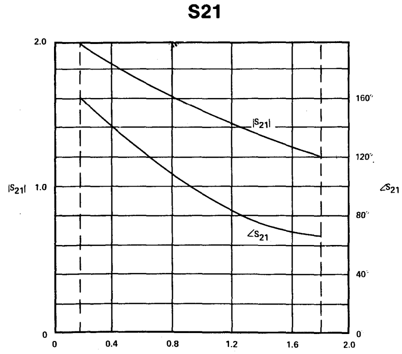
S11



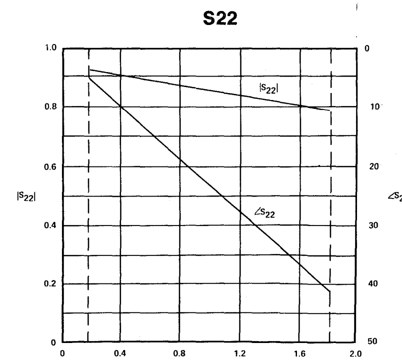
S12



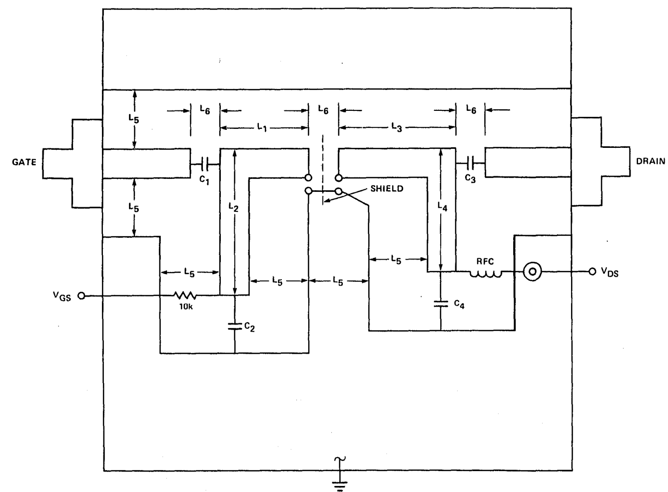
S21



S22



1GHz NOISE FIGURE AND POWER GAIN TEST FIXTURE



DIALECTRIC IS 1/16″ TEFLON-FIBERGLASS (3M-K6098-11)
ALL MICROSTRIP WIDTH = 0.175″

L1 = 0.48″
L2 = 1.52″
L3 = 0.64″
L4 = 1.36″
L5 = 5/16″
L6 = 1/8″

C1 = C2 = C3 = 0.8-10pF
Johanson 5201
C4 = 1.20pF
Johanson 5501
RFC = 10 TURNS 26 AWG ¼″ DIA.
1000pF BYPASS
CORY FT4-01-2
LAUNCHERS—OSM248-2

NOTE: SHIELD AND 4 TUNABLE CAPACITORS ON GROUND PLANE SIDE OF AMPLIFIER.

FEATURES

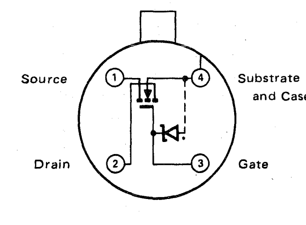
- LOW FEEDBACK CAPACITANCE — 0.30pF
- LOW DRAIN NODE CAPACITANCE — 1.3pF
- LOW GATE NODE CAPACITANCE — 2.4pF
- LOW FEEDTHROUGH AND FEEDBACK TRANSIENTS
- ION-IMPLANTED FOR GREATER RELIABILITY
- EXCELLENT ISOLATION FROM INPUT TO OUTPUT — 120dB
- 35V DRAIN-TO-SOURCE VOLTAGE FOR SD210/211

APPLICATIONS

SWITCH DRIVER
ANALOG SWITCH
MULTIPLEXERS
DIGITAL SWITCH
SAMPLE AND HOLD
CHOPPERS
A-TO-D CONVERTERS
D-TO-A CONVERTERS

PIN CONFIGURATION

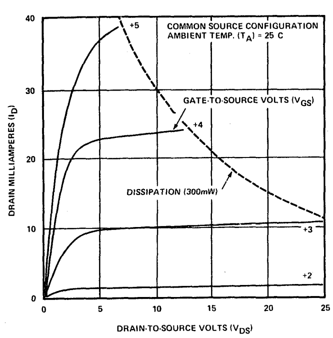
DE PACKAGE



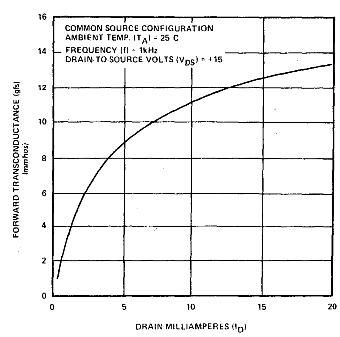
*Diode protection on SD211/213/215 only.

CHARACTERISTIC CURVES

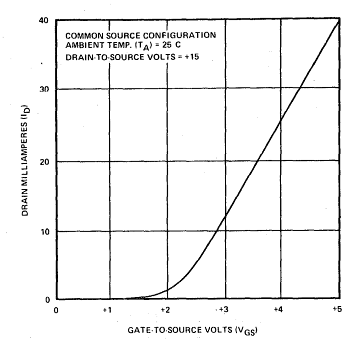
DRAIN CURRENT VS DRAIN-TO-SOURCE VOLTAGE



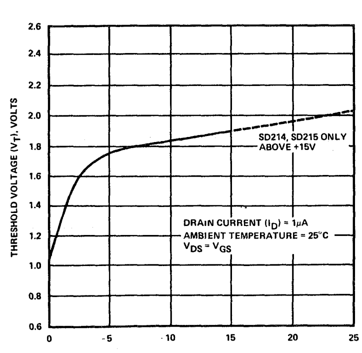
1kHz FORWARD TRANSCONDUCTANCE VS DRAIN CURRENT



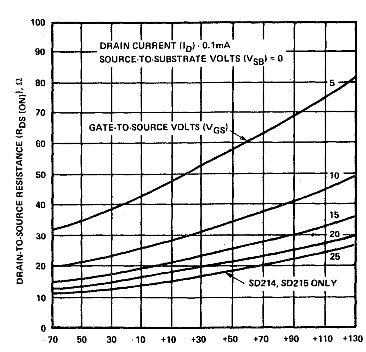
DRAIN CURRENT VS GATE-TO-SOURCE VOLTAGE



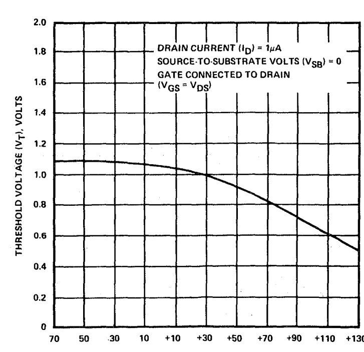
THRESHOLD VOLTAGE VS SOURCE-TO-SUBSTRATE VOLTAGE



DRAIN-TO-SOURCE RESISTANCE VS TEMPERATURE

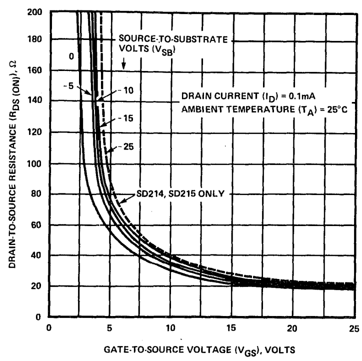


THRESHOLD VOLTAGE VS TEMPERATURE

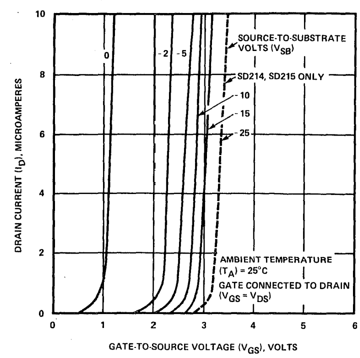


CHARACTERISTIC CURVES (Continued)

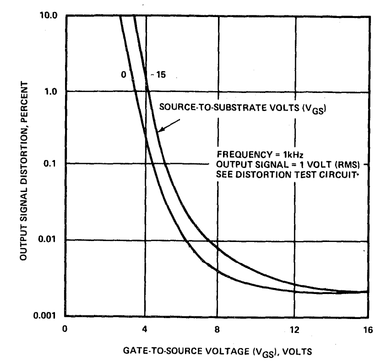
DRAIN-TO-SOURCE RESISTANCE VS GATE-TO-SOURCE VOLTAGE



DRAIN CURRENT VS GATE-TO-SOURCE VOLTAGE



DISTORTION VS GATE-TO-SOURCE VOLTAGE

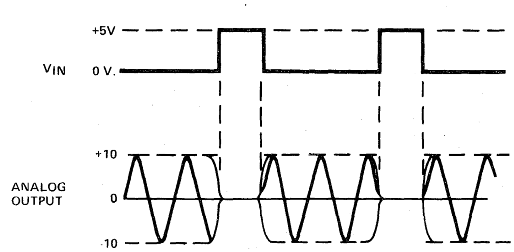


SWITCHING CHARACTERISTICS

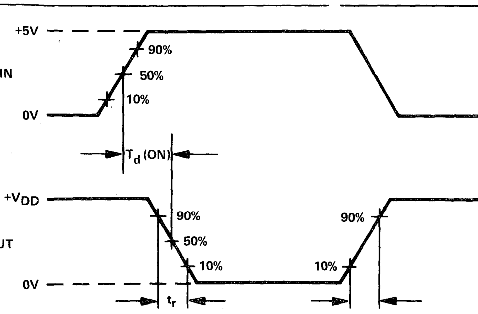
		t_d (ON) (ns)		t_r (ns)		t_{OFF} (ns)	
V_{DD}	R_L	TYP	MAX	TYP	MAX	TYP	MAX
5	680	0.6	1.0	0.7	1.0	9.0	*
10	680	0.7		0.8		9.0	
15	1k	0.9		1.0		14.0	

*t_{OFF} is dependent on R_L and C_L and does not depend on the device characteristics.

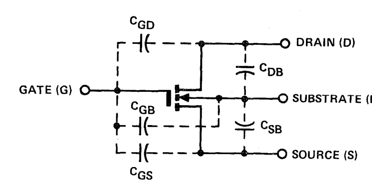
TYPICAL WAVEFORMS



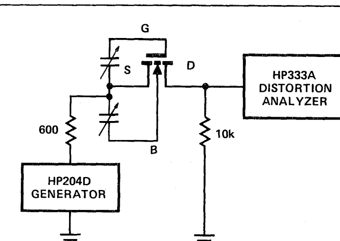
SWITCHING WAVEFORMS



CAPACITANCE MODEL

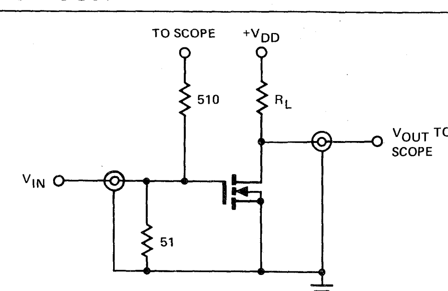


DISTORTION TEST CIRCUIT



NOTE: ALL RESISTORS STANDARD AND ARE MEASURED IN OHMS.

TEST CIRCUIT

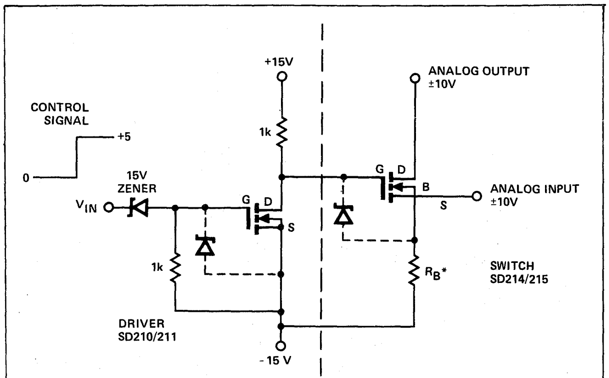


NOTE: ALL RESISTORS STANDARD AND ARE MEASURED IN OHMS.

INPUT PULSE
t_d, t_F 1ns
PULSE WIDTH = 100ns
REP RATE = 1MHz

SAMPLING SCOPE
t_r 360ps
R_{IN} = 1M
C_{IN} = 2.0pF

D-MOS DRIVER/SWITCH APPLICATION



R_B* OPTIONAL CURRENT LIMITING RESISTOR

NOTE: ALL RESISTORS STANDARD AND ARE MEASURED IN OHMS.

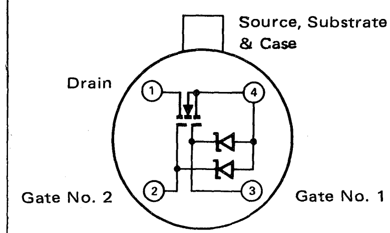
GENERAL FEATURES

- **Lower cross-modulation and wider dynamic range than bipolar or single gate FETs**
- **Reverse AGC capability**
- **Linear mixing capability**
- **Diode protected gates**
- **High forward transconductance - gfs = 10,000umhos**
- **Ion-implanted**
- **Positive bias only**

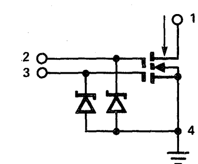
PARAMETER	SD 300	SD301	SD 303	SD304	UNIT
High Gain Through UHF Range	13	14	14		dB at 1GHz
High Gain Through VHF Range				16	dB at 500MHz
Low Noise Through UHF Range	8	6	5.5		dB at 1GHz
Low Noise Through VHF Range				5	dB at 500MHz
Low Input Capacitance	2.0	2.0	3.0	2.5	pF
Low Feedback Capacitance	0.02	0.02	0.02	0.03	pF
Low Output Capacitance	1.0	0.6	0.6	1.0	pF

PIN CONFIGURATION

PACKAGE

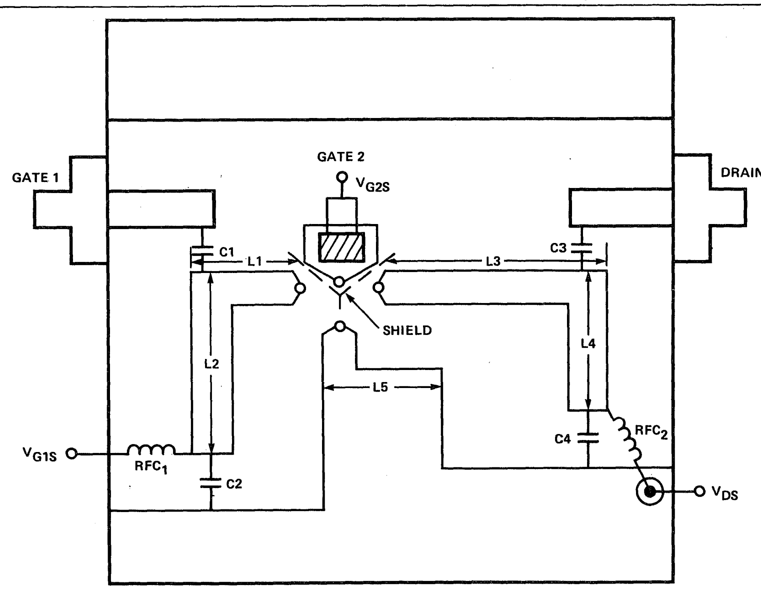


DUAL GATE CASCODE BIAS SCHEME



$+V_{DS} = 0 \rightarrow +20$ Volts
$+V_{G1S} = 0 \rightarrow +4$ Volts
$+V_{G2S} = 0 \rightarrow +10$ Volts
$+I_{DS} = 0 \rightarrow +20$mA

TEST FIXTURE (1GHz) (Used With SD300, 301, 303)



DIELECTRIC IS 1/16" TEFLON-FIBERGLASS (3M-K6098-11).
ALL MICROSTRIP WIDTH = 0.175 INCH.

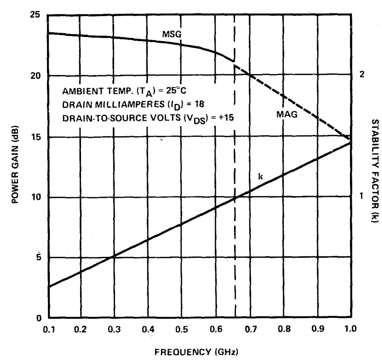
L_1 = 0.42 INCH	C_1 = 0.8-10pF JOHANSON 5201
L_2 = 1.68 INCHES	$C_2 = C_4$ = 1.20pF JOHANSON 5501
L_3 = 0.64 INCH	C_3 = 0.4-6.0pF JOHANSON 4642
L_4 = 1.52 INCHES	RFC_1 = 0.22μH
L_5 = 0.30 INCH	RFC_2 = 18μH

NOTE: SHIELD AND ALL PASSIVE COMPONENTS ON GROUND PLANE SIDE OF AMPLIFIER.
1000pF BYPASSES ARE:
DRAIN: CORY FT4-01-2
GATE 2: AMERICAN TECHNICAL CERAMICS ATC100B (CHIP CAPACITOR)
LAUNCHERS ARE OSM248-2

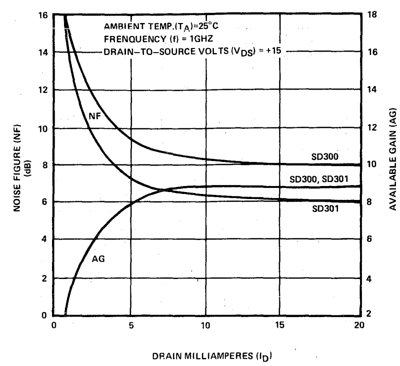
CHARACTERISTIC CURVES

SD300, 301

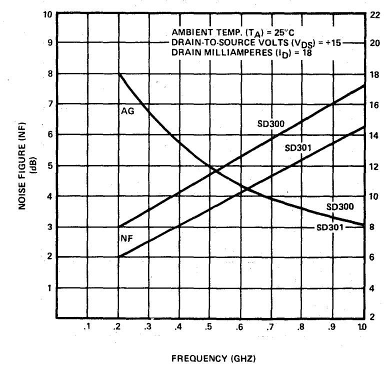
POWER GAIN VS FREQUENCY



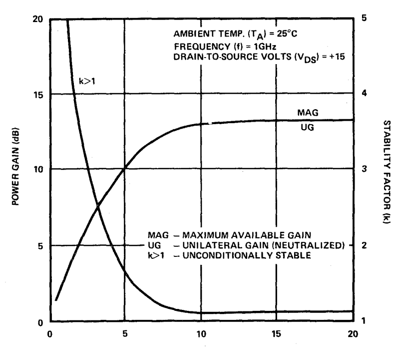
NOISE FIGURE AND AVAILABLE GAIN VS DRAIN CURRENT



NOISE FIGURE AND AVAILABLE GAIN VS FREQUENCY

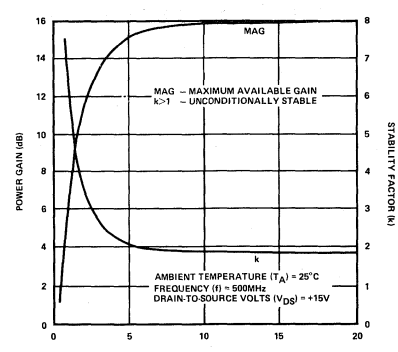


POWER GAIN VS DRAIN CURRENT

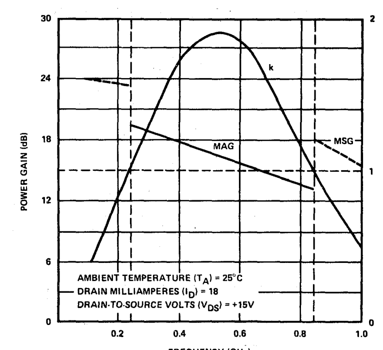


SD304

POWER GAIN VS DRAIN CURRENT

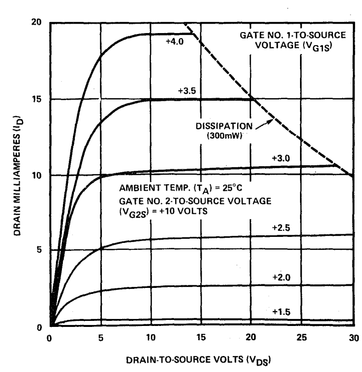


POWER GAIN VS FREQUENCY

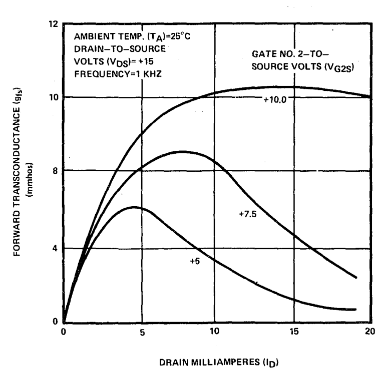


SD300, 301, 304

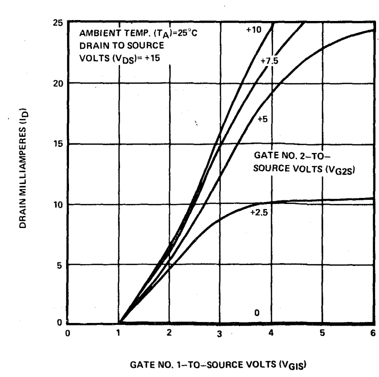
DRAIN CURRENT VS DRAIN-TO-SOURCE VOLTAGE



1kHz FORWARD TRANSCONDUCTANCE VS DRAIN CURRENT



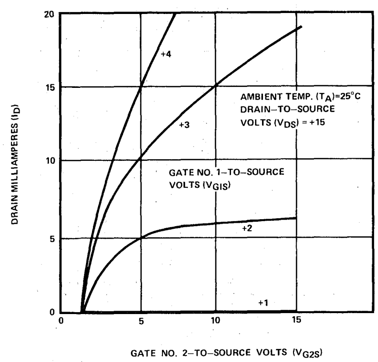
DRAIN CURRENT VS GATE NO. 1-TO-SOURCE VOLTAGE



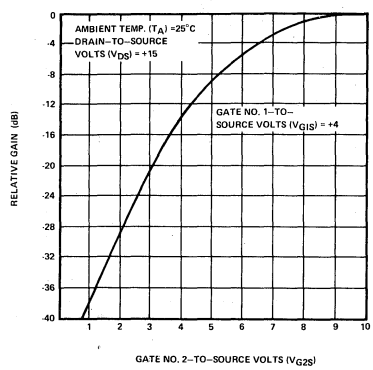
CHARACTERISTIC CURVES (Continued)

SD 300, 301, 304

DRAIN CURRENT VS GATE NO. 2-TO-SOURCE VOLTAGE

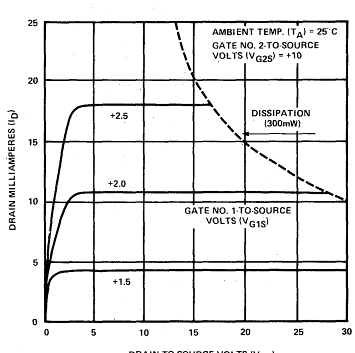


AUTOMATIC GAIN CONTROL RANGE AT 500MHz

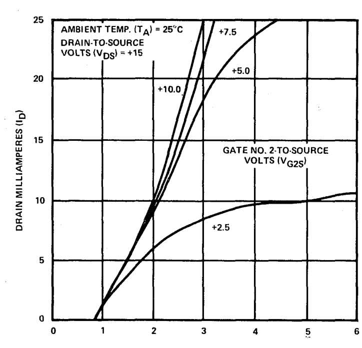


SD303

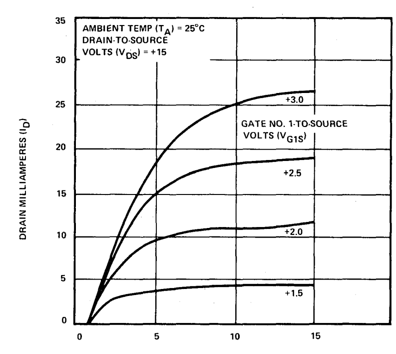
DRAIN CURRENT VERSUS DRAIN-TO-SOURCE VOLTAGE



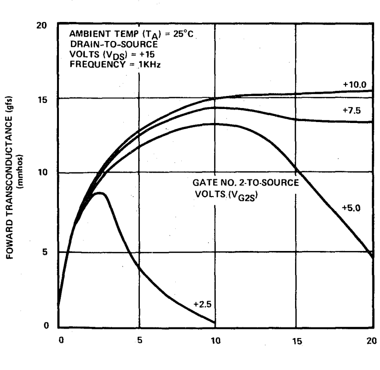
DRAIN CURRENT VERSUS GATE NO. 1-TO-SOURCE VOLTAGE



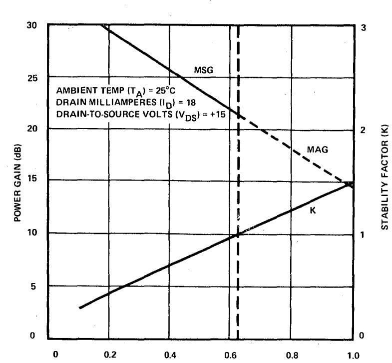
DRAIN CURRENT VERSUS GATE NO. 2-TO-SOURCE VOLTAGE



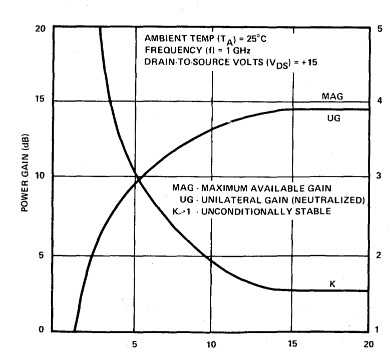
1kHz FORWARD TRANSCONDUCTANCE VERSUS DRAIN CURRENT



POWER GAIN VERSUS FREQUENCY



POWER GAIN VERSUS DRAIN CURRENT

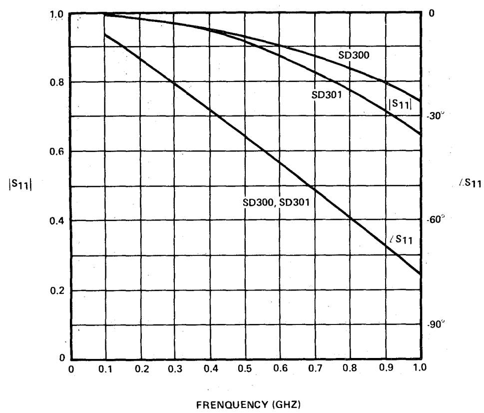


CHARACTERISTIC CURVES (Continued)

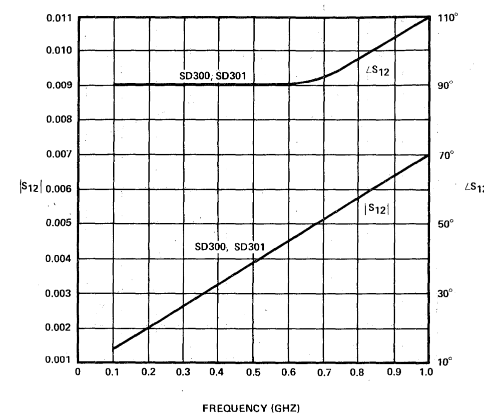
SD300/301

S PARAMETERS
AMBIENT TEMP. (T_A) = +25°C
DRAIN MILLIAMPERES (I_D) = 18
DRAIN-TO-SOURCE VOLTS (V_{DS}) = +15

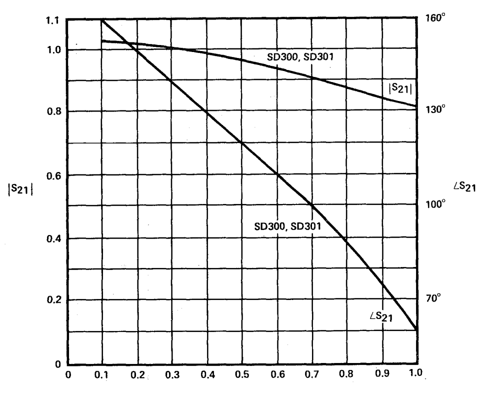
S_{11}



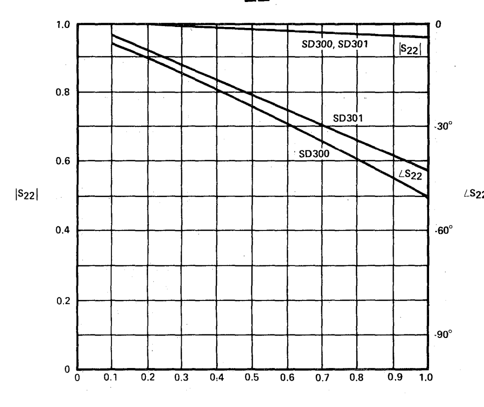
S_{12}



S_{21}



S_{22}



ANALOG

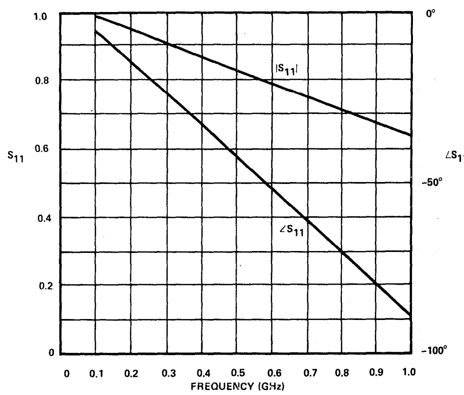
CHARACTERISTIC CURVES (Continued)

SD303

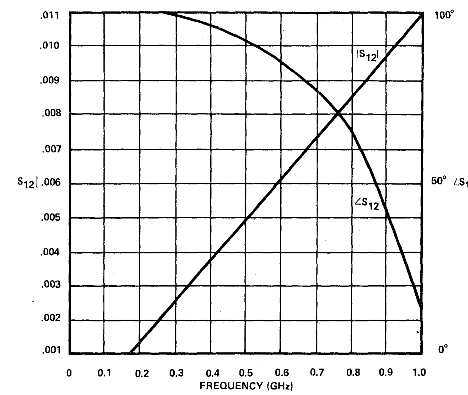
S PARAMETERS

AMBIENT TEMP. (T_A) = 25°C
DRAIN MILLIAMPERES (I_D) = 18
DRAIN-TO-SOURCE VOLTS (V_{DS}) = +15

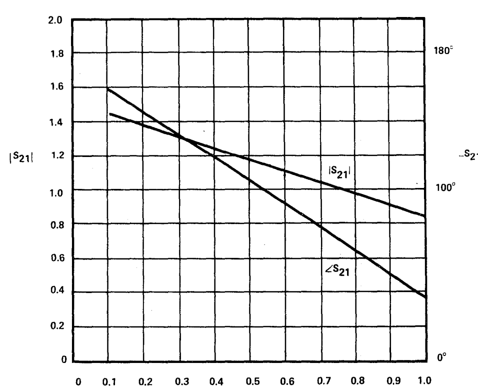
S_{11}



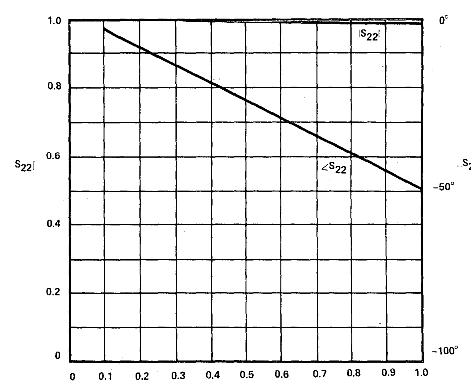
S_{12}



S_{21}



S_{22}



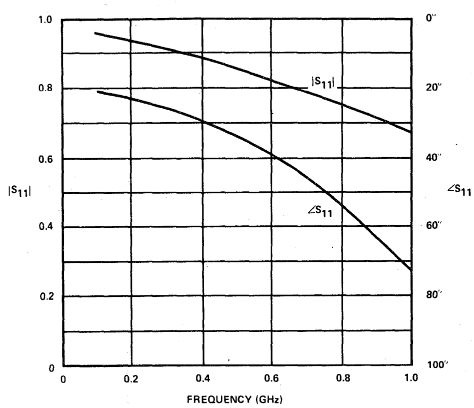
CHARACTERISTIC CURVES (Continued)

SD304

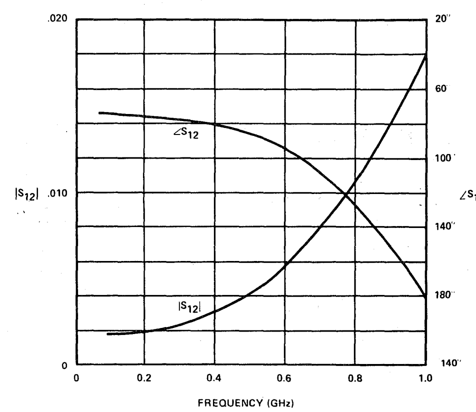
S PARAMETERS

AMBIENT TEMP. (T_A) = +25°C
DRAIN MILLIAMPERES (I_D) = 18
DRAIN-TO-SOURCE VOLTS (V_{DS}) = +15

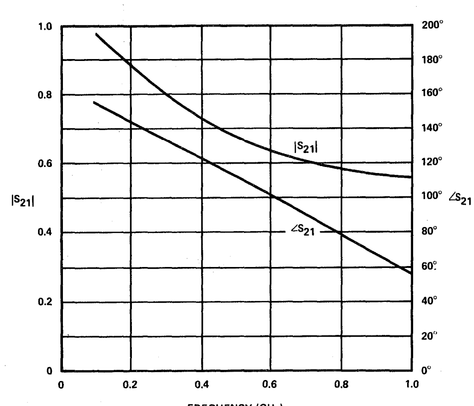
S_{11}



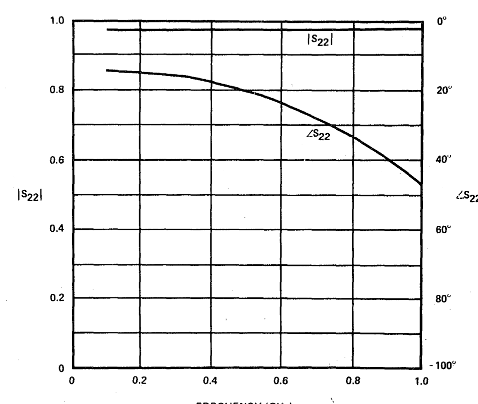
S_{12}



S_{21}



S_{22}

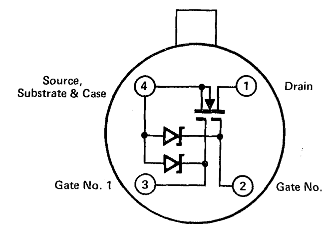


FEATURES

- Positive bias only
- Low gate voltage
- Enhancement mode operation
- Wide AGC range - 50dB at 200MHz
- Zener diode gate protection
- Ion implanted for greater reliability
- High conversion gain - 17dB at 200MHz with VG1S = VG2S for biasing simplicity
- Excellent isolation from gate no. 1 (RF) to gate no. 2 (LO) - 20dB at 200MHz
- Low input capacitance - 4.0pF
- Low feedback capacitance - 0.03pF
- Excellent cross modulation performance and low noise operation
- High transconductance - 27mmhos

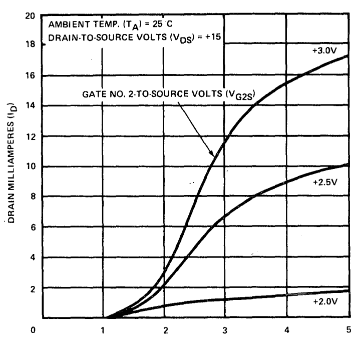
PIN CONFIGURATION

PACKAGE

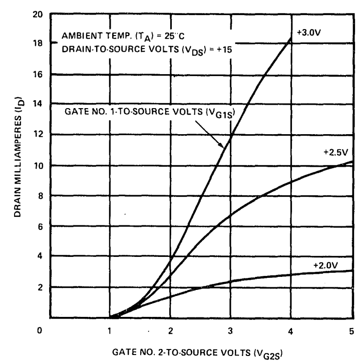


CHARACTERISTIC CURVES

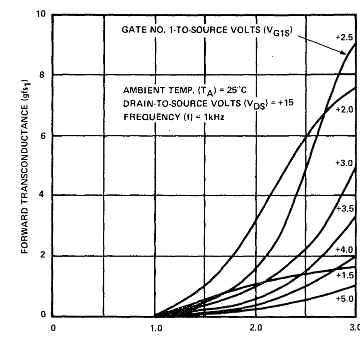
DRAIN CURRENT VS GATE NO. 1-TO-SOURCE VOLTAGE



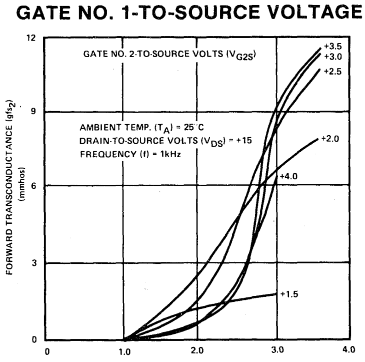
DRAIN CURRENT VS GATE NO. 2-TO-SOURCE VOLTAGE



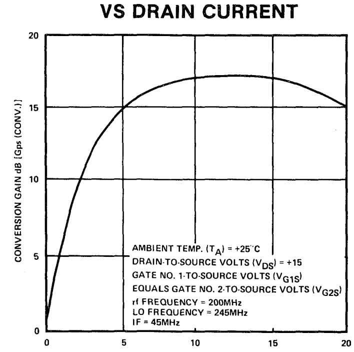
GATE NO. 1 FORWARD TRANSCONDUCTANCE VS GATE NO. 2-TO-SOURCE VOLTAGE



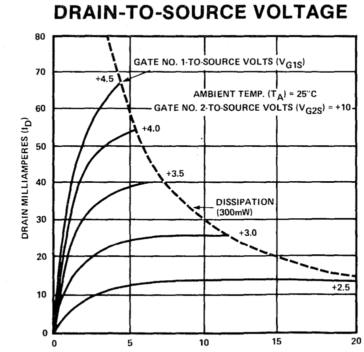
GATE NO. 2 FORWARD TRANSCONDUCTANCE VS GATE NO. 1-TO-SOURCE VOLTAGE



CONVERSION GAIN VS DRAIN CURRENT

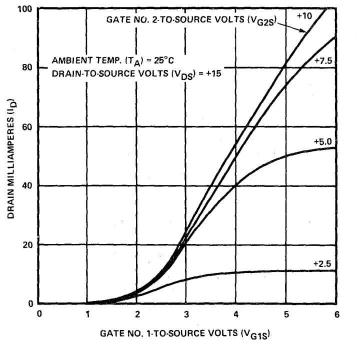


DRAIN CURRENT VS DRAIN-TO-SOURCE VOLTAGE

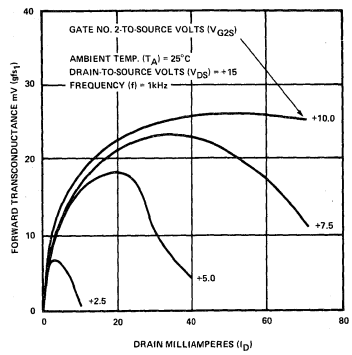


CHARACTERISTIC CURVES (Continued)

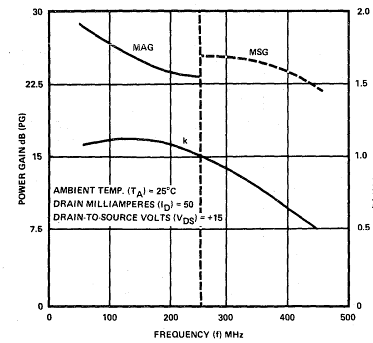
DRAIN CURRENT VS GATE NO. 1-TO-SOURCE VOLTAGE



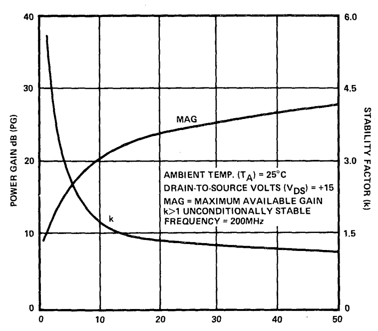
GATE NO. 1 FORWARD TRANSCONDUCTANCE VS DRAIN CURRENT



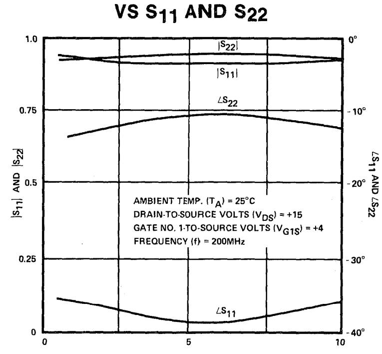
POWER GAIN VS FREQUENCY



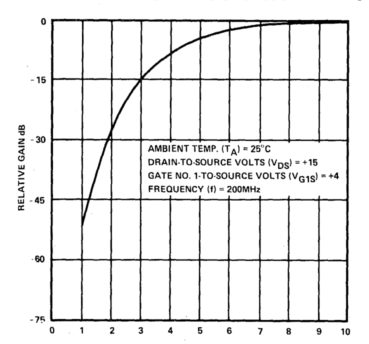
POWER GAIN VS DRAIN CURRENT



AUTOMATIC GAIN CONTROL VS S_{11} AND S_{22}



AUTOMATIC GAIN CONTROL RANGE

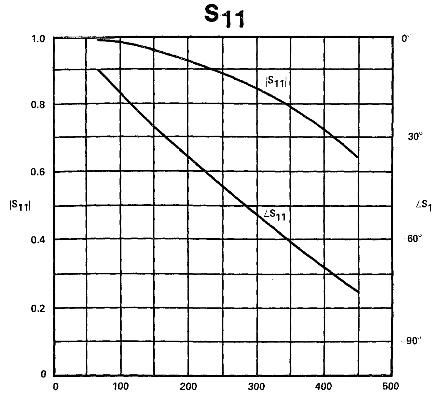


S PARAMETERS

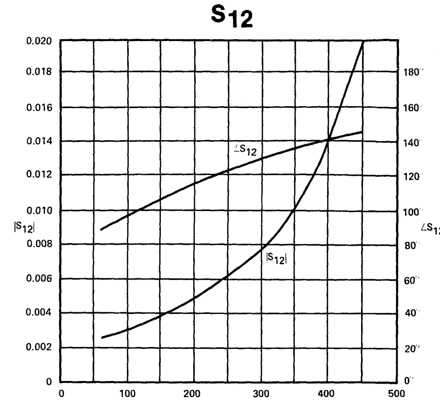
AMBIENT TEMP. (T_A) = +25°C
DRAIN-TO-SOURCE VOLTS (V_{DS}) = +15

DRAIN MILLIAMPERES (I_D) = 8
GATE NO. 1-TO-SOURCE VOLTS = GATE NO. 2-TO-SOURCE VOLTS

S_{11}

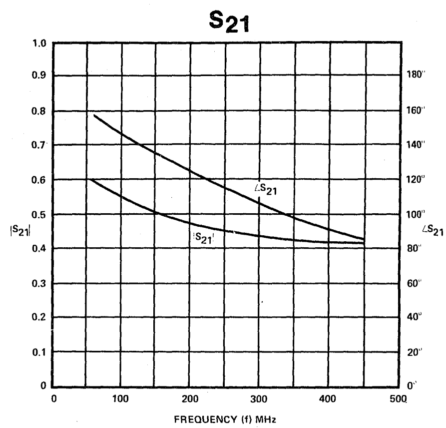


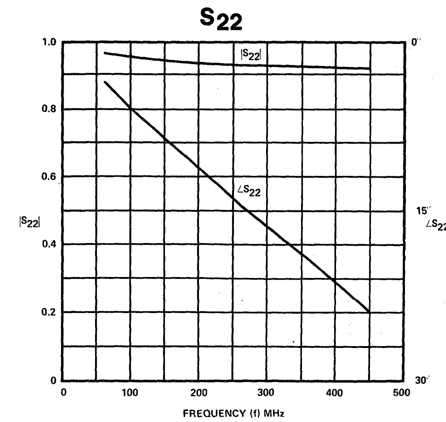
S_{12}



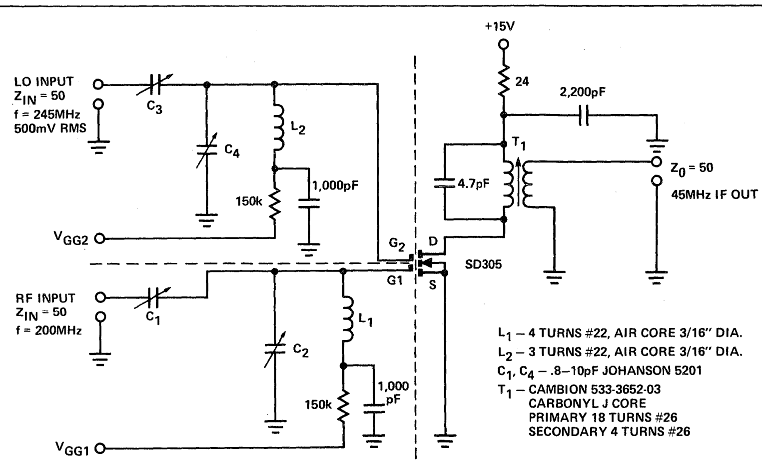
ANALOG

CHARACTERISTIC CURVES (Continued)





200MHz/45MHz MIXER TEST CIRCUIT

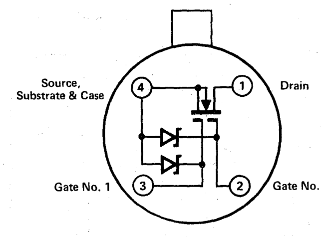


FEATURES

- Positive bias only
- Low gate voltage
- Enhancement mode operation
- Wide AGC range - 50dB at 200MHz
- Zener diode gate protection
- Ion implanted for greater reliability
- High power gain without neutralization - 20dB at 200MHz
- Low noise figure - 1.5dB at 200MHz
- Low input and output capacitance - 3.3pF and 1.0pF constant with AGC
- Low feedback capacitance - 0.03pF
- Superior cross modulation performance
- High transconductance - 15mmhos

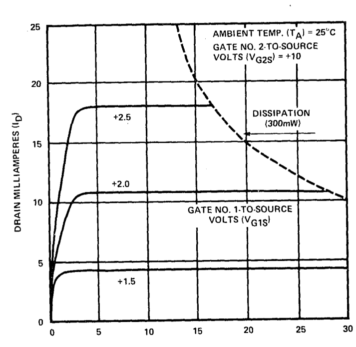
PIN CONFIGURATION

DE PACKAGE

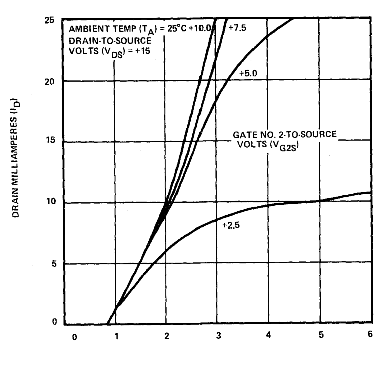


CHARACTERISTIC CURVES

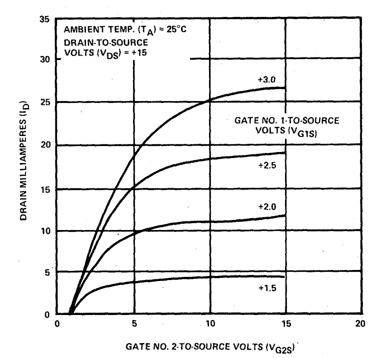
DRAIN CURRENT VS DRAIN-TO-SOURCE VOLTAGE



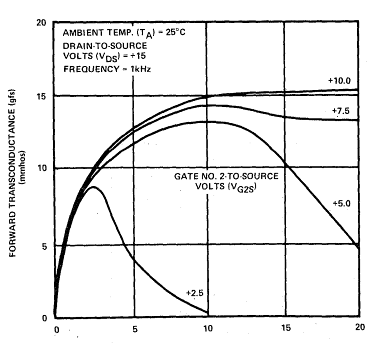
DRAIN CURRENT VS GATE NO. 1-TO-SOURCE VOLTAGE



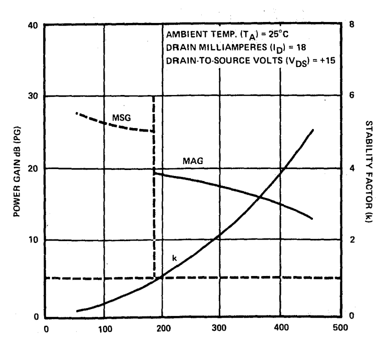
DRAIN CURRENT VS GATE NO. 2-TO-SOURCE VOLTAGE



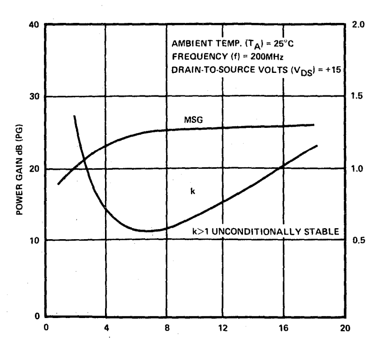
1kHz FORWARD TRANSCONDUCTANCE VS DRAIN CURRENT



POWER GAIN VS FREQUENCY

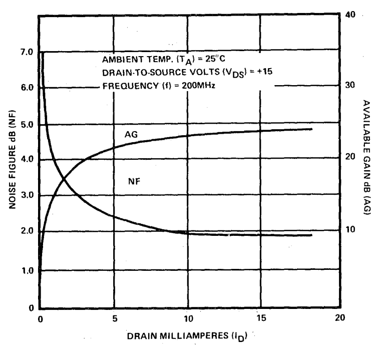


POWER GAIN VS DRAIN MILLIAMPERES

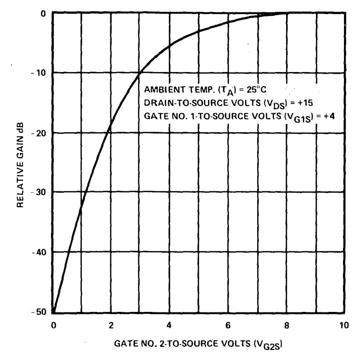


CHARACTERISTIC CURVES (Continued)

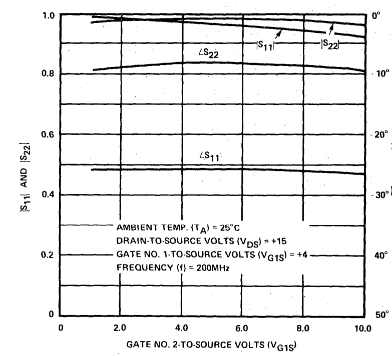
NOISE FIGURE AND AVAILABLE GAIN VS DRAIN CURRENT



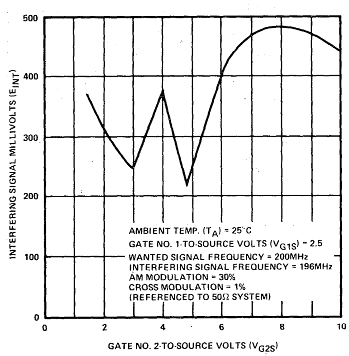
AUTOMATIC GAIN CONTROL RANGE AT 200MHz



S11 AND S22 VS AUTOMATIC GAIN CONTROL

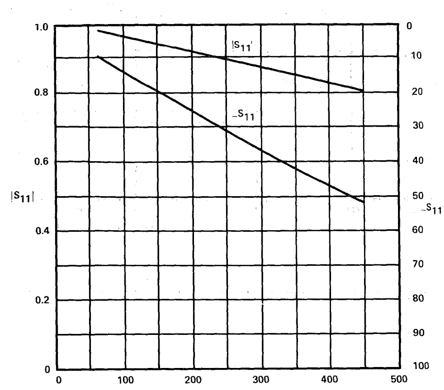


INTERFERING SIGNAL LEVEL VS GATE NO. 2-TO-SOURCE VOLTS

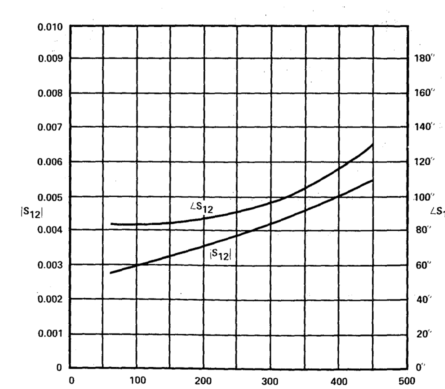


S PARAMETERS
AMBIENT TEMP. (T_A) = +25°C
DRAIN MILLIAMPERES (I_D) = 18
DRAIN-TO-SOURCE VOLTS (V_{DS}) = 15

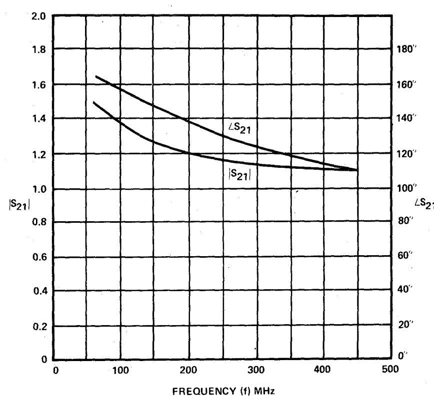
S_{11}

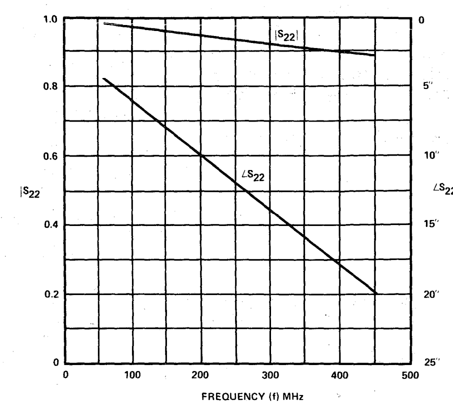


S_{12}

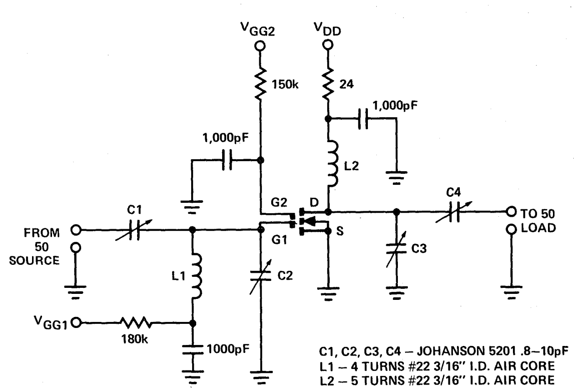


CHARACTERISTIC CURVES (Continued)

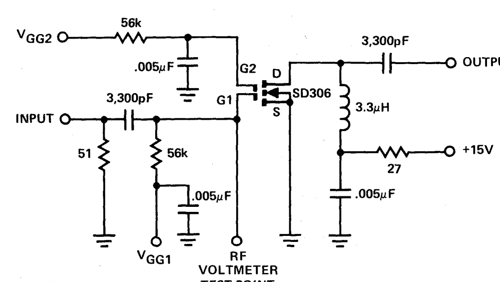




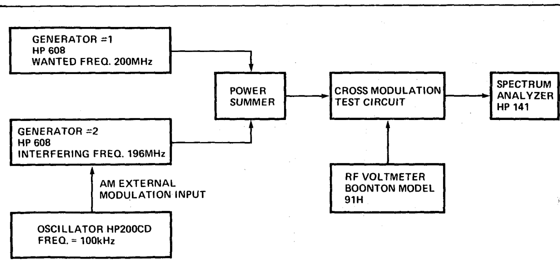
200MHz TEST AMPLIFIER; POWER GAIN, NOISE FIGURE



CROSS MODULATION TEST CIRCUIT



BLOCK DIAGRAM OF CROSS MODULATION TEST



TEST PROCEDURE FOR CROSS MODULATION

DISTORTION MEASUREMENTS

1. Modulation on Generator #2 is set at 100kHz, 30% AM modulation (sidebands down 15.6dB) with an output signal frequency equal to 196MHz.
2. Generator #2 is set at approximately -15dbm, 200MHz.
3. While observing the test circuit output spectrum, adjust the signal level of the interfering frequency so that the sidebands on the desired frequency are 46dB down from the carrier. This corresponds to 1% cross modulation.
4. Turn off Generator #1 and turn off the modulation on Generator #2.
5. Using the RF voltmeter, measure the amplitude of the interfering signal at the test point.

D-MOS FET QUAD SWITCH ARRAYS, MULTIPLEXERS AND DRIVER

SD5000/5001 5100/5101/5200

FEATURES

- Low input capacitance — 2.4pF
- Low feedback capacitance—0.3pF
- Low output capacitance—1.3pF
- ±10V analog signal range
- Low propagation delay time—600ps
- Low on resistance—30Ω
- Low feedthrough and feedback transients
- Ion implanted for greater reliability
- High channel-to-channel isolation—107dB
- Transient protection for gates

SD5000 APPLICATIONS

Analog switching (up to very high frequencies)

Audio routing

Choppers

Crosspoint switches

Sample and hold

SD5100 APPLICATIONS

Multiplexing

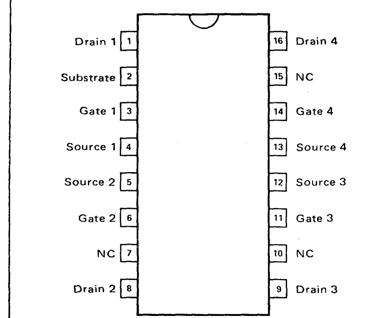
Current summing

SD5200 APPLICATIONS

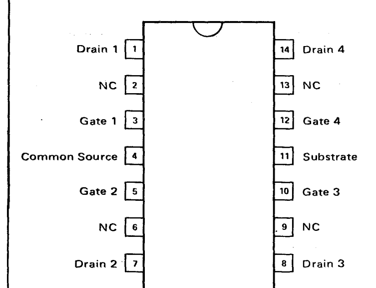
Switch drivers

PIN CONFIGURATION

SD5000, SD5001, SD5200
B PACKAGE

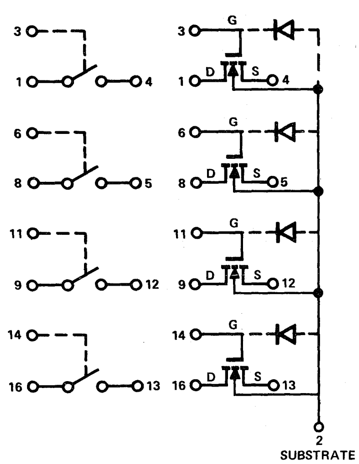


SD5100, SD5101
A PACKAGE

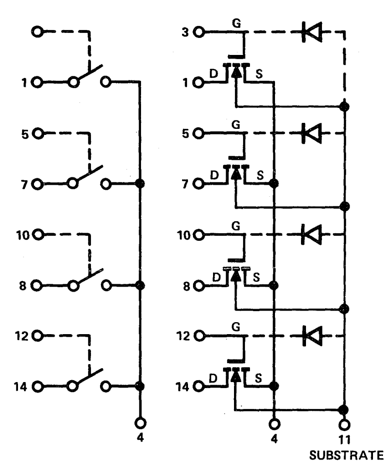


FUNCTIONAL AND SCHEMATIC DIAGRAMS

SD5000, 5001, 5200

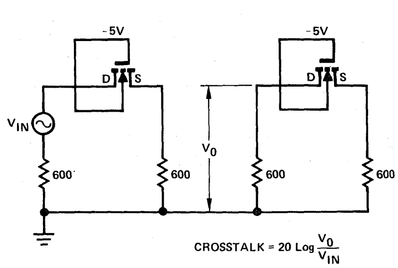


SD5100, 5101



CROSSTALK MEASUREMENT

QUAD SWITCH
(SD5000/SD5001)

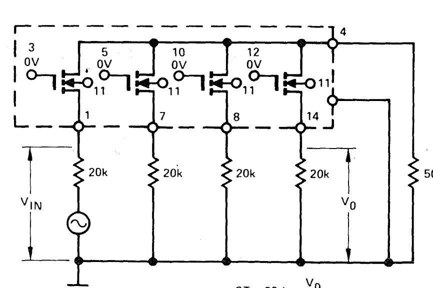


CROSSTALK = 20 Log $\frac{V_0}{V_{IN}}$

WHERE V_{IN} = 1V RMS AT 3kHz

TEST CIRCUIT NO. 1

MULTIPLEXER
(SD5100/SD5101)



CT = 20 Log $\frac{V_0}{V_{IN}}$

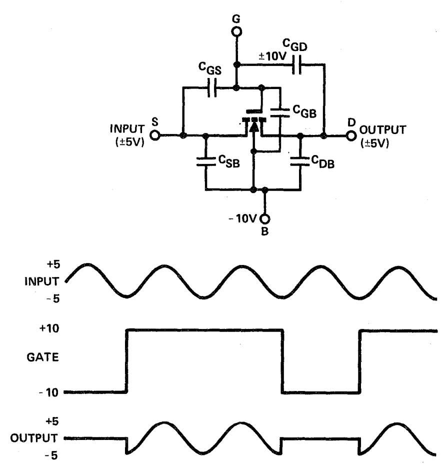
WHERE V_{IN} = 1V RMS AT 3kHz

TEST CIRCUIT NO. 2

THEORY OF OPERATION

The SD 5000 series consists of four SPST switches with analog signal capability of up to ±10 volts for the SD5000 and up to ±5 volts for the SD5001. Each switch of the array is a D-MOS N-channel field-effect transistor of the enhancement-mode type; that is, the device is normally off when gate-to-source voltage (V_{GS}) is zero volts. When V_{GS} exceeds the threshold voltage V_T the FET switch starts to turn on. With V_{GS} in excess of +10 volts, a low resistance path (typically 30Ω) exists between input and output of the switch. Figure 1 below shows the normal mode of operation of a single switch of the array for ±5 volt analog signal processing. Note that the source is recommended for the input since feedback or reverse transfer capacitance is lower when drain is used as the output. In this case, the switch is driven by ±10 volts for which the SD5200 could be used as discussed later.

FIGURE 1



When analog signals are routed from one point to another the important factor are **isolation, cross-talk** between switches, **feedthrough** and **feedback transients, insertion loss** and **speed** of operation. The SD5000 series offers superior performance in all these areas.

Isolation. ON resistance is typically 30Ω and OFF resistance is typically 10^{10}Ω, which means the OFF to ON resistance ratio is in excess of 10^9. Isolation from output to input from 3kHz analog signals is -107dB.

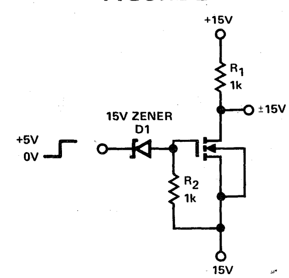
Feedback and feedthrough transients. These are kept to a minimum because of the very low feedback and feedthrough capacitances. This means that "glitchless" or "clean" signals appear at the output.

Insertion loss. This depends upon the source and load impedances involved. As an example for 600Ω source impedance the insertion loss for voice signal (1V RMS at 3kHz) is less than 0.3dB. This indicates that the SD5000 series would make good telephone cross-point switches.

Speed. Because of the low ON resistance and low input capacitance the SD5000 switches turn on at sub-nano-second speeds. They are also capable of handling very high frequency analog signals and still maintain excellent isolation (20-30dB at 1GHz).

The SD5200 is intended as a driver for the SD5000/5001 but is capable of driving any system which requires ±15 volts. Four drivers are in each package and Figure 2 shows how a single driver is biased for ±15 volts. Two external resistors R_1, R_2 and a zener diode D_1 are required per driver. The input is 5V open collector TTL.

FIGURE 2



The SD5100 series is four channel multiplexers. the SD5100 has 0-30 volts input voltage capability and the SD5101 has 0-15 volts input voltage capability. Each circuit has a common source. The signals at the source are limited to ±200mV and therefore these circuits are used where switching is performed at the virtual ground point of an op amp. In this case, no external driver is required nor are any additional power supplies required. Because the ON resistance of both the SD5000 and SD5001 is very low (30Ω typ) and matched within 5Ω, the need for a compensating FET is minimized and in some cases eliminated. The parts can be driven directly from TTL, either +5 volts or +15 volts open collector.

ANALOG SWITCH/DRIVER APPLICATION

The SD5200 operates as an inverting switch capable of driving 30 volts maximum. This wide range capability with high speed fulfills most analog switching applications. Figure 3 demonstrates how the SD5200 drives the SD5000 in a typical analog switching application.

ANALOG MULTIPLEXER APPLICATION

The SD5100 series is easy to use as shown in Figure 4. Driver circuitry can be TTL or if very low R_{ON} is required (19Ω typ), then TTL open collector logic can drive the SD5100 up to +20 volts. The common source is kept at or near ground and each drain will withstand +30 volts with isolation typically 120dB.

If a compensation transistor is required in series with R_2, then the maximum mismatch error for $R_1 = R_2 = 10k\Omega$ would be:

$$\text{Error} = \frac{R_2 + 65\Omega}{R_1 + 70\Omega} = .05\%$$

Without the compensation transistor the error would be:

$$\text{error} = \frac{R_2}{R_1 + 70\Omega} = .7\%$$

ANALOG

FIGURE 3

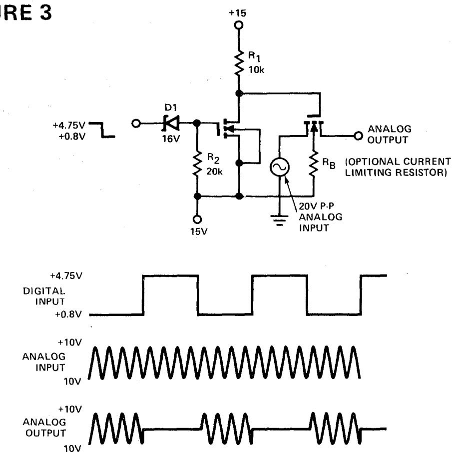
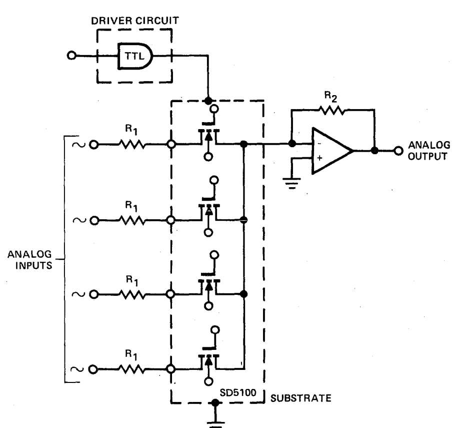


FIGURE 4

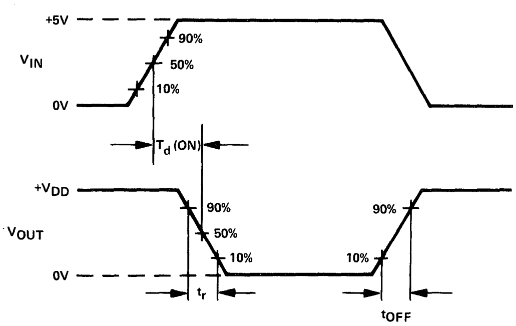


SWITCHING CHARACTERISTICS

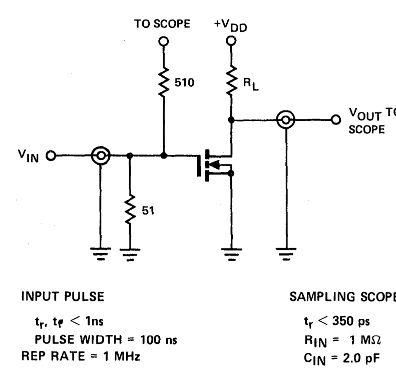
		t_d (ON) (ns)		t_r (ns)		t_{OFF} (ns)	
V_{DD}	R_L	TYP	MAX	TYP	MAX	TYP	MAX
5	680	0.6	1.0	0.7	1.0	9.0	*
10	680	0.7		0.8		9.0	
15	1k	0.9		1.0		14.0	

*t_{OFF} is dependent on R_L and C_L and does not depend on the device characteristics.

SWITCHING WAVEFORMS

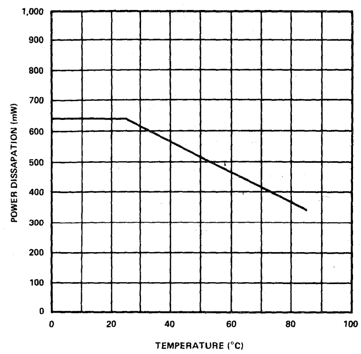


TEST CIRCUIT

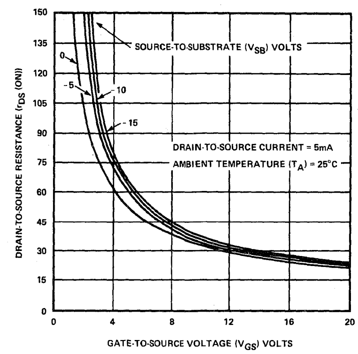


CHARACTERISTIC CURVES

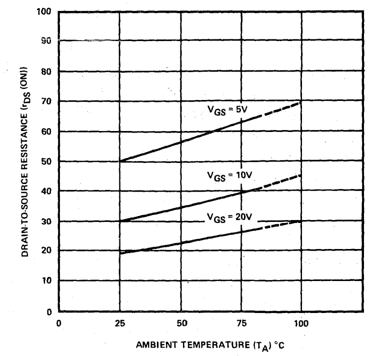
MAXIMUM POWER DISSIPATION VS TEMPERATURE



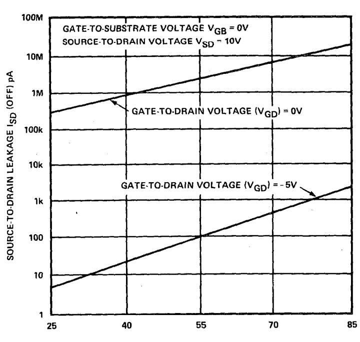
DRAIN-TO-SOURCE RESISTANCE VS SOURCE-TO-SUBSTRATE AND GATE-TO-SOURCE VOLTAGE



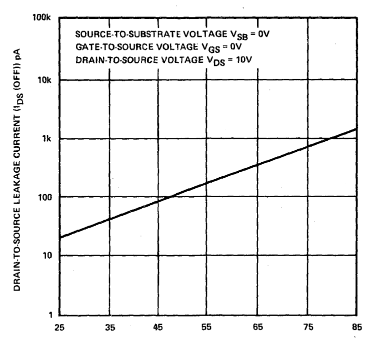
DRAIN-TO-SOURCE RESISTANCE VS TEMPERATURE



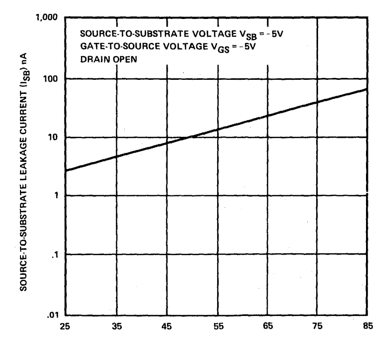
SOURCE-TO-DRAIN LEAKAGE CURRENT VS TEMPERATURE



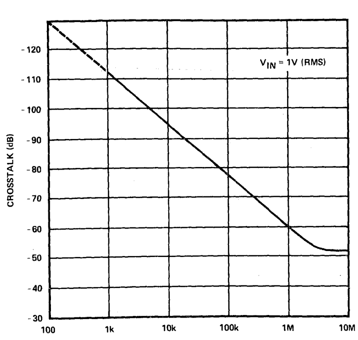
DRAIN-TO-SOURCE LEAKAGE CURRENT VS TEMPERATURE



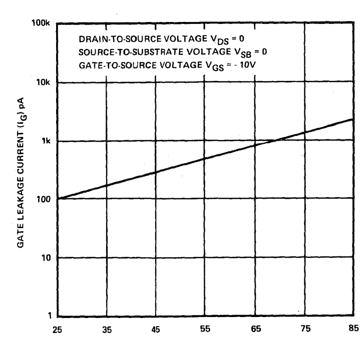
SOURCE-TO-SUBSTRATE LEAKAGE CURRENT VS TEMPERATURE



CROSSTALK VS FREQUENCY



GATE LEAKAGE CURRENT VS TEMPERATURE



ANALOG

SD6000-V

GENERAL FEATURES

- Positive bias only
- Low gate voltages
- Enhancement mode operation
- Zener diode gate protection
- Ion implanted for greater reliability

FEATURES (RF AMP Section)

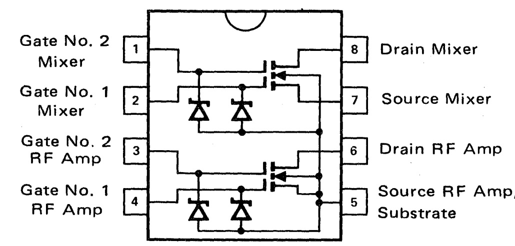
- High power gain without neutralization—25dB at 100MHz
- Low noise figure—2.5dB at 100MHz
- Low input and output capacitances constant with AGC—3.0pF and 1.0pF
- Low feedback capacitance—0.025pF
- Superior cross modulation performance
- High transconductance—15mmhos
- Wide AGC range—50dB at 100MHz

FEATURES (Mixer Section)

- High conversion gain—17dB at 100MHz with VG1S = VG2S for biasing simplicity
- Excellent isolation from gate no. 1 (RF) to gate no. 2 (LO)
- Low input capacitance—4.0pF
- Low feedback capacitance—0.03pF
- Excellent cross modulation performance and low noise operation
- High conversion transconductance at low drain currents—10mmhos

PIN CONFIGURATION

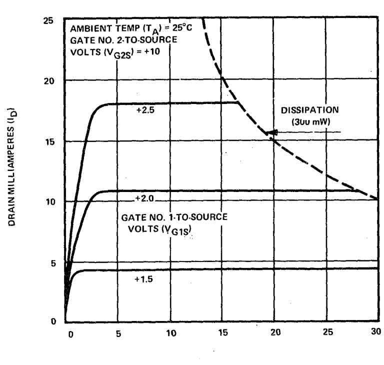
V PACKAGE



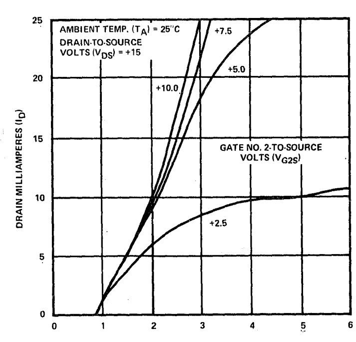
CHARACTERISTIC CURVES

RF AMP SECTION

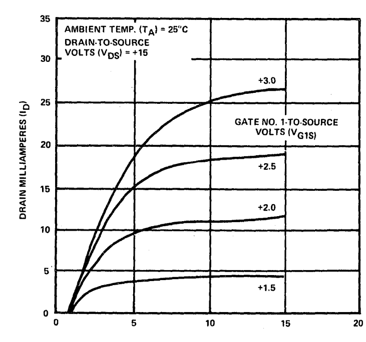
DRAIN CURRENT VS DRAIN-TO-SOURCE VOLTAGE



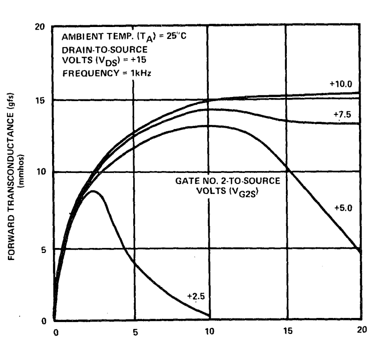
DRAIN CURRENT VS GATE NO. 1-TO-SOURCE VOLTAGE



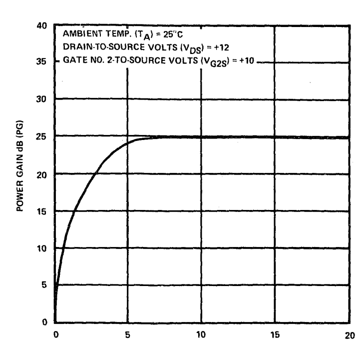
DRAIN CURRENT VS GATE NO. 2-TO-SOURCE VOLTAGE



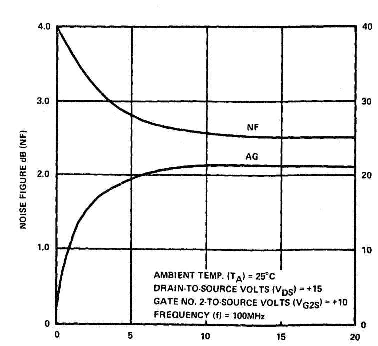
1kHz FORWARD TRANSCONDUCTANCE VS DRAIN CURRENT



POWER GAIN VS DRAIN CURRENT

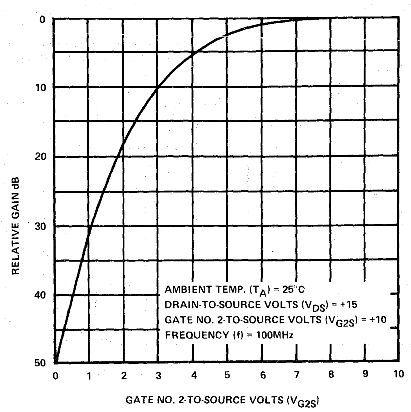


NOISE FIGURE AND AVAILABLE GAIN VS DRAIN CURRENT

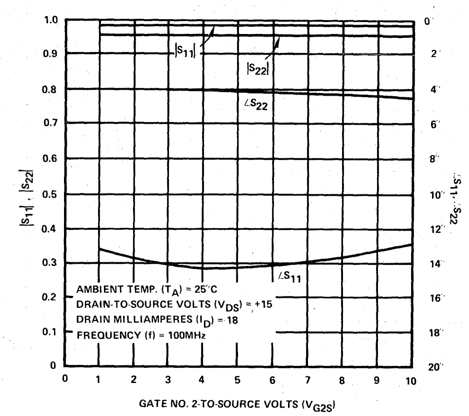


CHARACTERISTIC CURVES (Continued)

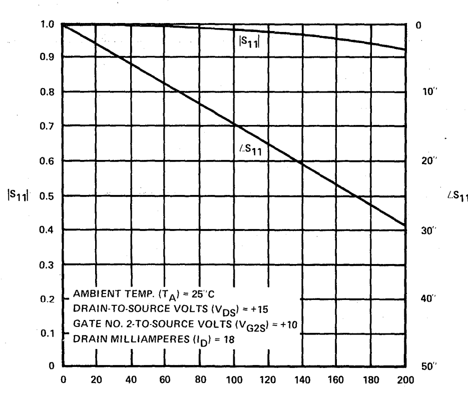
AUTOMATIC GAIN CONTROL RANGE



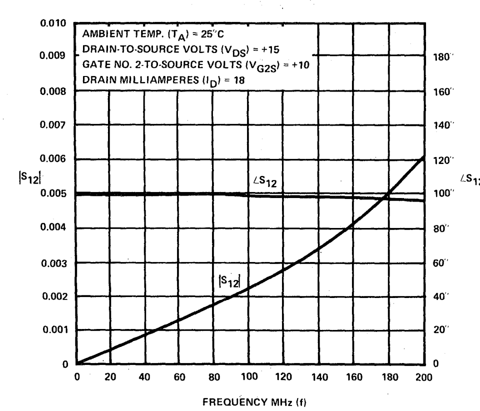
S11 AND S22 VS GATE NO. 2-TO-SOURCE VOLTAGE



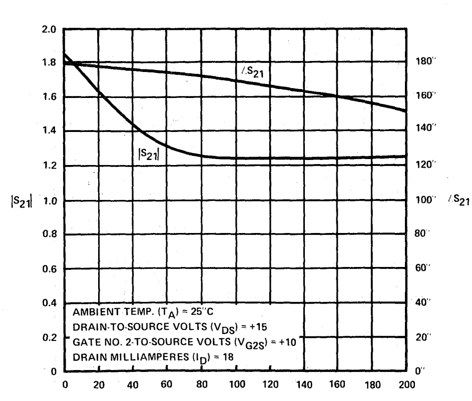
S11 VS FREQUENCY



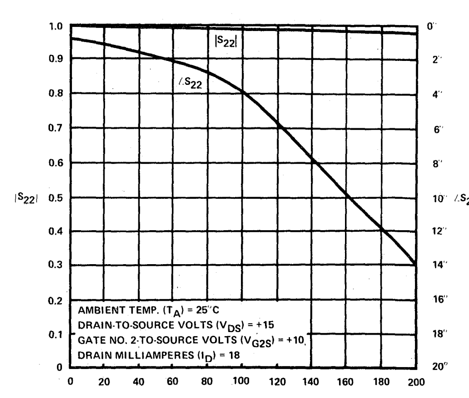
S12 VS FREQUENCY



S21 VS FREQUENCY



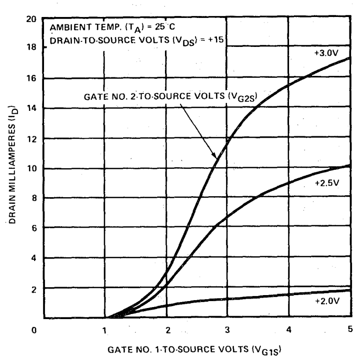
S22 VS FREQUENCY



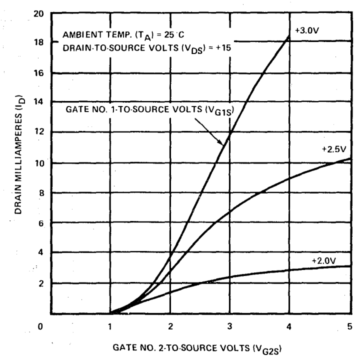
CHARACTERISTIC CURVES (Continued)

MIXER SECTION

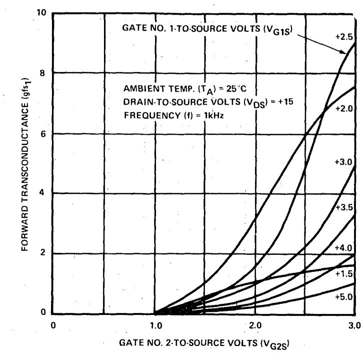
DRAIN CURRENT VS GATE NO. 1-TO-SOURCE VOLTAGE



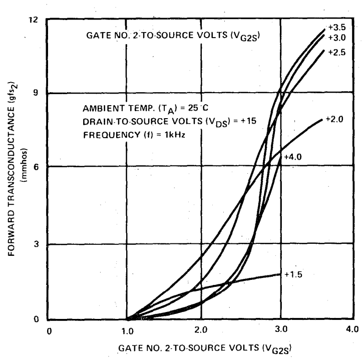
DRAIN CURRENT VS GATE NO. 2-TO-SOURCE VOLTAGE



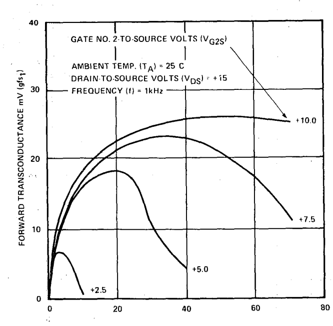
GATE NO. 1 FORWARD TRANSCONDUCTANCE VS GATE NO. 2-TO-SOURCE VOLTAGE



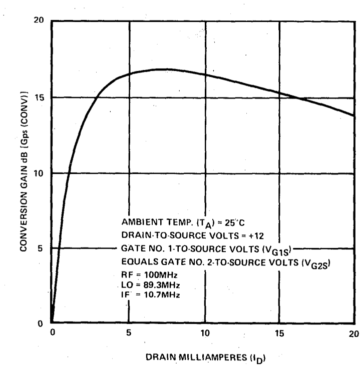
GATE NO. 2 FORWARD TRANSCONDUCTANCE VS GATE NO. 1-TO-SOURCE VOLTAGE



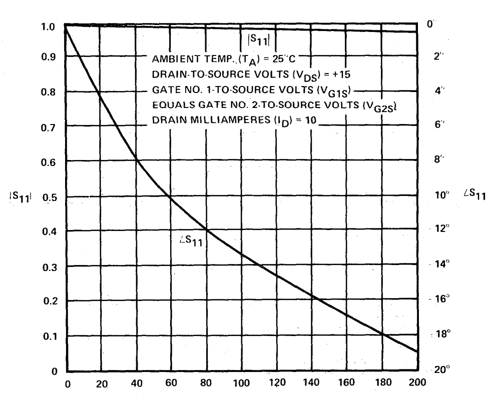
GATE NO. 1 FORWARD TRANSCONDUCTANCE VS DRAIN CURRENT



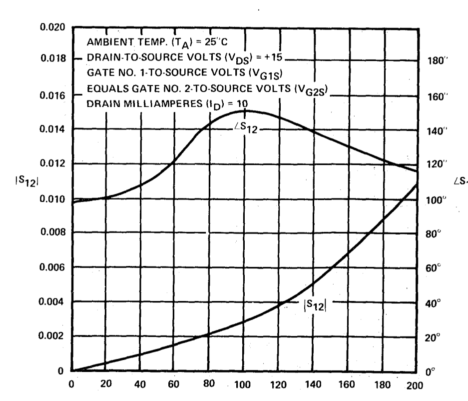
CONVERSION GAIN VS DRAIN CURRENT



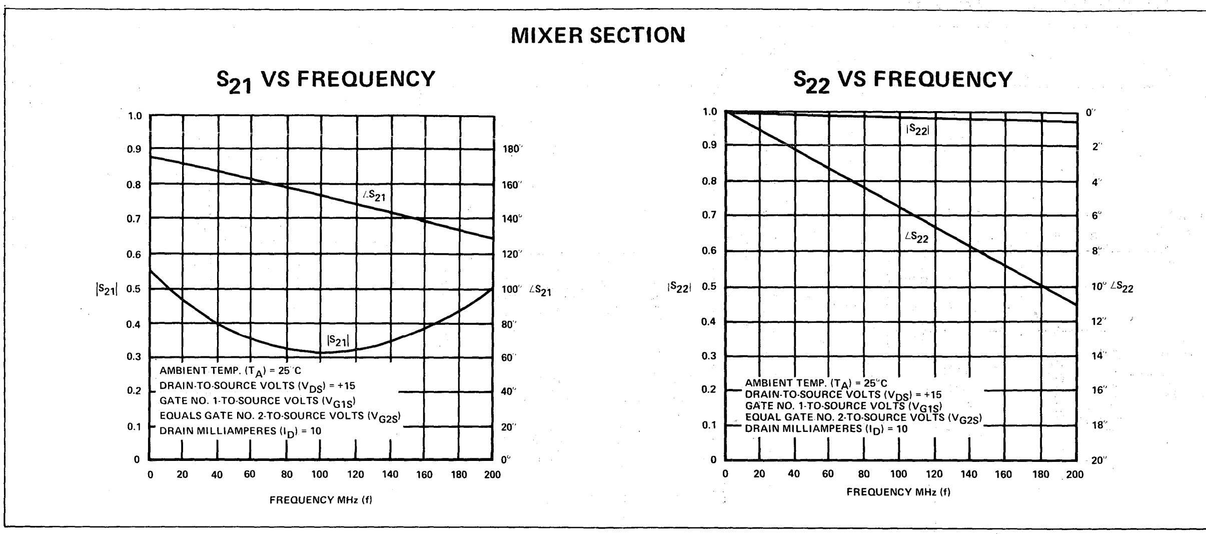
S_{11} VS FREQUENCY



S_{12} VS FREQUENCY

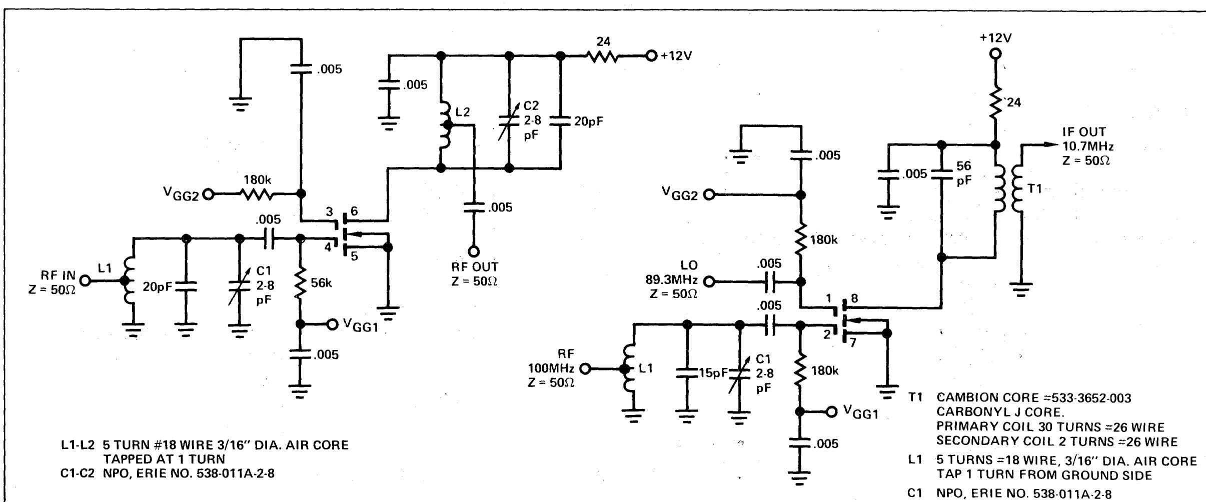


CHARACTERISTIC CURVES



RF AMP SECTION TEST CIRCUIT

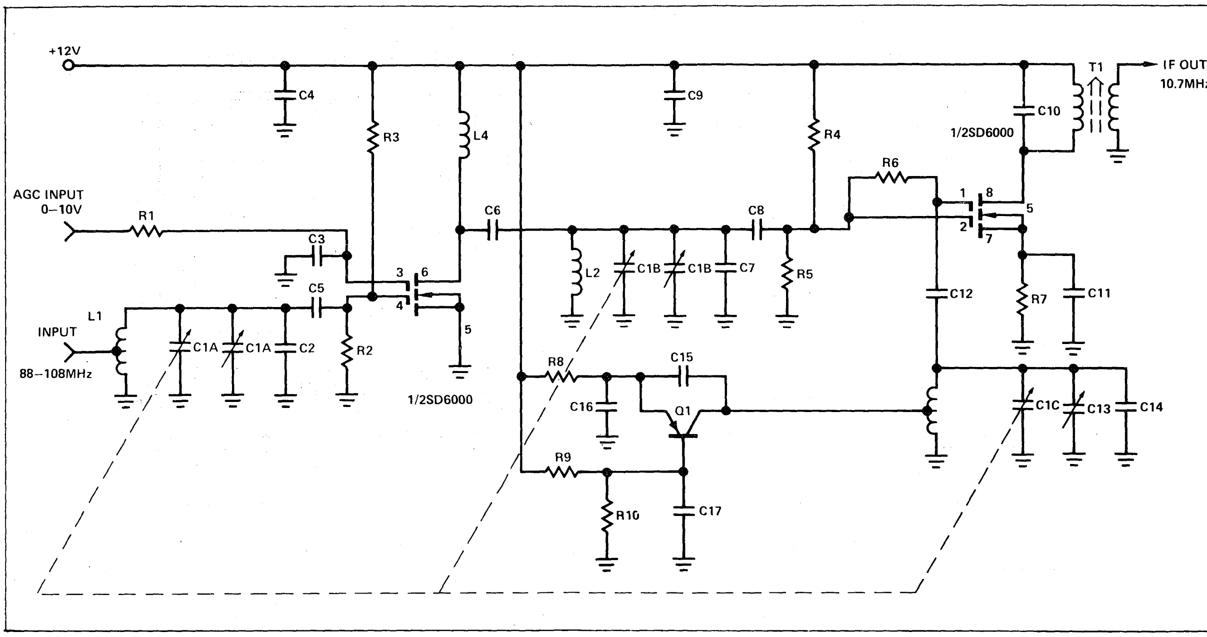
MIXER SECTION TEST CIRCUIT



FM TUNER USING SD6000 ELECTRICAL DATA

PARAMETER	TEST CONDITIONS	TYP
Supply Voltage		+12V
Supply Current	AGC voltage +10V	25mA
Frequency Range		88MHz to 108MHz
Bandwidth	RF Amp (−3dB) Mixer (−3dB)	2.5MHz 300kHz
Input Impedance		75Ω
Output Impedance		50Ω
IF Output Frequency		10.7MHz
Oscillator Stability w/respect to Supply Voltage		40kHz/volt
Oscillator Stability w/respect to Temperature		10kHz/°C
Power Gain	88MHz to 108MHz	30dB Min
Noise Figure	@ 100MHz	3.0dB Max

FM TUNER USING SD6000



PARTS LIST

1. Transistors

	Description	Type
Q1	PNP Silicon	2N4126

2. Integrated Circuits

U1	Dual D-MOS FET	SD6000V

3. Resistors (All carbon resistors in ohms ±10% tolerance.)

	Value
R1	30k
R2	68k
R3	200k
R4	150k
R5	39k
R6	82k
R7	120
R8	6800
R9	13k
R10	3k

4. Capacitors

	Value	Type
C1	5-20pF	3 Gang Tuning Capacitor
C2	20pF	±5% NPO
C3, 4, 5, 6, 8 9, 11, 12, 17	.005	+80% - 20% Ceramic
C7	10pF	±5% NPO
C10	56pF	±5% MICA or Ceramic
C13	2-8pF	Trimmer
C14	12pF	±5% NPO
C15	10pF	±5% NPO
C16	10pF	±5% NPO

5. Miscellaneous Components

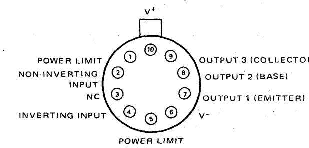
T1	IF Transformer	Cambion 533-3652-003 Jcore Prim. 30T #26 Sec. 2T #26
L1	RF Input Coil	4 turns #18 on 3/16" dia. Air core — Tap 1 Turn from ground side.
L2	RF Output Coil	4 turns #18 on 3/16" dia. air core.
L3	Oscillator Coil	4 turns #18 on 3/16" dia. air core center-tapped.
L4		33μh RF choke

FEATURES

- INTERNAL CURRENT LIMITING
- LOW STANDBY CURRENT
- HIGH OUTPUT CURRENT CAPABILITY
- WIDE POWER BANDWIDTH
- LOW DISTORTION

PIN CONFIGURATION

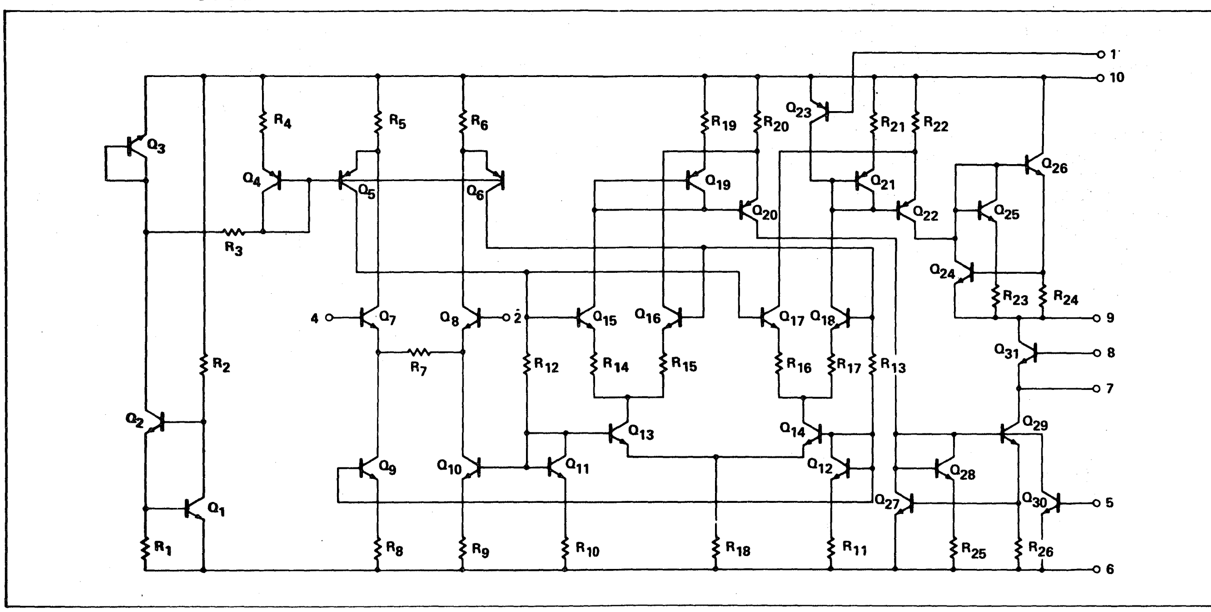
L PACKAGE



ABSOLUTE MAXIMUM RATINGS

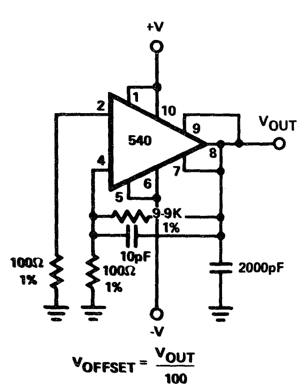
Supply Voltage	±27 Volts SE540
	±22 Volts NE540
Operating Temperature Range	−55°C to +125°C SE540
	0°C to +70°C NE540
Storage Temperature Range	−65°C to +150°C
Output Short Circuit Duration (Not exceeding maximum dissipation.)	Indefinite

SCHEMATIC DIAGRAM

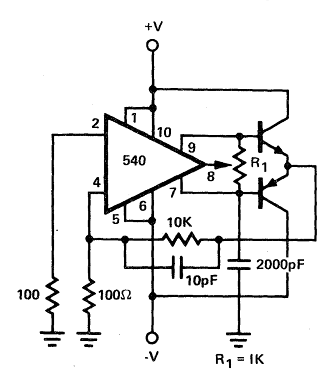


TEST CIRCUITS

OFFSET VOLTAGE MEASUREMENT



OUTPUT BIAS CONTROL

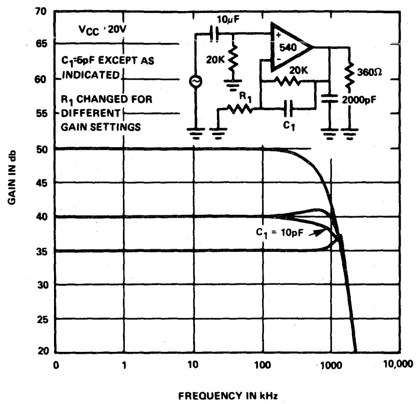


ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified)

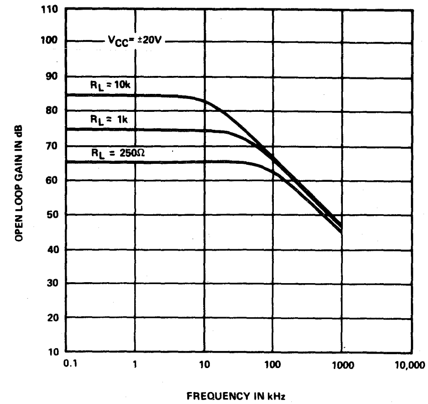
PARAMETER	TEST CONDITIONS	SE 540 MIN	SE 540 TYP	SE 540 MAX	NE540 MIN	NE540 TYP	NE540 MAX	UNIT
Operating Temperature Range		−55		+125	0		+70	°C
Operating Supply Voltage		±5		±25	±5		±20	Volts
Quiescent Current			13	20		13	20	mA
Input Offset Voltage			5	7		7	10	mV
Input Offset Current			0.3	0.7		0.5	1	μA
Input Bias Current			1.5	3		2	5	μA
Input Impedance	40 dB Gain		20			20		kΩ
Current Gain		80	100		70	90		dB
Gain Variation Over Temperature Range	40 dB Gain		±0.1			±0.1		dB
Frequency Response	40 dB Gain ±1 dB		500			100		kHz
Distortion	40 dB Gain Output 3 dB below maximum R_L = 600Ω		0.25	0.5		0.5	1.0	%
	R_L = 2KΩ		0.06			0.06		
Equivalent Input Noise Voltage	R_S = 600Ω 50 Hz to 500 kHz		10			10		μV
Power Supply Rejection Ratio	40 dB Gain	80	90		60	80		dB
Common Mode Rejection Ratio			110			90		dB
Output Drive Current		±120	±150		±80	±100		mA
Slew Rate	V_S = ±20V V_{OUT} = ±15V		200			200		V/μs

TYPICAL PERFORMANCE CHARACTERISTICS

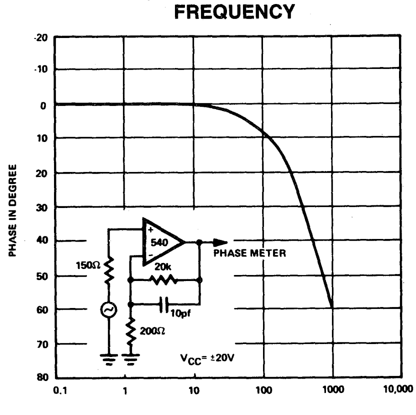
CLOSED LOOP FREQUENCY RESPONSE



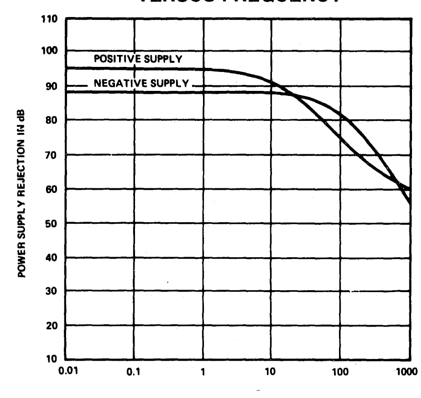
OPEN LOOP GAIN AND FREQUENCY RESPONSE



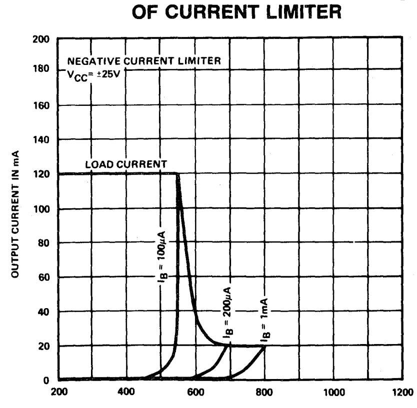
PHASE RESPONSE VERSUS FREQUENCY



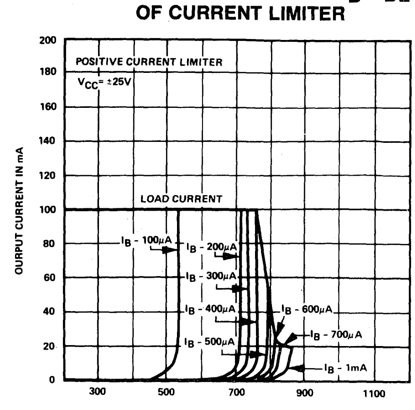
POWER SUPPLY REJECTION VERSUS FREQUENCY



OUTPUT CURRENT VERSUS I_B/V_{BE} OF CURRENT LIMITER

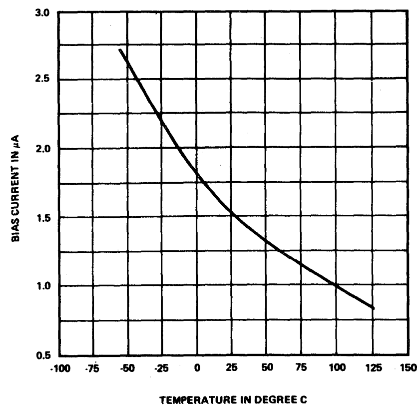


OUTPUT CURRENT VERSUS I_B/V_{BE} OF CURRENT LIMITER

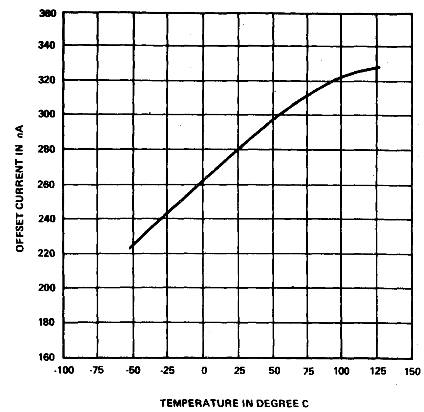


TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

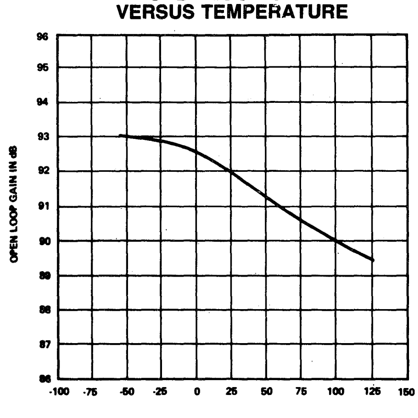
BIAS CURRENT VERSUS TEMPERATURE



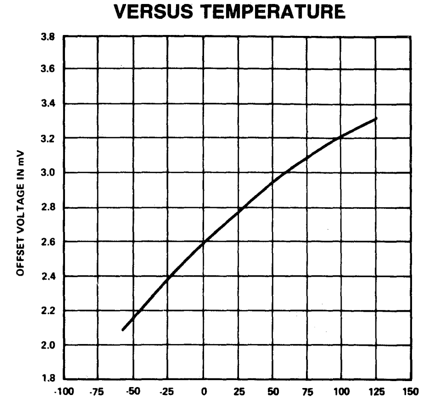
OFFSET CURRENT VERSUS TEMPERATURE



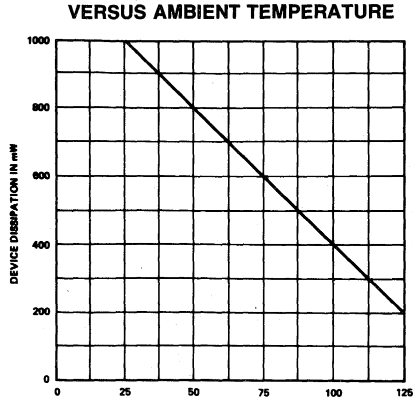
OPEN LOOP GAIN VERSUS TEMPERATURE



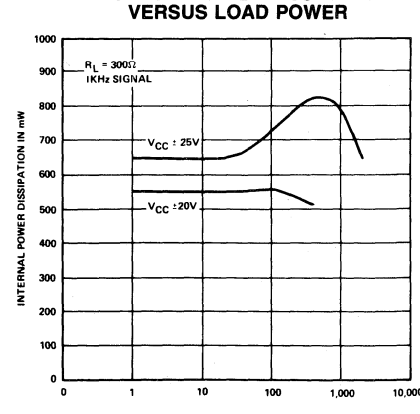
OFFSET VOLTAGE VERSUS TEMPERATURE



MAXIMUM DISSIPATION VERSUS AMBIENT TEMPERATURE

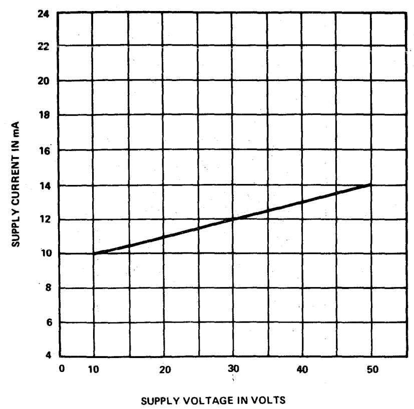


INTERNAL POWER DISSIPATION VERSUS LOAD POWER

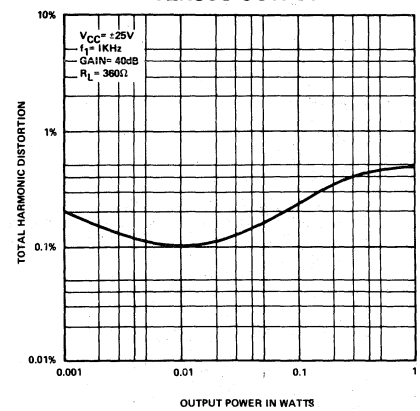


TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

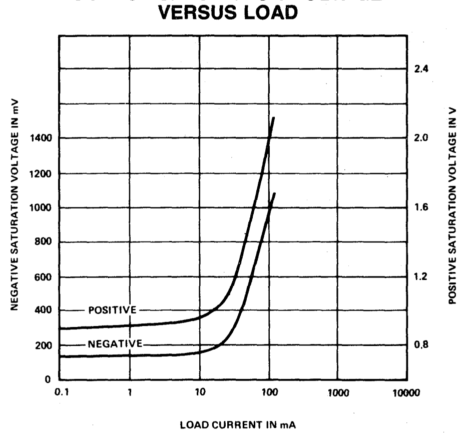
QUIESCENT CURRENT VERSUS SUPPLY VOLTAGE



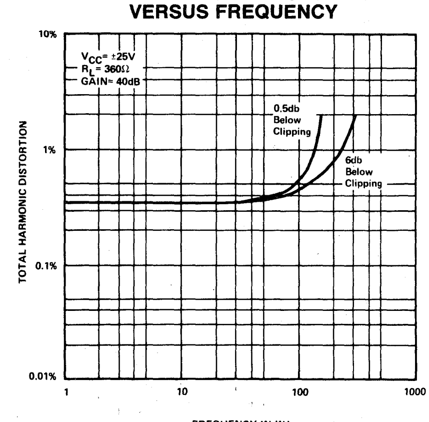
TOTAL HARMONIC DISTORTION VERSUS OUTPUT



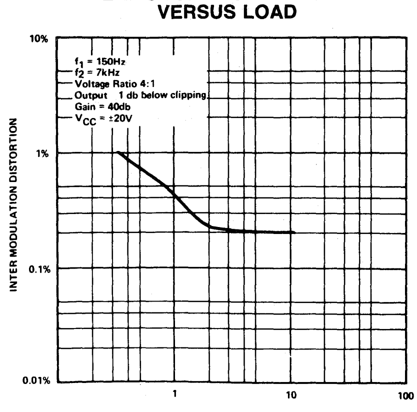
OUTPUT SATURATION VOLTAGE VERSUS LOAD



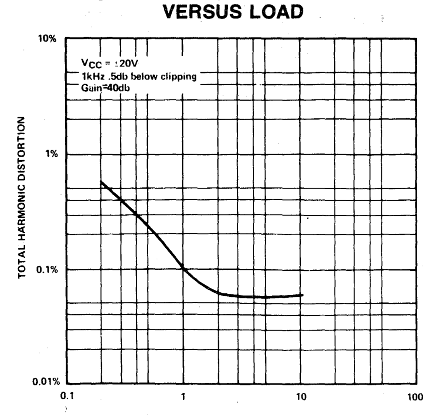
TOTAL HARMONIC DISTORTION VERSUS FREQUENCY



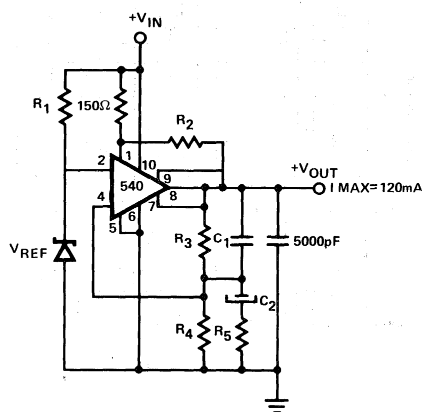
INTERMODULATION DISTORTION VERSUS LOAD

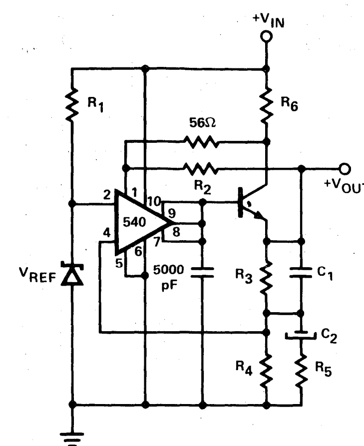


TOTAL HARMONIC DISTORTION VERSUS LOAD



NEGATIVE VOLTAGE REGULATORS

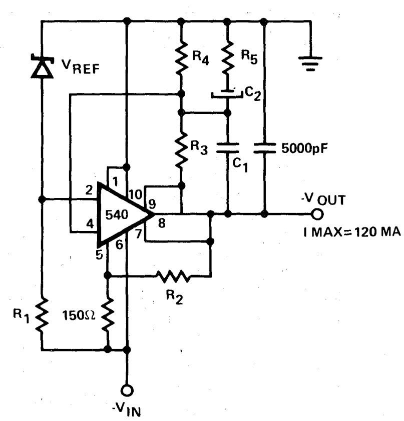


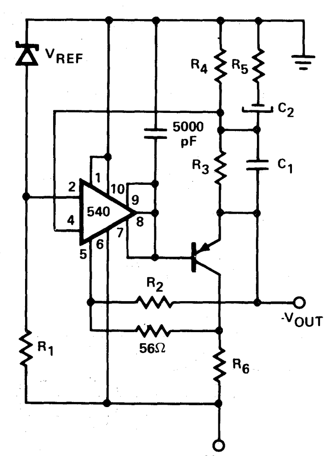


$V_{OUT} \simeq \frac{R_3 + R_4}{R_4} V_{REF}$ $\quad R_5 \simeq \frac{R_3}{100}$

$R_1 \simeq \frac{V_{IN} \cdot V_{REF}}{I_{ZENER}}$ $\quad C_1 \simeq \frac{0.2}{R_3}\ \mu F$

$R_2 \simeq \frac{2\ V_{IN} \cdot V_{OUT}}{4mA}$ $\quad C_2 \simeq 10 \mu F$





$V_{OUT} \simeq \frac{R_3 + R_4}{R_4} V_{REF}$ $\quad R_5 \simeq \frac{R_3}{100}$

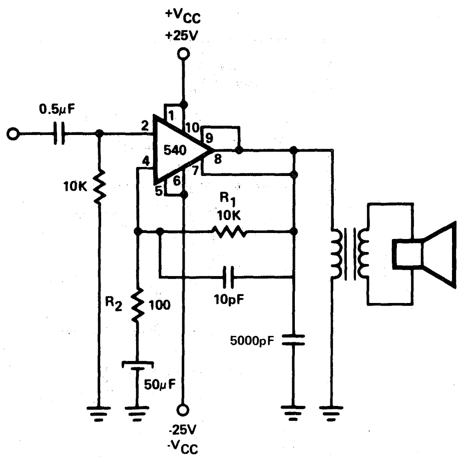
$R_1 \simeq \frac{V_{IN} \cdot V_{REF}}{I_{ZENER}}$ $\quad C_1 \simeq \frac{0.2}{R_3}\ \mu F$

$R_2 \simeq \frac{2\ V_{IN} \cdot V_{OUT}}{4mA}$ $\quad C_2 \simeq 10 \mu F$

TYPICAL APPLICATIONS

POWER AMPLIFIERS

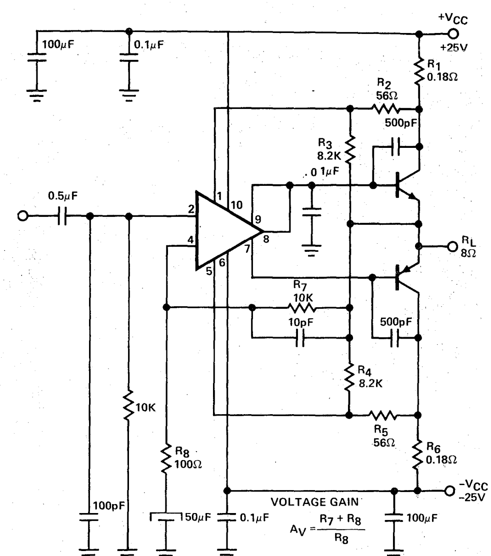
1 Watt



VOLTAGE GAIN

$A_V \simeq \frac{R_1 + R_2}{R_2}$

35 Watts



VOLTAGE GAIN

$A_V = \frac{R_7 + R_8}{R_8}$

CURRENT LIMITING

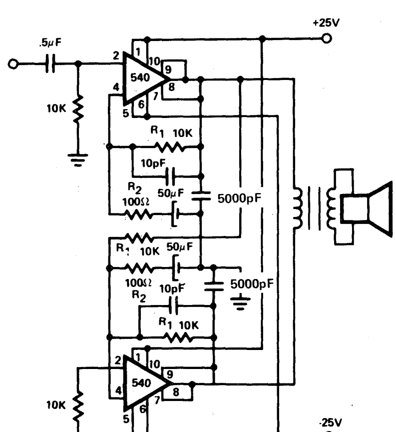
$R_1 = R_6 \simeq \frac{650mV}{I_{peak}}$

POWER LIMITING

$R_2 = R_5 \simeq 56\Omega$

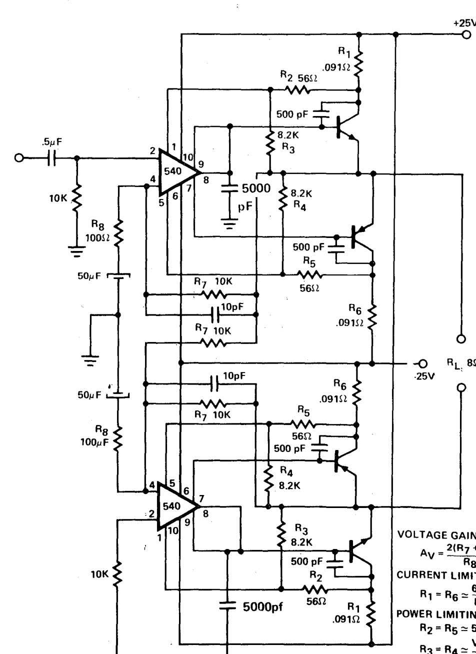
$R_3 = R_4 \simeq \frac{V_{CC}}{3mA}$

3 Watts



$A_V = \frac{Z(R_1+R_2)}{R_2}$

70 Watts



VOLTAGE GAIN

$A_V = \frac{2(R_7 + R_8)}{R_8}$

CURRENT LIMITING

$R_1 = R_6 \simeq \frac{650mV}{I_{peak}}$

POWER LIMITING

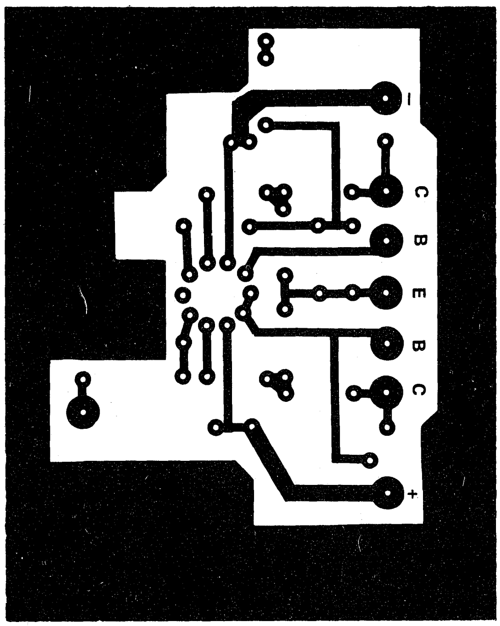
$R_2 = R_5 \simeq 56\Omega$

$R_3 = R_4 \simeq \frac{V_{CC}}{3mA}$

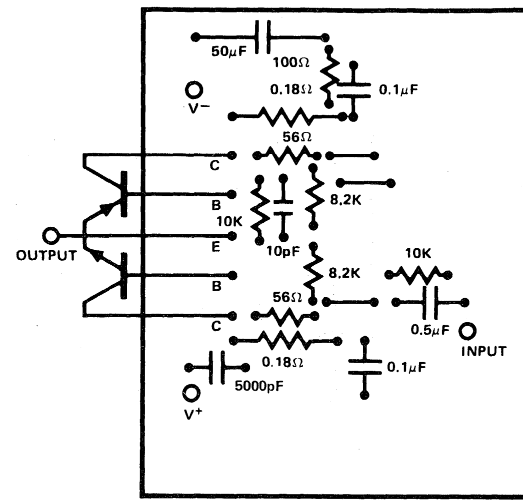
ANALOG

35 WATT AMPLIFIER

P.C. BOARD LAYOUT (BOTTOM VIEW)



PARTS LAYOUT (TOP VIEW)



FEATURES

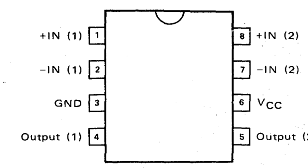
- LOW NOISE—.7μV TOTAL INPUT NOISE
- HIGH GAIN—104dB OPEN LOOP
- SINGLE SUPPLY OPERATION
- WIDE SUPPLY RANGE 9 TO 24V
- POWER SUPPLY REJECTION 110dB
- LARGE OUTPUT VOLTAGE SWING (V_{CC} −2V p-p)
- WIDE BANDWIDTH 15MHz UNITY GAIN
- POWER BANDWIDTH 100kHz (15V p-p)
- INTERNALLY COMPENSATED (STABLE AT 10dB)
- SHORT CIRCUIT PROTECTED
- HIGH SLEW RATE 5V/μs

ABSOLUTE MAXIMUM RATINGS

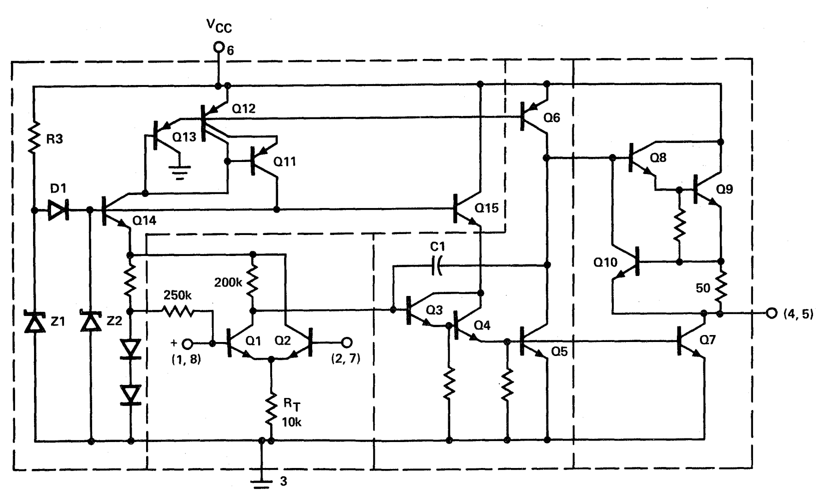
Supply Voltage	+24V
Power Dissipation	500mW
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 sec)	+300°C

PIN CONFIGURATION

V PACKAGE



EQUIVALENT CIRCUIT

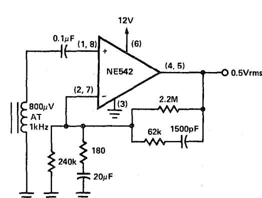


ELECTRICAL CHARACTERISTICS T_A = +25°C, V_{CC} = 14V (Unless Otherwise Noted)

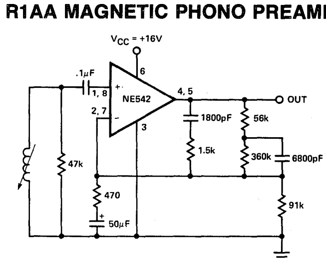
PARAMETER	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Supply Voltage		9		24	V
Supply Current	V_{CC} = 9 to 18V, $R_L = \infty$		9	12	mA
Voltage Gain	Open Loop		160,000		V/V
Input Resistance					
Positive Input			100k		Ω
Negative Input			200k		Ω
Input Current					
Negative Input			.5		μA
Output Resistance	Open Loop		150		Ω
Output Current	Source	8	14		mA
	Sink (Linear Operation)	2	3		mA
Output Voltage Swing		V_{CC} −2.5	V_{CC} − 2		V
Small Signal Bandwidth			15		MHz
Slew Rate			5		V/μs
Power Bandwidth	15V p-p		100		kHz
Maximum Input Voltage	Linear Operation			300	mV rms
Supply Rejection Ratio	f = 60, 120Hz		100		dB
	f = 1kHz		110		dB
Channel Separation	f = 1kHz		70		dB
Total Harmonic Distortion	75dB Gain, f = 1kHz		.1		%
Total Equivalent Input					
Noise	R_S = 600Ω, 100-10,000 Hz		.7	1.2	μV rms
Noise Figure	R_S = 50kΩ, 10-10,000 Hz		1.2		dB
	R_S = 20kΩ, 10-10,000Hz		1.2		dB
	R_S = 10kΩ, 10-10,000Hz		1.5		dB
	R_S = 5kΩ, 10-10,000 Hz.		2.4		dB

TYPICAL APPLICATIONS

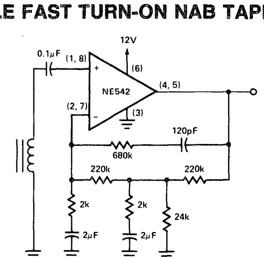
TYPICAL TAPE PLAYBACK AMPLIFIER



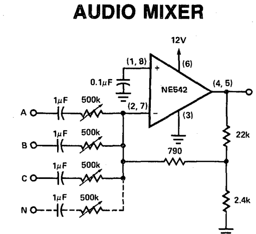
R1AA MAGNETIC PHONO PREAMP



TWO-POLE FAST TURN-ON NAB TAPE PREAMP



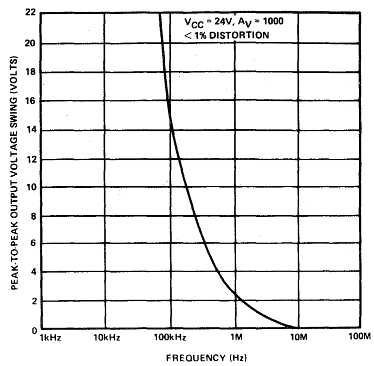
AUDIO MIXER



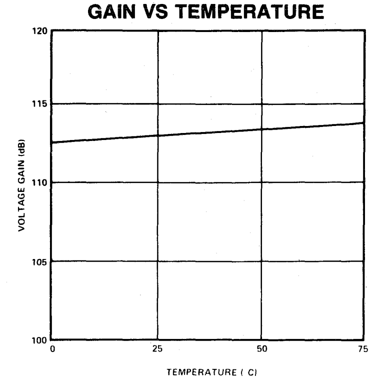
NOTE: ALL RESISTORS VALUES ARE TYPICAL AND IN OHMS.

TYPICAL CHARACTERISTICS

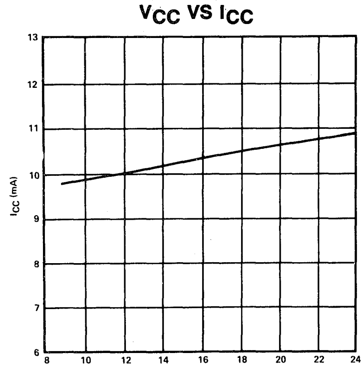
LARGE SIGNAL FREQUENCY RESPONSE



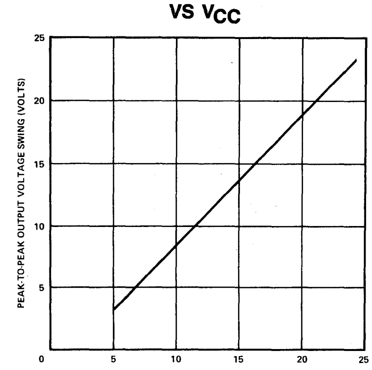
GAIN VS TEMPERATURE



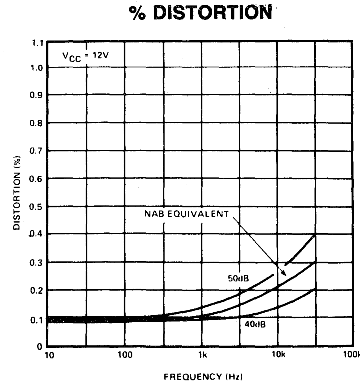
V_{CC} VS I_{CC}



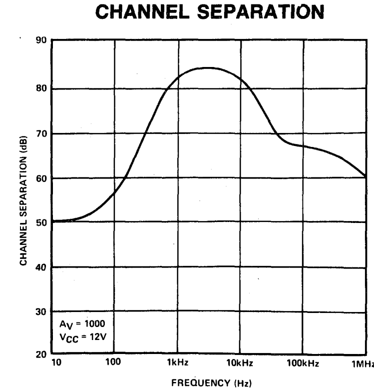
P-P OUTPUT VOLTAGE SWING VS V_{CC}



% DISTORTION

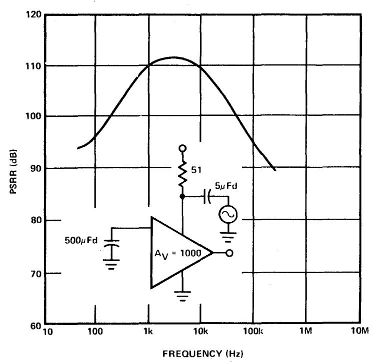


CHANNEL SEPARATION

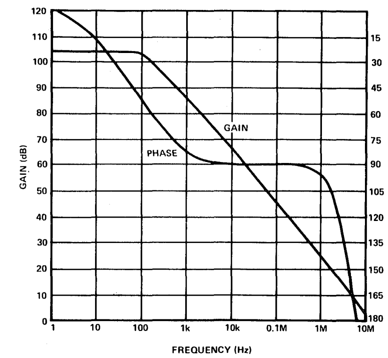


TYPICAL CHARACTERISTICS (Continued)

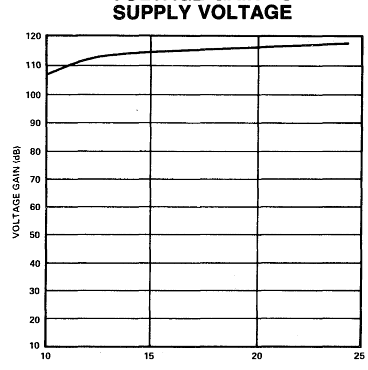
PSRR VS FREQUENCY



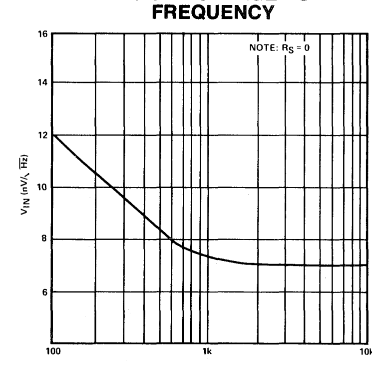
GAIN AND PHASE RESPONSE



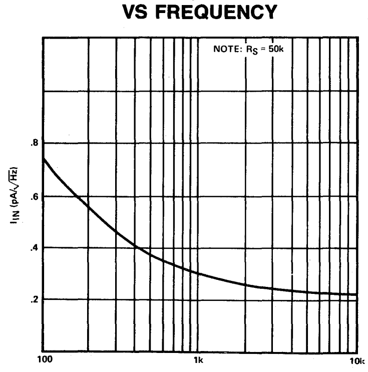
VOLTAGE GAIN VS SUPPLY VOLTAGE



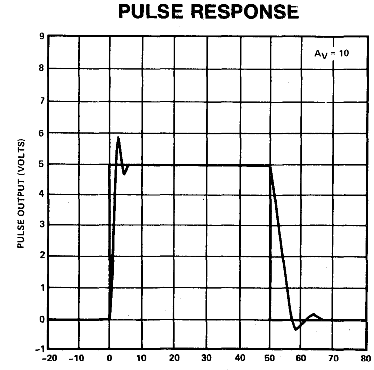
NOISE VOLTAGE VS FREQUENCY



NOISE CURRENT VS FREQUENCY



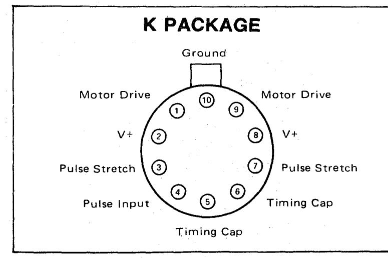
PULSE RESPONSE



FEATURES

- 450mA LOAD CURRENT CAPABILITY WITHOUT EXTERNAL POWER TRANSISTORS
- BIDIRECTIONAL BRIDGE OUTPUT WITH SINGLE POWER SUPPLY
- LOW STANDBY POWER DRAIN

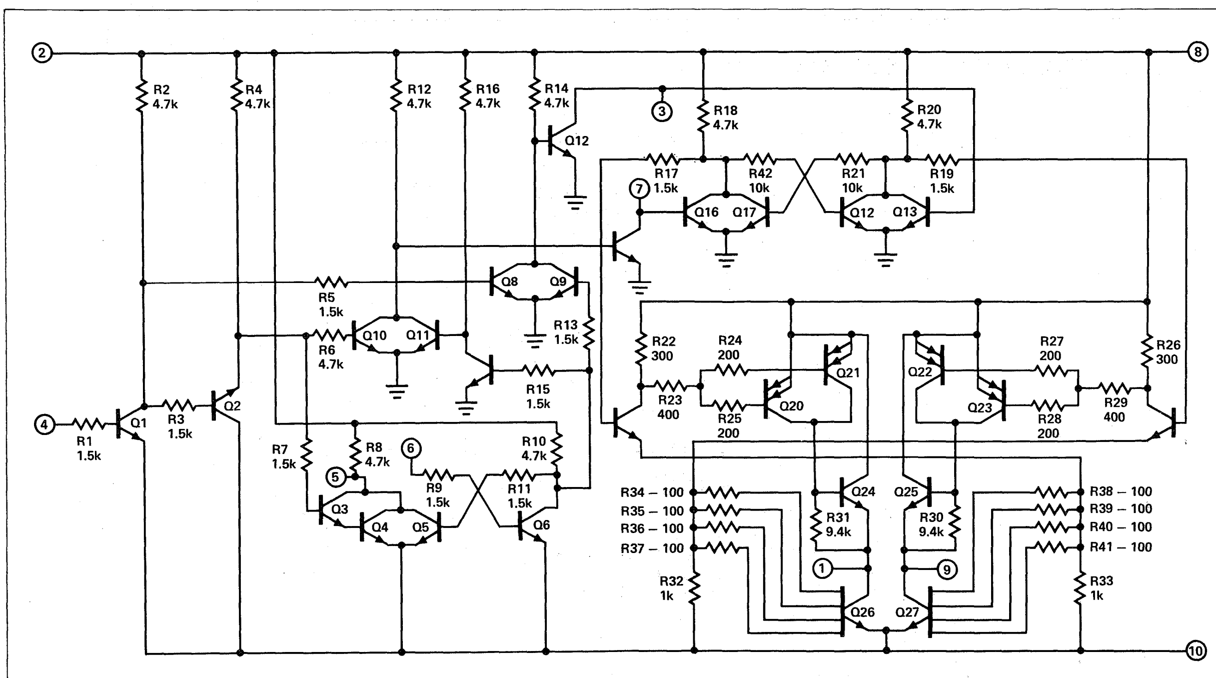
PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

Supply Voltage	6 V
Power Dissipation (T_A = +25°C)	830mw
Output Current (T_A = +25°C)	450 mA

EQUIVALENT CIRCUIT



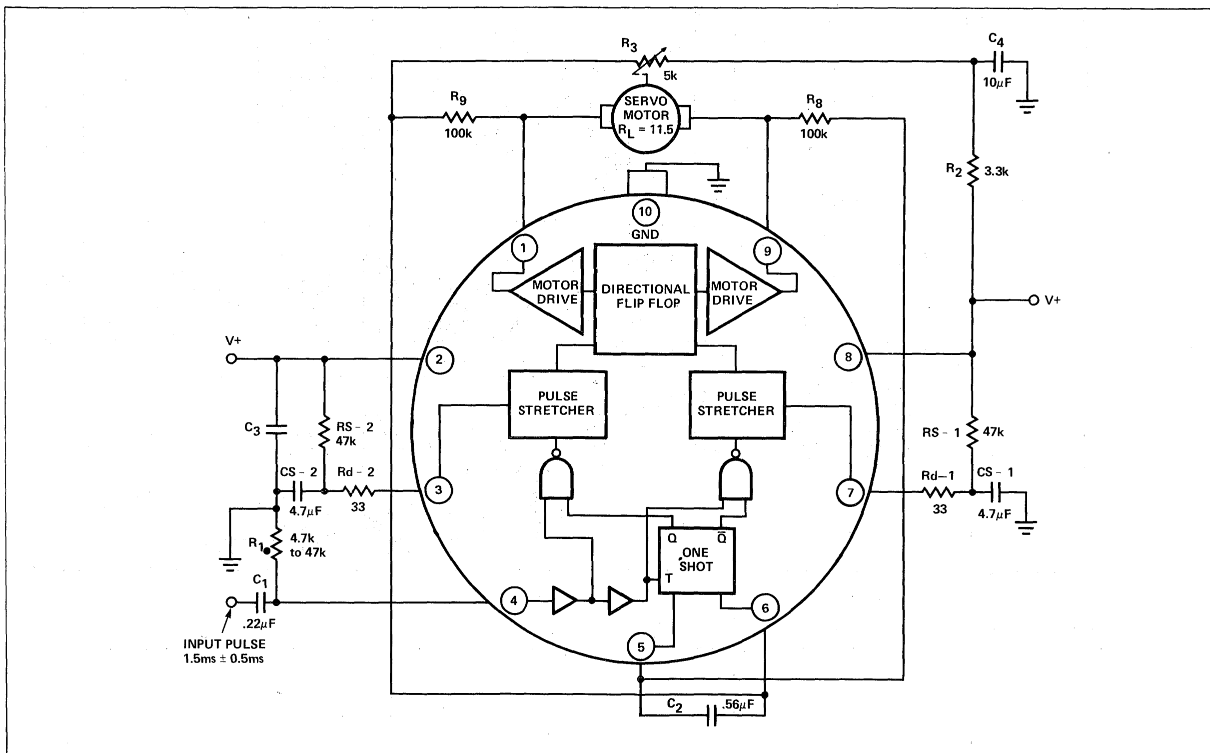
NOTE: ALL RESISTOR VALUES ARE SHOWN IN OHMS.

ANALOG

ELECTRICAL CHARACTERISTICS T_A = +25°C, V+ = 4.8V Unless Otherwise Noted

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage		3.6	4.8	6.0	V
Idle Current			8.0	10.0	mA
Input Bias Current			24	50	μA
Input Impedance	Pin 4 or Pin 6 to Ground	1.9	2.4	2.8	kΩ
Output Voltage	V_S = 4.8V, R_L = 35Ω	3.30	3.75		V
Output Current	V_S = 6.0V, R_L = 11.5Ω	340	385		mA
	V_S = 4.8V, R_L = 11.5Ω	270	280		mA
	V_S = 3.6V, R_L = 11.5Ω	185	200		mA
Output Impedance		4.0	4.8	5.4	ohms
Power Dissipation	Quiescent, R_L = ∞		39	48	mW
	R_L = 11.5Ω		350		mW

BLOCK DIAGRAM AND TYPICAL CONNECTION



NE543 SERVO DRIVER CONNECTION

The servo driver receives a nominal 1.5mS pulse from the receiver-decoder. The length of the input pulse is compared with an internally generated pulse. If the pulse durations differ by more than an allowed amount (the deadband), a pulse derived from the difference is stretched and applied to the output stage. If the input pulse is shorter, the motor is driven so as to reduce the value of R3 and, hence, the internal pulse width. If the input pulse is longer, the motor is driven the other way so that R3 increases and the internal pulse is lengthened. In this way, the control surface position can be made to follow the input pulse. The servo output moves over 100 degrees for pulses between 1 and 2 mS. The pulses occur at 16mS intervals.

The internal pulse generator pulse width is determined by C2 and R2 in series with R3. Capacitor C4 decouples the pulse generator from the supply.

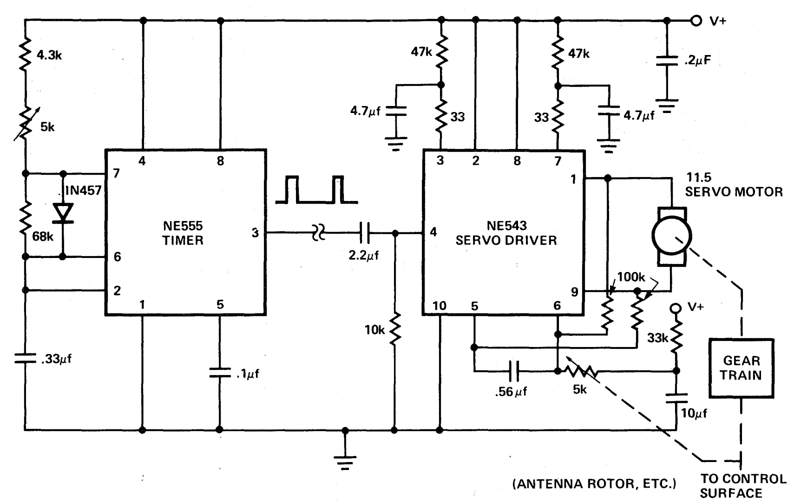
Deadband is controlled by Rd-1 and Rd-2. The 33 ohm resistor sets deadband at about 4-5 microseconds (that is, the circuit will not drive the motor until the input pulse is 4 to 5 microseconds different from the internally generated pulse).

Resistors RS-1 and RS-2 determine the amount of pulse stretching. Capactiors CS-1 and CS-2 are the pulse stretching capacitors. The value is not critical, but if changed RS-1 and RS-2 will have to be changed proportionately.

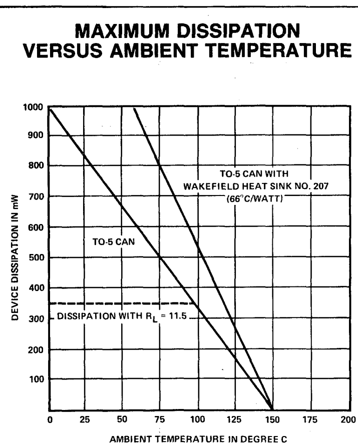
Resistors R8 and R9 are feedback resistors which prevent overshoot by adjusting the closed-loop damping.

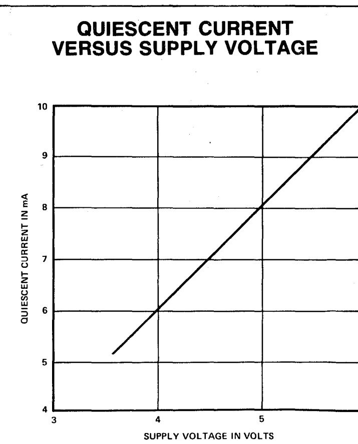
Capacitor C1 is the input coupling capacitor. Resistor R1 can be any value in the range shown, but noise immunity is improved if it is at the low end of the range. Capacitor C3 bypasses the power supply at the device.

TYPICAL APPLICATION



TYPICAL CHARACTERISTICS

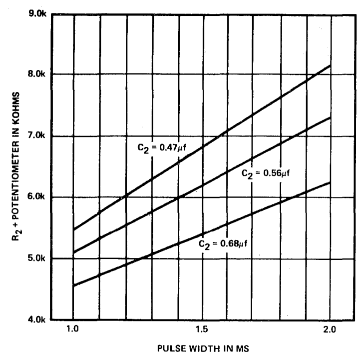




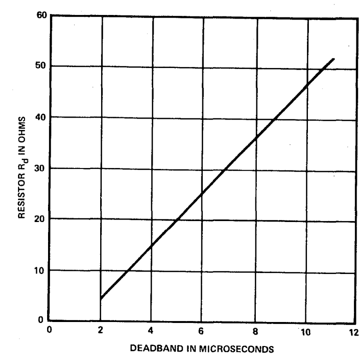
ANALOG

TYPICAL CHARACTERISTICS (Continued)

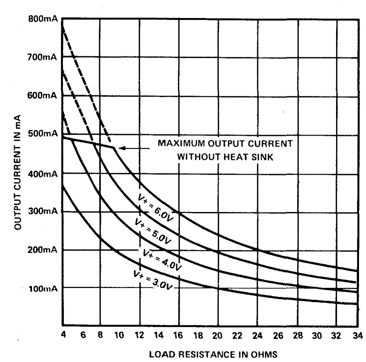
INTERNAL PULSEWIDTH VERSUS R_3 AND C_2



DEADBAND VERSUS RESISTOR R_d



OUTPUT CURRENT VERSUS LOAD RESISTANCE

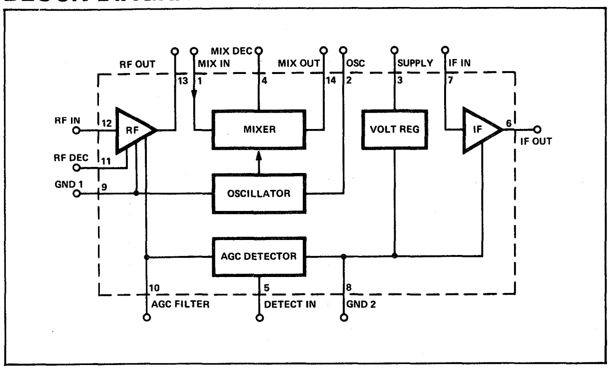


546A

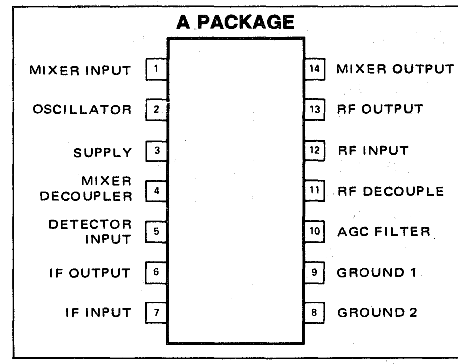
FEATURES

- LOW NOISE
- BUILD IN AGC CIRCUIT
- SEPARATELY ACCESSABLE AMPLIFIERS
- MIXER-OSCILLATOR STAGE WITH INTERNAL FEEDBACK
- HIGH SELECTIVITY
- HIGH IMAGE REJECTION

BLOCK DIAGRAM



PIN CONFIGURATION

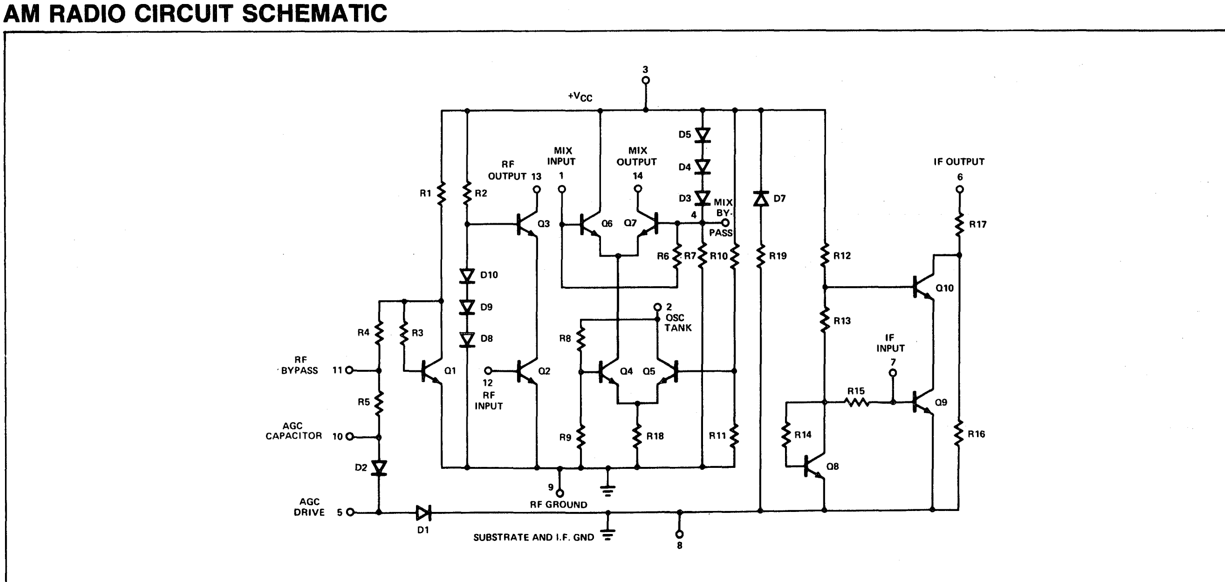


ABSOLUTE MAXIMUM RATINGS

V_{CC} Supply Voltage Pins 3, 13, 14 at Pin 6	16V
DC Supply Voltage (V+)	40V
DC Supply Current	35mA
Internal Power Dissipation (Note 1)	750mW
Lead Temperature	300°C
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C

NOTE
Rating applies for temperatures up to 55°C. Derate linearly at 6.67mW/°C above 55°C.

AM RADIO CIRCUIT SCHEMATIC



ELECTRICAL CHARACTERISTICS (T_A=25°C at V_{CC}=11.0V)

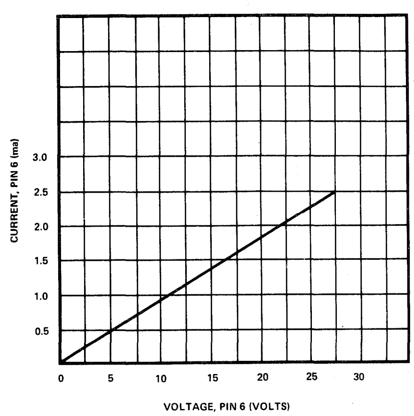
CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
DC Voltage:						
Supply Voltage	$+V_{CC}$		9.0		15.0	
Mixer balance	V_{OS} (V_1-V_4)			1.0	10	mV
Zener voltage	V_3		5.5	6.0	7.0	V
At Terminal 5 AGC voltage	V_5		0.1	0.25	0.4	V
Pin 7 voltage	V_7		0.55	0.70	0.80	V
Pin 12 voltage	V_{12}		0.6	0.71	0.8	V
Pin 13 voltage	V_{13}			4.0		V
DC Current:						
Supply current	I_{CC}		15	18	22	mA
Oscillator current	I_2			1.0		mA
Zener current	I_3		12	14	16	mA
IF current	I_6		3.5	4.3	6	mA
RF current	I_{13}			4.0	5	mA
Mixer current	I_{14}			0.17	0.38	mA
Static:						
I.F. breakdown & linearity	V_6	Apply 5 volts to Pin 6 only. V_{CC}=0 volts. Measure IPin 6	400	500	600	μA
I.F. breakdown & linearity	V_6	Apply 25 volts to Pin 6 only. V_{CC}=0 volts. Measure IPin 6. Note: Linearity @ 25V should be within 5% of linearity @ 5V.	2.0	2.5	3.0	mA
Performance Characteristics in Circuit of Figure 3						
Saturation		Per sensitivity test interrupting input signal measure output voltage.	500			mV
Sensitivity		Input Signal to Dummy Antenna at f_{IN} = 1 MHz, 30% AM Modulation at f_{MOD}= 400 Hz, for 11 mV output at V_O.		2.5	5	μV
Signal-to-Noise Ratio	S/N	Ratio of Output at V_O with Modulation ON and then OFF, Input Signal = 100μV, 30% AM Modulation at f_{MOD} = 400 Hz.	34	40		dB
Overload Distortion		Input Signal set at 1 MHz, 90% AM Modulation, Distortion at V_O must be ≤10%	100	155	250	mV

Dynamic Characteristics for Indicated Stages in Circuit of Figure 3

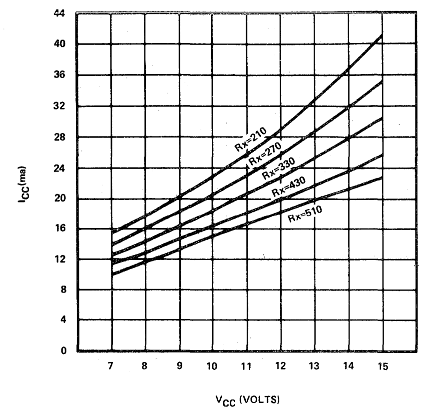
STAGE	PARALLEL CAPACITANCE INPUT pF	PARALLEL CAPACITANCE OUTPUT pF	PARALLEL RESISTANCE INPUT Ω	PARALLEL RESISTANCE OUTPUT Ω	TRANSCONDUCTANCE AT 1 MHz CARRIER μmhos
RF Amplifier	20	6	670	2×10^6 min	150,000 @ 1 MHz
IF Amplifier	35	3.5	850	10^4	100,000 @ 262.5 kHz
Mixer	4	2	2000	2×10^6 min	10,000

TYPICAL CHARACTERISTICS

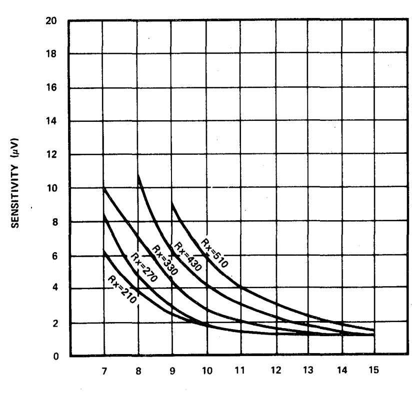
IF OUTPUT LINEARITY



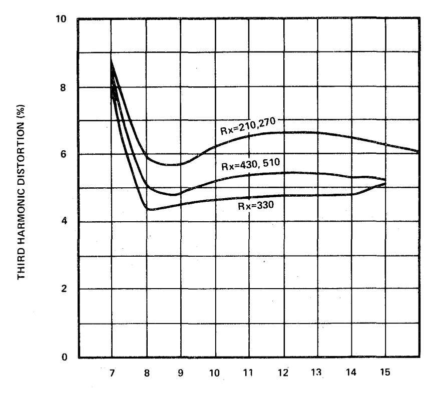
ICC VS. SUPPLY VOLTAGE



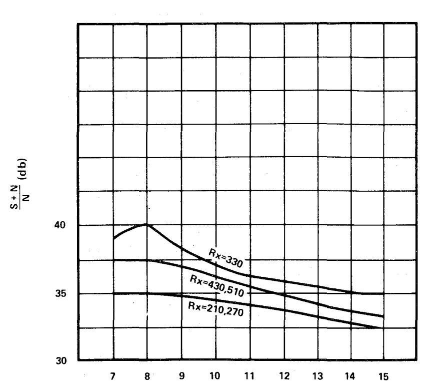
SENSITIVITY VS. SUPPLY VOLTAGE



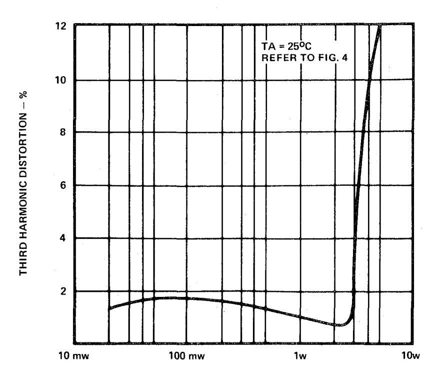
THIRD HARMONIC DISTORTION VS. SUPPLY VOLTAGE



SIGNAL TO NOISE VS. SUPPLY VOLTAGE



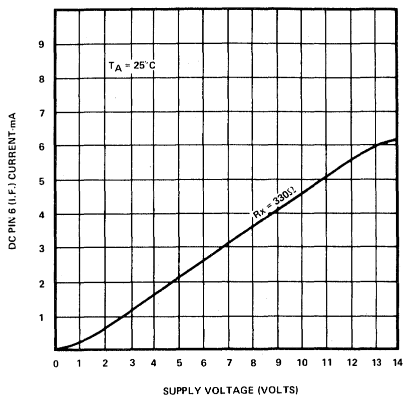
THIRD HARMONIC DISTORTION VERSUS OUTPUT POWER



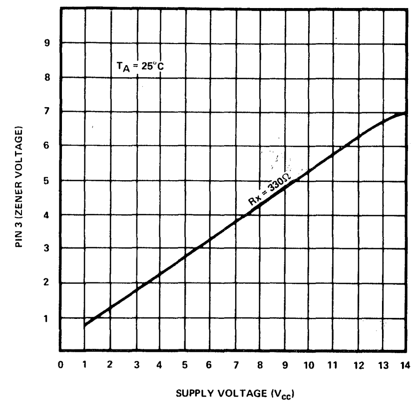
NOTE: Rx is external resistor between pins 3 and V supply.

TYPICAL CHARACTERISTICS (Cont'd)

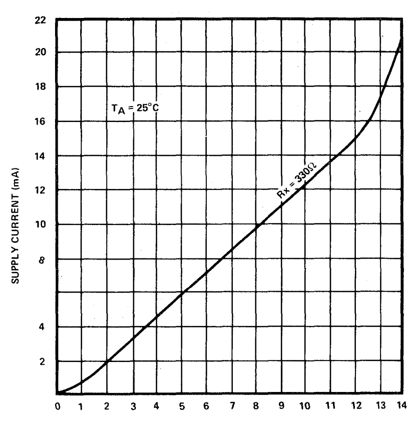
IF CURRENT VERSUS SUPPLY VOLTAGE



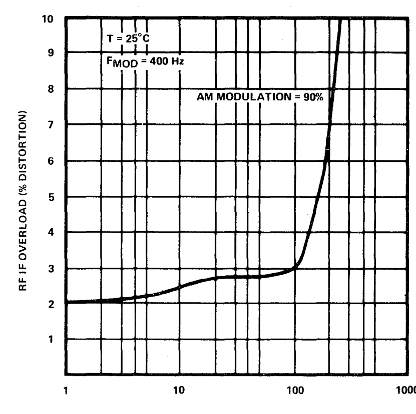
PIN 3 VOLTAGE VERSUS SUPPLY VOLTAGE



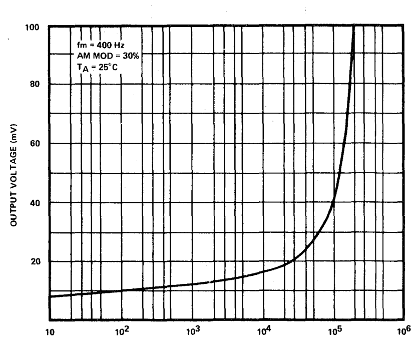
I_{CC} VERSUS V_{CC}



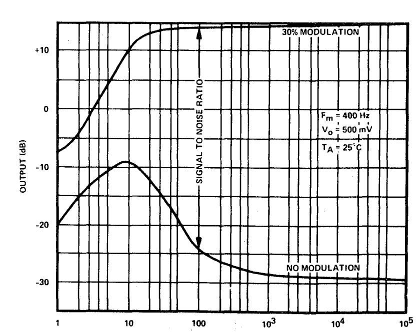
OVERLOAD RESPONSE DISTORTION VERSUS RF INPUT



AGC CURVE



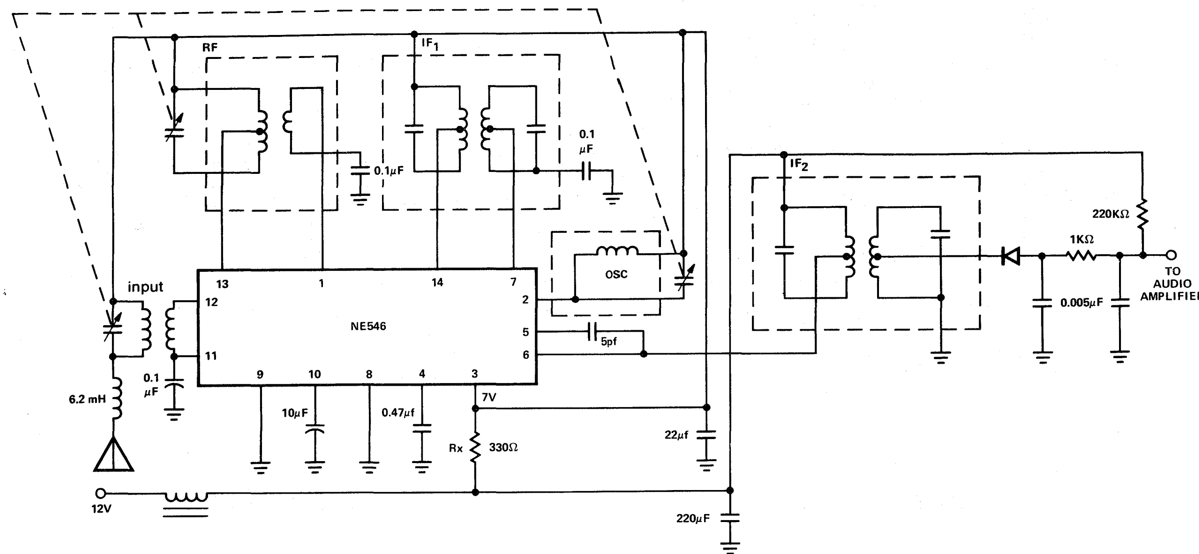
SIGNAL TO NOISE RATIO



NOTE: Rx is external resistor between pins 3 and V supply.

TYPICAL APPLICATIONS

AM RADIO (Capacitor Tuned)



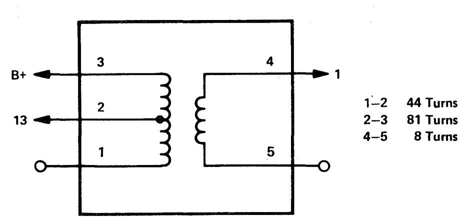
VARIABLE CAPACITOR (Air Varicon)

ANT & RF	13 pF ~ 190 pF
OSC	12 pF ~ 80 pF

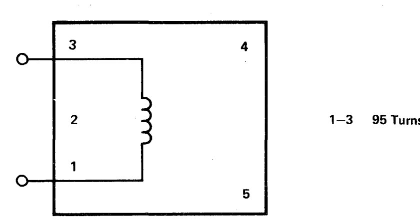
ANTENNA COIL

10 mm ϕ < 120 mm Ferrite Antenna

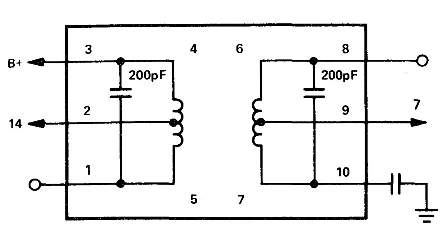
RF COIL



OSC COIL



1st. IF COIL



2nd IF COIL

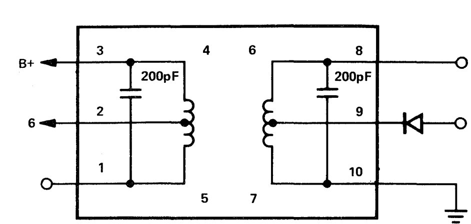


FIGURE 1

TYPICAL APPLICATIONS (Cont'd)

AM CAR RADIO (Slug Tuned)

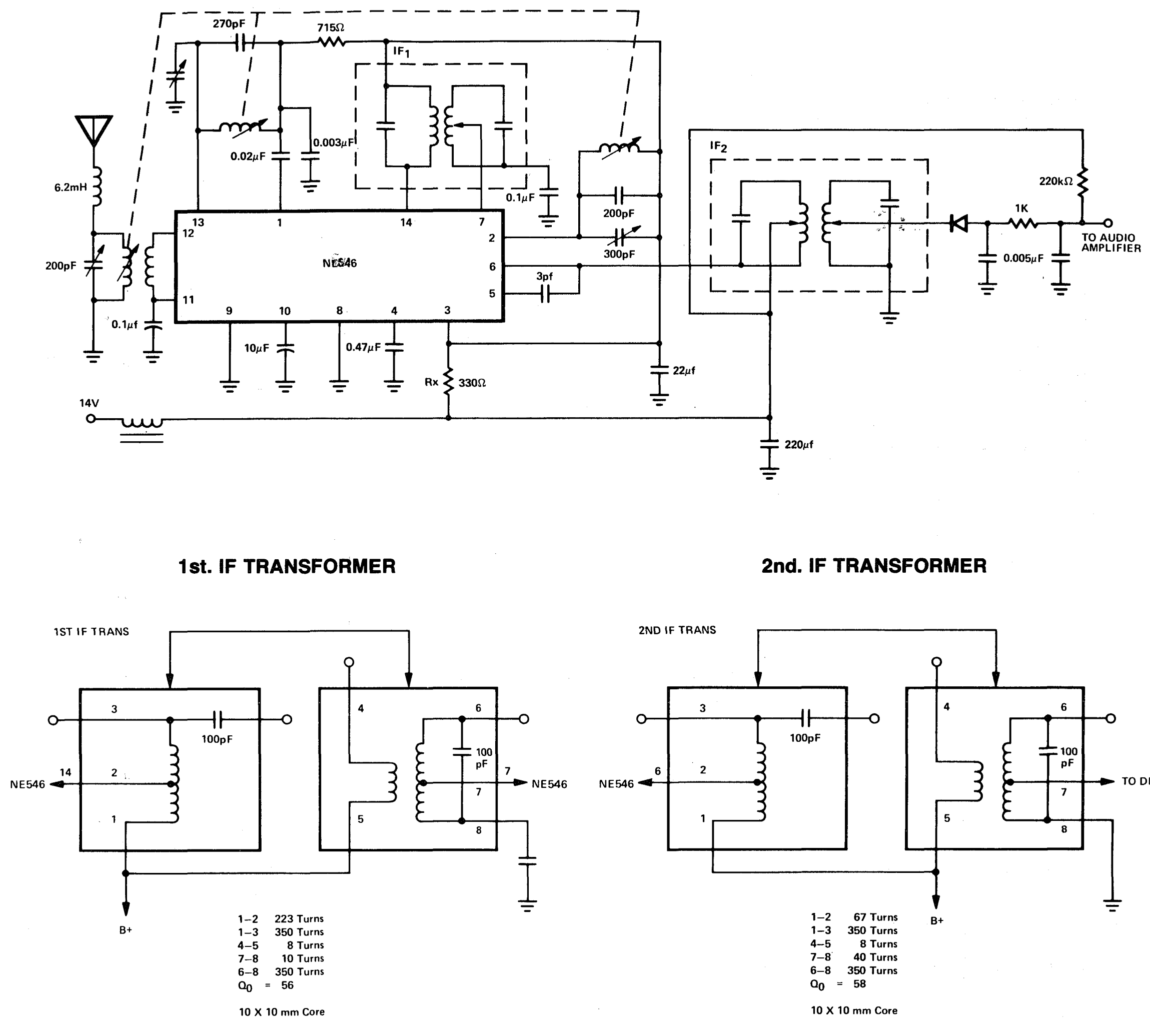


FIGURE 2

SCHEMATIC DIAGRAM

AM RADIO RECEIVER USING NE546

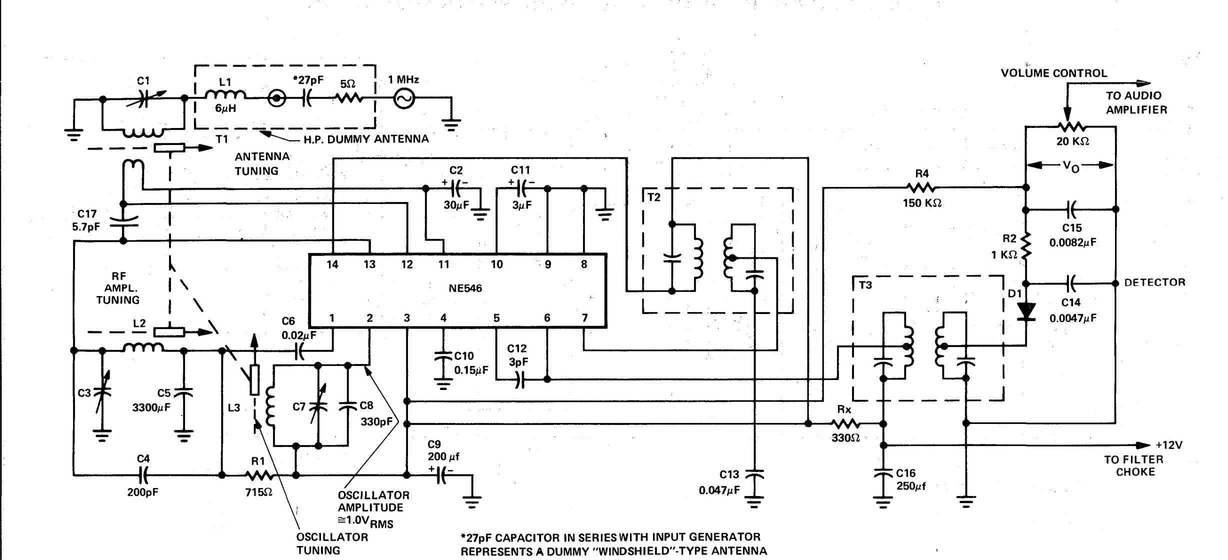


FIGURE 3

TRANSFORMER	SYMBOL	FREQUENCY	INDUCTANCE μh = (≈)	CAPACITANCE pF (≈)	Q (≈)	TOTAL TURNS TO TAP TURNS RATIO
First IF:						
Primary	T_2	262.5 kHz	2840	130	60	**none**
Secondary			2840	130	60	30:1 or 13:1
Second IF:						
Primary	T_3	262.5 kHz	2840	130	60	8.5:1
Secondary			2840	130	60	8.5:1
Antenna:						
Primary	T_1	1 MHz	195	$(C_1)-130$	65	
Secondary		Adjusted to an impedance of 75Ω with primary resonant at 1 MHz. Coupling should be as tight as practical. Wire should be wound around end of coil away from tuning core.				
Coils	L_1	7.9 MHz	6		50	
	L_2	1 MHz	55		50	
	L_2	1.262 MHz	41		40	

SCHEMATIC DIAGRAM

COMPLETE AM RADIO WITH AUDIO DRIVER AND OUTPUT STAGE

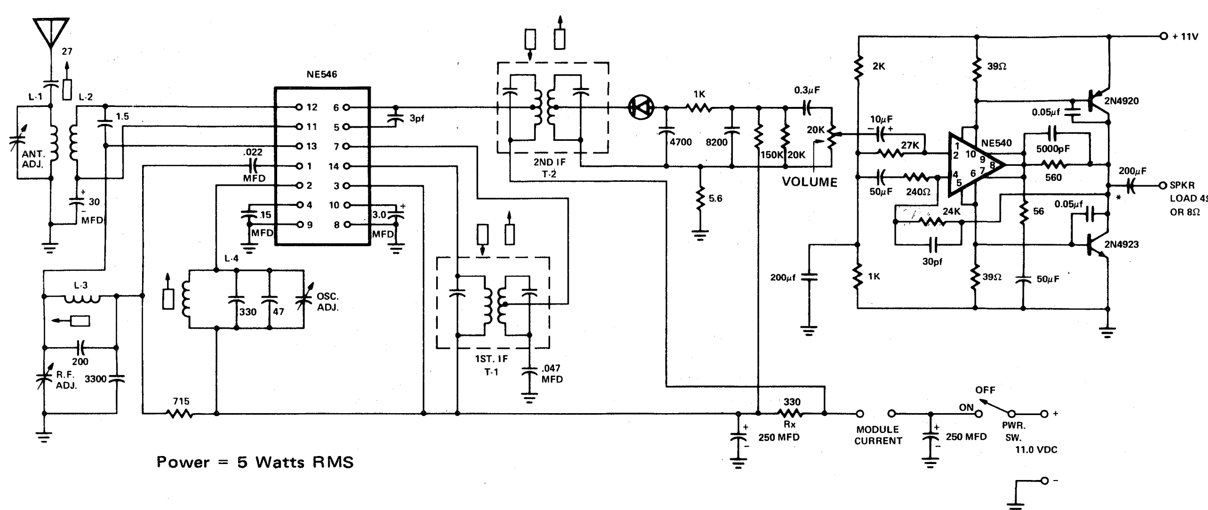


FIGURE 4

FEATURES
- FM DEMODULATION WITHOUT TUNED CIRCUITS
- NARROW BANDPASS - TO ± 14% ADJUSTABLE
- TRACKING RANGE
- EXACT FREQUENCY DUPLICATION IN HIGH NOISE ENVIRONMENT
- WIDE TRACKING RANGE ±15%
- HIGH LINEARITY - 1% DISTORTION MAX
- FREQUENCY MULTIPLICATION AND DIVISION
- THROUGH HARMONIC LOCKING

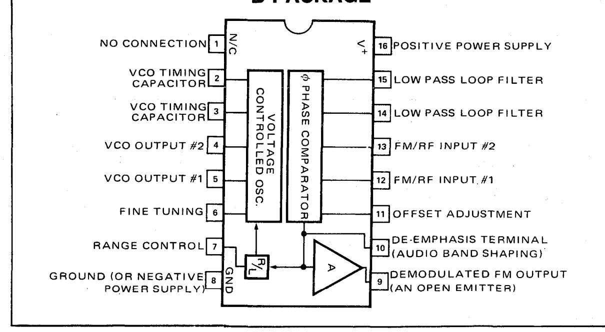
APPLICATIONS
TONE DECODERS
FM IF STRIPS
TELEMETRY DECODERS
DATA SYNCHRONIZERS
SIGNAL RECONSTITUTION
SIGNAL GENERATORS
MODEMS
TRACKING FILTERS
SCA RECEIVERS
FSK RECEIVERS
WIDE BAND HIGH LINEARITY DETECTORS

ABSOLUTE MAXIMUM RATINGS

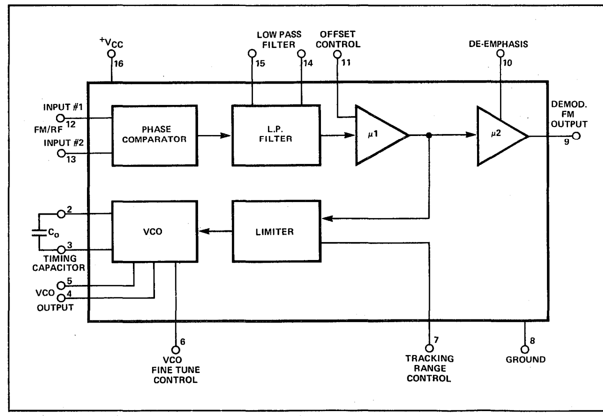
Maximum Operating Voltage	26V
Input Voltage	1V Rms
Storage Temperature	−6°C to 150°C
Operating Temperature	0°C to 70°C
Power Dissipation	300 mw

Limiting values above which serviceability may be impaired

PIN CONFIGURATION



BLOCK DIAGRAM



ANALOG

GENERAL ELECTRICAL CHARACTERISTICS

(15KΩ Pin 9 to GND, Input Pin 12 or Pin 13 AC Ground Unused Input, Optional Controls Not Connected, V+ = 18V Unless Otherwise Specified T_A = 25°C)

CHARACTERISTICS	LIMITS				TEST CONDITIONS
	MIN	TYP	MAX	UNITS	
Lowest Practical Operating Frequency		0.1		Hz	
Maximum Operating Frequency	15	30		MHz	
Supply Current	7	9	11	Ma	
Minimum Input Signal for Lock		100		μV	
Dynamic Range		60		dB	
VCO Temp Coefficient*		± 0.06	±0.12	%/°C	Measured at 2 MHz, with both inputs AC grounded
VCO Supply Voltage Regulation		± 0.3	±2	%/V	
Input Resistance		2		KΩ	Measured at 2 MHz
Input Capacitance		4		Pf	
Input DC Level		+ 4		V	
Output DC Level	+12	+14	+16	V	
Available Output Swing		4		Vp-p	
AM Rejection*	30	40		dB	
De-emphasis Resistance		8		KΩ	Measured at Pin 9 See Figure 1

*ACC Test Sub Group C.

ELECTRICAL CHARACTERISTICS (For FM Applications, Figure 2)

(15KΩ Pin 9 to GND, Input Pin 12 or 13, AC Ground Unused Input, Optional Controls Not Connected, V+ = 18V Unless Otherwise Specified T_A = 25°C)

CHARACTERISTICS	LIMITS				TEST CONDITIONS
	MIN	TYP	MAX	UNITS	
10.7 MHz Operation	**Deviation 75 kHz Source Impedance = 50Ω**				
Detection Threshold		120	300	μV	
Demodulated Output Amplitude	30	60		mV	V_{in} = 1 mv Rms Modulation Frequency 1 kHz
Distortion*		.3	1	%T.H.D.	V_{in} = 1 mv Rms Modulation Frequency 1 kHz
Signal to Noise Ratio $\frac{S+N}{N}$		35		dB	V_{in} = 1 mv Rms Modulation Frequency 1 kHz
4.5 MHz Operation	**Deviation = 25 kHz, Source Impedance = 50Ω**				
Detection Threshold		120	300	μV	
Demodulation Output Amplitude	30	60		mV	V_{in} = 1 mv Rms Modulation Frequency 1 kHz
Distortion		0.3	1.0	%T.H.D	V_{in} = 1 mv Rms Modulation Frequency 1 kHz
Signal to Noise Ratio $\frac{S+N}{N}$		35		dB	V_{in} = 1 mv Rms Modulation Frequency 1 kHz
Wide Deviation	**ΔF/fo = 5% Input = 4.5 MHz Deviation = 225 kHz a 1 kHz Modulation Rate**				
Detection Threshold		1	5	mV	
Demodulated Output	0.2	0.5		Vrms	V_{in} = 5 mv Rms
Distortion		0.8		%T.H.D	V_{in} = 5 mv Rms
Signal to Noise Ratio $\frac{S+N}{N}$		50		dB	V_{in} = 5 mv Rms

*ACC Test Sub Group C.

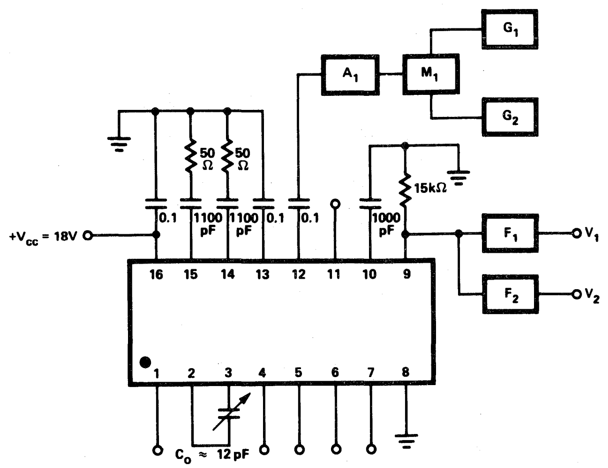
ELECTRICAL CHARACTERISTICS (For Tracking Filter, Figure 3)

(15KΩ Pin 9 to GND, Input Pin 12 or Pin 13 AC Ground Unused Input, Optional Controls Not Connected, V+ = 18V Unless Otherwise Specified T_A = 25°C)

CHARACTERISTICS	LIMITS				
	MIN	TYP	MAX	UNITS	
Tracking Range	±5	±15		% of f_o	V_{in} = 5 mv Rms
Minimum Signal to Sustain Lock 0°C to 70°C		0.8		mvRms	Input 2 MHz - See Characteristic Curves
VCO Output Impedance		1		kΩ	Input 2 MHz Measured with high impedance Probe with less than 10 Pf Capacitance
VCO Output Swing	0.4	0.6		V_{p-p}	
VCO Output DC Level		+6.5		V	Input 2 MHz with ± 100 kHz Side Band Separation and 3 kHz Low Pass Filter
Side Band Suppression		35		dB	Input 1 mv Peak for Carrier Each Side Band C_1 = 0.01 μF R_1 = 0

TYPICAL TEST CIRCUITS

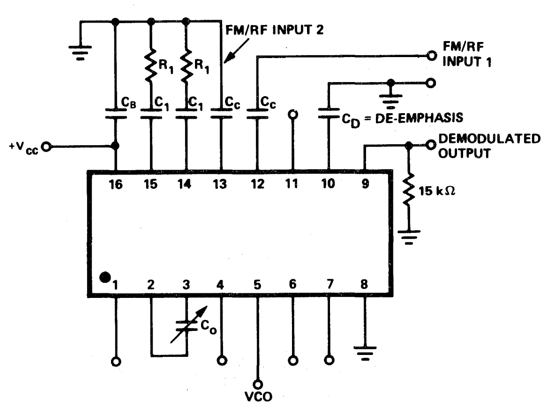
AM REJECTION



G_1 = FM Generator with $f_C = f_O \approx 4$ MHz
$\Delta f = 40$ kHz
$f_{mod} = 1$ kHz
G_2 = Audio Generator with $f_A = 400$ Hz
M_1 = Balanced Modulator Carrier Supplied by G_1, Am modulation provided by G_2.
A_1 = 50Ω attenuator pad with signal level into pin 12 adjusted to 1 mV rms.
F_1 = 1 kHz Bandpass filter, Q = 20
F_2 = 400 Hz Bandpass filter with Q = 50, with 1 kHz trap.
AMR $= \frac{V1}{V2}$ in dB
V_1 and V_2 are rms voltmeter readings.

FIGURE 1

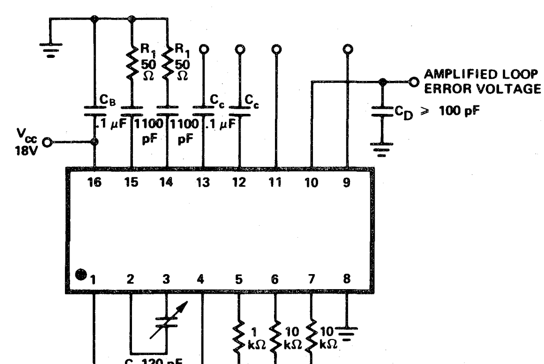
FM DEMODULATION



C_b = Bypass Capacitor
C_C = Coupling Capacitors
C_1 = Low Pass Filter Capacitors
C_0 = Frequency Determining Capacitor
T_d = De-emphasis time constant = (C_D) (8kΩ)

FIGURE 2

TRACKING FILTER



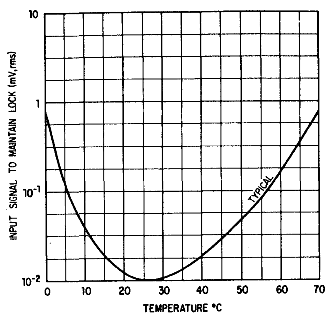
C_C = Coupling Capacitors
C_B = Bypass Capacitor
C_1 = Low Pass Filter Capacitor
C_o = VCO Frequency Set Capacitor

FIGURE 3

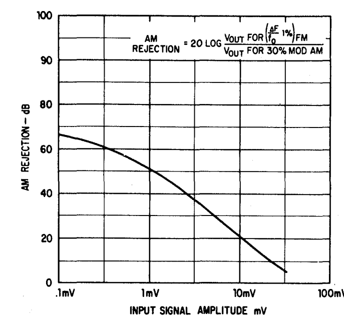
ANALOG

TYPICAL CHARACTERISTIC CURVES

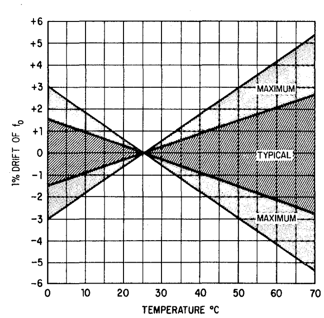
MINIMUM INPUT SIGNAL AMPLITUDE NECESSARY TO MAINTAIN LOCK AS A FUNCTION OF TEMPERATURE WITH $f_{signal} = fo_{25°C} = 2.0$ MHz



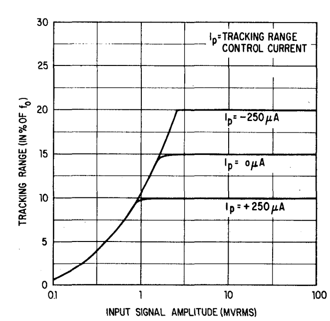
AM REJECTION AS A FUNCTION OF INPUT SIGNAL LEVEL f_o = 10 MHz



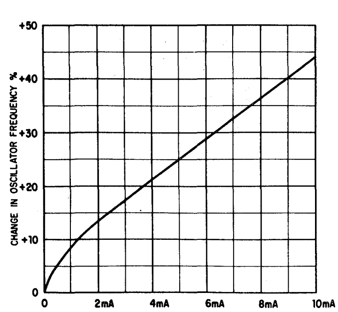
THERMAL DRIFT OF VCO FREE RUNNING FREQUENCY (f_o)



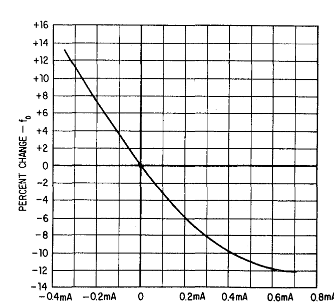
TYPICAL TRACKING RANGE AS A FUNCTION OF INPUT SIGNAL



CHANGE OF FREE RUNNING OSCILLATOR FREQUENCY AS A FUNCTION OF FINE TUNING CIRCUIT

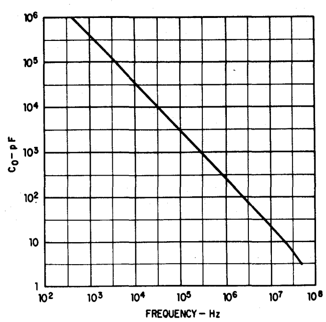


CHANGE OF FREE RUNNING OSCILLATOR FREQUENCY AS A FUNCTION OF RANGE CONTROL CURRENT

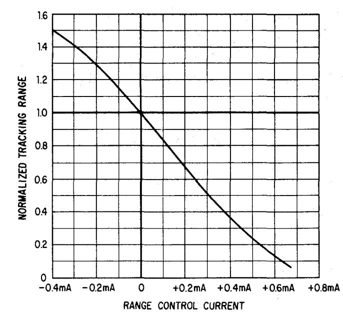


TYPICAL CHARACTERISTIC CURVES (Cont'd)

FREE RUNNING OSCILLATOR FREQUENCY AS A FUNCTION OF VCO TIMING CAPACITANCE

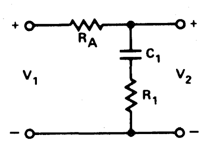


NORMALIZED TRACKING RANGE AS A FUNCTION OF RANGE CONTROL CURRENT



EXTERNAL CONTROLS

1. **Loop Low Pass Filter (Pins 14 and 15)**
The equivalent circuit for the loop low-pass filter can be represented as:



where RA (6K Ω) is the effective resistance seen looking into Pin 14 or Pin 15.
The corresponding filter transfer characteristics are:

$$\frac{V_2}{V_1}(S) = (S) = \frac{1 + S\,R_1C_1}{1 + S\,(R_1 + R_A)\,C_1}$$

where S is the complex frequency variable.

2. **Loop Gain (Threshold) Control**
The overall Phase Locked Loop gain can be reduced by connecting a feedback resistor, RF, across the low-pass filter terminals, Pins 14 and 15. This causes the loop gain and the detection sensitivity to decrease by a factor α ($\alpha<1$)
where:

$$\alpha = \frac{R_F}{2\,R_A + R_F}$$

Reduction of loop gain may be desirable at high input signal levels (Vin > 30 mV) and at high frequencies (fo >5 MHz) where excessively high loop gain may cause instability.

3. **Tracking Range Control (Pin 7)**
Any bias current, Ip, injected into the tracking range control, reduces the tracking range of the PLL by decreasing the output of the limiter. The variation of the tracking range and the center frequency, as a function of Ip, are shown in the characteristic curves with Ip defined positive going into the tracking range control terminal. This terminal is normally at a DC level of +0.6 Volts and presents an impedance of 600Ω.

4. **External Fine Tuning (Pin 6)**
Any bias current injected into the fine tuning terminal increases the frequency of oscillation, fo, as shown in the characteristic curves. This current is defined Positive into the fine tuning terminal. This terminal is at a typical DC level of +1.3 Volts and has a dynamic impedance of 100Ω to ground.

5. **Offset Adjustment (pin 11)**
Application of a bias voltage to the offset adjustment terminal modifies the current in the output amplifier setting the DC level at the output. The effect on the loop is to modify the relationship between the VCO free running frequency and the lock range, allowing the VCO free running frequency to be positioned at different points throughout the lock range.
Nominally this terminal is at +4V DC and has an input impedance of 3KΩ. The offset adjustment is optional. The characteristics specified correspond to operation of the circuit with this terminal open circuited.

6. **De-emphasis Filter (Pin 10)**
The de-emphasis terminal is normally used when the PLL is used to demodulate Frequency Modulated Audio signals. In this application, a capacitor from this terminal to ground provides the required de-emphasis. For other applications, this terminal may be used for band shaping the output signal. The 3 dB bandwidth of the output amplifier in the system block diagram (see Figure 2) is related to the de-emphasis capacitor, C_D, as:

$$f_{3db} = \frac{1}{2\,R_a\,C_D}$$

where RD is the 8000 ohm resistance seen looking into the de-emphasis terminal.
When the PLL system is utilized for signal conditioning, and the loop error voltage is not utilized, de-emphasis terminal should be AC grounded.

ANALOG

FEATURES
- FM DEMODULATION WITHOUT TUNED CIRCUITS
- SYNCHRONOUS AM DETECTION
- NARROW BAND PASS TO ±1%
- EXACT FREQUENCY DUPLICATION IN HIGH NOISE ENVIRONMENT
- ADJUSTABLE TRACKING RANGE
- WIDE TRACKING RANGE ±15%
- HIGH LINEARITY - 1% DISTORTION MAX
- FREQUENCY MULTIPLICATION AND DIVISION THROUGH HARMONIC LOCKING

ABSOLUTE MAXIMUM RATINGS

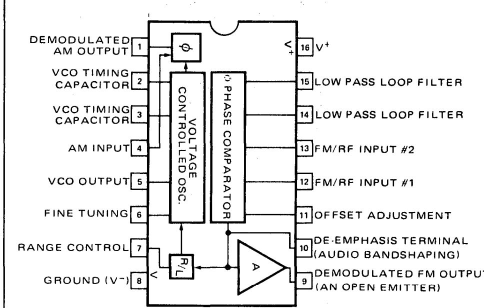
Maximum Operating Voltage	26V
Input Voltage	1V RMS
Storage Temperature	−65°C to 150°C
Operating Temperature	0°C to 70°C
Power Dissipation	300mW

Limiting values above which serviceability may be impaired

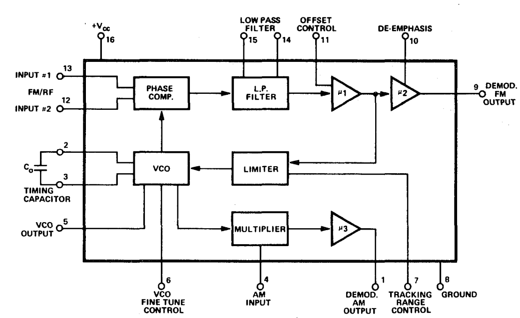
APPLICATIONS
TONE DECODERS
AM-FM-IF STRIPS
TELEMETRY DECODERS
DATA SYNCHRONIZERS
SIGNAL RECONSTITUTION
SIGNAL GENERATORS
MODEMS
TRACKING FILTERS
SCA RECEIVERS
FSK RECEIVERS
WIDE BAND HIGH LINEARITY DETECTORS
SYNCHRONOUS DETECTORS
AM RECEIVER

PIN CONFIGURATION

B PACKAGE



BLOCK DIAGRAM



GENERAL ELECTRICAL CHARACTERISTICS

(15KΩ Pin 9 to GND, Input Pin 12 or Pin 13 AC Ground Unused Input, Optional Controls Not Connected, V+ = 18V Unless Otherwise Specified T_A = 25°C)

CHARACTERISTICS	LIMITS				TEST CONDITIONS
	MIN	TYP	MAX	UNITS	
Lowest Practical Operating Frequency		0.1		Hz	
Maximum Operating Frequency	15	30		MHz	
Supply Current	8	10	12	Ma	
Minimum Input Signal for Lock		100		μV	
Dynamic Range		60		dB	
VCO Temp Coefficient*		± 0.06	±0.12	%/°C	Measured at 2 MHz, with both inputs AC grounded
VCO Supply Voltage Regulation		± 0.3	±2	%/V	Measured at 2 MHz
Input Resistance		2		kΩ	
Input Capacitance		4		pf	
Input DC Level		+ 4		V	
Output DC Level	±12	+14	+16	V	
Available Output Swing		4		V_{p-p}	Measured at Pin 9
AM Rejection*	30	40		dB	See Figure 3
De-emphasis Resistance		8		kΩ	

*ACC Test Sub Group C.

ELECTRICAL CHARACTERISTICS (For Tracking Filter, Figure 3) (15KΩ Pin 9 to GND, Input Pin 12 or Pin 13 AC Ground Unused Input, Optional Controls Not Connected, V+ = 18V Unless Otherwise Specified T_A = 25°C)

CHARACTERISTICS	LIMITS				TEST CONDITIONS
	MIN	TYP	MAX	UNITS	
Tracking Range	±5	±20	% of f_o		Vin = 5 mv Rms
Minimum Signal to Sustain Lock 0°C to 70°C		0.8	mvRms		Input 2 MHz - See Characteristic Curves
VCO Output Impedance		1	kΩ		
VCO Output Swing	0.4	0.6	V_{p-p}		Input 2 MHz Measured with high impedance Probe with less than 10 Pf Capacitance
VCO Output DC Level		+6.5	V		
Side Band Suppression		35	dB		Input 2 MHz with ± 100 kHz Side Band Separation and 3 kHz Low Pass Filter Input 1 mv Peak for Carrier Each Side Band C_1 = 0.01 μF R_1 = 0

ELECTRICAL CHARACTERISTICS (For FM Applications, Figure 2) (15KΩ Pin 9 to GND, Input Pin 12 or 13, AC Ground Unused Input, Optional Controls Not Connected, V+ = 18V Unless Otherwise Specified T_A = 25°C)

CHARACTERISTICS	LIMITS				TEST CONDITIONS
	MIN	TYP	MAX	UNITS	
10.7 MHz Operation	**Deviation 75 kHz Source Impedance = 50Ω**				
Detection Threshold		120	300	μV	
Demodulated Output Amplitude	30	60		mV	Vin = 1 mv Rms Modulation Frequency 1 kHz
Distortion*		.3	1	%T.H.D.	Vin = 1 mv Rms Modulation Frequency 1 kHz
Signal to Noise Ratio $\frac{S+N}{N}$		35		dB	Vin = 1 mv Rms Modulation Frequency 1 kHz
4.5 MHz Operation	**Deviation = 25 kHz, Source Impedance = 50Ω**				
Detection Threshold		120	300	μV	
Demodulation Output Amplitude	30	60		mV	Vin = 1 mv Rms Modulation Frequency 1 kHz
Distortion		0.3	1.0	%T.H.D	Vin = 1 mv Rms Modulation Frequency 1 kHz
Signal to Noise Ratio $\frac{S+N}{N}$		35		dB	Vin = 1 mv Rms Modulation Frequency 1 kHz
Wide Deviation	**$\Delta F/f_o$ = 5% Input = 4.5 MHz Deviation = 225 kHz a 1 kHz Modulation Rate**				
Detection Threshold		1	5	mV	
Demodulated Output	0.2	0.5		Vrms	Vin = 5 mv Rms
Distortion		0.8		%T.H.D	Vin = 5 mv Rms
Signal to Noise Ratio $\frac{S+N}{N}$		50		dB	Vin = 5 mv Rms

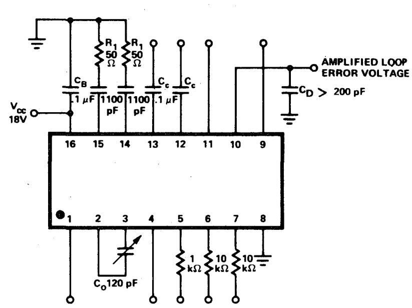
*ACC Test Sub Group C.

ELECTRICAL CHARACTERISTICS (For AM Synchronous Detector, Figure 4) (15KΩ Pin 9 to GND, Input Pin 12 or Pin 13 AC Ground Unused Input, Optional Controls Not Connected, V + = 18V Unless Otherwise Specified T_A = 25°C)

CHARACTERISTICS	LIMITS				TEST CONDITIONS
	MIN	TYP	MAX	UNITS	
Input Impedance		3		kΩ	
Output Impedance		8		kΩ	
Output DC Level	+10	+14	+17	V	
AM Conversion Gain	3	12		dB	See Definition of Terms
Out of Band Rejection		30		dB	See Definition of Terms
Distortion		1		%T.H.D	

TYPICAL TEST CIRCUITS

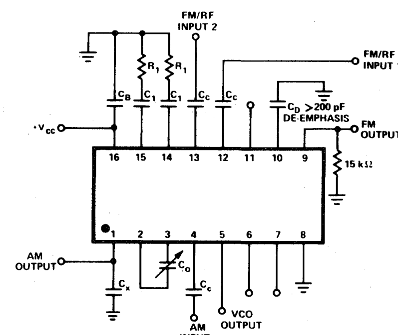
TEST CIRCUIT FOR TRACKING FILTER



C_C = Coupling Capacitors
C_B = Bypass Capacitor
C_1 = Low Pass Filter Capacitor
C_0 = VCO Frequency Set Capacitor

FIGURE 1

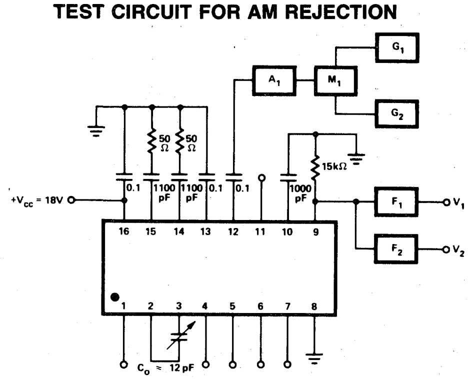
TEST CIRCUIT FOR FM DEMODULATION



C_B = Bypass Capacitor
C_C = Coupling Capacitors
C_1 = Low Pass Filter Capacitors
C_0 = Frequency Determining Capacitors
C_x = AM Post Detection Filter

FIGURE 2

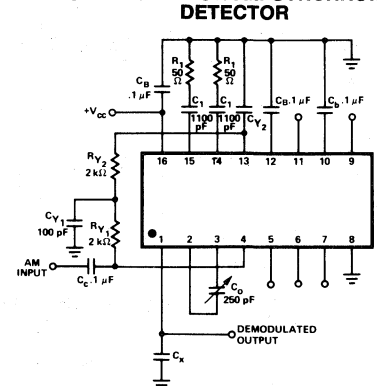
TEST CIRCUIT FOR AM REJECTION



G_1 = FM Generator with f_C = fo ≈ 4 MHz
Δf = 40 kHz, f_{mod} = 1 kHz
G_2 = Audio Generator with f_A = 400 kHz
M_1 Balanced Modulator Carrier Supplied by G_1, Am modulation provided by G_2
A_1 = 50Ω attenuator pad with signal level into pin 12 adjusted to 1 mV rms.
F_1 = 1 kHz Bandpass filter, Q = 20
F_2 = 400 Hz Bandpass filter with Q = 50, with 1 kHz trap.
AMR = $\frac{V_1}{V_2}$ in db V_1 and V_2 are rms voltmeter readings.

FIGURE 3

TEST CIRCUIT FOR AM SYNCHRONOUS DETECTOR

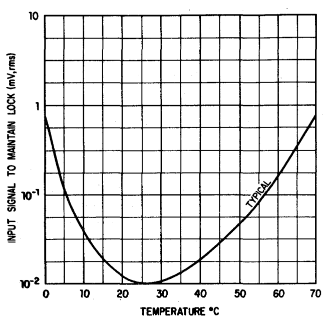


C_B = Bypass Capacitor
C_C = Coupling Capacitor
$Ry_1Cy_1 = Ry_2Cy_2 = \frac{1}{2\pi fo}$
C_x = AM Post Detection Filter

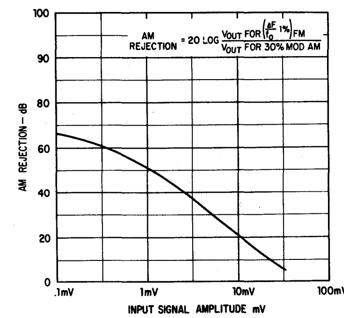
FIGURE 4

TYPICAL CHARACTERISTIC CURVES

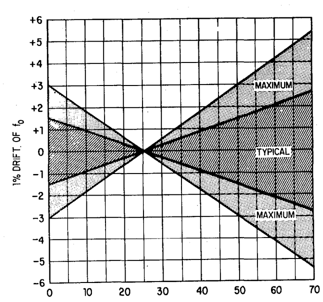
MINIMUM INPUT SIGNAL AMPLITUDE NECESSARY TO MAINTAIN LOCK AS A FUNCTION OF TEMPERATURE WITH fsignal = $fo_{25°C}$ = 2.0 MHz



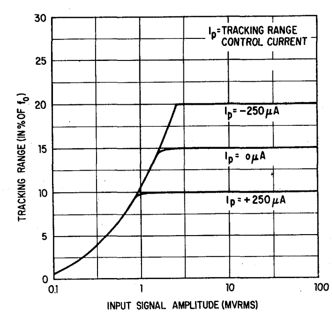
AM REJECTION AS A FUNCTION OF INPUT SIGNAL LEVEL f_o = 10 MHz



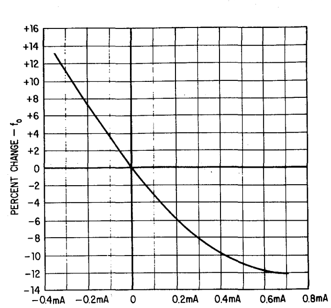
THERMAL DRIFT OF VCO FREE RUNNING FREQUENCY (f_o)



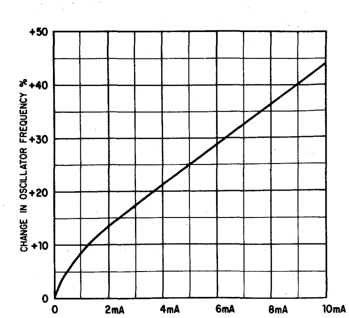
TYPICAL TRACKING RANGE AS A FUNCTION OF INPUT SIGNAL



CHANGE OF FREE RUNNING OSCILLATOR FREQUENCY AS A FUNCTION OF RANGE CONTROL CURRENT

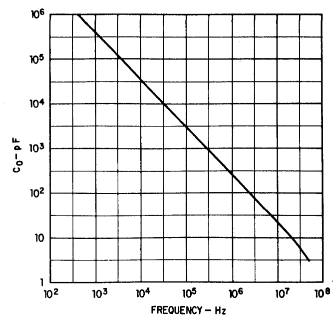


CHANGE OF FREE RUNNING OSCILLATOR FREQUENCY AS A FUNCTION OF FINE TUNING CIRCUIT

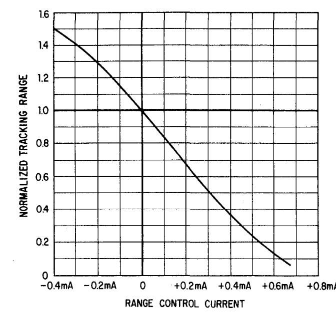


BLOCK DIAGRAM

FREE RUNNING OSCILLATOR FREQUENCY AS A FUNCTION OF VCO TIMING CAPACITANCE

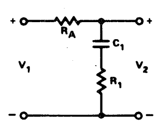


NORMALIZED TRACKING RANGE AS A FUNCTION OF RANGE CONTROL CURRENT



EXTERNAL CONTROLS

1. **Loop Low Pass Filter (Pins 14 and 15)**
   The equivalent circuit for the loop low-pass filter can be represented as:



where RA (6KΩ) is the effective resistance seen looking into Pin 14 or Pin 15.
The corresponding filter transfer characteristics are:

$$\frac{V_2}{V_1}(S) = F(S) = \frac{1 + S R_1 C_1}{1 + S (R_1 + R_A) C_1}$$

where S is the complex frequency variable.

2. **Loop Gain (Threshold) Control**
   The overall Phase Lock of loop gain can be reduced by connecting a feedback resistor, RF, across the low-pass filter terminals, Pins 14 and 15. This causes the loop gain and the detection sensitivity to decrease by a factor ($\alpha<1$), where

$$\alpha = \frac{R_F}{2R_A + R_F}$$

Reduction of loop gain may be desirable at high input signal levels (Vin >30 mV) and at high frequencies (fo > 5MHz) where excessively high PLL loop gain may cause instability within the loop.

3. **Tracking Range Control (Pin 7)**
   Any bias current, Ip, injected into the tracking range control, reduces the tracking range of the PLL by decreasing the output of the limiter. The variation of the tracking range and the center frequency, as a function of Ip, are shown in the characteristic curves with Ip defined positive going into the tracking range control terminal. This terminal is normally at a DC level of +0.6 Volts and presents an impedance of 600Ω.

4. **External Fine Tuning (Pin 6)**
   Any bias current injected into the fine tuning terminal increases the frequency of oscillation, fo, as shown in the characteristic curves. This current is defined Positive into the fine tuning terminal. This terminal is at a typical DC level of +1.3 Volts and has a dynamic impedance of 100Ω to ground.

5. **Offset Adjustment (Pin 11)**
   Application of a bias voltage to the offset adjustment terminal modifies the current in the output amplifier setting the DC level at the output. The effect on the loop is to modify the relationship between the VCO free running frequency and the lock range, allowing the VCO free running frequency to be positioned at different points throughout the lock range.
   Nominally this terminal is at +4V DC and has an input impedance of 3kΩ. The offset adjustment is optional. The characteristics specified correspond to operation of the circuit with this terminal open circuited.

6. **De-emphasis Filter (Pin 10)**
   The de-emphasis terminal is normally used when the PLL is used to demodulate Frequency Modulated Audio signals. In this application, a capacitor from this terminal to ground provides the required de-emphasis. For other applications, this terminal may be used for band shaping the output signal. The 3 dB bandwidth of the output amplifier in the system block diagram (see Figure 2) is related to the de-emphasis capacitor, CD, as:

$$f_{3dB} = \frac{1}{2\pi R_D C_D}$$

where RD is the 8000 ohm resistance seen looking into the de-emphasis terminal.
When the PLL system is for signal conditioning, and the loop error voltage is not utilized, de-emphasis terminal should be AC grounded.

7. **AM Post-Detection Filter (Pin 1)**
   The capacitor Cx connected between Pin 1 and ground serves as a low-pass filter for synchronous AM detection with a transfer characteristic, F2(S), given as:

$$F_2(S) = \frac{1}{1 + S R_X C_X}$$

where $R_X = 8k\Omega$ is the resistance seen looking into Pin #1.

FEATURES

- FREQUENCY MULTIPLICATION AND DIVISION
- SIGNAL CONDITIONING AND SIDE-BAND SUPPRESSION
- FM DEMODULATION WITHOUT TUNED CIRCUITS
- NARROW BANDPASS — TO ±1%
- ADJUSTABLE TRACKING RANGE — TO ±15%
- EXACT FREQUENCY DUPLICATION IN HIGH NOISE ENVIRONMENT
- HIGH LINEARITY — 1% DISTORTION MAXIMUM AT 1% DEVIATION

APPLICATIONS

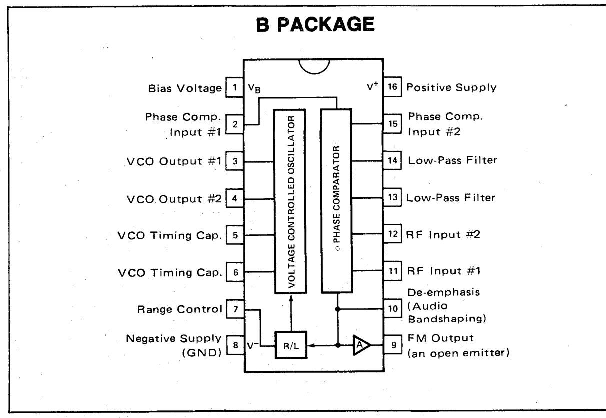
FREQUENCY SYNTHESIZERS
DATA SYNCHRONIZERS
SIGNAL CONDITIONING
TRACKING FILTERS
TELEMETRY DECODERS
MODEMS
FM IF STRIPS AND DEMODULATORS
TONE DECODERS
FSK RECEIVERS
WIDEBAND HIGH LINEARITY FM DEMODULATORS

ABSOLUTE MAXIMUM RATINGS

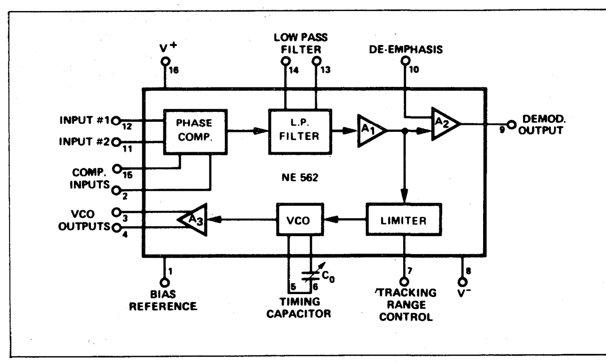
(Limiting values above which serviceability may be impaired)

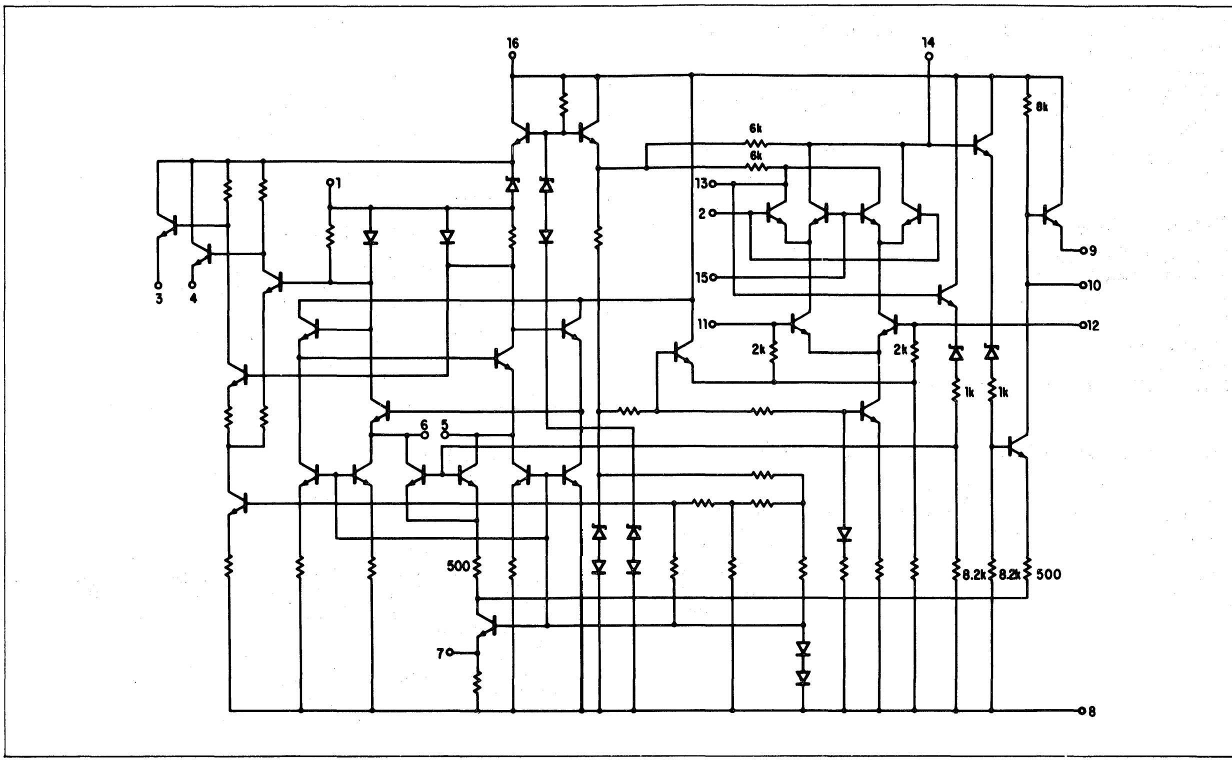
Maximum Operating Voltage	30V
Input Voltage	3V rms
Storage Temperature	−65°C to 150°C
Operating Temperature	0°C to 70°C
Power Dissipation	300mW

PIN CONFIGURATION



BLOCK DIAGRAM





GENERAL ELECTRICAL CHARACTERISTICS

(15,000 ohms pin 9 to ground, 12,000 ohms pins 3 and 4 to ground, pins 2 and 15 to pin 1 through 1,000 ohms, input to pin 11 or 12 with unused input at AC ground, range control not connected and V+ = 18 volts unless otherwise specified. T_A = 25°C.)

CHARACTERISTICS	LIMITS			UNITS	TEST CONDITIONS
	MIN	TYP	MAX		
Lowest Practical Operating Frequency		0.1		Hz	
Maximum Operating Frequency	15	30		MHz	
Supply Current	10	12	14	mA	
Minimum Input Signal for Lock		200		μV	
Dynamic Range		80		dB	
VCO Temp Coefficient*		± 0.06	±0.15	%/°C	Measured at 2 MHz
VCO Supply Voltage Regulation		± 0.3	±2	%/V	Measured at 2 MHz
Input Resistance		2		KΩ	
Input Capacitance		4		pf	
Input DC Level	+2	+4	+6	V	
Output DC Level	±12	+14	+16	V	
Available Output Swing		4		Vp-p	Measured at Pin 9
AM Rejection*	30	40		dB	See Definition of Terms
De-emphasis Resistance		8		KΩ	
Bias Reference		+8		V	

*ACC Test Sub Group C.

ELECTRICAL CHARACTERISTICS FOR FM APPLICATIONS (15,000 ohms pin 9 to ground, input to pin 11 or pin 12, AC ground unused input, range control not connected and V+ = 18 volts. T_A = 25°C)

CHARACTERISTICS	LIMITS MIN	TYP	MAX	UNITS	TEST CONDITIONS
10.7 MHz Operation — **Deviation 75 kHz Source Impedance = 50Ω**					
Detection Threshold		200	500	μV	V_{in} = 1 mv Rms Modulation Frequency 1 kHz
Demodulated Output Amplitude	30	70		mVrms	V_{in} = 1 mv Rms Modulation Frequency 1 kHz
Distortion*		0.5		%T.H.D.	V_{in} = 1 mv Rms Modulation Frequency 1 kHz
Signal to Noise Ratio $\frac{S+N}{N}$		35		dB	
4.5 MHz Operation — **Deviation = 25 kHz, Source Impedance = 50Ω**					
Detection Threshold		200	500	μV	V_{in} = 1 mv Rms Modulation Frequency 1 kHz
Demodulated Output Amplitude	30	60		mV rms	V_{in} = 1 mv Rms Modulation Frequency 1 kHz
Distortion		0.5		%T.H.D	V_{in} = 1 mv Rms Modulation Frequency 1 kHz
Signal to Noise Ratio $\frac{S+N}{N}$		35		dB	
Wide Deviation — **ΔF/fo = 5% Input = 4.5 MHz Deviation = 225 kHz a 1 kHz Modulation Rate**					
Detection Threshold		1	5	mV	V_{in} = 5 mv Rms
Demodulated Output		1		V rms	V_{in} = 5 mv Rms
Distortion	0.3	0.8		%T.H.D	V_{in} = 5 mv Rms
Signal to Noise Ratio $\frac{S+N}{N}$		50		dB	

ELECTRICAL CHARACTERISTICS FOR SIGNAL CONDITIONER AND FREQUENCY SYNTHESIS APPLICATIONS (Input to pin 11 or pin 12, AC ground unused input, range control not connected, V+ = 18 volts. T_A = 25°C)

CHARACTERISTIC	LIMITS MIN	TYP	MAX	UNITS	TEST CONDITIONS
Tracking Range	±5	±15		% of fo	200 mV p-p square wave input
Input Resistance		2		kΩ	
Input Capacitance		4		pF	
Input DC Level		4		V	
VCO Output Impedance		1.3	2.5	kΩ	
VCO Output Swing	3	4.5		V p-p	
VCO Output DC Level		12		V	
VCO Signal/Noise Ratio		60		db	Inputs at AC ground

TEST CIRCUIT

TEST CIRCUIT FOR FM DEMODULATION

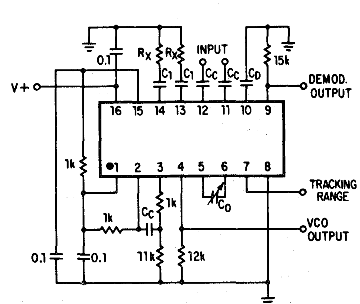
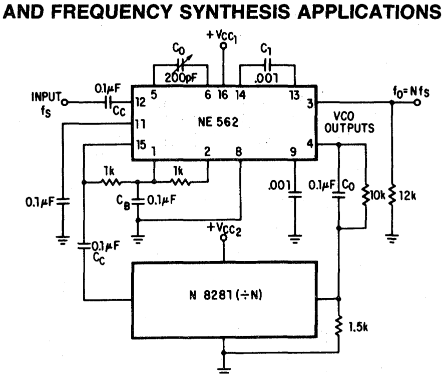


FIGURE 1

TEST CIRCUIT FOR SIGNAL CONDITIONER AND FREQUENCY SYNTHESIS APPLICATIONS



C_B = Bypass Capacitor
C_C = Coupling Capacitor
C_1 = Low Pass Filter Capacitor
C_0 = Frequency Capacitor Set

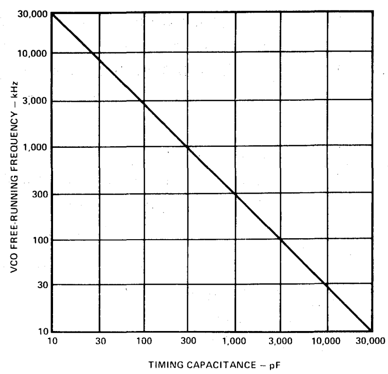
Note: Fanout to divide by N counter is one.

FIGURE 2

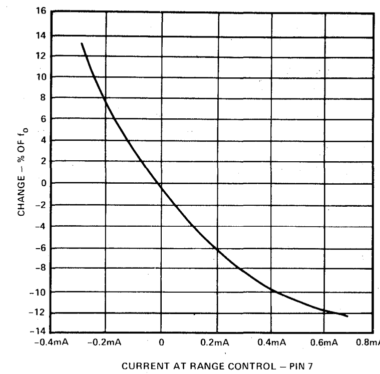
ANALOG

TYPICAL CHARACTERISTIC CURVES

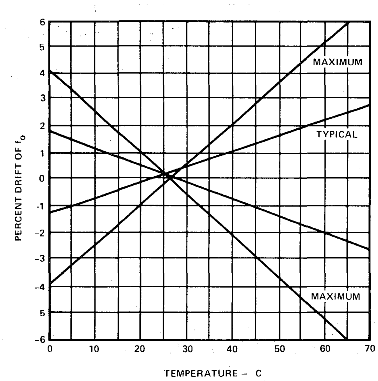
FREE RUNNING VOLTAGE CONTROLLED OSCILLATOR FREQUENCY AS A FUNCTION OF TIMING CAPACITANCE



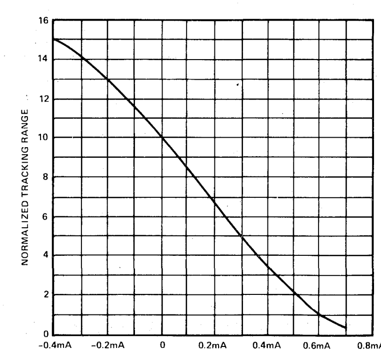
CHANGE OF FREE RUNNING OSCILLATOR FREQUENCY AS A FUNCTION OF RANGE CONTROL CURRENT



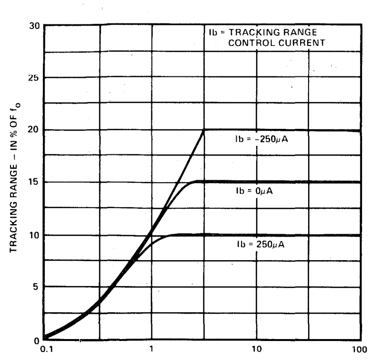
THERMAL DRIFT OF FREE RUNNING FREQUENCY AS A FUNCTION OF TEMPERATURE



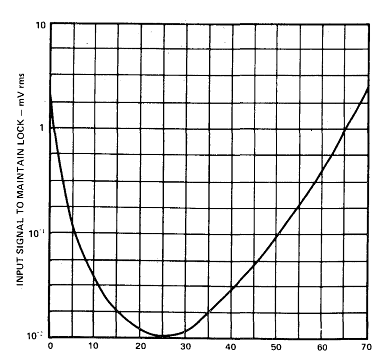
NORMALIZED TRACKING RANGE AS A FUNCTION OF RANGE CONTROL CURRENT



TYPICAL TRACKING RANGE AS A FUNCTION OF INPUT SIGNAL AMPLITUDE

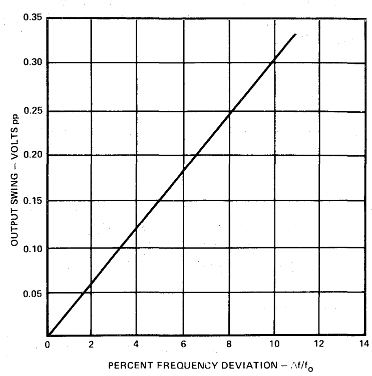


INPUT SIGNAL AMPLITUDE TO MAINTAIN LOCK AS A FUNCTION OF TEMPERATURE (fsignal = fo = 2.0 MHz)

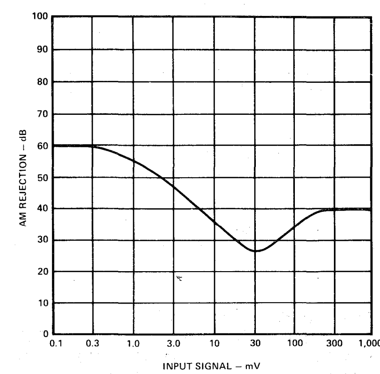


TYPICAL CHARACTERISTIC CURVES (Cont'd)

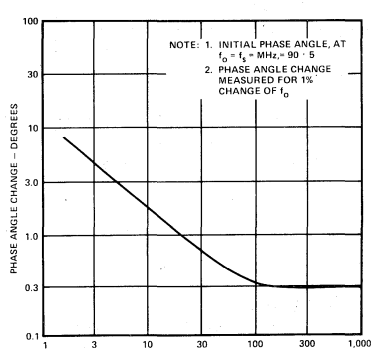
562 PHASE LOCKED LOOP DEMODULATED OUTPUT SWING AS A FUNCTION OF % FM DEVIATION



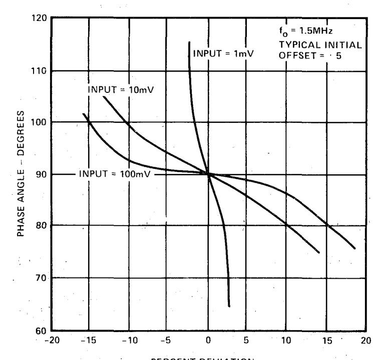
AM REJECTION AS A FUNCTION OF INPUT SIGNAL LEVEL



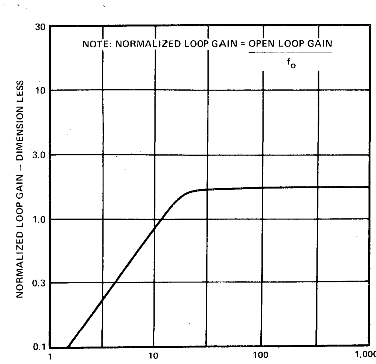
CHANGE IN PHASE ANGLE, fo RELATIVE TO fs, AS A FUNCTION OF INPUT SIGNAL AMPLITUDE



VCO OUTPUT PHASE AS A FUNCTION OF PERCENT FREQUENCY DEVIATION



NORMALIZED LOOP GAIN AS A FUNCTION OF INPUT SIGNAL AMPLITUDE



ANALOG

562 APPLICATIONS INFORMATION

1. BIAS REFERENCE

Pin 1 of the 562 is an internally regulated bias reference voltage supply which should be used as a source of bias current for the phase comparator input terminals, Pins 2 and 15. Biasing may be achieved as shown in Figure 3.

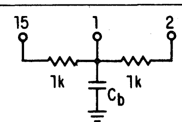


FIGURE 3

2. PHASE COMPARATOR LOOP INPUTS

Of the Signetics high frequency phase locked loops, the 562 is unique in that the loop is open between the VCO and the phase comparator. Once biasing of the comparator is accomplished, as described in Bias Reference above, loop closure can be accomplished by capacitive coupling between either one or both inputs of the phase comparator and the VCO output. A divider or counter may be enclosed in the loop at this point for frequency synthesis applications or a flip-flop may be used to ensure that the output waveform has a 50% duty cycle. If large signal swings, greater than 2 volts, are to be applied to the phase comparator inputs, a 1000 ohm current limiting buffer resistor should be used in series with the coupling capacitors.

3. VCO OUTPUT

Square wave VCO outputs of both polarities (0°C and 180°C) buffered by an amplifier are available at pins 3 and 4. For proper operation of the buffer amplifier, pins 3 and 4 must be returned to ground (or the negative supply) through resistors, typically 12,000 ohms. The value of these resistors may be reduced provided that total power dissipated in the 562 does not exceed 300 milliwatts or the total average current in each emitter does not exceed 4 mA. The output amplitude is typically 4.5 volts peak referenced at +12 volts with respect to pin 8.

4. VCO TUNING

Setting the free-running frequency of the VCO is accomplished easily with one timing capacitor connected between pins 5 and 6. For the 562 Phase Locked Loop, fine tuning of the free-running frequency may be accomplished in either or both of two ways. The first method uses a trimmer capacitor connected in parallel with the VCO timing capacitor. This is the simplest technique and requires the smallest number of extra components but at the lower frequencies may be difficult to implement. The second technique incorporates two resistors and a voltage source. The resistors are connected between each of the timing capacitor terminals and a voltage source as shown in Figure 4.

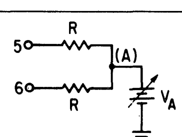


FIGURE 4

The percent change in the VCO free-running frequency, fo, as a function of the voltage applied to point (A) is shown in the curves of Figure 5. Note that with this fine tuning technique, it is possible to *increase* the VCO free-running frequency to a value greater than possible with just a trimmer capacitor alone. A formula for the approximation of the VCO frequency as a function of the voltage at point (A), the resistance values and the starting frequency, is given below:

$$f = f_O \left[1 - \frac{V_A - 6.4}{1300R} \right]$$

The recommended resistance range of R is 20,000 to 60,000 ohms.

CHANGE IN VCO FREQUENCY AS A FUNCTION OF FINE TUNING VOLTAGE

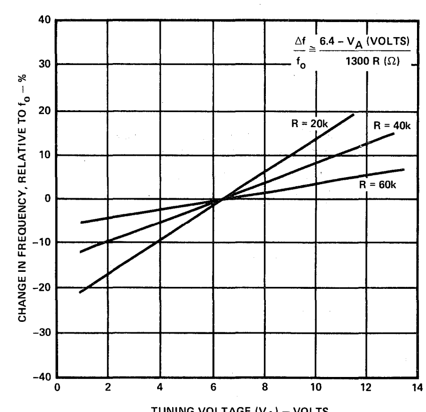


FIGURE 5

5. LOOP GAIN CHARACTERISTICS

The overall open loop gain of the 562 PLL can be expressed as:

$K_O = K_1K_2$

where:

K_O = total open loop gain

K_1 = phase comparator and amplifier conversion gain

K_2 = VCO conversion gain

The VCO conversion gain, K_2, is the change of VCO frequency per unit of error voltage. In this particular design, it is numerically equal to the VCO frequency, i.e.,

$K_2 = f_O$ Hz/Volt

or

$K_2 = 2\pi f_O$ radians/Volt-second

The phase comparator and amplifier conversion gain, K_1, is proportional to input signal amplitude for low input levels, $V_S \leq 40$mV rms, and is constant and equal to about 1.5 volts/radian for higher input amplitudes. Therefore, K_1 can be approximated as:

$$K_1 \cong \frac{.04\ V_S}{\sqrt{1 + \left(\frac{V_S}{40}\right)^2}}$$

where

V_S = input signal in mV rms.

562 APPLICATIONS INFORMATION (Cont'd.)

6. SIGNAL INPUT

The input structure is basically differential and may be used in this manner. Biasing is supplied to the input terminals from an internal regulated supply so signal inputs must be capacitively coupled. In most applications where the input is single-ended, the unused input should be bypassed to ground.

7. DEMODULATED OUTPUT

Pin 9 is a low impedance output terminal for the loop error voltage. It is at this point that the demodulated FM output is obtained. When used, it must be biased by a resistor to ground (or negative supply), and the resistor value may be adjusted downward provided that the output current does not exceed 5mA or the dissipation in the 562 does not exceed the absolute maximum ratings. When not used, pin 9 may be left open.

8. DE-EMPHASIS FILTER

The de-emphasis terminal, pin 10, is normally required when the PLL is used to demodulate Frequency Modulated Audio signals. In this application, a capacitor from this terminal to ground provides the required de-emphasis. For other applications it may be used to shape the output response. The 3 dB bandwidth of the output amplifier is related to the de-emphasis capacitor, C_D, as:

$$f_{3dB} = \frac{1}{2\pi R_D C_D}$$

where R_D is 8000 ohms.

When the PLL system is utilized for applications not requiring the use of the output amplifier, pin 10 should be by-passed to ground.

9. TRACKING RANGE CONTROL (Pin 7)

Any bias current, Ip, injected into the tracking range control, reduces the tracking range of the PLL by decreasing the output of the limiter. The variation of the tracking range and the center frequency, as a function of Ip, are shown in the characteristic curves with Ip defined positive going into the tracking range control terminal. This terminal is normally at a DC level of +0.6 volts and presents an impedance of 600Ω.

10. LOW PASS FILTER

In most applications, a loop low-pass filter should be connected between pins 13 and 14 and ground. It is used to set the loop response time, controlling the capture range and the rejection of out of band information. Four filter configurations and their transfer functions are shown in Figures 6 through 9. For VCO operating grequencies below 5 MHz, configurations shown in Figures 6 and 7 may be used. At higher frequencies, configurations shown in Figures 8 and 9 should be used to ensure loop stability. R is the impedance seen looking into the low pass filter terminals, Pins 13 and 14; and, in the 562, is nominally 6000 ohms.

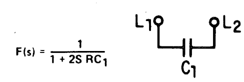


FIGURE 6

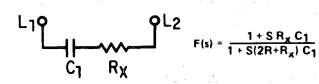


FIGURE 7

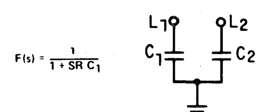


FIGURE 8

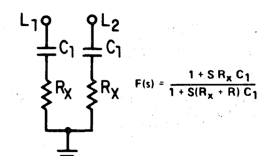


FIGURE 9

11. LOOP GAIN (Threshold) CONTROL

The overall Phase Locked Loop gain can be reduced by connecting a resistor, R_F, across the low-pass filter terminals, pins 13 and 14. This causes the loop gain and the detection sensitivity to decrease by a factor α, where:

$$\alpha = \frac{R_F}{12{,}000 + R_F}$$

Reduction of loop gain may be desirable at operating frequencies greater than 5 MHz because, at these frequencies, high loop gain may cause instability.

12. STATIC LOOP PHASE-ERROR

When the PLL is in lock, the VCO outputs have a nominal ±90°C phase shift with respect to the input signal. Due to internal offsets, this nominal angle at perfect lock condition may shift a few degrees, typically ±5°C or less.

FEATURES

- EXTREME STABILITY OF CENTER FREQUENCY (200ppm/°C typ)
- WIDE RANGE OF OPERATING VOLTAGE (±5 to ±12 VOLTS) WITH VERY SMALL FREQUENCY DRIFT (100ppm/% typ)
- VERY HIGH LINEARITY OF DEMODULATED OUTPUT (0.2% typ)
- CENTER FREQUENCY PROGRAMMING BY MEANS OF A RESISTOR, CAPACITOR, VOLTAGE OR CURRENT
- TTL AND DTL COMPATIBLE SQUARE-WAVE OUTPUT; LOOP CAN BE OPENED TO INSERT DIGITAL FREQUENCY DIVIDER
- HIGHLY LINEAR TRIANGLE WAVE OUTPUT
- REFERENCE OUTPUT FOR CONNECTION OF COMPARATOR IN FREQUENCY DISCRIMINATOR
- BANDPASS, ADJUSTABLE FROM <±1% to >±60%
- FREQUENCY ADJUSTABLE OVER 10 TO 1 RANGE WITH SAME CAPACITOR

APPLICATIONS

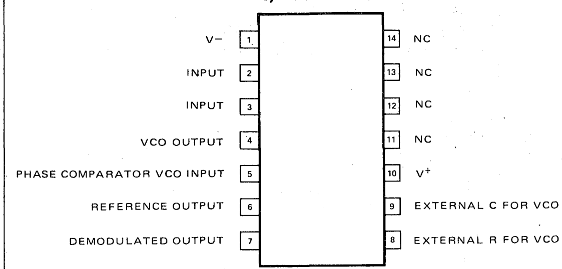
FREQUENCY SHIFT KEYING
MODEMS
TELEMETRY RECEIVERS
TONE DECODERS
SCA RECEIVERS
WIDEBAND FM DISCRIMINATORS
DATA SYNCHRONIZERS
TRACKING FILTERS
SIGNAL RESTORATION
FREQUENCY MULTIPLICATION & DIVISION

ABSOLUTE MAXIMUM RATINGS

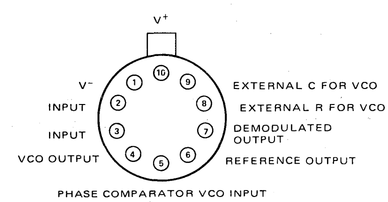
Maximum Operating Voltage	26V
Storage Temperature	−65°C to 150°C
Power Dissipation	300mW

PIN CONFIGURATION

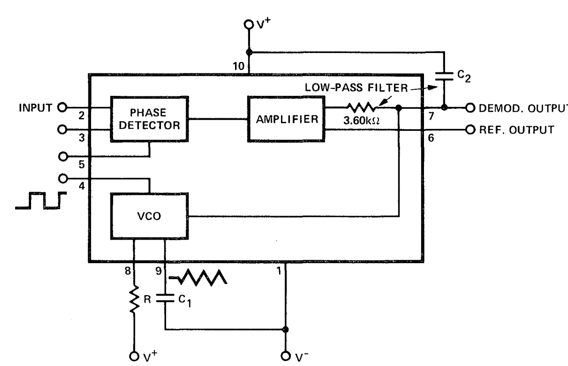
A,F PACKAGE



K PACKAGE



BLOCK DIAGRAM



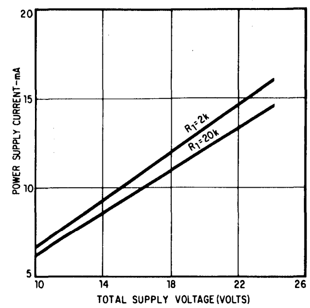
ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_{CC} = ±6 Volts unless otherwise noted)

PARAMETER	TEST CONDITIONS	SE565			NE565			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
SUPPLY REQUIREMENTS								
Supply Voltage		±5		±12	±5		±12	V
Supply Current			8	12.5		8	12.5	mA
INPUT CHARACTERISTICS								
Input Impedance	−4V≤V2, V3≤+1V	7	10		5	10		kΩ
Input Level Required for Tracking	f_0 = 50 kHz ±10% frequency deviation	10	1		10	1		mVrms
VCO CHARACTERISTICS								
Center Frequency								
Maximum Value	C_1 = 2.7 pF	300	500			500		kHz
Distribution	Distribution taken about $f_0 \simeq$ 50 kHz	−10	0	+10	−30	0	+30	%
Drift with Temperature	R_1 = 5.0k, C_1 = 1200 pF f_0 = 50 kHz	+75	+100	+525		+200		ppm/°C
Drift with Supply Voltage	f_0 = 50 kHz V_{CC} = ±6 to ±7 Volts		0.1	1.0		0.2	1.5	%/V
Triangle Wave								
Output Voltage Level		1.9	0		1.9	0		V
Amplitude			2.4	3		2.4	3	Vp-p
Linearity			0.2			0.5		%
Square Wave								
Logical "1" Output Voltage	f_0 = 50 kHz V_{CC} = ±6 Volts	+4.9	+5.2		+4.9	+5.2		V
Logical "0" Output Voltage	f_0 = 50 kHz V_{CC} = ±6 Volts		−0.2	+0.2		−0.2	+0.2	V
Duty Cycle	f_0 = 50 kHz	45	50	55	40	50	60	%
Rise Time			20	100		20		nsec
Fall Time			50	200		50		nsec
Output Current (sink)		0.6	1		0.6	1		mA
Output Current (source)		5	10		5	10		mA
DEMODULATED OUTPUT CHARACTERISTICS								
Output Voltage Level	(pin 7) V_{CC} = ±6 Volts	4.25	4.5	4.75	4.0	4.5	5.0	V
Maximum Voltage Swing	(pin 7)		2			2		Vp-p
Output Voltage Swing	±10% frequency deviation	250	300		200	300		mVp-p
Total Harmonic Distortion			0.2	0.75		0.2	1.5	%
Output Impedance			3.6			3.6		kΩ
Offset Voltage [V6−V7]	T_A = 25°C		30	100		50	200	mV
vs Temperature (drift)			50			100		μV/°C
AM Rejection		30	40			40		dB

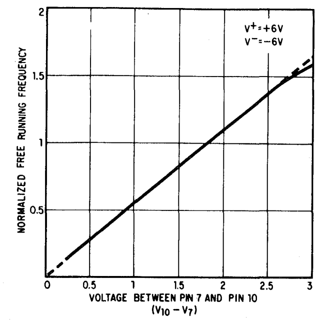
NOTES:
1. Both input terminals (pins 2 and 3) must receive identical dc bias. This bias may range from 0 volts to −4 volts.
2. The external resistance for frequency adjustment (R1) must have a value between 2kΩ and 20kΩ. Larger values minimize initial warmup drift.
3. Output voltage swings negative as input frequency increases.
4. Output not buffered.

TYPICAL PERFORMANCE CHARACTERISTICS

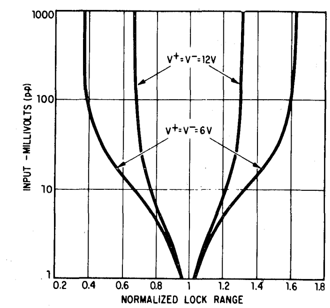
POWER SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



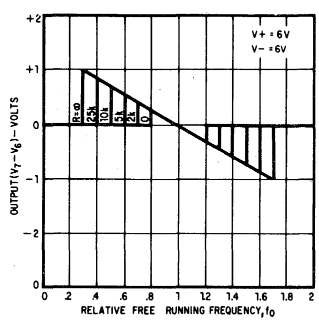
FREE-RUNNING VCO FREQ. AS A FUNCTION OF VOLTAGE BETWEEN PIN 7 & 10 (VCO CONVERSION GAIN)



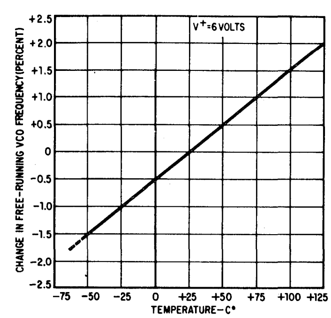
LOCK RANGE AS A FUNCTION OF INPUT VOLTAGE



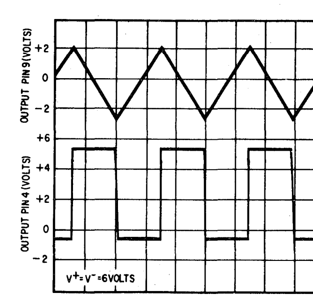
LOCK RANGE AS A FUNCTION OF GAIN SETTING RESISTANCE (PIN 6 - 7)



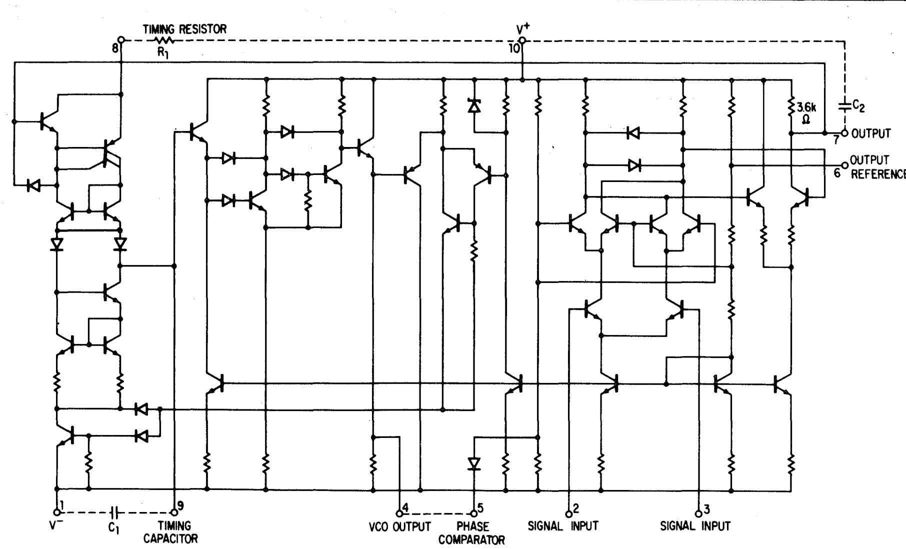
CHANGE IN FREE-RUNNING VCO FREQUENCY AS A FUNCTION OF TEMPERATURE



VCO OUTPUT WAVEFORM



SCHEMATIC DIAGRAM



DESIGN FORMULAS

Free-running frequency of VCO $f_o = \frac{1.2}{4R_1C_1}$ in Hz

Lock-range $f_L = \pm \frac{8f_o}{V_{CC}}$ in Hz

Capture-range $f_C \simeq \pm \frac{1}{2\pi} \sqrt{\frac{2\pi f_L}{\tau}}$

where $\tau = (3.6 \times 10^3) \times C_2$

TYPICAL APPLICATIONS

FM DEMODULATION

The 565 Phase Locked Loop is a general purpose circuit designed for highly-linear FM demodulation. During lock, the average dc level of the phase comparator output signal is directly proportional to the frequency of the input signal. As the input frequency shifts, it is this output signal which causes the VCO to shift its frequency to match that of the input. Consequently, the linearity of the phase comparator output with frequency is determined by the voltage-to-frequency transfer function of the VCO.

Because of its unique and highly linear VCO, the 565 PLL can lock to and track an input signal over a very wide range (typically ±60%) with very high linearity (typically, within 0.5%).

A typical connection diagram is shown in Figure 1. The VCO free-running frequency is given approximately by

$f_o = \frac{1.2}{4R_1C_1}$ and should be adjusted to be at the center of the input signal frequency range. C1 can be any value, but R1 should be within the range of 2000 to 20,000 ohms with an optimum value on the order of 4000 ohms. The source can be direct coupled if the dc resistances seen from pins 2 and 3 are equal and there is no dc voltage difference between the pins. A short between pins 4 and 5 connects the VCO to the phase comparator. Pin 6 provides a dc reference voltage that is close to the dc potential of the demodulated output (pin 7). Thus, if a resistance (R2 in Figure 1) is connected between pins 6 and 7, the gain of the output stage can be reduced with little change in the dc voltage level at the output. This allows the lock range to be decreased with little change in the free-running frequency. In this manner the lock range can be decreased from ±60% of fo to approximately ±20% of fo (at ±6V).

A small capacitor (typically 0.001 μF) should be connected between pins 7 and 8 to eliminate possible oscillation in the control current source.

A single-pole loop filter is formed by the capacitor C2, connected between pin 7 and positive supply, and an internal resistance of approximately 3600 ohms.

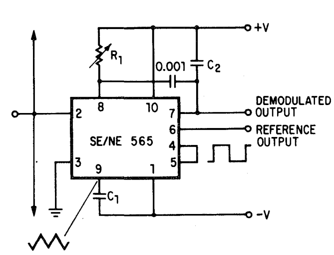


FIGURE 1

FREQUENCY SHIFT KEYING (FSK)

FSK refers to data transmission by means of carrier which is shifted between two preset frequencies. This frequency shift is usually accomplished by driving a VCO with the binary data signal so that the two resulting frequencies correspond to the "0" and "1" states (commonly called space and mark) of the binary data signal.

A simple scheme using the 565 to receive FSK signals of 1070 Hz and 1270 Hz is shown in Figure 2. As the signal appears at the input, the loop locks to the input frequency and tracks it between the two frequencies with a corresponding dc shift at the output.

The loop filter capacitor C2 is chosen smaller than usual to eliminate overshoot on the output pulse, and a three-stage RC ladder filter is used to remove the carrier component from the output. The band edge of the ladder filter is chosen to be approximately half way between the maximum keying rate (in this case 300 baud or 150 Hz) and twice the input frequency (approximately 2200 Hz). The output signal can now be made logic compatible by connecting a voltage comparator between the output and pin 6 of the loop. The free-running frequency is adjusted with R1 so as to result in a slightly-positive voltage at the output at f_{in} = 1070 Hz.

The input connection is typical for cases where a dc voltage is present at the source and therefore a direct connection is not desirable. Both input terminals are returned to ground with identical resistors (in this case, the values are chosen to effect a 600-ohm input impedance).

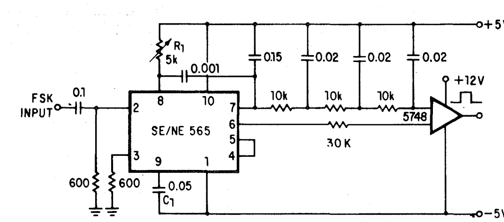


FIGURE 2

FREQUENCY MULTIPLICATION

There are two methods by which frequency multiplication can be achieved using the 565:

1. Locking to a harmonic of the input signal.
2. Inclusion of a digital frequency divider or counter in the loop between the VCO and phase comparator.

The first method is the simplest, and can be achieved by setting the free-running frequency of the VCO to a multiple of the input frequency. A limitation of this scheme is that the lock range decreases as successively higher and weaker harmonics are used for locking. If the input frequency is to be constant with little tracking required, the loop can generally be locked to any one of the first 5 harmonics. For higher orders of multiplication, or for cases where a large lock range is desired, the second scheme is more desirable. An example of this might be a case where the input signal varies over a wide frequency range and a large multiple of the input frequency is required.

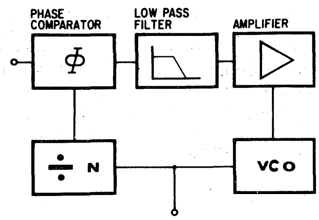


FIGURE 3

A block diagram of the second scheme is shown in Figure 3. Here the loop is broken between the VCO and the phase comparator, and a frequency divider is inserted. The fundamental of the divided VCO frequency is locked to the input frequency in this case, so that the VCO is actually running at a multiple of the input frequency. The amount of multiplication is determined by the frequency divider. A typical connection scheme is shown in Figure 4. To set up the circuit, the frequency limits of the input signal must be determined. The free-running frequency of the VCO is then adjusted by means of R1 and C1 (as discussed under FM demodulation) so that the output frequency of the divider is midway between the input frequency limits. The filter capacitor, C2, should be large enough to eliminate variations in the demodulated output voltage (at pin 7), in order to stabilize the VCO frequency. The output can now be taken as the VCO squarewave output, and its fundamental will be the desired multiple of the input frequency (f1) as long as the loop is in lock.

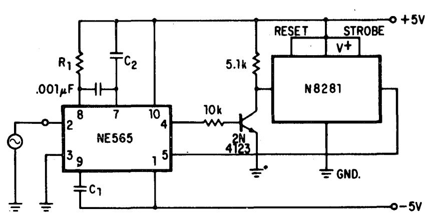


FIGURE 4

SCA (BACKGROUND MUSIC) DECODER

Some FM stations are authorized by the FCC to broadcast uninterrupted background music for commercial use. To do this a frequency modulated subcarrier of 67 kHz is used. The frequency is chosen so as not to interfere with the normal stereo or monaural program; in addition, the level of the subcarrier is only 10% of the amplitude of the combined signal.

The SCA signal can be filtered out and demodulated with the NE565 Phase Locked Loop without the use of any resonant circuits. A connection diagram is shown in Figure 5. This circuit also serves as an example of operation from a single power supply.

A resistive voltage divider is used to establish a bias voltage for the input (pins 2 and 3). The demodulated (multiplex) FM signal is fed to the input through a two-stage high-pass filter, both to effect capacitive coupling and to attenuate the strong signal of the regular channel. A total signal amplitude, between 80mV and 300mV, is required at the input. Its source should have an impedance of less than 10,000 ohms.

The Phase Locked Loop is tuned to 67 kHz with a 5000 ohm potentiometer; only approximate tuning is required, since the loop will seek the signal.

The demodulated output (pin 7) passes through a three-stage low-pass filter to provide de-emphasis and attenuate the high-frequency noise which often accompanies SCA transmission. Note that no capacitor is provided directly at pin 7; thus, the circuit is operating as a first-order loop. The demodulated output signal is in the order of 50 mV and the frequency response extends to 7 kHz.

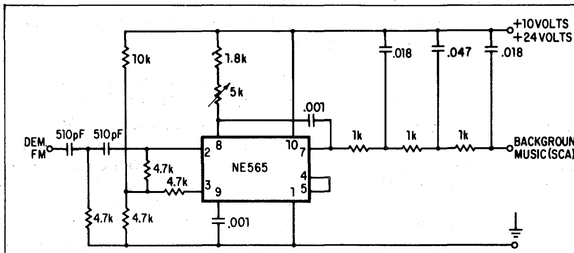


FIGURE 5

FEATURES

- WIDE RANGE OF OPERATING VOLTAGE (10 to 24 volts)
- VERY HIGH LINEARITY OF MODULATION
- EXTREME STABILITY OF FREQUENCY (100 ppm/°C typical)
- HIGHLY LINEAR TRIANGLE WAVE OUTPUT
- HIGH ACCURACY SQUARE WAVE OUTPUT
- FREQUENCY PROGRAMMING BY MEANS OF A RESISTOR, CAPACITOR, VOLTAGE OR CURRENT
- FREQUENCY ADJUSTABLE OVER 10 TO 1 RANGE WITH SAME CAPACITOR

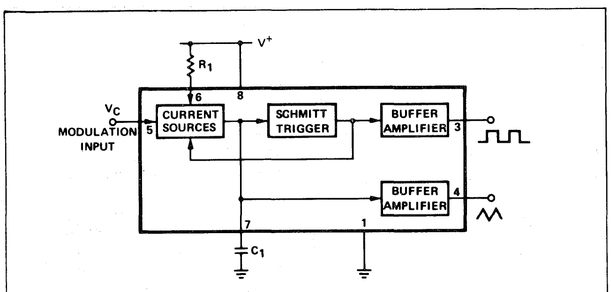
APPLICATIONS

TONE GENERATORS
FREQUENCY SHIFT KEYING
FM MODULATORS
CLOCK GENERATORS
SIGNAL GENERATORS
FUNCTION GENERATORS

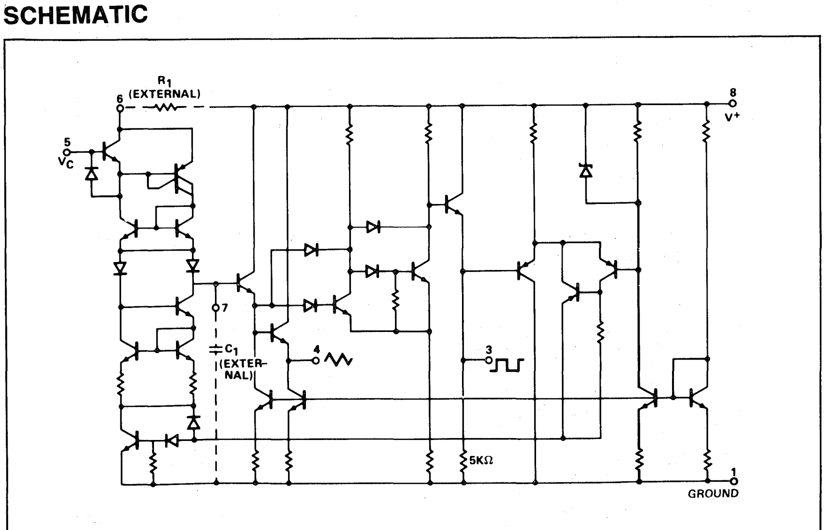
ABSOLUTE MAXIMUM RATINGS

Maximum Operating Voltage	26V
Storage Temperature	−65°C to 150°C
Power Dissipation	300mW

BLOCK DIAGRAM

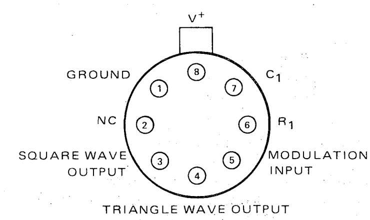


SCHEMATIC

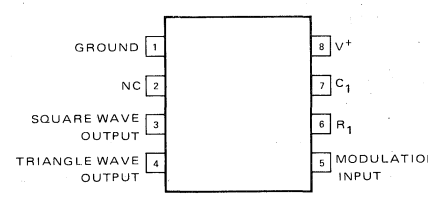


PIN CONFIGURATION

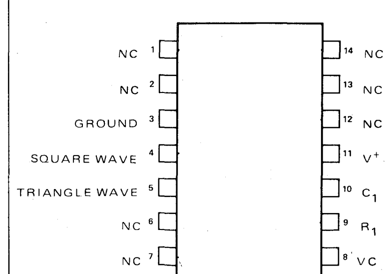
T PACKAGE



V PACKAGE



F PACKAGE



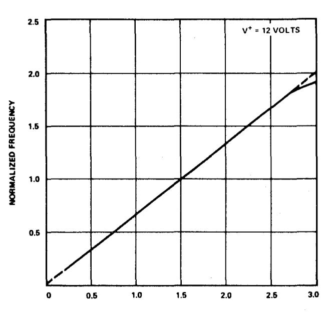
ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_{CC} = 12$ V unless otherwise stated

CHARACTERISTICS	SE566 MIN	SE566 TYP	SE566 MAX	NE566 MIN	NE566 TYP	NE566 MAX	UNITS
GENERAL							
Operating Temperature Range	−55		125	0		70	°C
Operating Supply Voltage			24			24	V
Operating Supply Current		7	12.5		7	12.5	mA
VCO (Note 1)							
Maximum Operating Frequency		1			1		MHz
Frequency Drift with Temperature		100			200		ppm/°C
Frequency Drift with Supply Voltage		1			2		%/V
Control Terminal Input Impedance (Note 2)		1			1		MΩ
FM Distortion (±10% Deviation)		0.2	0.75		0.2	1.5	%
Maximum Sweep Rate		1			1		MHz
Sweep Range		10:1			10:1		
OUTPUT							
Triangle Wave Output-							
Impedance		50			50		Ω
Voltage	1.9	2.4		1.9	2.4		V pp
Linearity		0.2			0.5		%
Square Wave Output-							
Impedance		50			50		Ω
Voltage	5	5.4		5	5.4		V pp
Duty Cycle	45	50	55	40	50	60	%
Rise Time		20			20		ns
Fall Time		50			50		ns

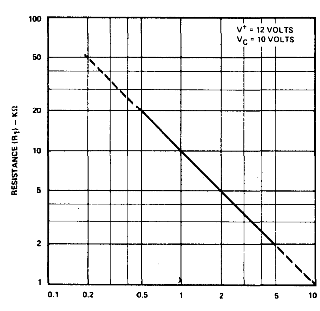
NOTES:
1. The external resistance for frequency adjustment (R_1) must have a value between 2kΩ and 20KΩ.
2. The bias voltage (Vc) applied to the control terminal (pin 5) whould be in the range $¾V+ \leq V_C \leq V+$.

TYPICAL PERFORMANCE CHARACTERISTICS

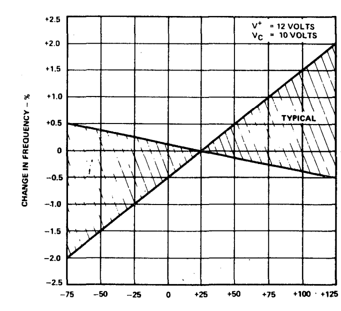
NORMALIZED FREQUENCY AS A FUNCTION OF CONTROL VOLTAGE



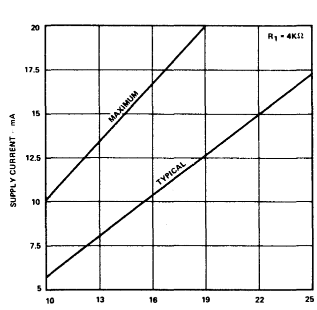
NORMALIZED FREQUENCY AS A FUNCTION OF RESISTANCE (R1)



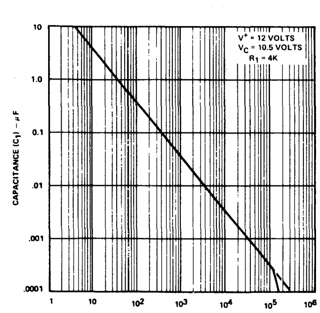
CHANGE IN FREQUENCY AS A FUNCTION OF TEMPERATURE



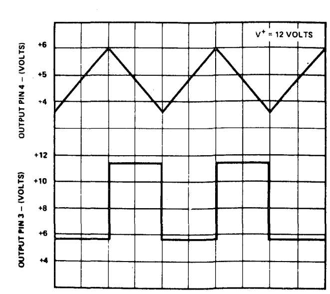
POWER SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



FREQUENCY AS A FUNCTION OF CAPACITANCE (C1)



VCO OUTPUT WAVEFORMS



OPERATING INSTRUCTIONS

The SE/NE 566 Function Generator is a general purpose voltage controlled oscillator designed for highly linear frequency modulation. The circuit provides simultaneous square wave and triangle wave outputs at frequencies up to 1 MHz. A typical connection diagram is shown in Figure 1. The control terminal (pin 5) must be biased externally with a voltage (VC) in the range

$$3/4\ V+ \leq V_C \leq V+$$

where V_{CC} is the total supply voltage. In Figure 1, the control voltage is set by the voltage divider formed with R_2 and R_3. The modulating signal is then ac coupled with the capacitor C_2. The modulating signal can be direct coupled as well, if the appropriate dc bias voltage is applied to the control terminal. The frequency is given approximately by

$$f_o \simeq \frac{2(V+ - V_C)}{R_1 C_1 V+}$$

and R_1 should be in the range $2K < R_1 < 20K\Omega$.

A small capacitor (typically 0.001 μf) should be connected between pins 5 and 6 to eliminate possible oscillation in the control current source.

If the VCO is to be used to drive standard logic circuitry, it may be desirable to use a dual supply of ±5 volts as shown in Figure 2. In this case the square wave output has the proper dc levels for logic circuitry. RTL can be driven directly from pin 3. For DTL or T^2L gates, which require a current sink of more than 1 mA, it is usually necessary to connect a 5KΩ resistor between pin 3 and negative supply. This increases the current sinking capability to 2 mA. The third type of interface shown uses a saturated transistor between the 566 and the logic circuitry. This scheme is used primarily for T^2L circuitry which requires a fast fall time (<50 nsec) and a large current sinking capability.

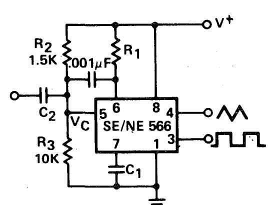


FIGURE 1

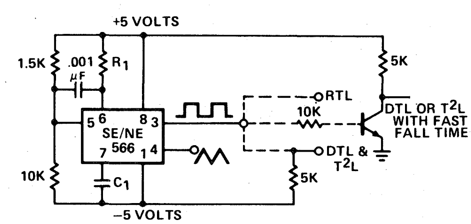


FIGURE 2

ANALOG

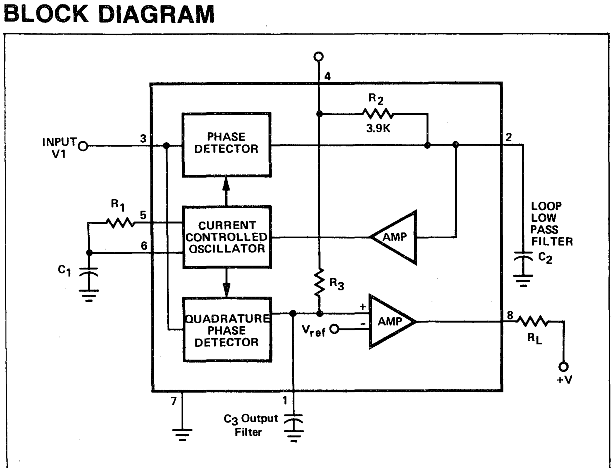
FEATURES
- WIDE FREQUENCY RANGE (.01Hz TO 500kHz)
- HIGH STABILITY OF CENTER FREQUENCY
- INDEPENDENTLY CONTROLLABLE BANDWIDTH (0 TO 14 PERCENT)
- HIGH OUT-BAND SIGNAL AND NOISE REJECTION
- LOGIC-COMPATIBLE OUTPUT WITH 100mA CURRENT SINKING CAPABILITY
- INHERENT IMMUNITY TO FALSE SIGNALS
- FREQUENCY ADJUSTMENT OVER A 20 TO 1 RANGE WITH AN EXTERNAL RESISTOR

APPLICATIONS
TOUCH TONE® DECODING
CARRIER CURRENT REMOTE CONTROLS
ULTRASONIC CONTROLS (REMOTE TV, ETC.)
COMMUNICATIONS PAGING
FREQUENCY MONITORING AND CONTROL
WIRELESS INTERCOM
PRECISION OSCILLATOR

ABSOLUTE MAXIMUM RATINGS

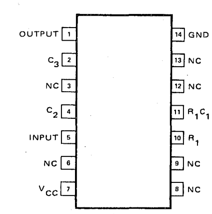
Operating Temperature	0°C to 70°C NE567 −55°C to 125°C SE567
Operating Voltage	10V
Positive Voltage at Input	0.5V above Supply Voltage (Pin 4)
Negative Voltage at Input	−10 VDC
Output Voltage (collector of output transistor)	15 VDC
Storage Temperature	−65°C to 150°C
Power Dissipation	300mW

BLOCK DIAGRAM

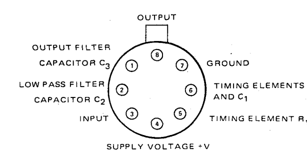


PIN CONFIGURATION

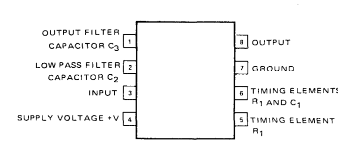
F PACKAGE



T PACKAGE



V PACKAGE



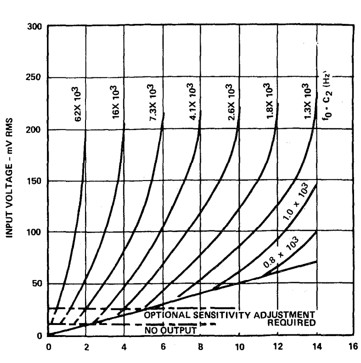
ELECTRICAL CHARACTERISTICS ($V+=5.0$ Volts, $T_A=25°C$ unless noted)

PARAMETER	TEST CONDITIONS	SE567 MIN	SE567 TYP	SE567 MAX	NE567 MIN	NE567 TYP	NE567 MAX	UNITS
CENTER FREQUENCY (NOTE 1)								
Highest Center Frequency (f_o)		100	500		100	500		kHz
Center Frequency Stability (Note 2)	−55 to 125°C		35±140			35±140		ppm/°C
	0 to 70°C		35±60			35±60		ppm/°C
Center Frequency Shift with Supply Voltage	f_o=100KHz		0.5	1		0.7	2	%/V
DETECTION BANDWIDTH								
Largest Detection Bandwidth	f_o=100KHz	12	14	16	10	14	18	% of fo
Largest Detection Bandwidth Skew			1	2		2	3	% of fo
Largest Detection Bandwidth—Variation with Temperature	V_i=300mVrms		±0.1			±0.1		%/°C
Largest Detection Bandwidth—Variation with Supply Voltage	V_i=300mVrms		±2			±2		%/V
INPUT								
Input Resistance			20			20		KΩ
Smallest Detectable Input Voltage(V_i)	I_L=100mA, f_i=t_o		20	25		20	25	mV rms
Largest No-Output Input Voltage	I_L=100mA, f_i=f_o	10	15		10	15		mV rms
Greatest Simultaneous Outband Signal to Inband Signal Ratio			+6			+6		dB
Minimum Input Signal to Wideband Noise Ratio	Bn=140KHz		−6			−6		dB
OUTPUT								
Fastest On-Off Cycling Rate			fo/20			fo/20		
"1" Output Leakage Current			0.01	25		0.01	25	μA
"0" Output Voltage	I_L=30mA		0.2	0.4		0.2	0.4	V
	I_L=100mA		0.6	1.0		0.6	1.0	V
Output Fall Time (Note 3)	R_L=50Ω		30			30		ns
Output Rise Time (Note 3)	R_L=50Ω		150			150		ns
GENERAL								
Operating Voltage Range		4.75		9.0	4.75		9.0	V
Supply Current Quiescent			6	8		7	10	mA
Supply Current—Activated	R_L=20KΩ		11	13		12	15	mA
Quiescent Power Dissipation			30			35		mW

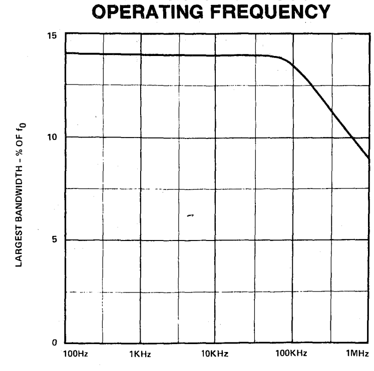
NOTES:
1. Frequency determining resistor R_1 should be between 1 and 20KΩ.
2. Applicable over 4.75 to 5.75 volts. See graphs for more detailed information.
3. Pin 8 to Pin 1 feedback R_L network selected to eliminate pulsing during turn-on and turn-off.

TYPICAL CHARACTERISTIC CURVES

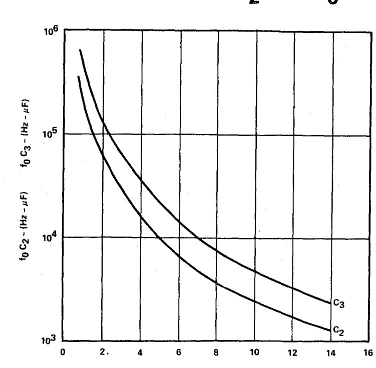
BANDWIDTH VERSUS INPUT SIGNAL AMPLITUDE



LARGEST DETECTION BANDWIDTH VERSUS OPERATING FREQUENCY

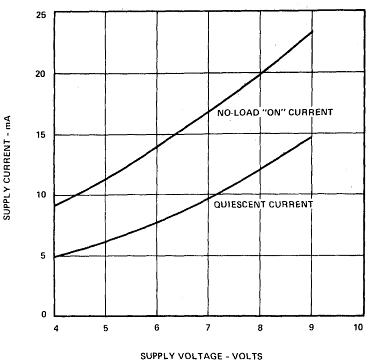


DETECTION BANDWIDTH AS A FUNCTION OF C_2 AND C_3

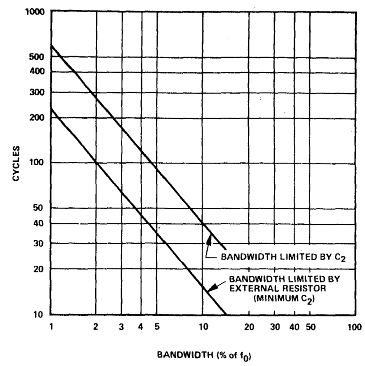


TYPICAL CHARACTERISTIC CURVES (CONT'D)

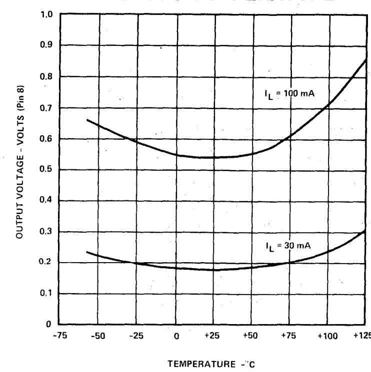
TYPICAL SUPPLY CURRENT VERSUS SUPPLY VOLTAGE



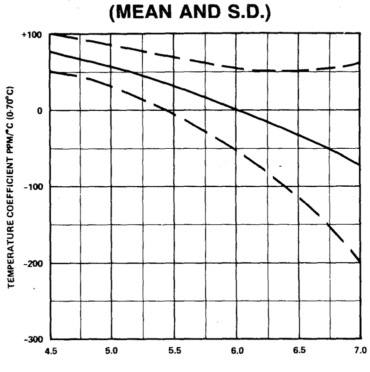
GREATEST NUMBER OF CYCLES BEFORE OUTPUT



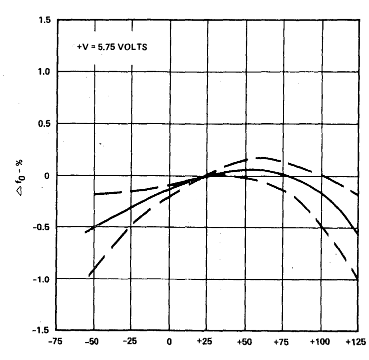
TYPICAL OUTPUT VOLTAGE VERSUS TEMPERATURE



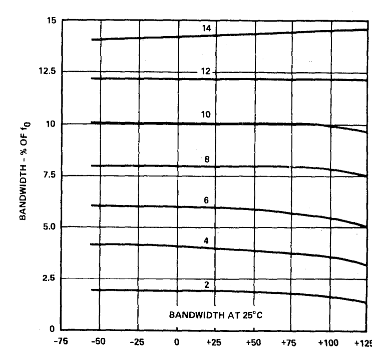
CENTER FREQUENCY COEFFICIENT TEMPERATURE (MEAN AND S.D.)



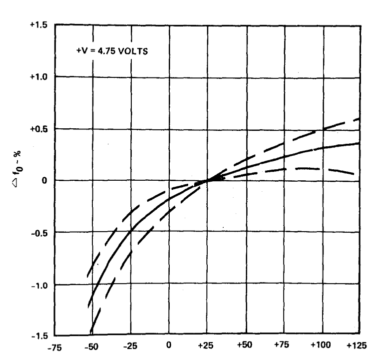
TYPICAL FREQUENCY DRIFT WITH TEMPERATURE (MEAN AND S.D.)



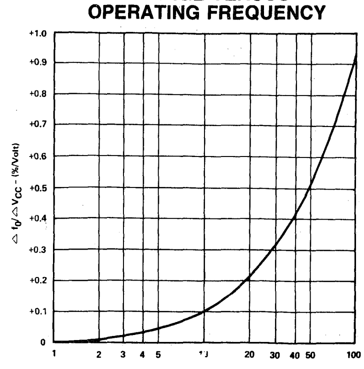
TYPICAL BANDWIDTH VARIATION WITH TEMPERATURE



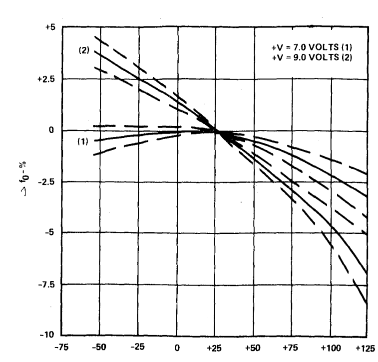
TYPICAL FREQUENCY DRIFT WITH (MEAN AND S.D.) TEMPERATURE



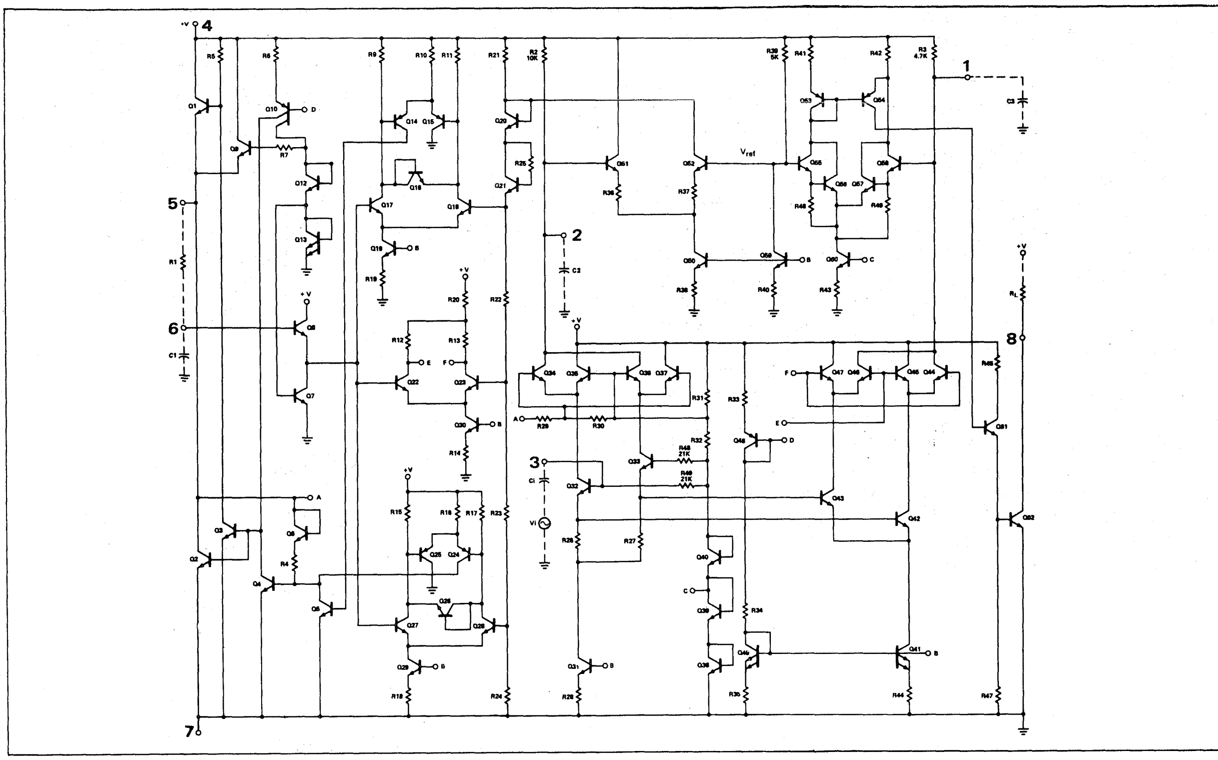
CENTER FREQUENCY SHIFT WITH SUPPLY VOLTAGE CHANGE VERSUS OPERATING FREQUENCY



TYPICAL FREQUENCY DRIFT WITH TEMPERATURE (MEAN AND S.D.)



SCHEMATIC DIAGRAM



DESIGN FORMULAS

$$f_0 \simeq \frac{1.1}{R_1C_1}$$

$$BW \simeq 1070\sqrt{\frac{V_i}{f_0C_2}} \text{ in \% of } f_0,\ V_{IN} \lesssim 200mV \text{ (RMS)}$$

Where
V_i=Input Voltage (Volts RMS)
C_2=Low-Pass Filter Capacitor (μF)

PHASE LOCKED LOOP TERMINOLOGY

CENTER FREQUENCY (f_0)

The free-running frequency of the current controlled oscillator (CCO) in the absence of an input signal.

DETECTION BANDWIDTH (BW)

The frequency range, centered about f_0, within which an input signal above the threshold voltage (typically 20mV rms) will cause a logical zero state on the output. The detection bandwidth corresponds to the loop capture range.

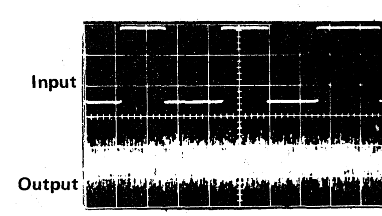
LARGEST DETECTION BANDWIDTH

The largest frequency range within which an input signal above the threshold voltage will cause a logical zero state on the output. The maximum detection bandwidth corresponds to the loop lock range.

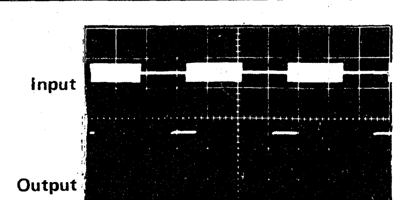
DETECTION BAND SKEW

A measure of how well the largest detection band is centered about the center frequency, f_0. The skew is defined as $(f_{max} + f_{min} - 2f_0)/f_0$ where fmax and fmin are the frequencies corresponding to the edges of the detection band. The skew can be reduced to zero if necessary by means of an optional centering adjustment.

TYPICAL RESPONSE



Response to 100mV RMS tone burst.
R_L = 100 ohms.



Response to same input tone burst with wideband noise.

$\frac{S}{N}$ = -6db $\qquad R_L$ = 100 ohms

Noise Bandwidth = 140 Hz

OPERATING INSTRUCTIONS

Figure 1 shows a typical connection diagram for the 567. For most applications, the following three-step procedure will be sufficient for choosing the external components R_1, C_1, C_2 and C_3.

1. Select R_1 and C_1 for the desired center frequency. For best temperature stability, R_1 should be between 2K and 20K ohm, and the R_1C_1 product should have sufficient stability, over the projected temperature range to meet the necessary requirements.
2. Select the low pass capacitor, C_2, by referring to the Bandwidth versus Input Signal Amplitude graph. If the input amplitude variation is known, the appropriate value of f_OC_2 necessary to give the desired bandwidth may be found. Conversely, an area of operation may be selected on this graph and the input level and C_2 may be adjusted accordingly. For example, constant bandwidth operation requires that input amplitude be above 200m Vrms. The bandwidth, as noted on the graph, is then controlled solely by the f_OC_2 product (F_O (Hz), C_2 (μfd).).
3. The value of C_3 is generally non-critical. C_3 sets the band edge of a low pass filter which attenuates frequencies outside the detection band to eliminate spurious outputs. If C_3 is too small, frequencies just outside the detection band will switch the output stage on and off at the beat frequency, or the output may pulse on and off during the turn-on transient. If C_3 is too large, turn-on and turn-off of the output stage will be delayed until the voltage on C_3 passes the threshold voltage. (Such delay may be desirable to avoid spurious outputs due to transient frequencies.) A typical minimum value for C_3 is $2C_2$.

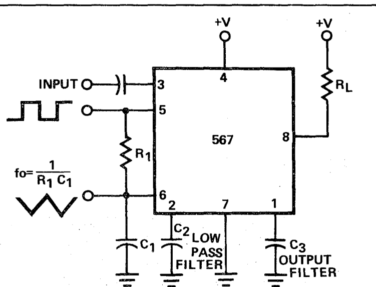


FIGURE 1

AVAILABLE OUTPUTS (Figure 2)

The primary output is the uncommitted output transistor collector, pin 8. When an in-band input signal is present, this transistor saturates; its collector voltage being less than 1.0 volt (typically 0.6V) at full output current (100mA). The voltage at pin 2 is the phase detector output, a linear function of frequency, over the range of 0.95 to 1.05 f0, with a slope of about 20mV/% frequency deviation. The average voltage at pin 1 is, during lock, a function of the inband input amplitude in accordance with the transfer characteristic given. Pin 5 is the controlled oscillator square wave output of magnitude ($V+ -2Vbe$)$\approx$($V+ -1.4V$) having a dc average of V+/2. A 1KΩ load may be driven from pin 5. Pin 6 is an exponential traingle of 1 volt peak-to-peak with an average dc level of V+/2. Only high impedance loads may be connected to pin 6 without affecting the CCO duty cycle or temperature stability.

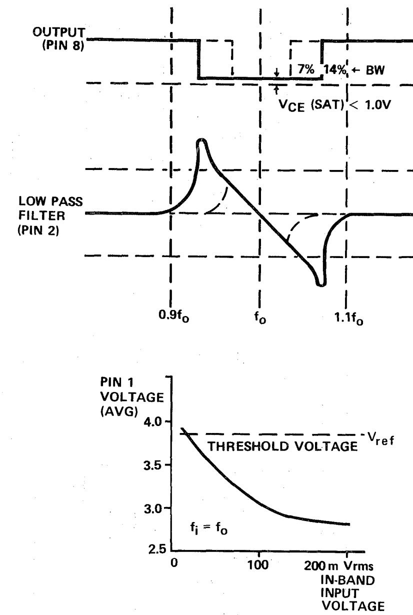


FIGURE 2

OPERATING PRECAUTIONS

A brief review of the following precautions will help the user attain the high level of performance of which the 567 is capable.

1. Operation in the high input level mode (above 200mV) will free the user from bandwidth variations due to changes in the in-band signal amplitude. The input stage is now limiting, however, so that out-band signals or high noise levels can cause an apparent bandwidth reduction as the in band signal is suppressed. Also, the limiting action will create in-band components from sub-harmonic signals, so the 567 becomes sensitive to signals at $f_O/3$, $f_O/5$, etc.
2. The 567 will lock onto signals near $(2n+1)\,f_O$, and will give an output for signals near $(4n+1)\,f_O$ where n=0, 1, 2, etc. Thus, signals at 5 f_O and 9 f_O can cause an unwanted output. If such signals are anticipated, they should be attenuated before reaching the 567 input.
3. Maximum immunity from noise and out-band signals is afforded in the low input level (Below 200mVrms) and reduced bandwidth operating mode. However, decreased loop damping causes the worse-case lock-up time to increase, as shown by the Greatest Number of Cycles Before Output vs. Bandwidth graph.
4. Due to the high switching speeds (20ns) associated with 567 operation, care should be taken in lead routing. Lead lengths should be kept to a minimum. The power supply should be adequately bypassed close to the 567 with an 0.01μF or greater capacitor; grounding paths should be carefully chosen to avoid ground loops and unwanted voltage variations. Another factor which must be considered is the effect of load energization on the power supply. For example, an incandescent lamp typically draws 10 times rated current at turn-on. This can cause supply voltage fluctuations which could, for example, shift the detection band of narrow-band systems sufficiently to cause momentary loss of lock. The result is a low-frequency oscillation into and out of lock. Such effects can be prevented by supplying heavy load currents from a separate supply, or increasing the supply filter capacitor.

SPEED OF OPERATION

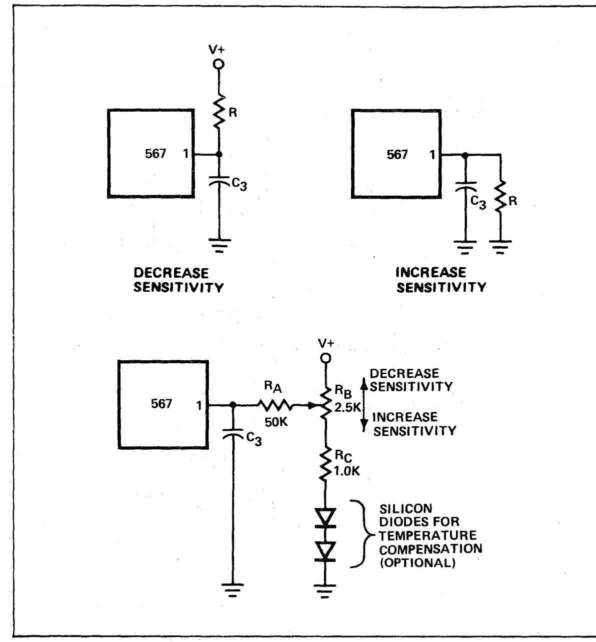
Minimum lock-up time is related to the natural frequency of the loop. The lower it is, the longer becomes the turn-on transient. Thus, maximum operating speed is obtained when C_2 is at a minimum. When the signal is first applied, the phase may be such as to initially drive the controlled oscillator **away** from the incoming frequency rather than toward it. Under this condition, which is of course unpredictable, the lock-up is transient is at its worst and the theoretical minimum lock-up time is not achievable. We must simply wait for the transient to die out.

The following expressions give the values of C_2 and C_3 which allow highest operating speeds for various band center frequencies. The minimum rate at which digital information may be detected without information loss due to the turn-on transient or output chatter is about 10 cycles per bit, corresponding to an information transfer rate of $f_0/10$ baud.

$$C_2 = \frac{130}{f_o}\ \mu F$$

$$C_3 = \frac{260}{f_o}\ \mu F$$

In cases where turn-off time can be sacrificed to achieve fast turn-on, the optional sensitivity adjustment circuit can be used to move the quiescent C_3 voltage lower (closer to the threshold voltage). However, sensitivity to beat frequencies, noise and extraneous signals will be increased.



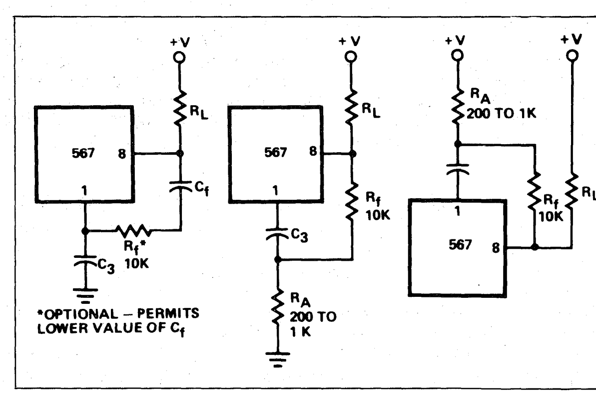
OPTIONAL CONTROLS

The 567 has been designed so that, for most applications, no external adjustments are required. Certain applications, however, will be greatly facilitated if full advantage is taken of the added control possibilities available through the use of additional external components. In the diagrams given, typical values are suggested where applicable. For best results resistors used, except where noted, should have the same temperature coefficient. Ideally, silicon diodes would be low-resistivity types, such as forward-biased transistor base-emitter junctions. However, ordinary low-voltage diodes should be adequate for most applications.

SENSITIVITY ADJUSTMENT

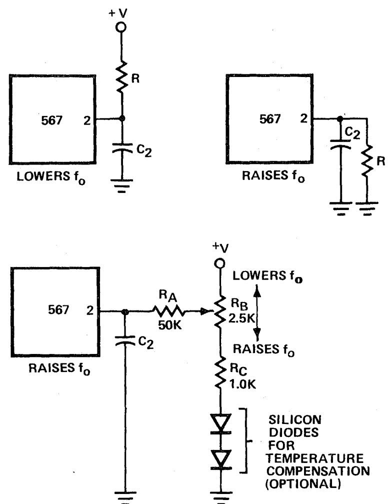
When operated as a very narrow band detector (less than 8 percent), both C_2 and C_3 are made quite large in order to improve noise and outband signal rejection. This will inevitably slow the response time. If, however, the output stage is biased closer to the threshold level, the turn-on time can be improved. This is accomplished by drawing additional current to terminal 1. Under this condition, the 567 will also give an output for lower-level signals (10m or lower).

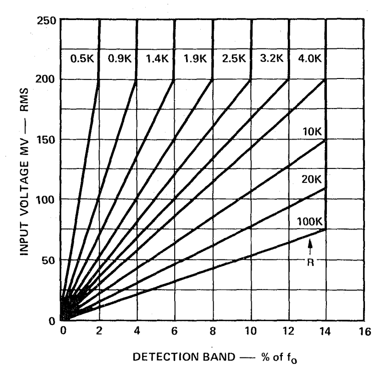
By adding current to terminal 1, the output stage is biased further away from the threshold voltage. This is most useful when, to obtain maximum operating speed, C_2 and C_3 are made very small. Normally, frequencies just outside the detection band could cause false outputs under this condition. By desensitizing the output stage, the outband beat notes do not feed through to the output stage. Since the input level must be somewhat greater when the output stage is made less sensitive, rejection of third harmonics or in-band harmonics (of lower frequency signals) is also improved.

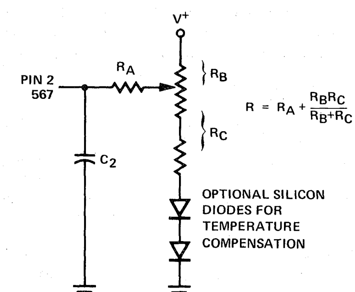


CHATTER PREVENTION

Chatter occurs in the output stage when C_3 is relatively small, so that the lock transient and the AC components at the quadrature phase detector (lock detector) output cause the output stage to move through its threshold more than once. Many loads, for example lamps and relays, will not respond to the chatter. However, logic may recognize the chatter as a series of outputs. By feeding the output stage output back to its input, (pin 1) the chatter can be eliminated. Three schemes for doing this are given above. All operate by feeding the first output step (either on or off) back to the input, pushing the input past the threshold until the transient conditions are over. It is only necessary to assure that the feedback time constant is not so large as to prevent operation at the highest anticipated speed. Although chatter can always be eliminated by making C_3 large, the feedback circuit will enable faster operation of the 567 by allowing C_3 to be kept small. Note that if the feedback time constant is made quite large, a short burst at the input frequency can be stretched into a long output pulse. This may be useful to drive, for example, stepping relays.







$$\frac{130}{f_o}\left(\frac{10K + R}{R}\right) < C_2 < \frac{1300}{f_o}\left(\frac{10K + R}{R}\right)$$

NOTE: Adjust control for symmetry o, detection band edges about fo.

DETECTION BAND CENTERING (OR SKEW) ADJUSTMENT

When is is desired to alter the location of the detection band (corresponding to the loop capture range) within the largest detection band (lock range), the circuits shown above can be used. By moving the detection band to one edge of the range, for example, input signal variations will expand the detection band in only one direction. This may prove useful when a strong but undesirable signal is expected on one side or the other of the center frequency. Since RB also alters the duty cycle slightly, this method may be used to obtain a precise duty cycle when the 567 is used as an oscillator.

ALTERNATE METHOD OF BANDWIDTH REDUCTION

Although a large value of C_2 will reduce the bandwidth, it also reduces the loop damping so as to slow the circuit response time. This may be undesirable. Bandwidth can be reduced by reducing the loop gain. This scheme will improve damping and permit faster operation under narrow-band operation. Note that the reduced impedance level at terminal 2 will require that a larger value of C_2 be used for a given filter cutoff frequency. If more than three 567s are to be used, the R_B, R_C network can be eliminated and the R_A resistors connected together. A capacitor between this junction and ground may be required to shunt high frequency components.

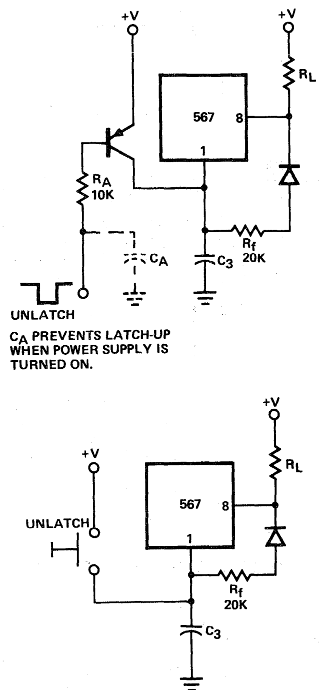
OUTPUT LATCHING

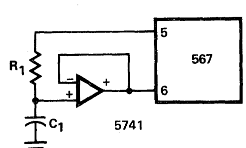
To latch the output on after a signal is received, it is necessary to provide a feedback resistor around the output stage (between pins 8 and 1). Pin 1 is pulled up to unlatch the output stage.

REDUCTION OF C1 VALUE

For precision, very low-frequency applications, where the value of C_1 becomes large, an overall cost savings may be achieved by inserting a voltage follower between the R_1 C_1 junction and pin 6, so as to allow a higher value of R_1 and a lower value of C_1 for a given frequency.

OUTPUT LATCHING (Cont'd)



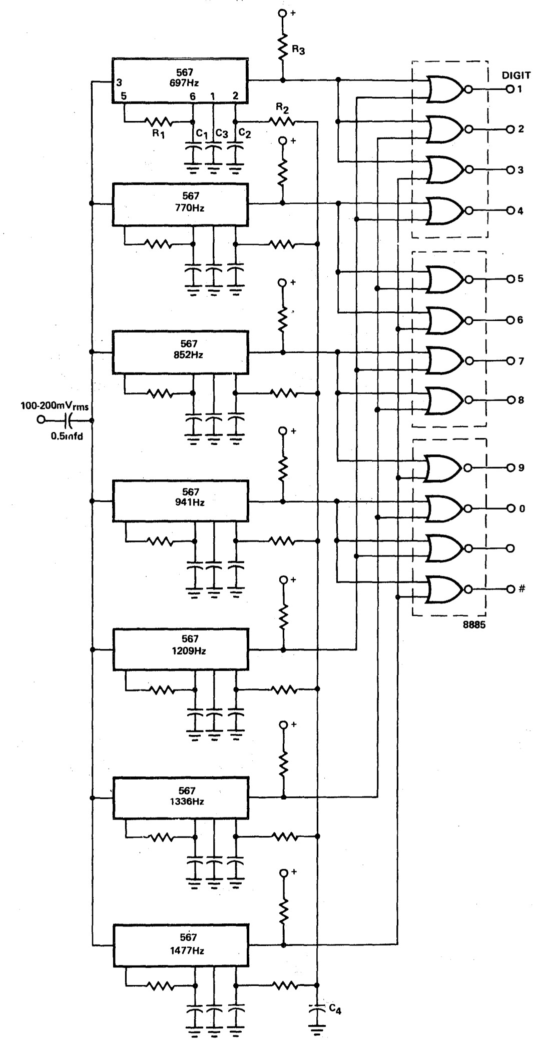


PROGRAMMING

To change the center frequency, the value of R_1 can be changed with a mechanical or solid state switch, or additional C_1 capacitors may be added by grounding them through saturating npn transistors.

TYPICAL APPLICATIONS

TOUCH-TONE ® DECODER

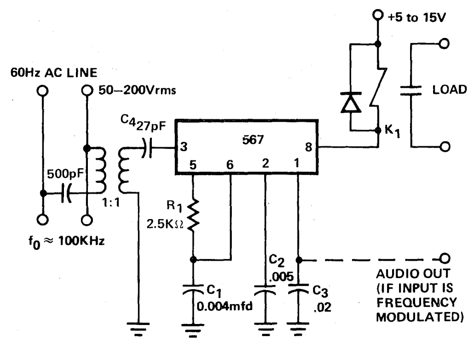


Component Values (Typical)

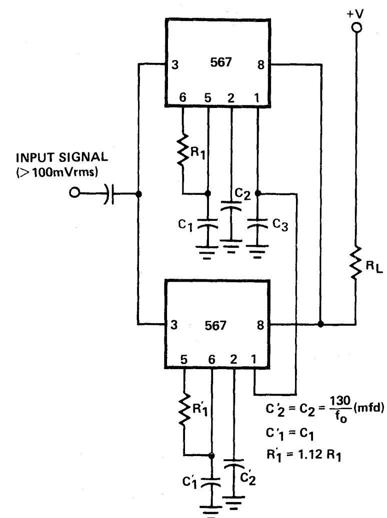
R_1	6.8 to 15K ohm
R_2	4.7K ohm
R_3	20K ohm
C_1	0.10 mfd
C_2	1.0 mfd 6V
C_3	2.2mfd 6V
C_4	250 μF 6V

TYPICAL APPLICATIONS (Cont'd)

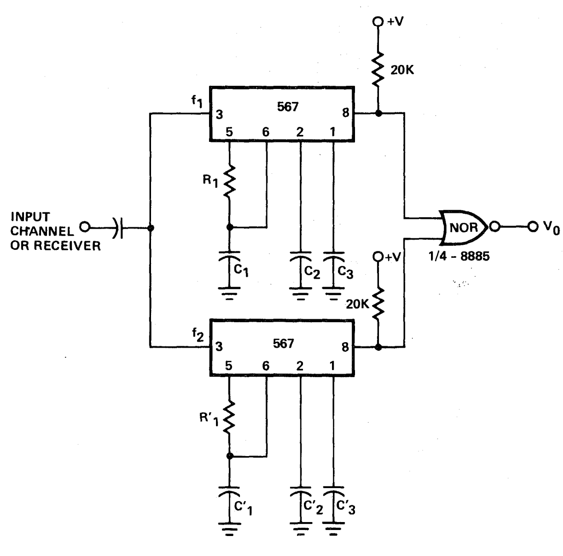
CARRIER-CURRENT REMOTE CONTROL OR INTERCOM



24% BANDWIDTH TONE DECODER

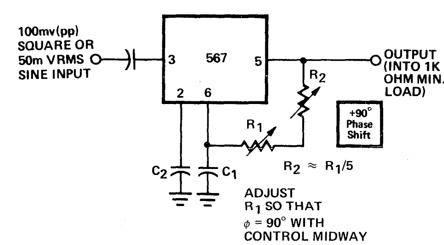


DUAL-TONE DECODER



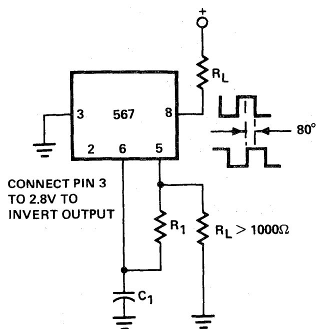
1. Resistor and capacitor values chosen for desired frequencies and bandwidth.
2. If C_3 is made large so as to delay turn-on of the top 567, decoding of sequential (f_1, f_2) tones is possible.

0° TO 180° PHASE SHIFTER

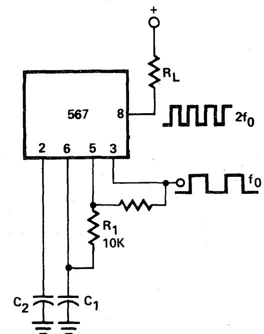


TYPICAL APPLICATIONS (Cont'd.)

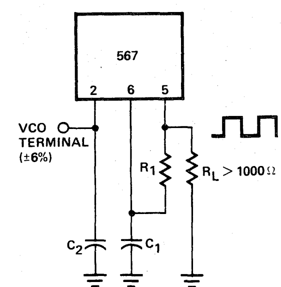
OSCILLATOR WITH QUADRATURE OUTPUT



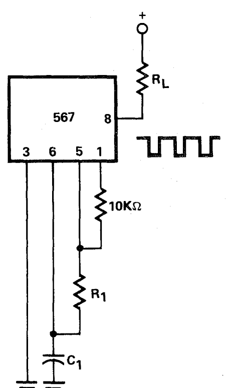
OSCILLATOR WITH DOUBLE FREQUENCY OUTPUT



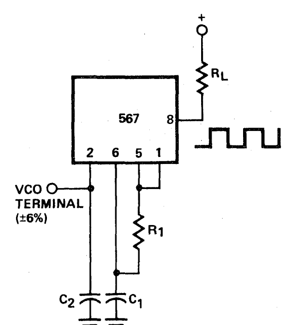
PRECISION OSCILLATOR WITH 20ns SWITCHING



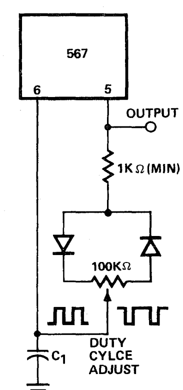
PULSE GENERATOR WITH 25% DUTY CYCLE



PRECISION OSCILLATOR TO SWITCH 100ma LOADS



PULSE GENERATOR



FEATURES

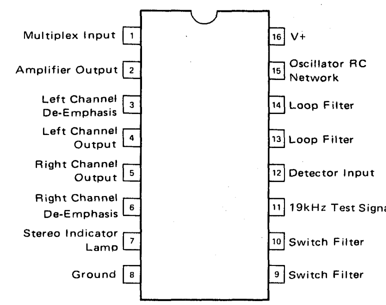
- **45dB CHANNEL SEPARATION**
- **AUTOMATIC STEREO/MONO SWITCHING**
- **70dB SCA REJECTION**
- **10V to 16V SUPPLY RANGE**
- **HIGH IMPEDANCE INPUT — LOW IMPEDANCE OUTPUT**

ABSOLUTE MAXIMUM RATINGS

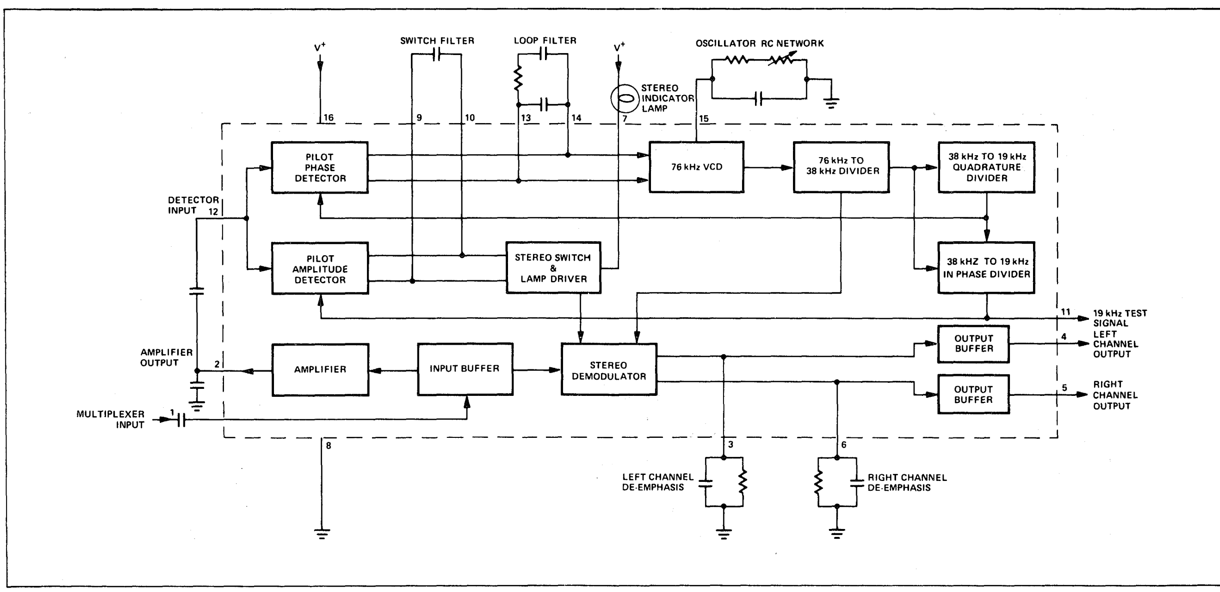
Supply Voltage	+18V
Supply Voltage (≤15 Seconds)	+22V
Voltage at Lamp Driver Terminal (LAMP OFF)	+22V
Internal Power Dissipation 730mW	
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−55°C to +125°C
Lead Temperature (60 Seconds)	300°C

PIN CONFIGURATION

B PACKAGE



BLOCK DIAGRAM

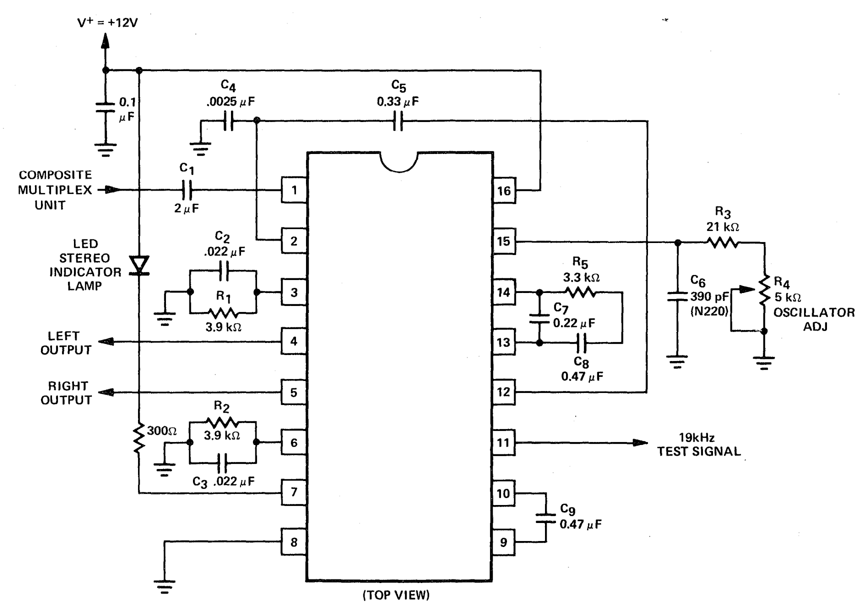


ELECTRICAL CHARACTERISTICS (T_A = 25°C, V+ = +12V, 19 kHz pilot level = 30 mVRMS, Multiplex Signal (L = R, pilot OFF) = 300 mVRMS, Modulation Frequency = 400 Hz or 1 kHz, Test Circuit 1, unless otherwise specified)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current	Lamp OFF		26	35	mA
Maximum Available Lamp Current		75	150		mA
Voltage at Lamp Driver Terminal	LAMP = 50 mA		1.3	1.8	V
DC Voltage Shift at Either Output Terminal	Stereo to Mono Operation		30	150	mV
Power Supply Ripple Rejection	200 Hz, 200 mV_{RMS}	35			dB
Input Resistance		20	35		kΩ
Output Resistance		0.9	1.3	2.0	kΩ
Channel Separation	100 Hz		40		dB
	400 Hz	30	45		dB
	10 kHz		45		dB
Channel Balance			0.3	1.5	dB
Voltage Gain	1 kHz	0.5	0.9	1.4	V/V
Pilot Input Level	Lamp Turn-On		15	20	mV_{RMS}
	Lamp Turn-Off	2.0	7.0		mV_{RMS}
Pilot Input Level Hysteresis	Lamp Turn-Off to Turn-On	3.0	7.0		dB
Capture Range		2.0	4.0	6.0	%
Total Harmonic Distortion	Multiplex Level = 600 mV_{RMS} Pilot OFF		0.4	1.0	%
19 kHz Rejection		25	35		dB
38 kHz Rejection		25	45		dB
SCA Rejection (Note 1)			70		dB
VCO Tuning Resistance (Note 2)		21.0	23.3	25.5	kΩ
VCO Frequency Drift	0°C≤T_A ≤25°C		+0.1	±2	%
	25°C≤T_A ≤70°C		−0.4	±2	%

NOTES:
1. Measured with a stereo composite signal consistency of 80% stereo, 10% pilot and 10% SCA as defined in the FCC Rules of Broadcasting.
2. Total resistance from pin 15 to ground, in test circuit 1, required to set reference frequency at pin 11 to 19 kHz ± 10 Hz.

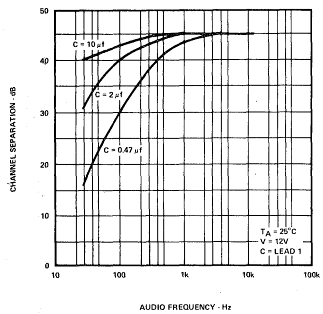
TEST CIRCUIT 1 AND TYPICAL APPLICATION



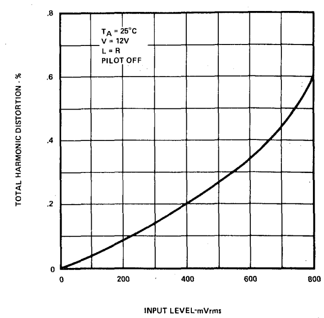
NOTE:
Tolerance on resistors is ±5% and tolerance on capacitors is ±20% unless otherwise specified. C1 Tolerance = +100%, −20%, C6 Tolerance = ±1% in test circuit and ±5% in typical applications, R3 Tolerance = ±1%, R4 Tolerance = ±10%, R1 and R2 Tolerances = ±1% in test circuit and ±5% in typical application.

TYPICAL CHARACTERISTICS CURVES

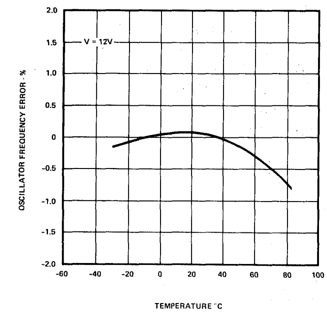
CHANNEL SEPARATION VS AUDIO FREQUENCY



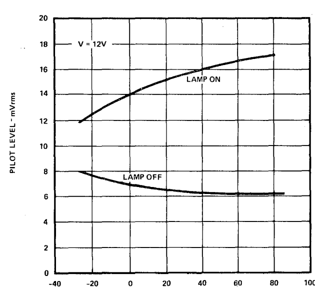
HARMONIC DISTORTION VS INPUT LEVEL



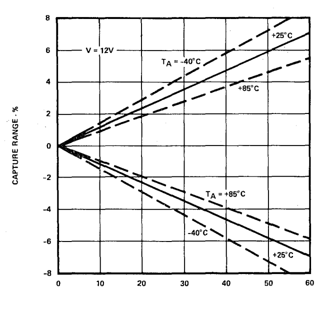
OSCILLATOR FREE RUNNING FREQUENCY ERROR VS AMBIENT TEMPERATURE



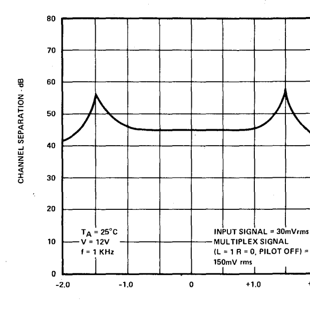
LAMP TURN ON & TURN OFF SENSITIVITY VS AMBIENT TEMPERATURE



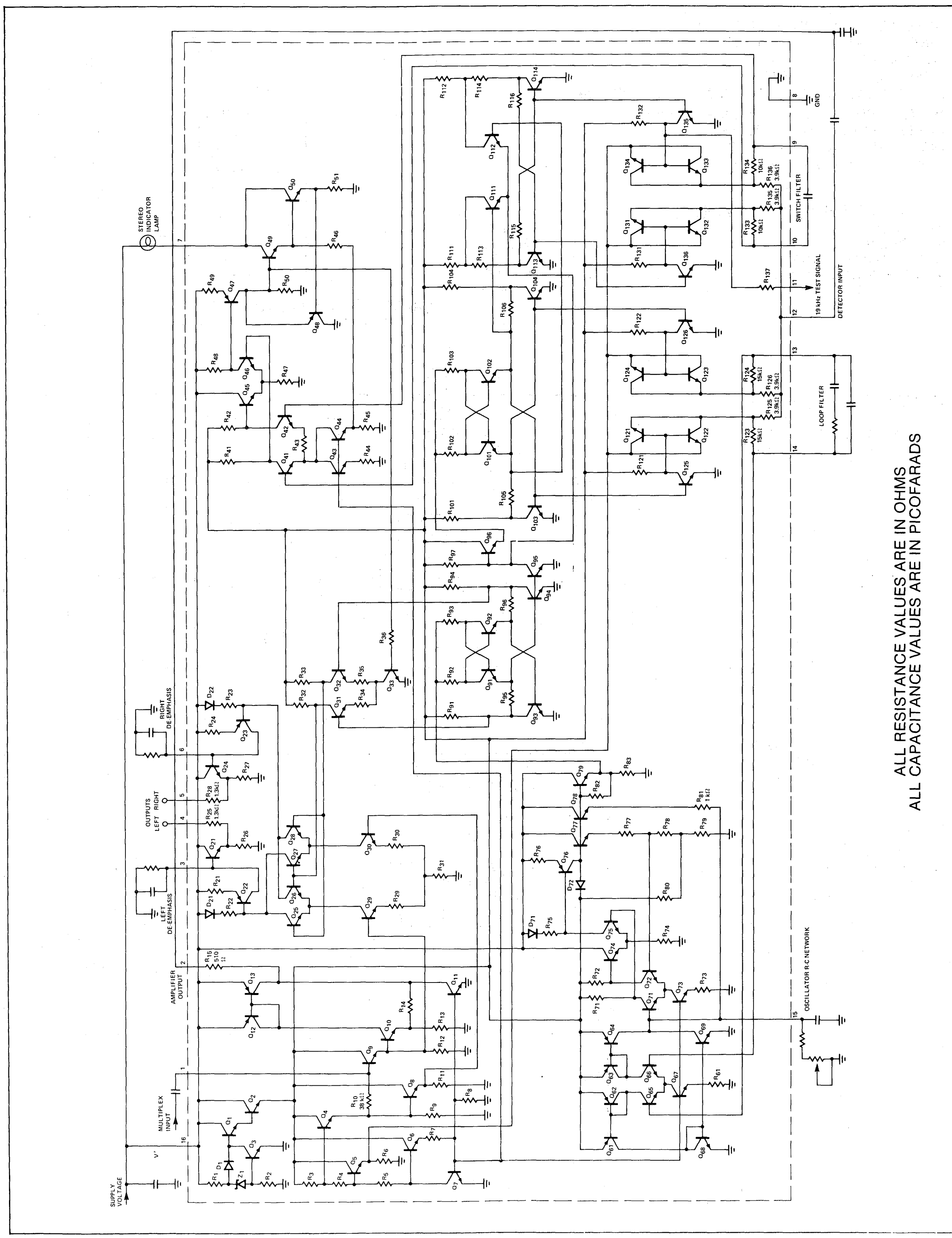
CAPTURE RANGES VS PILOT LEVEL



CHANNEL SEPARATION VS OSCILLATOR FREE RUNNING FREQUENCY ERROR



EQUIVALENT CIRCUIT

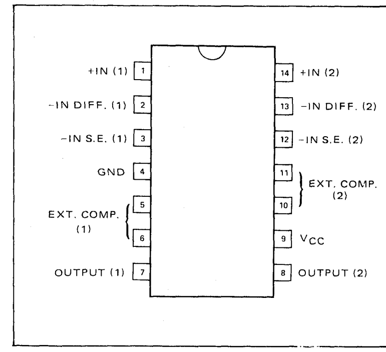


ANALOG

FEATURES

- LOW NOISE — .5μV TOTAL INPUT NOISE
- HIGH GAIN — 112dB OPEN LOOP
- SINGLE SUPPLY OPERATION
- WIDE SUPPLY RANGE 9 TO 40V
- POWER SUPPLY REJECTION — 120dB
- LARGE OUTPUT VOLTAGE SWING (V_{CC} −2V p-p)
- WIDE BANDWIDTH — 15MHz UNITY GAIN
- POWER BANDWIDTH — 75kHz, 20V p-p
- INTERNALLY COMPENSATED
- SHORT CIRCUIT PROTECTED

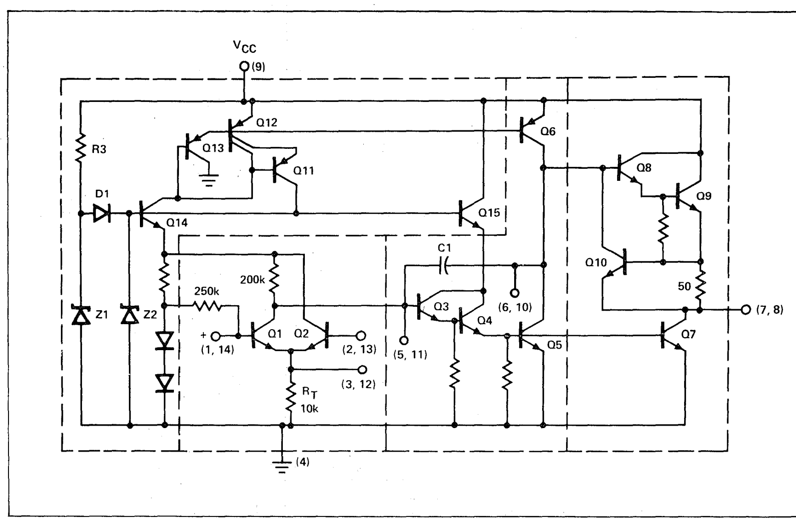
PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

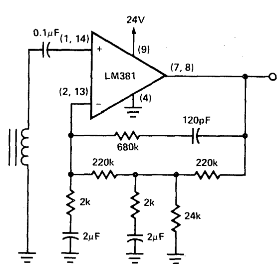
Supply Voltage	+40V
Power Dissipation	600mW
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 sec)	+300°c

EQUIVALENT CIRCUIT

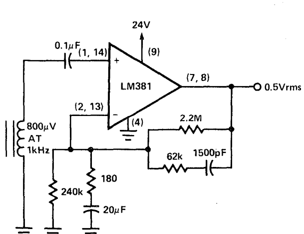


TYPICAL APPLICATIONS

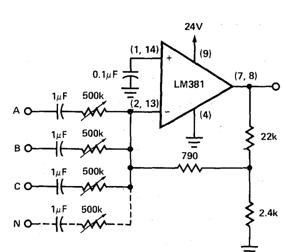
TWO-POLE FAST TURN-ON NAB TAPE PREAMP



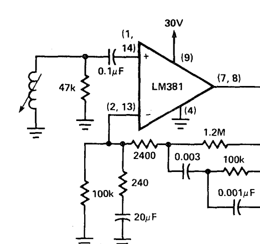
TYPICAL MAGNETIC PHONO PREAMP



TYPICAL MAGNETIC PHONO PREAMP



AUDIO MIXER



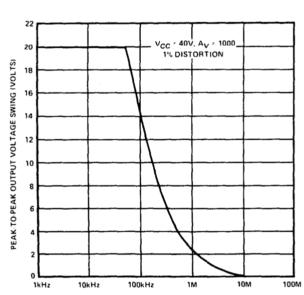
ELECTRICAL CHARACTERISTICS T_A = +25°C, V_{CC} = 14V (Unless Otherwise Noted)

PARAMETER	TEST CONDITIONS	LIMITS MIN	TYP	MAX	UNIT
Voltage Gain	Open Loop (Differential Input)		160,000		V/V
	Open Loop (Single Ended)		320,000		V/V
Supply Current	V_{CC} 9 to 40V, RL = ∞		10		mA
Input Resistance (Positive Input)			100		kΩ
(Negative Input)			200		kΩ
Input Current (Negative Input)			0.5		μA
Output Resistance	Open Loop		150		Ω
Output Current	Source		8		mA
	Sink		2		mA
Output Voltage Swing	Peak-to-Peak		V_{CC} −2		V
Small Signal Bandwidth			15		MHz
Power Bandwidth	20V p-p (V_{CC} = 24V)		75		kHz
Maximum Input Voltage	Linear Operation			300	mVrms
Supply Rejection Ratio	f = 1kHz		120		dB
Channel Separation	f = 1kHz		60		dB
Total Harmonic Distortion	75dB Gain, f = 1kHz		0.1		%
Total Equivalent Input Noise	RS = 600Ω, 100−10,000Hz (Single Ended Input)				
LM381A			0.5	0.7	μVrms
LM381			0.5	1.0	μVrms
Noise Figure	50kΩ, 100—10,000Hz (Single Ended Input)		⅛.?		DB
	10kΩ, 100—10,000Hz (Single Ended Input)		1.3		dB
	5kΩ, 100—10,000Hz (Single Ended Input)		1.6		dB

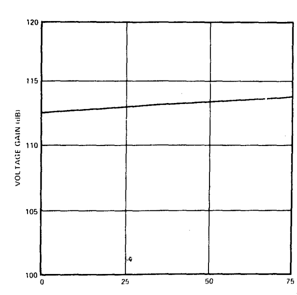
NOTE: ALL RESISTORS STANDARD AND ARE MEASURED IN OHMS.

TYPICAL CHARACTERISTICS

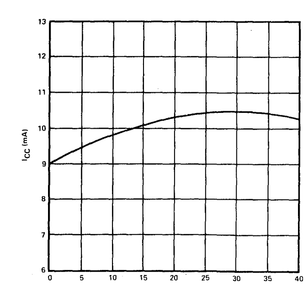
LARGE SIGNAL FREQUENCY RESPONSE



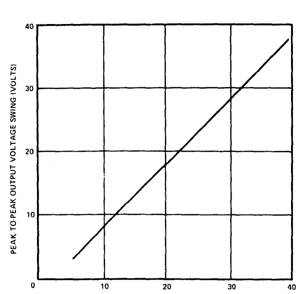
GAIN VS TEMPERATURE



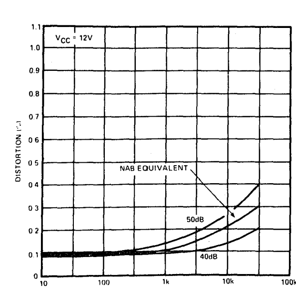
V_{CC} VS I_{CC}



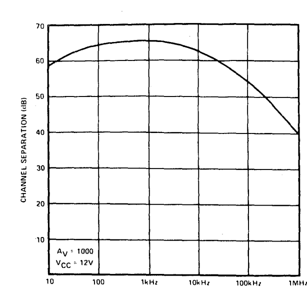
I-P OUTPUT VOLTAGE VS V_{CC}



% DISTORTION

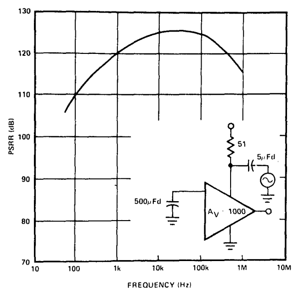


CHANNEL SEPARATION

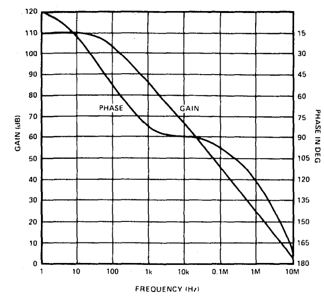


TYPICAL CHARACTERISTICS (Cont'd)

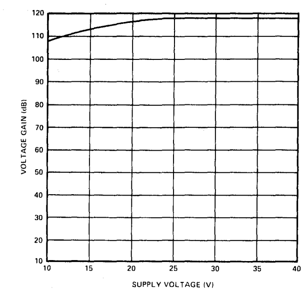
PSRR VS FREQUENCY



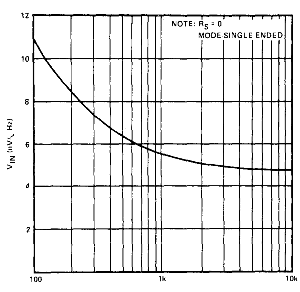
GAIN AND PHASE RESPONSE



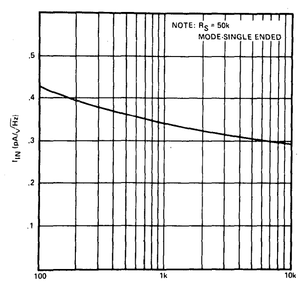
VOLTAGE GAIN VS SUPPLY VOLTAGE



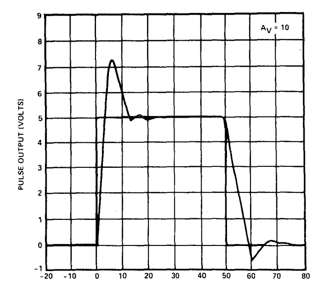
NOISE CURRENT VS FREQUNCY



NOISE VOLTAGE VS FREQUENCY



PULSE RESPONSE



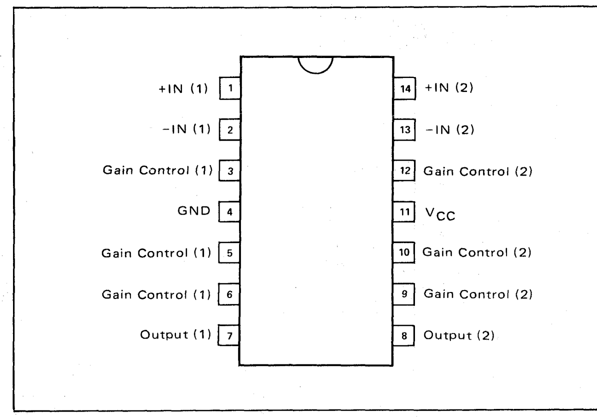
FEATURES

- LOW NOISE — 0.8μV TOTAL EQUIVALENT INPUT NOISE
- HIGH GAIN — 100dB OPEN LOOP
- SINGLE SUIPLY OPERATION
- WIDE SUPPLY RANGE 9 TO 40V
- POWER SUPPLY REJECTION — 120dB
- LARGE OUTPUT VOLTAGE SWING
- WIDE BANDWIDTH — 15MHz UNITY GAIN
- POWER BANDWIDTH — 75kHz, 20V p-p
- INTERNALLY COMPENSATED
- SHORT CIRCUIT PROTECTED

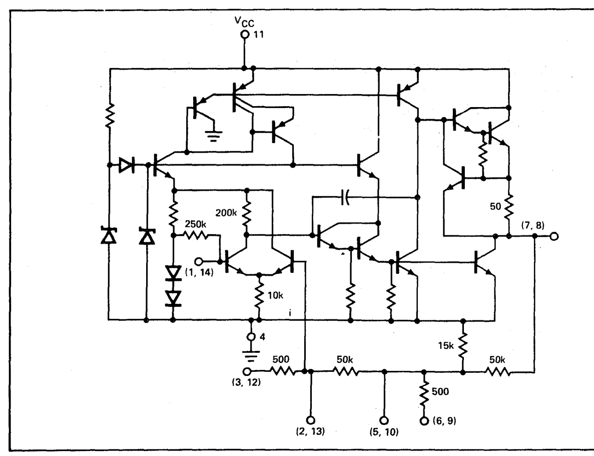
ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+40V
Power Dissipation	600mW
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 sec)	+300°C

PIN CONFIGURATION



EQUIVALENT CIRCUIT

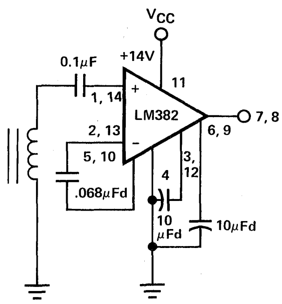


ELECTRICAL CHARACTERISTICS $T_A = +25°C$, $V_{CC} = 14V$ (Unless Otherwise Noted)

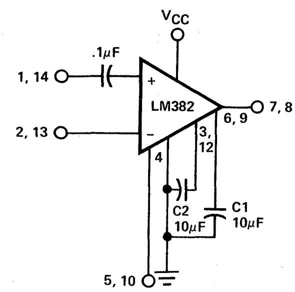
PARAMETER	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT
Voltage Gain	Open Loop (Differential Input)		100,000		V/V
Supply Current	V_{CC} 9 to 40V, $R_L = \infty$		10	16	mA
Input Resistance					
(Positive Input)			100		kΩ
(Negative Input)			200		kΩ
Input Current					
(Negative Input)			0.5		μA
Output Resistance	Open Loop		150		Ω
Output Current	Source		8		mA
	Sink		2		mA
Output Voltage Swing	Peak-to-Peak, R_L = 10k		$V_{CC}-2$		V
Small Signal Bandwidth			15		MHz
Power Bandwidth	20V p-p (V_{CC} = 24V)		75		kHz
Maximum Input Voltage	Linear Operation			300	mVrms
Supply Rejection Ratio	f = 1kHz		120		dB
Channel Separation	f = 1kHz	40	60		dB
Total Harmonic Distortion	60dB Gain, f = 1kHz		0.1	0.3	%
Total Equivalent Input Noise	R_S = 600Ω, 100−10,000Hz		0.8	1.2	μVrms
Noise Figure	50kΩ, 100−10,000Hz		1.0		dB
	10kΩ, 100−10,000Hz		1.6		dB
	5kΩ, 100−10,000Hz		2.8		dB

TYPICAL APPLICATIONS

TAPE PREAMPLIFIER (NAB EQUALIZATION)

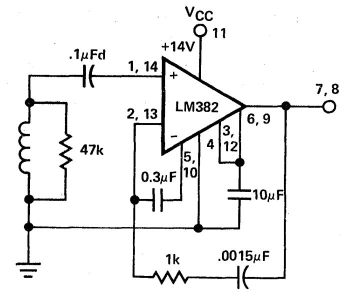


FLAT RESPONSE FIXED GAIN CONFIGURATION



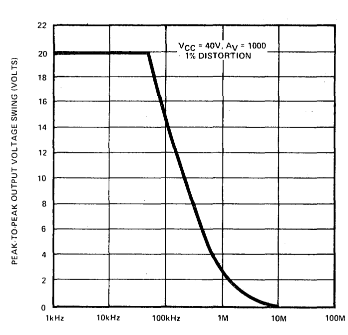
CAPACITOR	GAIN
C1 Only	40dB
C2 Only	55dB
C1 & C2	80dB

PHONO PREAMP (RIAA EQUALIZATION)

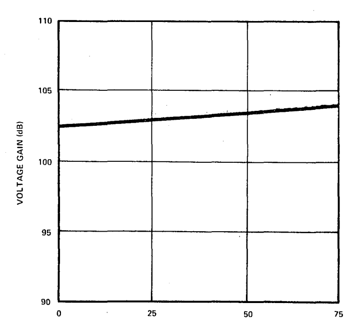


TYPICAL CHARACTERISTICS CURVES

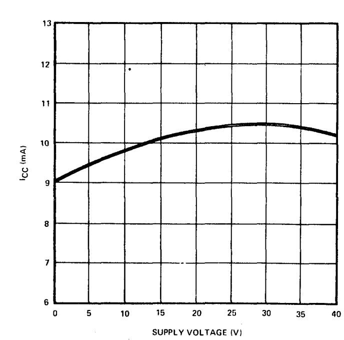
LARGE SIGNAL FREQUENCY RESPONSE



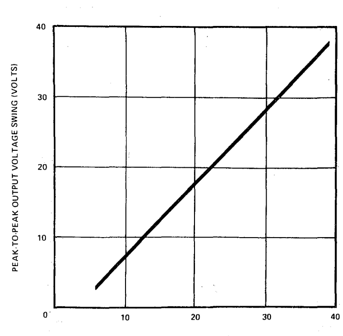
GAIN VS TEMPERATURE



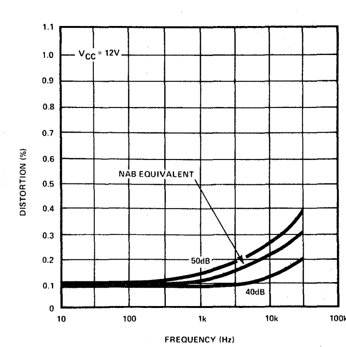
V_{CC} VS I_{CC}



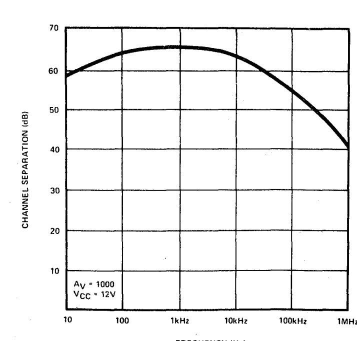
P-P OUTPUT VOLTAGE SWING VS V_{CC}



% DISTORTION

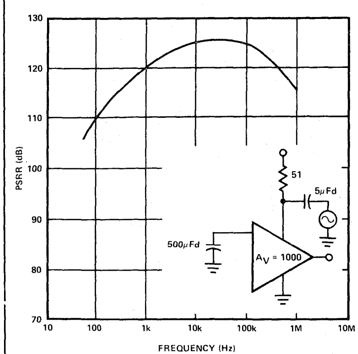


CHANNEL SEPARATION

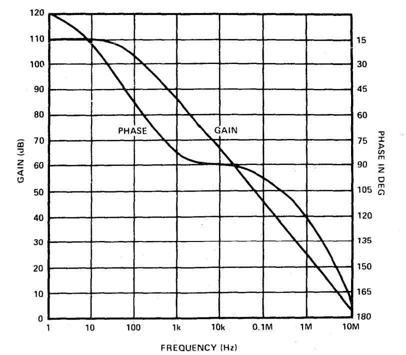


TYPICAL CHARACTERISTICS (Continued)

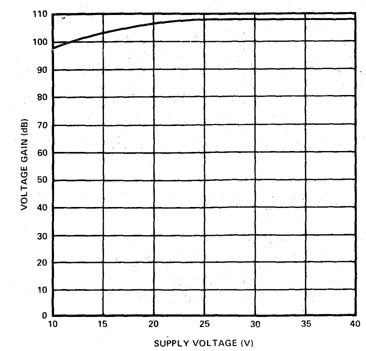
PSRR VS FREQUENCY



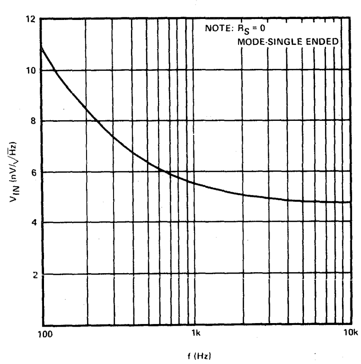
GAIN AND PHASE RESPONSE



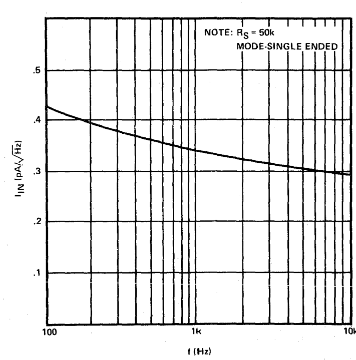
VOLTAGE GAIN VS SUPPLY VOLTAGE



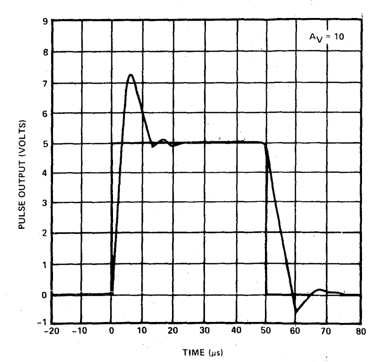
NOISE VOLTAGE VS FREQUENCY



NOISE CURRENT VS FREQUENCY



PULSE RESPONSE



ANALOG

DUAL LOW-NOISE PREAMP — LM387

FEATURES

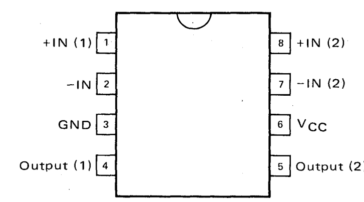
- LOW NOISE — 0.8μV TOTAL INPUT NOISE
- HIGH GAIN — 104dB OPEN LOOP
- SINGLE SUPPLY OPERATION
- WIDE SUPPLY RANGE 9 TO 40V
- POWER SUPPLY REJECTION — 110dB
- LARGE OUTPUT VOLTAGE SWING (VCC −2V p-p)
- WIDE BANDWIDTH — 15MHz UNITY GAIN
- POWER BANDWIDTH — 75kHz, 20V p-p
- INTERNALLY COMPENSATED
- SHORT CIRCUIT PROTECTED

ABSOLUTE MAXIMUM RATINGS

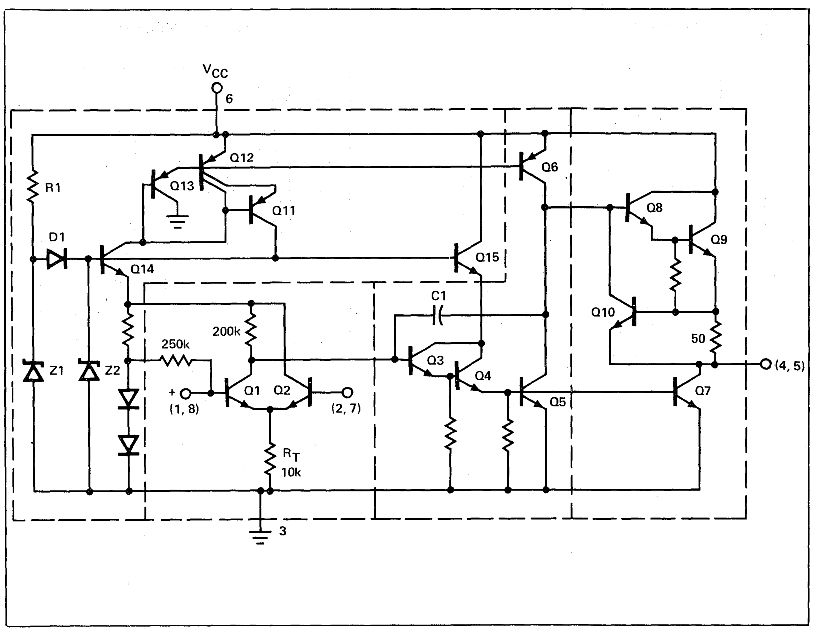
Supply Voltage	+40V
Power Dissipation	500mW
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 sec)	+300°C

PIN CONFIGURATION

V PACKAGE

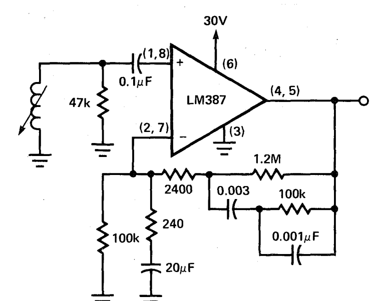


EQUIVALENT CIRCUIT

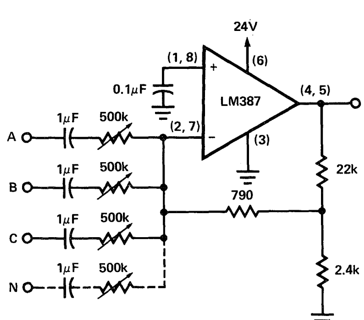


TYPICAL APPLICATIONS

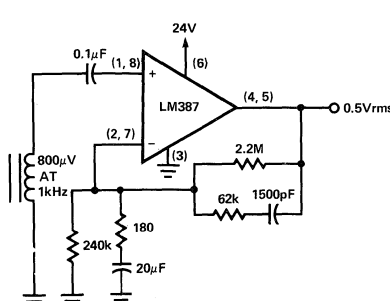
TYPICAL MAGNETIC PHONO PREAMPLIFIER



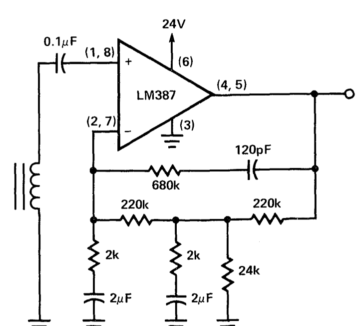
AUDIO MIXER



TYPICAL TAPE PLAYBACK AMPLIFIER



TWO-POLE FAST TURN-ON NAB TAPE PREAMPLIFIER

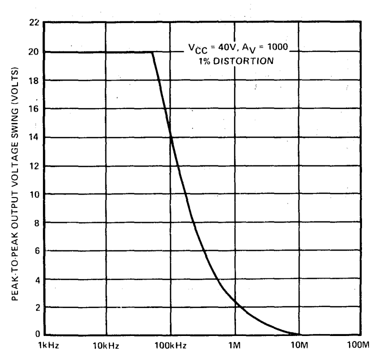


ELECTRICAL CHARACTERISTICS T_A = +25°C, V_{CC} = 14V (Unless Otherwise Noted)

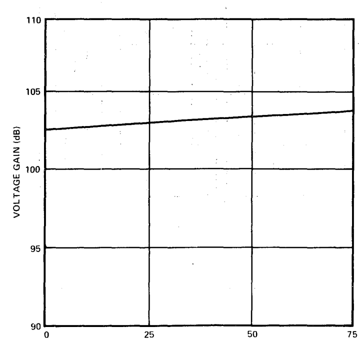
PARAMETER	TEST CONDITIONS	LIMITS MIN	TYP	MAX	UNIT
Voltage Gain	Open Loop		160,000		V/V
Supply Current	V_{CC} 9 to 40V, $R_L=\infty$		10		mA
Input Resistance					
(Positive Input)			100		kΩ
(Negative Input)			200		kΩ
Input Current					
(Negative Input)			0.5		μA
Output Resistance	Open Loop		150		Ω
Output Current	Source		8		mA
	Sink		2		mA
Output Voltage Swing	Peak-to-Peak		V_{CC} −2		V
Small Signal Bandwidth			15		MHz
Power Bandwidth	20V p-p (V_{CC} = 24V)		75		kHz
Maximum Input Voltage	Linear Operation			300	μVrms
Supply Rejection Ratio	f = 1kHz		110		dB
Channel Separation	f = 1kHz		60		dB
Total Harmonic Distortion	75dB Gain, f = 1kHz		0.1		%
Total Equivalent Input Noise	R_S = 600Ω, 100−10,000Hz		0.8	1.4	μVrms
Noise Figure	50kΩ, 100−10,000Hz		1.0		dB
	10kΩ, 100−10,000Hz		1.6		dB
	5kΩ, 100−10,000Hz		2.8		dB

TYPICAL CHARACTERISTICS

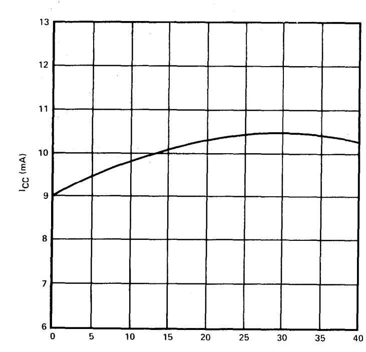
LARGE SIGNAL FREQUNCY RESPONSE



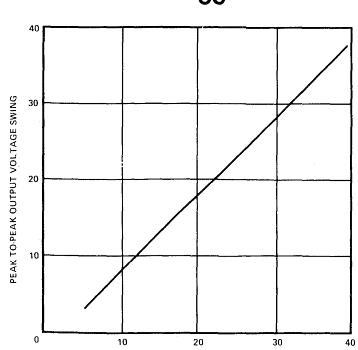
GAIN VS TEMPERATURE



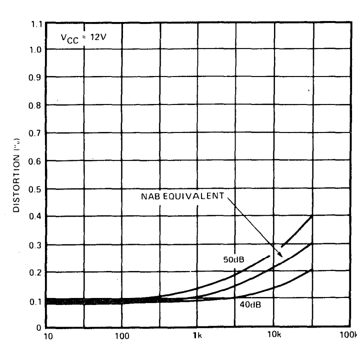
V_{CC} VS I_{CC}



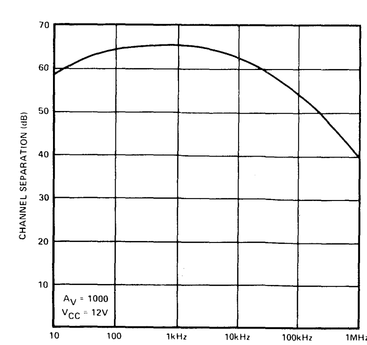
P-P OUTPUT VOLTAGE VS V_{CC}



% DISTORTION

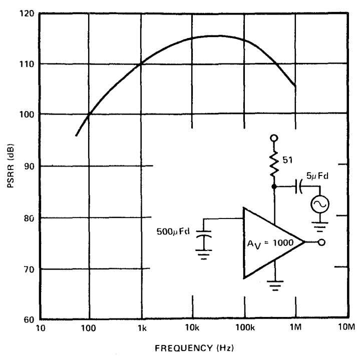


CHANNEL SEPARATION

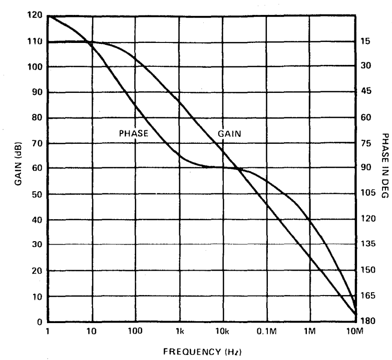


TYPICAL CHARACTERISTICS (Cont'd)

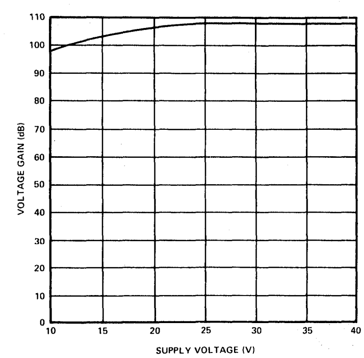
PSRR VS FREQUENCY



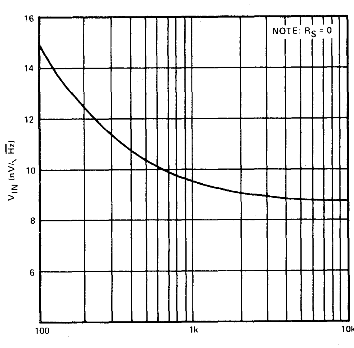
GAIN AND PHASE RESPONSE



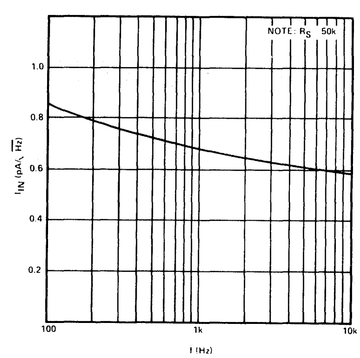
VOLTAGE GAIN VS SUPPLY VOLTAGE



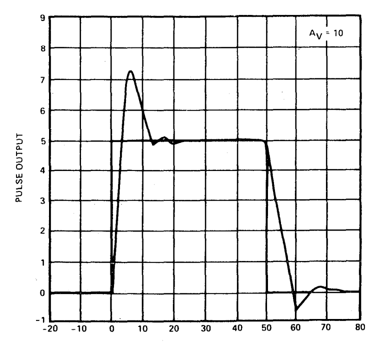
NOISE VOLTAGE VS FREQUENCY



NOISE CURRENT VS FREQUNCY



PULSE RESPONSE



5596/MC1496/MC1596-A,K

FEATURES

- **EXCELLENT CARRIER SUPPRESSION**
  65dB typ @ 0.5 MHz
  50dB typ @ 10 MHz
- **ADJUSTABLE GAIN AND SIGNAL HANDLING**
- **BALANCED INPUTS AND OUTPUTS**
- **HIGH COMMON-MODE REJECTION—85dB typ**

APPLICATIONS

SUPPRESSED CARRIER AND AMPLITUDE MODULATION
SYNCHRONOUS DETECTION
FM DETECTION
PHASE DETECTION
SAMPLING
SINGLE SIDEBAND
FREQUENCY DOUBLING

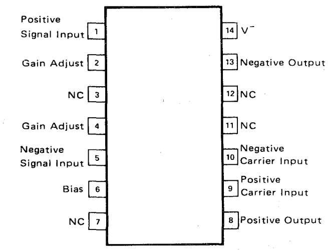
ABSOLUTE MAXIMUM RATINGS

Applied Voltage (Note 1)	30V
Differential Input Signal ($V_7 - V_8$)	±5.0V
Differential Input Signal ($V_4 - V_1$)	($5 \pm I_5 R_e$) V
Input Signal ($V_2 - V_1$, $V_3 - V_4$)	5.0V
Bias Current (I_5)	10mA
Power Dissipation (Pkg. Limitation)	
K-Package	680mW
Derate above 25°C	5.4mW/°C
A-Package (TO-116)	900mW
Derate above 25°C	7.2mW/°C
Operating Temperature Range	-555°C to +125°C
Storage Temperature Range	-65°C to +150°C

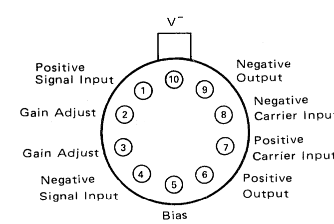
NOTES
1. Voltage applied between pins 6-7, 8-1, 9-7, 9-8, 7-4, 7-1, 8-4, 6-8, 2-5, 3-5.
2. Pin number references pertain to K package pinout only.

PIN CONFIGURATIONS (TOP VIEW)

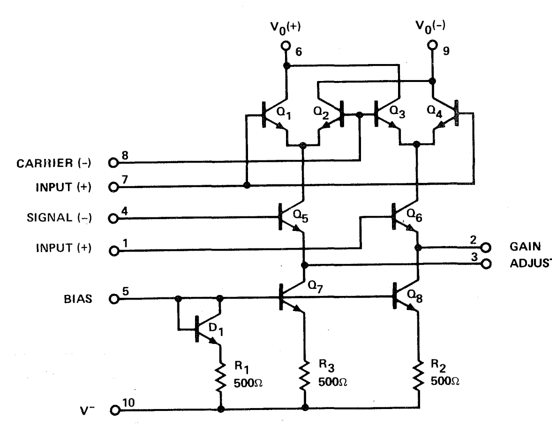
A PACKAGE



K PACKAGE



SCHEMATIC DIAGRAM



SIGNETICS BALANCED MODULATOR-DEMODULATOR ■ MC1596, MC1496

ELECTRICAL CHARACTERISTICS* (All input and output characteristics are single-ended unless otherwise noted.)

PARAMETER	MC1596 MIN	MC1596 TYP	MC1596 MAX	MC1496 MIN	MC1496 TYP	MC1496 MAX	UNITS
Carrier Feedthrough							μV(rms)
V_C = 60 mV(rms) sine wave and, f_C = 1.0 kHz		40			40		
offset adjusted to zero, f_C = 10 MHz		140			140		
V_C = 300 mVp-p square wave:							mV(rms)
offset adjusted to zero, f_C = 1.0 kHz		0.04	0.2		0.04	0.4	
offset not adjusted, f_C = 1.0 kHz		20	100		20	200	
Carrier Suppressions							dB
f_S = 10 kHz, 300 mV(rms)							
f_C = 500 kHz, 60 mV(rms) sine wave	50	65		40	65		
f_C = 10 MHz, 60 mV(rms) sine wave		50			50		
Transadmittance Bandwidth (Magnitude) (R_L = 50Ω)							MHz
Carrier Input Port, V_C = 60 mV(rms) sine wave		300			300		
f_S = 1.0 kHz, 300 mV(rms) sine wave							
Signal Input Port, V_S = 300 mV(rms) sine wave		80			80		
$\lvert V_C \rvert$ = 0.5V dc							
Signal Gain	2.5	3.5		2.5	3.5		V/V
V_S = 100 mV(rms), f = 1.0 kHz; $\lvert V_C \rvert$ = 0.5V dc							
Single-Ended Input Impedance, Signal Port, f = 5.0 MHz							
Parallel Input Resistance		200			200		kΩ
Parallel Input Capacitance		2.0			2.0		pF
Single-Ended Output Impedance, f = 10 MHz							
Parallel Output Resistance		40			40		kΩ
Parallel Output Capacitance		5.0			5.0		pF
Input Bias Current							μA
$I_{bS} = \frac{I_1 + I_4}{2}$		12	25		12	30	
$I_{bC} = \frac{I_7 + I_8}{2}$		12	25		12	30	
Input Offset Current		0.7	5.0		0.7	7.0	μA
$I_{ioS} = I_1 - I_4$; $I_{ioC} = I_7 - I_8$		0.7	5.0		0.7	7.0	
Average Temperature Coefficient of Input Offset Current (T_A = -55° to +125°C)		2.0			2.0		nA/°C
Output Offset Current ($I_6 - I_9$)		14	50		15	80	μA
Average Temperature Coefficient of Output Offset Current (T_A = -55°C to +125°C)		90			90		nA/°C
Common-Mode Input Swing, Signal Port, f_S = 1.0kHz		5.0			5.0		Vp-p
Common-Mode Gain, Signal Port, f_S = 1.0kHz, $\lvert V_C \rvert$ = 0.5V dc		-85			-85		dB
Common-Mode Quiescent Output Voltage (Pin 6 or Pin 9)		8.0			8.0		Vdc
Differential Output Voltage Swing Capability		8.0			8.0		Vp-p
Power Supply Current							mAdc
$I_6 + I_9$		2.0	3.0		2.0	4.0	
I_{10}		3.0	4.0		3.0	5.0	
DC Power Dissipation		33			33		mW

(V+ = +12V dc, V- = -8.0V dc, I_5 = 1.0mA dc, R_L = 3.9kΩ, R_e = 1.0kΩ, T_A = +25°C unless otherwise noted)

*Pin number references pertain to K package pinout only.

FEATURES

- MATCHED OPEN LOOP VOLTAGE GAIN
- LOW AUDIO NOISE
- SINGLE POWER SUPPLY
- WIDE POWER SUPPLY RANGE
- BUILT-IN POWER SUPPLY FILTER
- HIGH INPUT IMPEDANCE
- EMITTER FOLLOWER OUTPUT
- LOW DISTORTION
- SELF BIASING
- MINIMUM NUMBER OF EXTERNAL COMPONENTS
- OUTPUT CIRCUIT IS SHORT CIRCUIT PROTECTED
- HIGH CHANNEL SEPARATION
- VARIETY OF FEEDBACK OPTIONS
- NO CIRCUIT DAMAGE IF PLUGGED IN BACKWARDS
- 7.5V REGULATOR BIAS SOURCE

ABSOLUTE MAXIMUM RATINGS

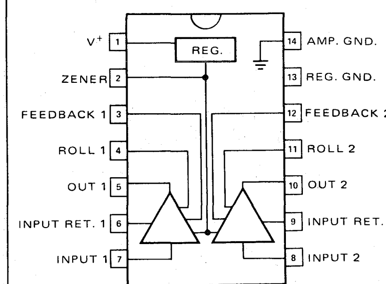
Supply Voltage	16V
Temperature	
Storage	−55°C to +150°C
Operating	−30°C to +85°C

APPLICATIONS

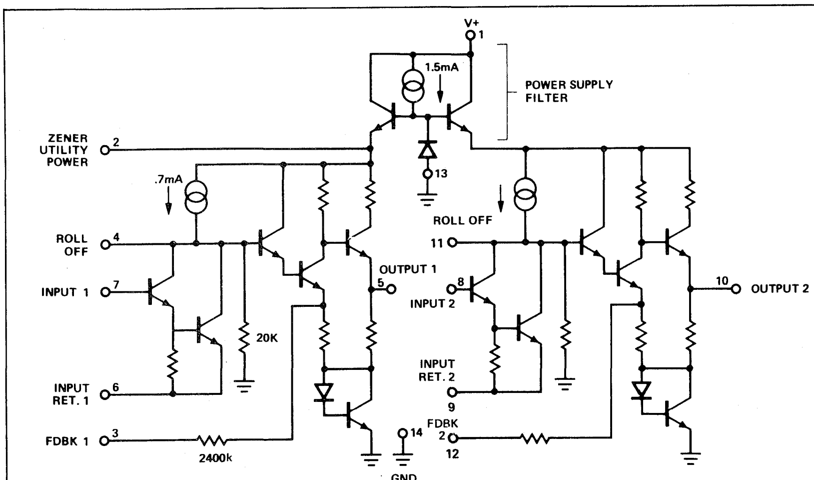
STEREO TAPE PLAYERS/RECORDERS
DICTATING EQUIPMENT
MOVIE PROJECTORS
PHONOGRAPHS
TV REMOTE CONTROL RECEIVER
MICROPHONE AMPLIFIERS
STEREO RADIO RECEIVER SYSTEMS
VIDEO PREAMPLIFICATION
NARROW BAND AMPLIFICATION
DRIVER-PREAMP FOR LOSSY NETWORKS
SUPER GAIN CASCADED AMPLIFIERS

CONFIGURATION

A PACKAGE



SCHEMATIC DIAGRAM



TEST CIRCUITS

CHANNEL SEPARATION

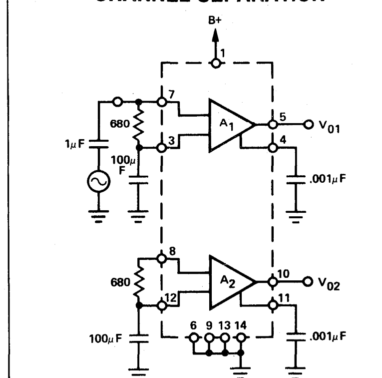


FIGURE 1

POWER SUPPLY REJECTION

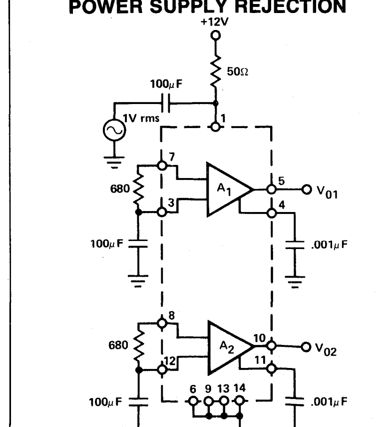


FIGURE 2

ELECTRICAL CHARACTERISTICS (25°C) (V_{CC}=12V)

PARAMETERS	MIN	TYP	MAX	UNITS
Supply Current (V_{CC} = 12V)		16	22	mA
Voltage Gain	65	68	71	dB
Gain Balance		0.3	2	dB
Channel Separation (f = 1 kHz), Figure 1	45	90		dB
Input Resistance	100K	250K		Ω
Signal Output		1.5		Vrms
Output Resistance		100		Ω
Power Supply Rejection (f = 1 kHz), Figure 2	45	55		dB
Total Harmonic Distortion Without Feedback (0.5V rms into 3kΩ Load, 1 kHz)		0.5	0.9	%
Input dc Bias Current		0.8	3	μA
Gain to Feedback Terminal 3, 12		45		dB
Impedance at Feedback Terminal		2400		Ω
Amplifier Noise Figure (100Hz to 10 kHz, 5kΩ Rs)		1.8		dB
Equivalent Input Noise (100Hz to 10 kHz, 680Ω Rs)		0.7	1.2	μV

TEST CIRCUITS (Cont'd)

NOISE

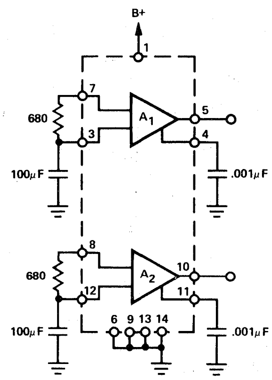


FIGURE 3

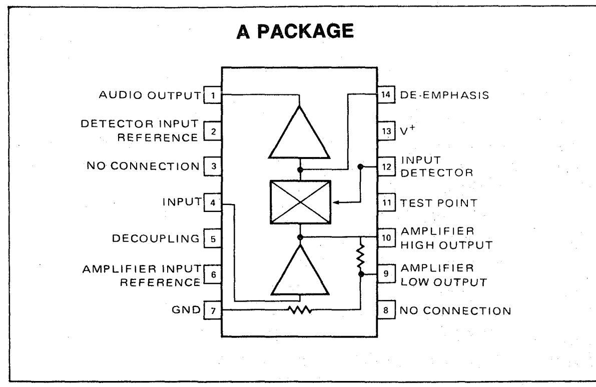
FEATURES

- HIGH SENSITIVITY—INPUT LIMITING VOLTAGE AT 4.5 MHz = 400μV
- HIGH IF VOLTAGE GAIN—60dB
- SIMPLIFIED TUNING—ONE RLC PHASE SHIFT NETWORK
- HIGH STABILITY
- LOW DISTORTION—1.0%
- WIDE FREQUENCY CAPABILITY—5kHz to 50MHz

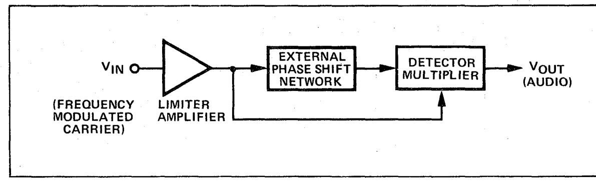
ABSOLUTE MAXIMUM RATINGS

Input Voltage (Pin 4)	+3.5V
Output Voltage	+15V
Supply Voltage (V+)	+15V
Junction Temperature	+150°C
Storage Temperature	−65°C to +150°C
Operating Temperature	0°C to +85°C
Thermal Resistance θ_{J-A}, Junction to Ambient	0.15°C /mW
Power Dissipation	300mW

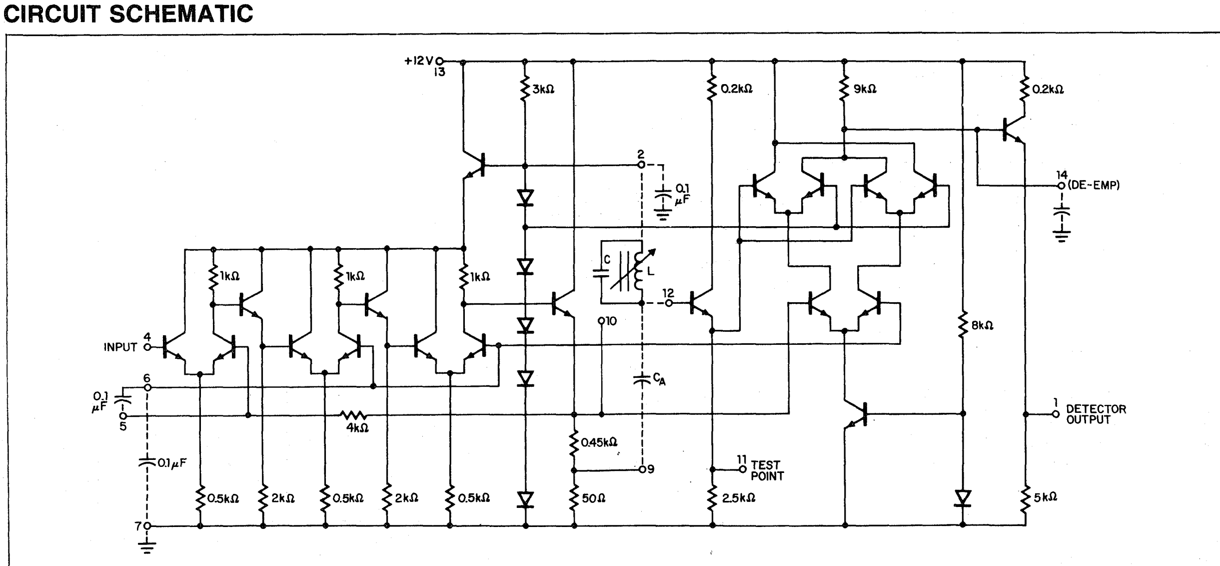
PIN CONFIGURATION



BLOCK DIAGRAM



CIRCUIT SCHEMATIC



ANALOG

ELECTRICAL CHARACTERISTICS Standard Conditions: V_{CC} = +12V ±10%, T_A = 25°C

	CHARACTERISTICS	TEST CONDITIONS	Pin	TEST FIGURE	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
I_{CC}	Supply Current		13		12.0	17	22	mA
V_{bias}	Amplifier Input Reference	Internally derived	6			1.45		V
V_{bias}	Detector Input Reference	Internally derived	2			3.65		V
V_{oh}	Amplifier High Output Level		10			1.45		V
V_{ol}	Amplifier Low Output Level		9			0.145		V
V_o	Detector Output Level		1		4.3	5.0	5.7	V
R_{in}	Amplifier Input Resistance		4			5.0		KΩ
C_{in}	Amplifier Input Capacitance		4			11		pF
R_{in}	Detector Injection Input Resistance		12			70		KΩ
C_{in}	Detector Injection Input Capacitance		12			2.7		pF
R_{out}	Amplifier High Output Resistance		10			60		Ω
R_{out}	Detector Output Resistance		1			200		Ω
R_{de}	De-Emphasis Resistance		14			9		KΩ
	FM Detection for Television Applications:	Detector injection voltage = 60mV$_{rms}$, f_o = 4.5 MHz, F deviation = 25 kHz, Peak separation = 150 kHz, FM modulating frequency = 400 Hz, Amplifier source resistance = 50Ω.						
V_g	Amplifier Voltage Gain	V_{in}≤0.3mV$_{rms}$ V_{cc} = 12V ±5%	10	1	55	58		dB
V_{oa}	Amplifier Output Voltage	V_{in} = 10mV$_{rms}$	10	1		1.45		V_{pp}
V_{th}	Input Limiting Threshold[1]		4	2		400	800	μV$_{rms}$
A_{vo}	Recovered Audio Output		1	2	0.5	0.6		V_{rms}
T_{hd}	Output Distortion	100% FM Modulation	1	2		1.5		%
AMR	AM Suppression[2]	V_{in} = 10mV$_{rms}$	1	3	40	46		dB
	FM Detection for 10.7 MHz Applications:	Detector injection voltage = 60mV$_{rms}$, f_o = 10.7 MHz, F deviation = 75 kHz, Peak separation = 550 kHz, FM modulating frequency = 400 Hz, Amplifier source resistance = 50Ω.						
V_g	Amplifier Voltage Gain	V_{in} ≤0.3mV$_{rms}$ V_{cc} = 12V ±5%	10	1		53		dB
V_{oa}	Amplifier Output Voltage	V_{in} = 10mV$_{rms}$	10	1		1.45		V_{pp}
V_{th}	Input Limiting Threshold		4	2		500		μV$_{rms}$
A_{vo}	Recovered Audio Output		1	2		0.45		V_{rms}
T_{hd}	Output Distortion	100% FM modulation	1	2		1.0		%
A_{MR}	AM Suppression[2]	V_{in} = 10mV$_{rms}$	1	3		40		dB

NOTES

1. The limiting threshold voltage is the FM input voltage V_i, expressed in rms volts, for a recovered V_{out} which is 3dB less than the recovered V_{out} at a V_i of 200 mV$_{rms}$.
2. The Amplitude Modulation Rejection in decibels, often abbreviated AMR, is given by the following formula:

$$AMR = \frac{20 \log V_{out} \text{ for 100\% FM modulated } V_i}{V_{out} \text{ for a 30\% AM } V_i}$$

USAGE INFORMATION

1. FM Detection.
   a. Tuning. Apply FM modulated signal through DC decoupling network to pin 4, V_{in} = 5mV$_{rms}$. Tune for maximum recovered audio at pin 1 or maximum RF voltage at pin 11.
   b. General
      (1) A DC path less than 100Ω shall be provided between pins 2 and 12. No other biasing provisions are required.
      (2) A DC path less than 300Ω should be provided between pins 2 and 12. No other biasing provisions are required.
      (3) The maximum AC load current can be increased by adding an external resistor between pins 1 and 7. The minimum value for this resistor is 800Ω, giving a maximum load current of 4mA$_{rms}$.
2. EXTERNAL DECOUPLING AND MOUNTING CONSIDERATIONS.
   a. All decoupling capacitors should be ceramic type with minimum residual inductance at the operating frequency.
   b. Decoupling capacitor leads at pins 5, 6, and 12 should be as short as possible.
   c. Connections from pin 4 should be as far removed as possible from connections at pins 9, 10, and 12.
   d. The power supply pin 13 should be decoupled with a 0.1μF ceramic capacitor, keeping the leads as short as possible.
   e. When using a large internal impedance power supply (voltage dropping resistor), decouple pin 13 for the lowest audio demodulation frequency.
   f. Keep appropriate distances between the input coil and any other coil in the phase shift network for the voltage gain between these points is high (40 to 60dB).

TEST CIRCUITS

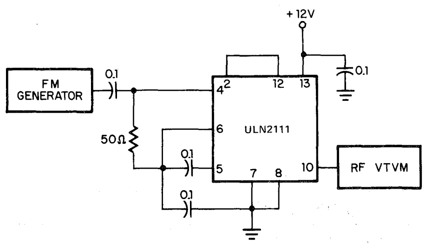


FIGURE 1

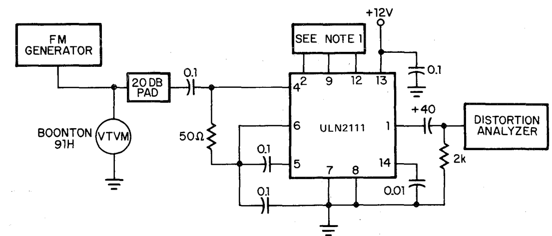


FIGURE 2

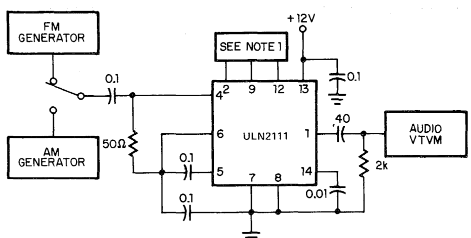


FIGURE 3

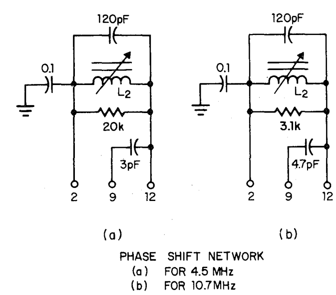
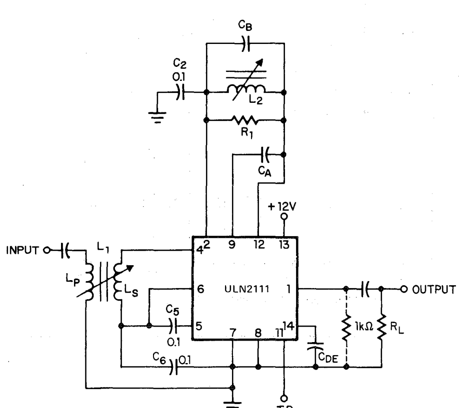


FIGURE 4

NOTES: 1. Phase shift network is specified in Figure 4.
2. All capacitors in microfarads unless otherwise noted.

APPLICATIONS

TYPICAL CIRCUIT REQUIREMENTS FOR FM DETECTION

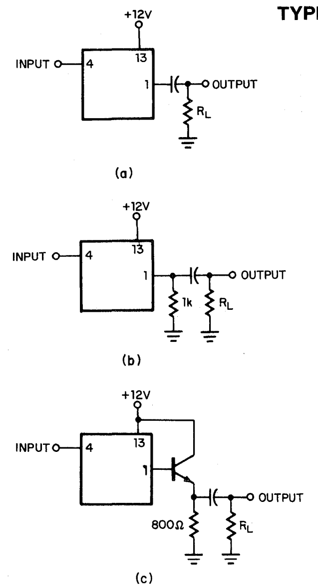


	Component Value	
	TV (4.5MHz)	**FM (10.7MHz)**
L_2 Inductance[2]	7-14μH	1.5-3μH
L_2 Nom. Unloaded Q	50	50
L_2 Nom. DC Resistance	50Ω	50Ω
C_A	3.0pF	4.7pF
C_B	120pF	120pF
R_1	20kΩ	3.1kΩ
Loaded Network Q	30	20
C_5 and C_6	0.1μF	0.1μF
C_2	0.1μF	0.1μF
C_{de}	0.01μF	0.01μF

NOTES: 1. Suggested coil source: 1.5-3μH Miller 9050, 7-14μH Miller 9052.
2. Use NPO type capacitor.

FIGURE 5

APPLICATIONS (Cont'd)



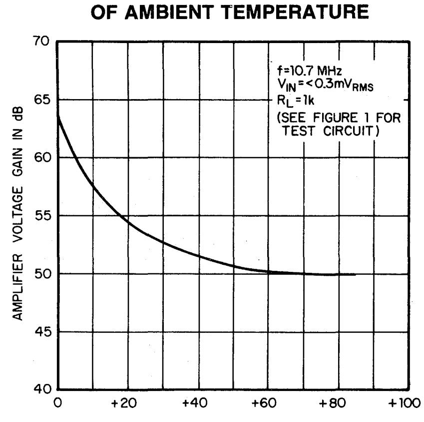
TYPICAL DRIVING CAPABILITIES at f_o = 4.5MHz

Figure	R_L (Ω)	V_o (mV rms) Δf = 7.5 kHz	Δf = 25 kHz	Remarks
A	2000	220	650	No Clipping
B	200	130	400	No Clipping
C	200	220	650	Clipping at V_o= 500mV_{rms}

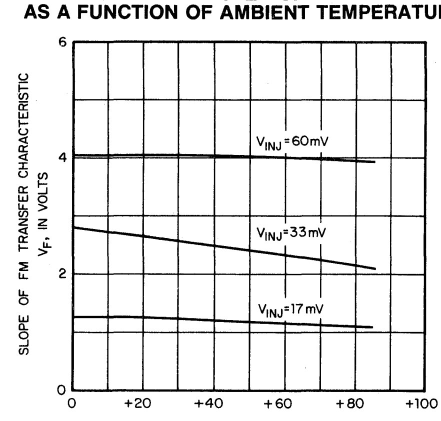
FIGURE 6

TYPICAL CHARACTERISTIC CURVES

AMPLIFIER GAIN AS A FUNCTION OF AMBIENT TEMPERATURE

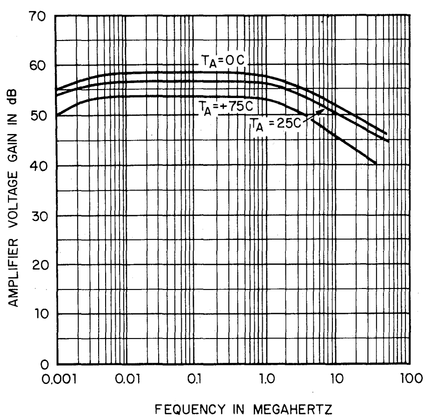


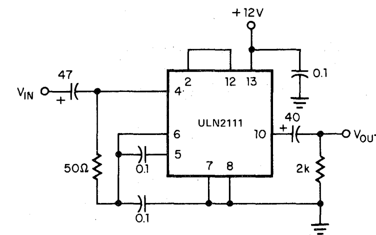
SLOPE OF FM TRANSFER CHARACTERISTICS AS A FUNCTION OF AMBIENT TEMPERATURE



TYPICAL CHARACTERISTIC CURVES (CONT'D)

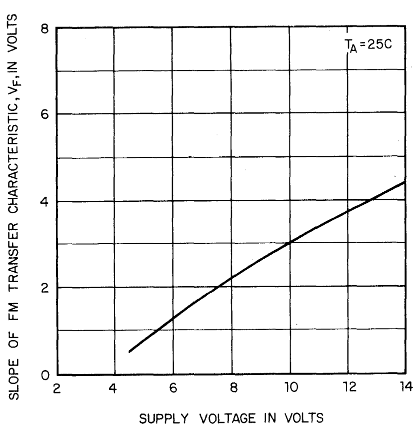
AMPLIFIER VOLTAGE GAIN AS A FUNCTION OF OPERATING FREQUENCY AT $V_{in} = 0.2mV_{ms}$



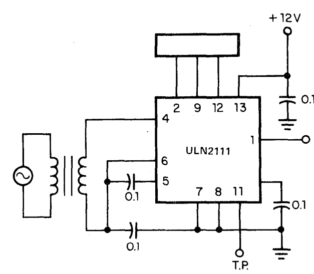


ALL CAPACITORS IN MICROFARADS

SLOPE OF FM TRANSFER CHARACTERISTIC AS A FUNCTION OF SUPPLY VOLTAGE

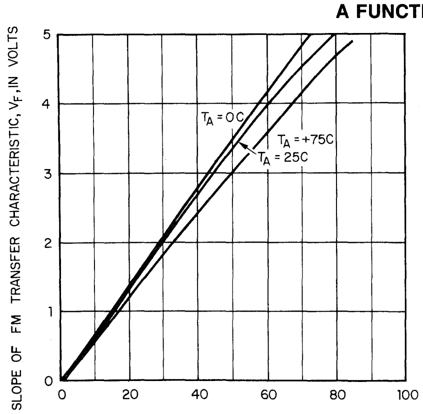


PHASE SHIFT NETWORK (See Figure 4)

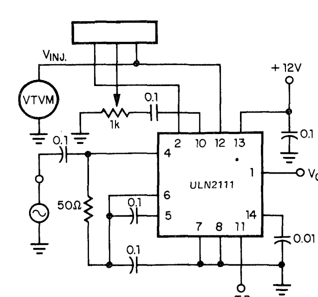


ALL CAPACITORS IN MICROFARADS

SLOPE OF FM TRANSFER CHARACTERISTICS AS A FUNCTION OF INJECTION VOLTAGE



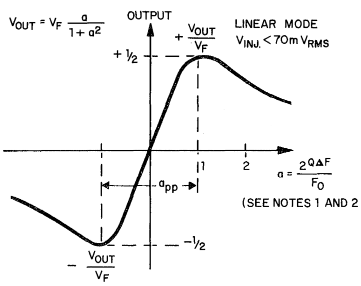
PHASE SHIFT NETWORK (See Figure 4)



ANALOG

TYPICAL CHARACTERISTIC CURVES (CONT'D)

TRANSFER CHARACTERISTICS FOR A SIMPLE LC NETWORK



OUTPUT = f (NORMALIZED DEVIATION)
(The units along the vertical axis are arbitrary units.)
Linear mode: Operation of the FM detector with no limiting after the phase shift network.

NOTES: 1. V_F defines the slope of the FM transfer characteristic, at origin:

$$V_f = \frac{dV_{out}}{da} \quad a = 0$$

V_F is primarily a function of bias current in the detector and injection voltage. V_F will decrease with decreasing V_{CC} or V_{INJ}.

2. a = normalized frequency deviation:

$$a = \frac{2Q\Delta F}{F_O}$$

FEATURES

- TYPICALLY 34dB GAIN AT 10.7MHz
- EXCELLENT TEMPERATURE STABILITY
- POWER SUPPLY REJECTION RATIO: 40dB TYPICAL
- OPERATING VOLTAGE RANGE: 10V—20V

APPLICATIONS

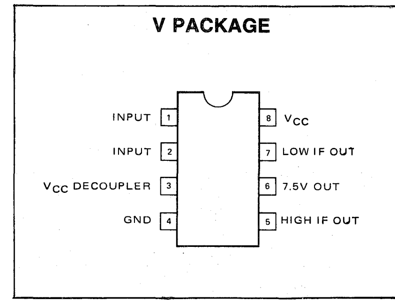
FM STEREO SYSTEMS
COMMUNICATIONS RECEIVERS
FM RADIOS

ABSOLUTE MAXIMUM RATINGS

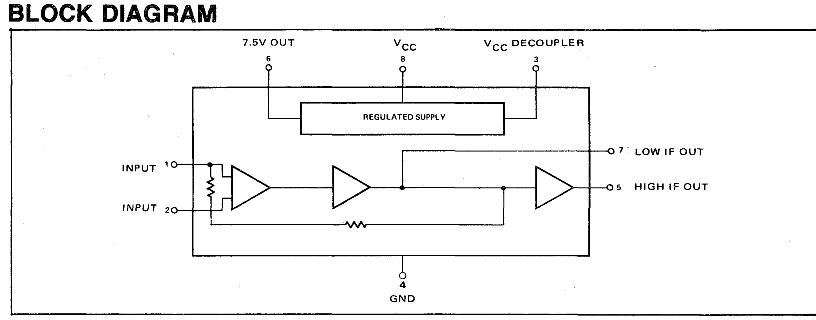
Supply Voltage, V_{CC}	20V
Supply Current, I_{CC}	22mA
Input Voltage (pins 1 and 3)	±3.0V
Power Consumption (Internal)	400mW
Output Current (pin 6)	10mA
Operating Temperature	−40°C to +85°C
Storage Temperature	−65°C to +150°C

*Derate at the rate of 8.3mW/°C at temperatures above +25°C.

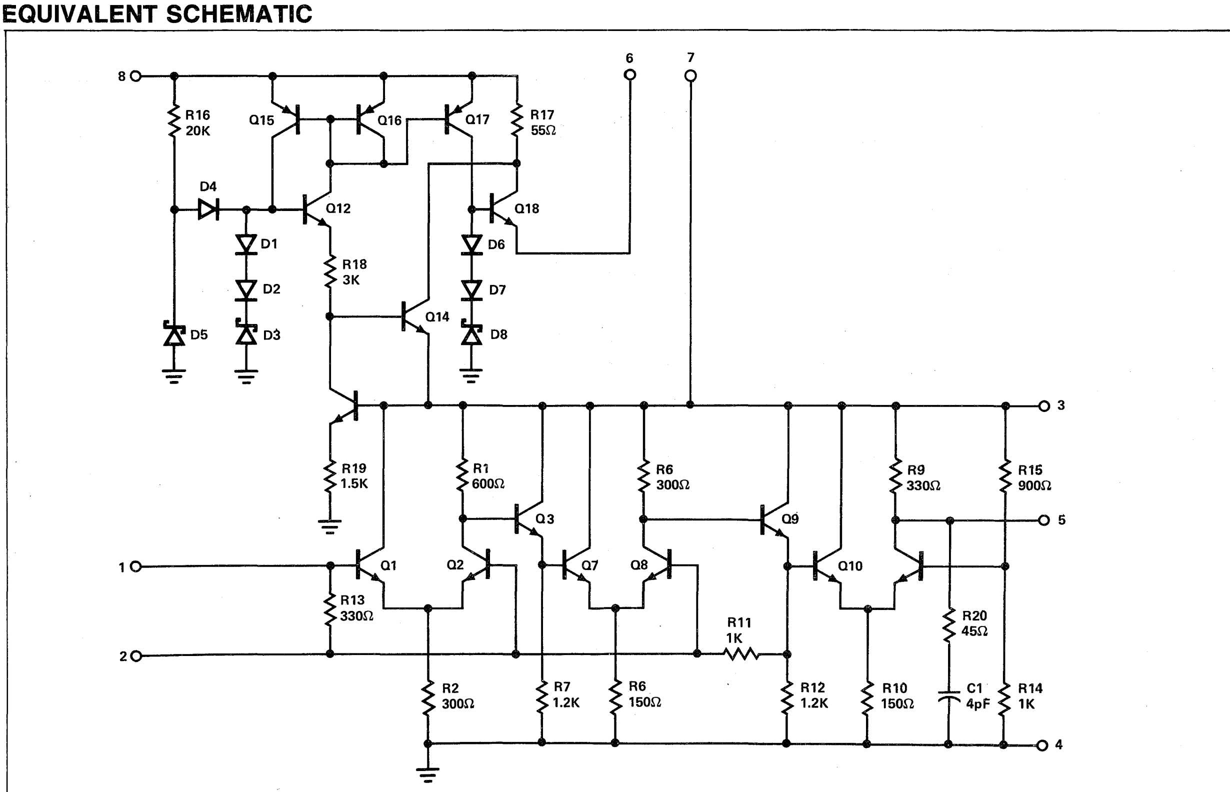
CONFIGURATION



BLOCK DIAGRAM



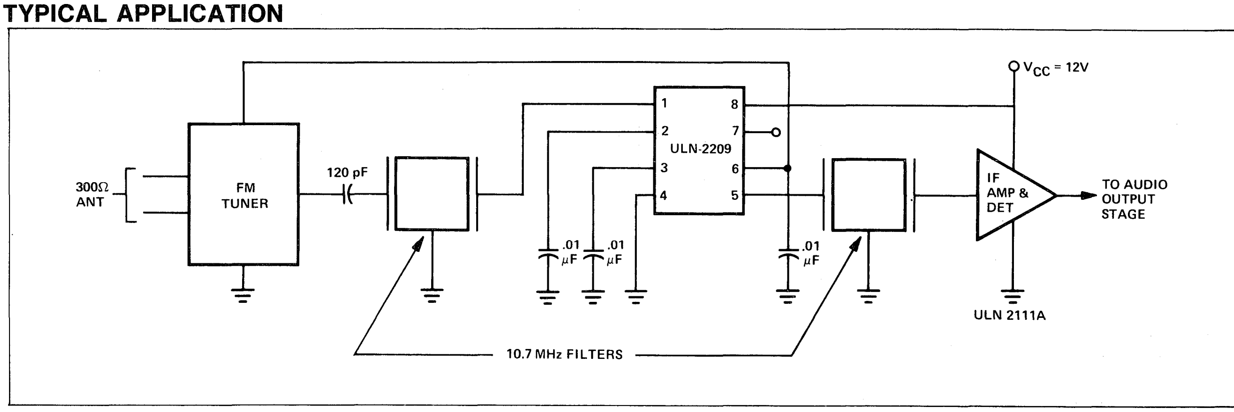
EQUIVALENT SCHEMATIC



ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_{CC} = +12V)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current		14	18	22	mA
Total Device Dissipation				400	mW
Terminal Voltage	Pin 1		1.2		V
	Pin 2		1.2		V
	Pin 3		2.4		V
	Pin 5		2.0		V
	Pin 6		7.5		V
Input Limiting Threshold	F = 10.7MHz		1500		μV
Output Voltage Swing	F = 10.7MHz		0.4		Vpp
Output Noise Voltage	F = 10.7MHz		1.5		mVrms
Input Impedance					
Parallel Input Resistance	F = 10.7MHz	270	330	390	Ω
Parallel Input Capacitance	F = 10.7MHz	5	7	10	pF
Output Voltage Gain	VIN = 100 mVrms F = 1MHz	30	34	40	dB
Power Supply Rejection	VIN = 250 mVrms F = 100Hz		−40		dB

TYPICAL APPLICATION



TYPE ULN2208 FM GAIN BLOCK WITH VOLTAGE REGULATOR

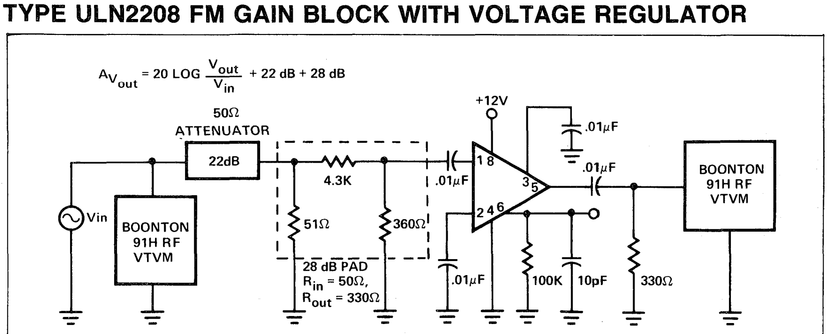


FIGURE 1

TYPE ULN2208 FM GAIN BLOCK WITH VOLTAGE REGULATOR (Cont'd)

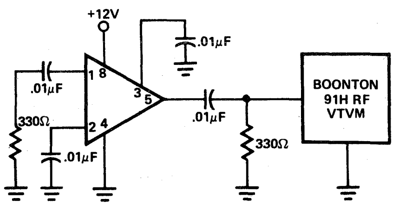


FIGURE 2

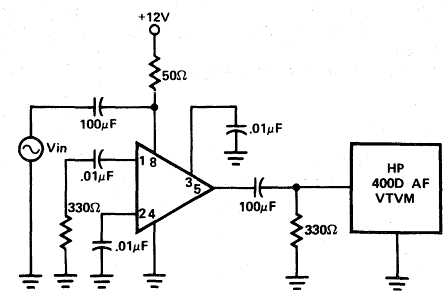


FIGURE 3

ULN2209-V

FEATURES

- TYPICALLY 50 dB GAIN AT 10.7 MHz
- EXCELLENT TEMPERATURE STABILITY
- POWER SUPPLY REJECTION RATIO: 40 dB TYPICAL
- OPERATING VOLTAGE RANGE: 10V—20V

APPLICATIONS

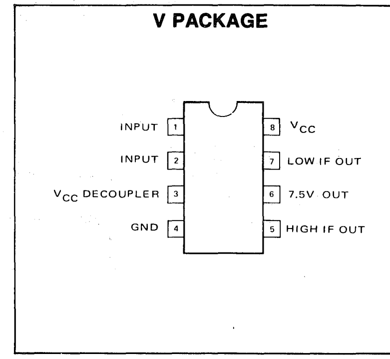
FM STEREO SYSTEMS
COMMUNICATIONS RECEIVERS
FM RADIOS

ABSOLUTE MAXIMUM RATINGS

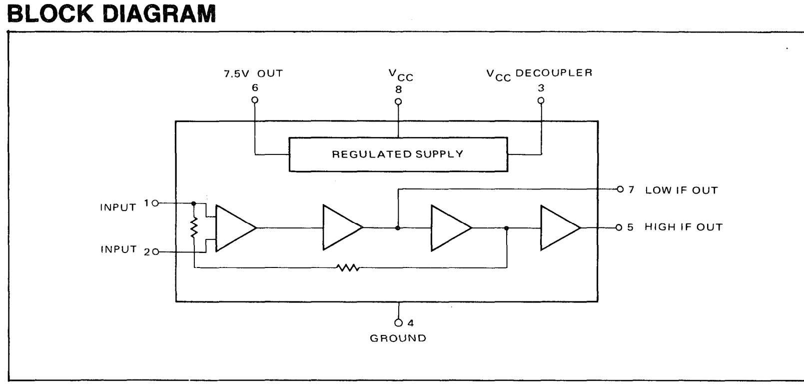
Supply Voltage, V_{CC}	20V
Supply Current, I_{CC}	22 mA
Input Voltage (pins 1 and 3)	±3,0V
Power Consumption (Internal)	400 mW
Output Current (pin 6)	10 mA
Operating Temperature	−40°C to +85°C
Storage Temperature	−65°C to +150°C

*Derate at the rate of 8.3 mW/°C at temperatures above +25°C.

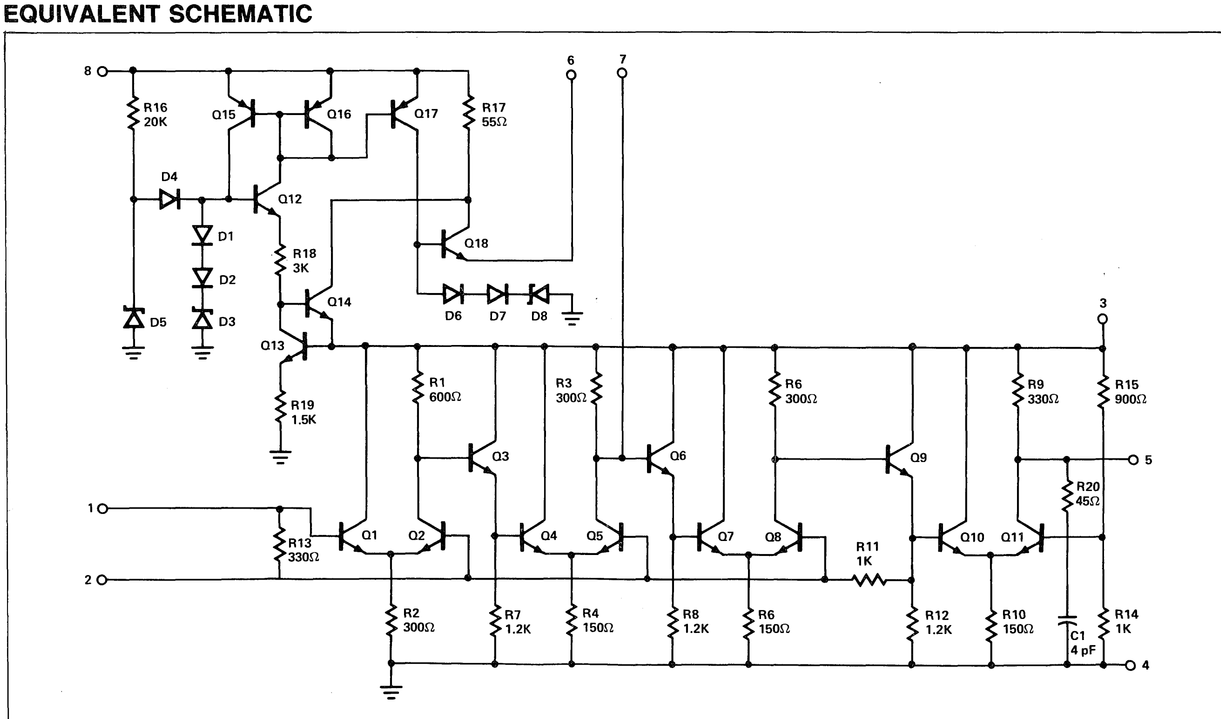
PIN CONFIGURATION



BLOCK DIAGRAM



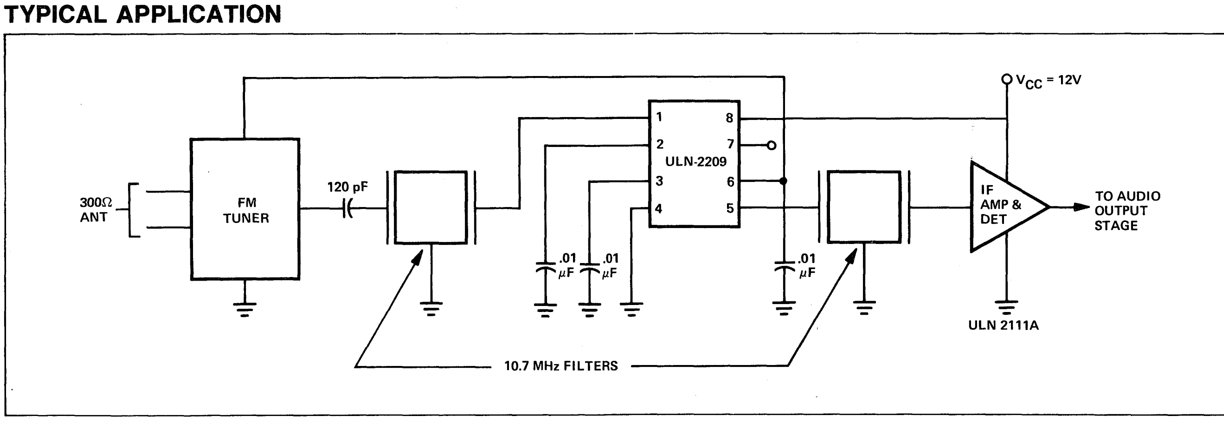
EQUIVALENT SCHEMATIC



ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_{CC} = +12V)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current		14	18	22	mA
Total Device Dissipation				400	mW
Terminal Voltage	Pin 1		1.2		V
	Pin 2		1.2		V
	Pin 3		2.4		V
	Pin 5		2.0		V
	Pin 6		7.5		V
Input Limiting Threshold	F = 10.7 MHz		400		μV
Output Voltage Swing	F = 10.7 MHz		0.5		Vpp
Output Noise Voltage	F = 10.7 MHz		4		mVrms
Input Impedance					
Parallel Input Resistance	F = 10.7 MHz	270	330	390	Ω
Parallel Input Capacitance	F = 10.7 MHz	5	7	10	pF
Output Voltage Gain	V_{IN} = 100 mVrms F = 1 MHz	47	50	55	dB
Power Supply Rejection	V_{IN} = 250 mVrms F = 100 Hz		−40		dB

TYPICAL APPLICATION



TYPE ULN2209 FM GAIN BLOCK WITH VOLTAGE REGULATOR

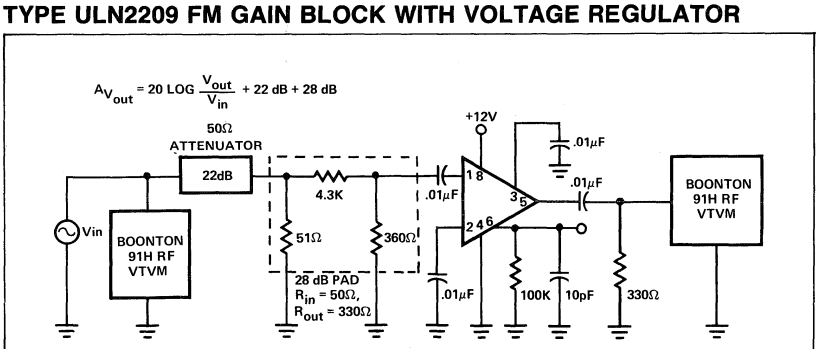


FIGURE 1

TYPE ULN2209 FM GAIN BLOCK WITH VOLTAGE REGULATOR (Cont'd)

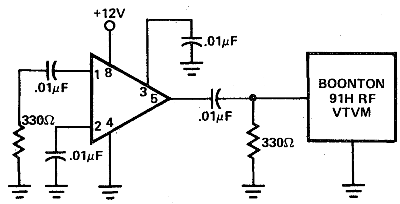


FIGURE 2

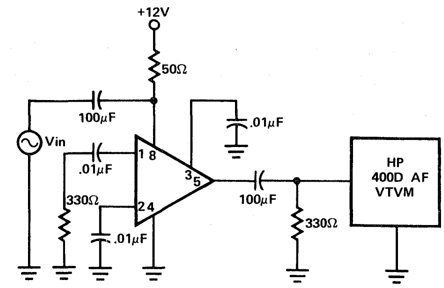


FIGURE 3

GROUPS

TBA 120S is delivered in groups

An attenuation of 30 dB requires a resistor from pin 5 to ground as indicated in the table.

Group	2	3	4	5
Value	1.9 to 2.2	2.1 to 2.5	2.4 to 2.9	2.8 to 3.3K

Groups are identified by marking ie TBA 120S—3 indicates group 3.

AMPLIFIER AND DEMODULATION DATA

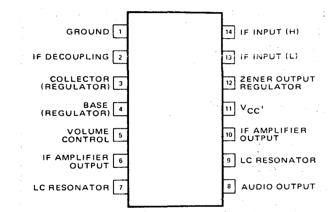
VCC = 12v
Temperature = 25°C

MAXIMUM RATINGS

Supply Voltage	18V
Operating Temperature Range	−15+70°C
Storage Temperature	−40+125°C
Power Dissipation	400mW
max 1 min	500mW
Supply Current	15mA
max 1 min	20mA
Current 13	2mA
14	1mA
Operating Supply Voltage	6-18V
Frequency Range	0-12MHz

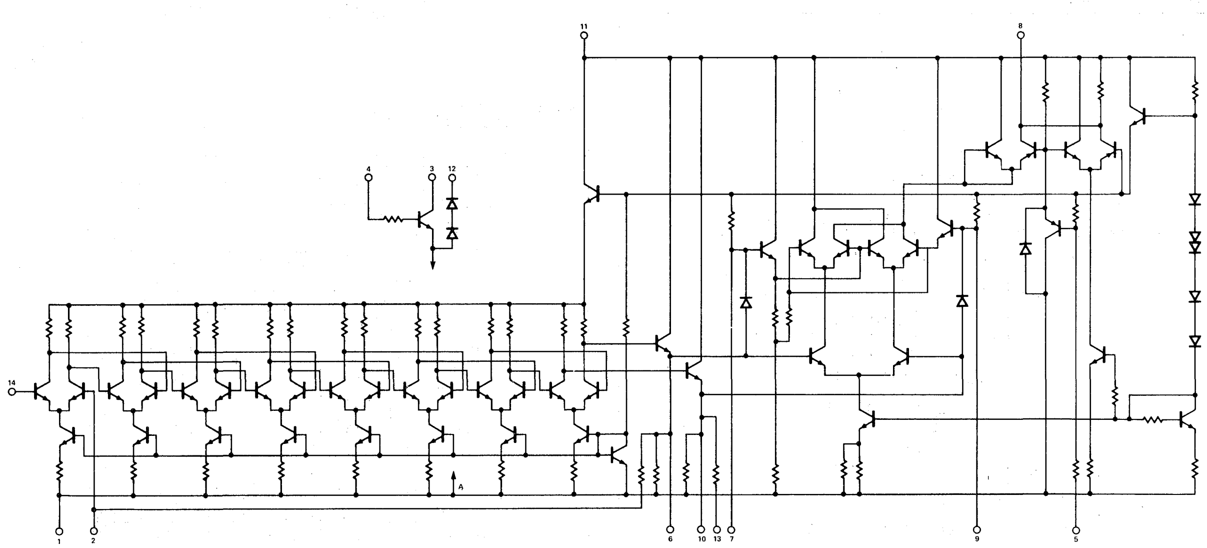
PIN CONFIGURATION

A PACKAGE



14 Pin Plastic DEP (TBA 120S) or Quad-in-Line (TBA 120AS)

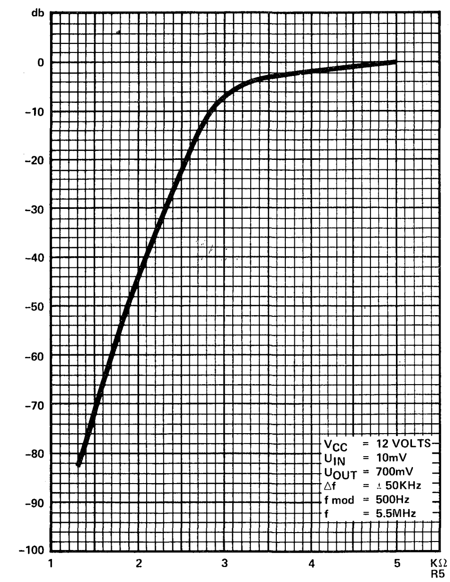
CIRCUIT SCHEMATIC



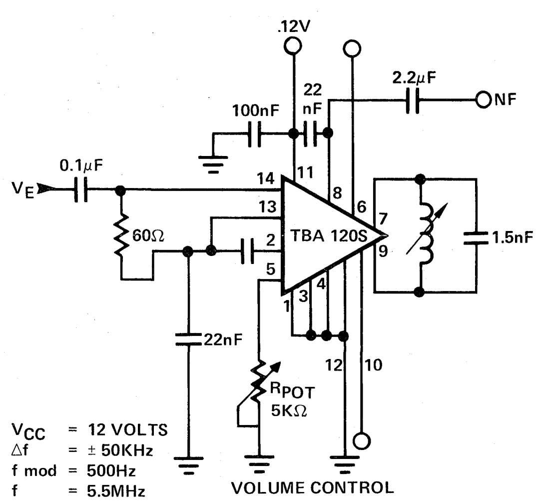
ELECTRICAL CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNITS
Power Supply Current (pin 5 open)	10	14	18	mA
Power supply current (pin 5-grounded)	12	15.2	20	mA
IF Gain		68		dB
IF Output Voltage		250		mV
AF Output		1.1		V
AF		0.55		V
Limiting Threshold				
Input Voltage		30	60	μ/V
Input Impedance				
5.5 mHZ	15/6	40/4.5		kΩ/pf
Output Impedance		2.6		kΩ
Volume Control Range (AGC)		70		dB
Output Signal Voltage		7.3		V
AM Rejection	45	55		dB
f=5.5 MHz f=±50KHz				
Vin=500 μV m=30%				
f(MOD)=1 KHz				
Potentiometer Impedance		3.7	4.7	kΩ
Voltage 1dB Attenuation		2.4	26	V
Potentiometer Impedance				
−70dB Attenuation	1.0	1.4		kΩ
Voltage −70dB Attenuation		1.3		V

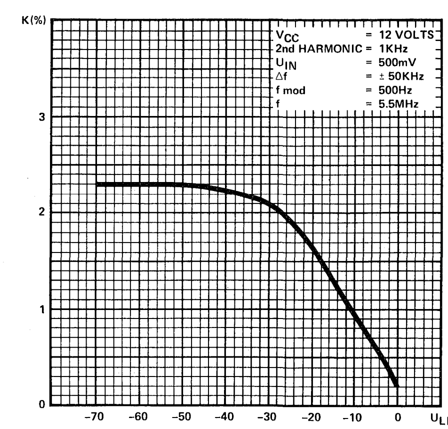
VOLUME CONTROL SIGNETICS TBA 120S



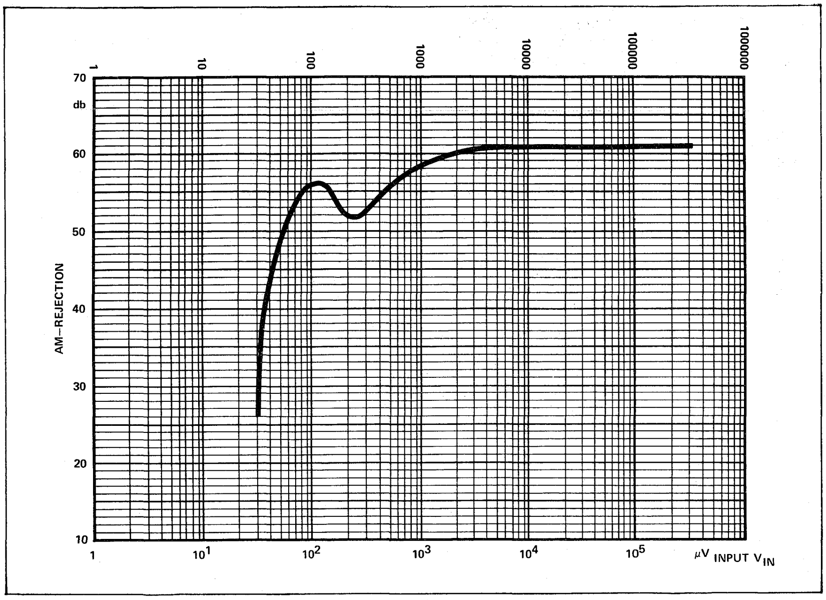
TEST CIRCUIT



TYPICAL CURVE FROM PRODUCT SELECTION Nr. 3



TYPICAL CURVE FROM PRODUCE-REFLECTION NR3.

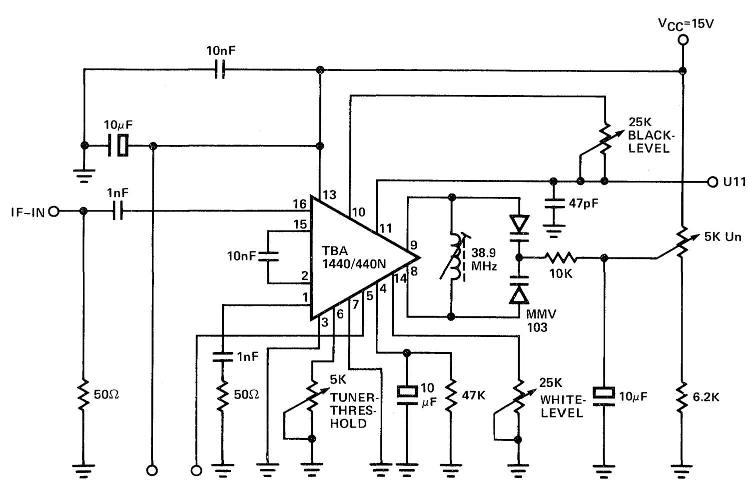


ANALOG

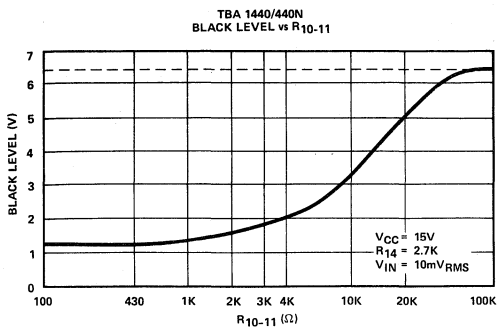
ELECTRICAL CHARACTERISTICS

PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}		10.5	15	16.5	V
I_{CC} (V_{CC}=15 V)			40	45	mA
V_{110}	V_{11}−DC/R_{14}=0	7.9	8.2	8.5	V
V_{11}	V_{11}−DC/R_{14}=∞	5.4	5.8	6.2	V
V_{120}	V_{12}−DC/R_{14}=0	2.4	2.8	3.0	V
V_{12}	V_{12}−DC/R_{14}=∞	1.25	1.6	1.8	V
$-V_{10}$	Threshold for sync. level (R_{10-11}=0)	0.7	1.0	1.3	V
$-V_7$	Negative gating pulse	0.25	1	7	V
	Gain control voltage:				
V_{4max}	Gain max		0.5	1	V
V_{4min}	Gain min		1.6	2	V
$V_{1/16}$	Minimum input voltage (V_{11}=3 Vpp)		500	750	μV
V_{11}	Videoband width (−3dB)	5.5	6	7	MHz
	AGC range	50	55		dB
	Maximum IF voltage Level present at Video outputs		60	70	mV
	Input impedance	Gain max	1.8		kΩ
			2.0		pF
		Gain min	1.9		kΩ
			1.9		pF

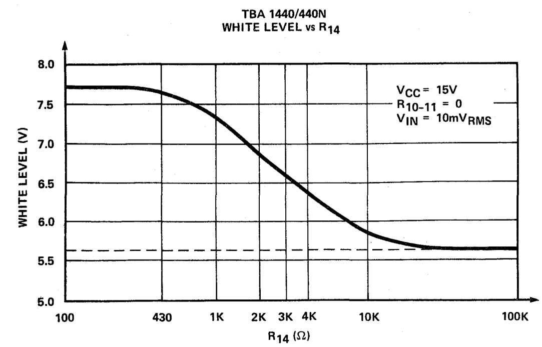
TEST CIRCUIT



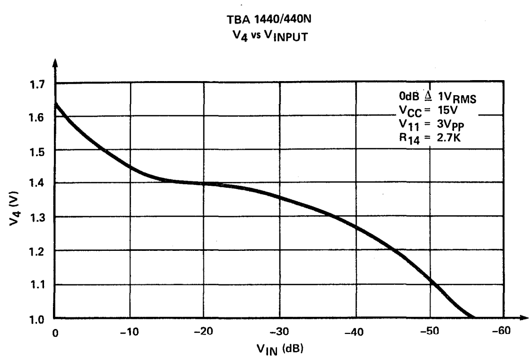
BLACK LEVEL VS. R_{10-11}



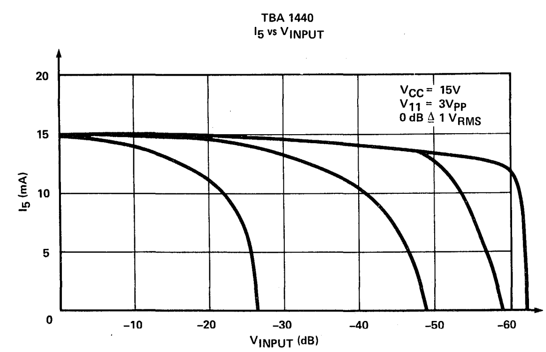
WHITE LEVEL VS. R_{14}



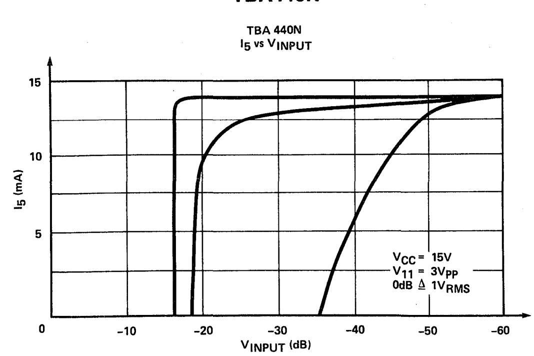
V_4 VS. V INPUT



I_5 VS. V INPUT TBA1440



I_5 VS. V INPUT TBA440N



ANALOG

ANALOG

MICROPROCESSOR 5

Microprocessors

Table of Contents

INTRODUCTION

The greatly increased sophistication and rising production costs of today's logic systems force the system designer to use every available resource in order to economically produce his system. In keeping with this cost reduction goal, Signetics has developed a powerful general purpose integrated microprocessor called the 2650. The first Signetics microprocessor, in conjunction with Signetics MOS and Bipolar memory and interface product lines, offers the system designer a viable and attractive alternative to the hard-wired approach to system design. For many applications, the system designer can use this general purpose microprocessor and standard memory and interface circuits to implement systems with lower cost than the hard-wired logic approach without sacrificing performance.

By using the 2650 and compatible products, the system designer can obtain two other major benefits of microcomputer systems. These benefits are greatly enhanced system flexibility and minimized design or modification cycles compared with the hard-wired logic approach.

The requirements of the majority of applications for integrated microprocessors (logic replacement and control functions) have defined a general set of processor parameters based on system and device economies, ease of use, and speed requirements.

These characteristics include:

Single chip
Fixed instruction set
Eight bit parallel structure
TTL compatibility

In addition to these characteristics, the design of the 2650 has been optimized around three generalized objectives:

Lowest system cost
Ease of use
Capable of a wide range of applications

The optimum technology choice for implementing these features is the low threshold ion-implanted N-Channel silicon gate process. This process has matured in the past few years, providing a combination of high density, low threshold voltage, moderate speed and good manufacturing yields. Using this technology, a total of 576 bits of ROM, approximately 250 bits of register and about 900 logic gates are used to implement the processor function on the 2650 chip.

The instruction set consists of 75 instructions, of which about 40% consists of arithmetic instructions. This class contains the Boolean, arithmetic, and compare operations, each of which may be executed using any one of eight addressing modes. Another 30% of the instruction set consists of branch instructions which incorporate six addressing modes. The remaining 30% of the instruction set includes, among others, I/O instructions, instructions for performing operations on the two status registers, a decimal adjust instruction and the HALT instruction.

Utilizing multiple addressing modes greatly increases coding efficiency, allowing functions to be performed using fewer instructions than less powerful machines. The resulting reduction in routine execution time and memory capacity requirements directly translates into improved system performance and reduced memory cost. In this way the powerful instruction set and addressing modes of the 2650 allow a significant reduction in the memory required to perform a given function, resulting in sizeable system cost savings without sacrificing performance.

In addition to the microprocessor itself, a number of support circuits and development tools are also required to design and manufacture microprocessor-based systems. This growing complement of circuits, hardware, and software development aids are also described in this catalog, providing the potential designer of a 2650-based system with the basic data required to select circuits and choose the most efficient method of system development.

FEATURES OF THE 2650 FAMILY

2650 FAMILY APPROACH

- **Low System Cost**
  - **Low cost N-Channel products**
  - **Intrinsic advantages of single 5V supply**
  - **Uses standard low cost memories**
  - **Low cost interfacing**
- **Ease of Use**
  - **Easy interfacing**
  - **Conventional instruction set**
  - **Ease of programming**
- **Wide Range of Applications**
  - **General purpose capability**
  - **Powerful architecture**
  - **Powerful instruction set**
  - **Flexible**
  - **Expanding family of devices**

FEATURES OF THE MICROPROCESSOR

Basic 2650 Processor Characteristics

- **Single chip 8-bit processor**
- **Signetics low threshold double ion-implanted silicon gate N-Channel technology**
- **Single +5V power supply**
- **Low power consumption: 525 mW maximum**
- **Single phase TTL-compatible clock**
- **Static operation: no minimum clock frequency**
- **Clock frequency: 1.25MHz maximum**
- **Cycle time: 2.4μs minimum**
- **Standard 40 pin DIP**

2650 Interfaces

- **TTL compatible inputs, outputs — no external resistors required**
- **Tri-state bus outputs for multiprocessor and direct memory access systems**
- **Asynchronous (handshaking) memory and I/O interface**
- **Accepts wide range of memory timing**
- **Interfaces directly with industry standard memories**
- **Powerful control interface**
- **Single-bit direct serial I/O path**
- **Parallel 8-bit I/O capability**

2650 Processor Architecture

- **8-bit bidirectional tri-state data bus**
- **Separate tri-state address bus**
- **32,768-byte addressing range**
- **Internal 8-bit parallel structure**
- **Seven 8-bit addressable general purpose registers**
- **Eight-level on-chip subroutine return address stack**
- **Program status word for flexibility and enhanced processing power**
- **Single-level hardware vectored interrupt capability**
- **Interrupt service routines may be located anywhere in addressable memory**
- **Separate adder for fast address calculation**

2650 Instruction Set

- General Purpose instruction set with substantial capabilities in arithmetic, character manipulation and control and I/O processing
- Fixed instruction set
- 75 instructions
- Up to eight addressing modes
- True indexing with optional auto increment/decrement
- One, two or three byte instructions
- One- and two-byte I/O instructions
- Selective test of individual bits
- Powerful instruction set and addressing modes minimize memory requirements

FEATURES OF COMPATIBLE PRODUCTS

2102, 2606, 1K RAMs

- Completely static operation
- N-Channel silicon gate technology
- 1024 X 1 organization 256×4 organization (2606)
- Single +5V power supply
- 200mW typical power dissipation
- Maximum access time:
  750ns : 2606
  500ns : 2102-1
- TTL-compatible
- Tri-state outputs
- Data I/O bus (2606 only)
- Standard 16 pin DIP

2608 8K ROM

- Completely static operation
- N-Channel silicon gate technology
- 1024 X 8 organization
- Single +5V power supply
- 400mW maximum power dissipation
- 650ns maximum access time
- TTL compatible
- Tri-state outputs
- Standard 24 pin DIP

8T26 Quad Transceiver

- Schottky TTL Technology
- Four pairs of bus drivers/receivers
- Separate drive and receive enable lines
- Tri-state outputs
- Low current pnp inputs
- High fan out — driver sinks 40mA
- 20ns maximum propagation delay
- Stndard 16 pin DIP

8T31 8-bit Bidirectional Port

- Schottky TTL technology
- Two independent bidirectional busses
- Eight bit latch register
- Independent read, write controls for each bus
- Bus A overrides if a write conflict occurs
- Register can be addressed as a memory location via Bus B Master Enable
- 30ns maximum propagation delay
- Low input current: 500μA
- High fan out — sinks 20mA
- Standard 24 pin DIP

8T95/6/7/8 Hex Buffers/Inverters

- Schottky TTL technology
- Six buffers or inverters per package
- Non-inverting (8T95, 8T97) or Inverting (8T96, 8T98)
- Buffered control lines
- Tri-state outputs
- Low current pnp inputs
- Standard 16 pin Dip

82S115/123/129 PROMs

- Schottky TTL technology
- Single +5V power supply
- 32 X 8 organization (82S123)
- 256 X 4 organization (82S129)
- 512 X 8 organization (82S115)
- Field programmable (Nichrome)
- On-chip storage latches (82S115 only)
- Low current pnp inputs
- Tri-state outputs
- 35ns typical access time
- Standard 24 pin DIP (82S115)
- Standard 16 pin DIP (82S123, 82S129)

PROCESSOR HARDWARE DESCRIPTION

ARCHITECTURE

GENERAL DESCRIPTION

A block diagram of the processor is shown in Figure 1. The first, second, and third bytes of instructions are read into the processor on the data bus and loaded into the Instruction Register, Holding Register, and Data Bus Register, respectively. The instructions are decoded through a combination of ROM and random logic.

The ALU performs arithmetic, Boolean, and combinatorial shifting functions. It operates on eight bits in parallel and utilizes carry-look-ahead logic. A second adder is used to increment the instruction address register and to calculate operand addresses for the indexed and relative addressing modes. This separate address adder allows complex addressing modes to be implemented with no increase in instruction execution time.

The General Purpose Register Stack and the Subroutine Return Address Stack are implemented with static RAM cells. The Register Stack consists of seven 8-bit registers. The Subroutine Stack can contain eight 15-bit addresses, thereby allowing eight levels of subroutine nesting. Placing the Subroutine Stack on the chip allows efficient ROM-only systems to be implemented in some applications. Separate 15-bit Instruction Address and Operand Address Registers and provided. The 2650 is an 8-bit binary processor with BCD capability. See Figure 2 for a diagram of the 2650 registers as seen by the programmer.

PROGRAM STATUS WORD

The Program Status Word (PSW) is a major feature of the 2650 with greatly increases its flexibility and processing power. The PSW is a special purpose register within the processor that contains status and control bits.

It is divided into two bytes called the Program Status Upper (PSU) and Program Status Lower (PSL). The PSW bits may be tested, loaded, stored, preset, or cleared using the instructions which affect the PSW. The bits are utilized as follows:

PSUO, 1,2	— SP	— **Pointer** for the Return Address **Stack.**
PSU5	— II	— Used to **Inhibit** recognition of additional **Interrupts.**
PSU6	— F	— **Flag** is a latch directly driving the flag output.
PSU7	— S	— **Sense** equals the state of the sense input.
PSL0	— C	— **Carry** stores any carry from the high-order bit of the ALU.

PSL1 — COM — **Compare** determines if a logical or arithmetic comparison is to be made.

PSL2 — OVF — **Overflow** is set if a two's complement overflow occurs.

PSL3 — WC — **With Carry** determines is the carry is used in arithmetic and rotate instructions.

PSL4 — RS — **Register Select** identifies which bank of 3 GP registers is being used.

PSL5 — IDC — **Inter Digit Carry** stores the bit-3-to-bit-4 carry in arithmetic operations.

PSL6, 7 — CC — **Condition Code** is affected by compare, test and arithmetic instructions.

INTERRUPT HANDLING CAPABILITY

The 2650 has a single level hardware vectored interrupt capability. When an interrupt occurs, the 2650 finishes the current instruction and sets the Interrupt Inhibit bit in the PSW. The processor then executes a Branch to Subroutine Relative to location Zero (ZBSR) instruction and sends out Interrupt Acknowledge and Operation Request signals. On receipt of the INTACK signal the interrupting device inputs an 8-bit address, the interrupt vector, on the data bus. The relative and relative indirect addressing modes combined with this 8-bit address allow interrupt service routines to begin at any addressable memory location.

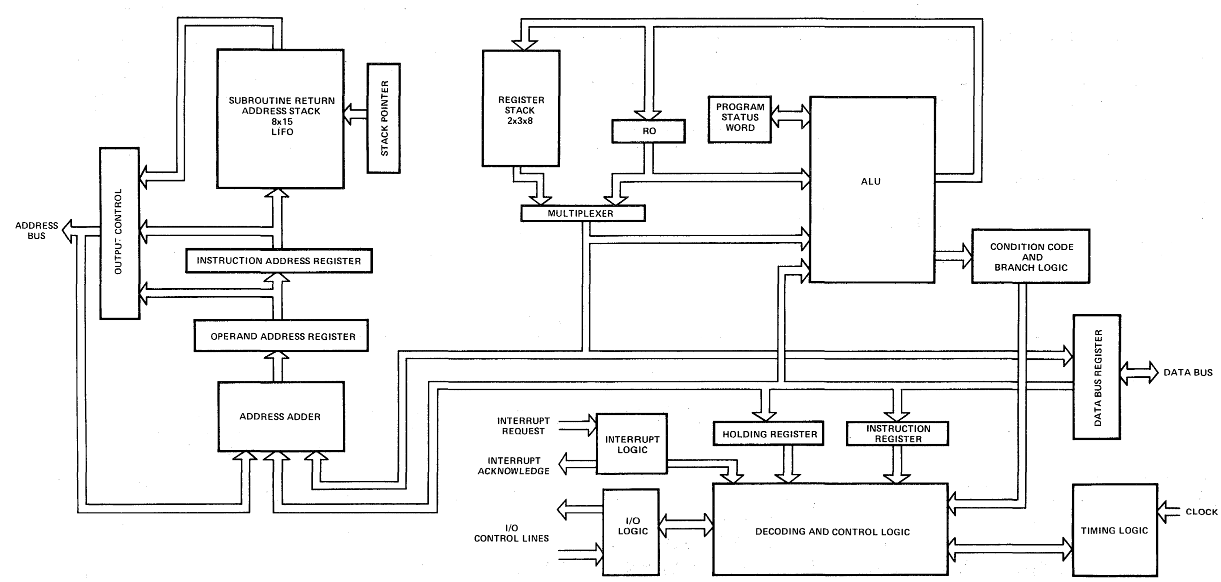


Figure 1. BLOCK DIAGRAM

INTERFACING

INTRODUCTION TO INTERFACING WITH THE 2650

Five key concepts have been incorporated in the 2650 to make interfacing easy and inexpensive. The extent to which these concepts have been incorporated in the Signetics 2650 provides unique benefits of system density and low cost to the system designer.

1. SINGLE 5V POWER SUPPLY

Low threshold double ion-implanted Silicon Gate N-Channel MOS technology is used to allow operation from one +5V power supply with resultant cost savings and improved reliability. This reduces power consumption significantly compared with the multi-power supply approach.

2. INTERFACE CIRCUIT COMPATIBILITY

The 2650 inputs and outputs are specified to be compatible with widely available, standard, low cost logic families such as TTL, CMOS and Low-power STTL. This includes the single phase clock input which saves the cost of high level multiphase clock driver circuitry. Bus outputs are tri-state and capable of driving one 7400 TTL load or four 74LS loads. The 2650 is capable of driving several loads of pnp-buffered STTL inputs. Many MSI, Interface and Memory LSI circuits (for example, in Signetics 82S00 and 8T00 series) have these low current pnp inputs and are recommended for use in 2650 microcomputer systems. See Table 1 for DC characteristics of the 2650.

3. USE OF STANDARD MEMORIES

One of the major 2650 design achievements is to operate efficiently in a system using industry standard memories, for example 1024 X 1 and 256 X 4 N-channel RAMs and 1024 X 8 N-Channel ROMs. These standard memories are widely available and used in volume with corresponding low cost. Non-standard memories, particularly those produced by only one manufacturer will be less available, run in lower volume and often cost 2 to 3 times as much per bit as industry standard products. The 2650 operates successfully with memories of any access time, due to the completely asynchronous interface that is provided for this purpose. Memories which respond in less than 0.8 microseconds allow the processor to operate at maximum speed.

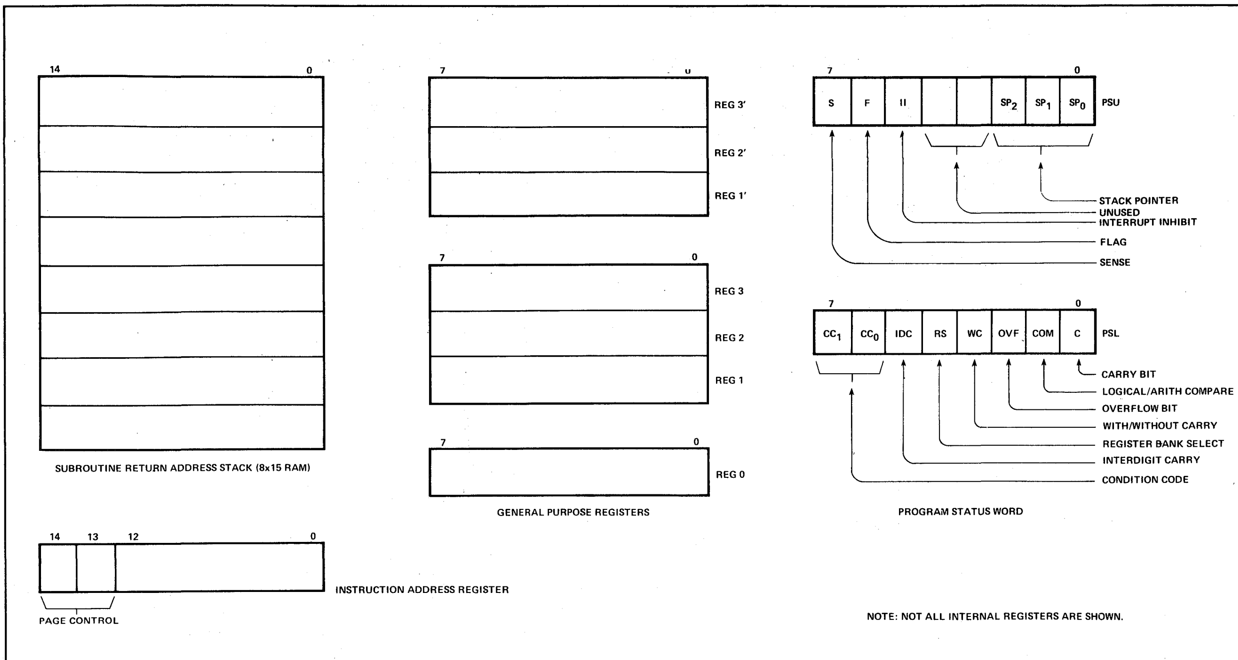


Figure 2. MAJOR 2650 REGISTERS

Table 1.
2650 DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS MIN	LIMITS MAX	UNIT
I_{LI}	Input Load Current	V_{IN}= 0 to 5.25V		10	μA
I_{LOH}	Output Leakage Current	ADREN, DBUSEN = 2.2V, V_{OUT} = 4V		10	μA
I_{LOL}	Output Leakage Current	ADREN, DBUSEN = 2.2V, V_{OUT} = 0.45V		10	μA
I_{CC}	Power Supply Current	V_{CC} = 5.25V, T_A = 0°C		100	mA
V_{IL}	Input Low		−0.6	0.8	V
V_{IH}	Input High		2.2	V_{CC}	V
V_{OL}	Output Low	I_{OL} = 1.6 mA	0.0	0.45	V
V_{OH}	Output High	I_{OH} = −100 μA	2.4	$V_{CC}-0.5$	V
C_{IN}	Input Capacitance	V_{IN} = 0V		10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		10	pF

Conditions: T_A = 0°C to 70°C, V_{CC} = 5V ±5%

4. NO SPECIAL INTERFACE PRODUCTS

Similarly, another major achievement is to operate efficiently in a system using no special I/O products. This approach avoids the problems of a system requiring high cost specialized components with restricted availability.

5. POWERFUL MEMORY AND I/O INTERFACE

The following features characterize the memory and I/O interfaces:

Both memory and input/output may operate in a completely asynchronous fashion. Consequently, devices operating at any speed up to the maximum data transfer rate may be connected without buffering. External latching of data from these interfaces in not required.

Data paths are driven with tri-state buffers, allowing multiprocessor and Direct Memory Access (DMA) configurations to be designed.

Eight-bit data paths communicate data in parallel.

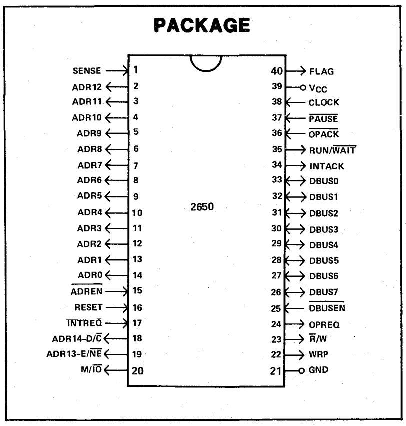
One- and two-byte I/O instructions provide maximum flexibility and efficiency when interfacing with I/O devices.

PIN CONFIGURATION AND INTERFACE SIGNAL DEFINITION

Refer to Figure 3 for the 2650 pin configuration. Signals are defined as follows:

ADR0-ADR12
: The low order 13 bits of address for memory access are on these pins. ADR0-ADR7 are also used in two-byte I/O instructions. These outputs are tri-state buffers controlled by ADREN.

PIN CONFIGURATION



ADR13-E/NE

This multiplexed output signal delivers the ADR13 address bit when M/IO is in the M phase or discriminates between Extended and Non-Extended I/O instructions when M/IO is in the I/O phase.

ADR14-D/C

Address 14 or Data/Control is a multiplexed output signal. This pin delivers the ADR14 address bit when M/IO is in the M phase, or discriminates between Data and Control I/O instructions when M/IO is in the I/O phase.

ADREN

Address Bus Enable is an input providing the external control for the ADR0-ADR12 tri-state buffer drivers.

DBUS0-DBUS7

This is the 8-bit, bidirectional tri-state bus over which most data is communicated into or out of the processor.

DBUSEN

Data Bus Enable is an input that controls the tri-state buffer drivers for DBUS0 to DBUS7.

OPREQ

Operation Request is an output signal that informs external devices that the information on other output pins is valid.

OPACK

Operation Acknowledge is an input which is used by external devices to end an I/O or memory signaling sequence.

M/IO

Memory/Input-Output. This output informs external devices whether Memory or Input/Output functions are being performed.

R/W

This output signal describes an I/O or memory operation as Read or Write, and defines whether the bidirectional DBUS is transmitting or receiving.

WRP

This Write Pulse is generated during write sequences and may be used to strobe memory or I/O devices.

SENSE

Is an input, independent of the other I/O signals, that provides a direct input to the processor.

FLAG

This pin provides a direct output signal that is completely independent of the other I/O signals.

INTREQ

Interrupt Request. This input is used by external devices to force the processor into the Interrupt sequence.

INTACK

Interrupt Acknowledge is the signal used by the processor to inform external devices that it has entered an interrupt sequence.

PAUSE

Pause is used to temporarily stop the processor at the end of the current instruction. It may stop processing for an indefinite length of time and is available to use for DMA (Direct Memory Access).

RUN/WAIT

Informs external circuits as to the Run/Wait status of the 2650 processor.

RESET

Is an input used to cause the 2650 to begin processing from a known state.

CLOCK

This is the only clock input to the processor. It accepts standard TTL levels.

VCC

+5V power.

GND

The logic and power supply ground for the processor.

2650 TIMING

The clock input to the 2650 provides the basic timing information that the processor uses for all its internal and external operations. The clock rate determines the instruction execution time, except to the extent that external memories and devices slow the processor down. The maximum clock rate of the standard 2650 is 1.25 Megacycles (one clock period is 800ns minimum). One unique feature of the 2650 is that the clock frequency may be slowed down to DC, allowing complete timing flexibility for interfacing. This feature permits single stepping the clock which can greatly simplify system checkout. It also provides an easy method to halt the processor. Each 2650 cycle is comprised of three clock periods. Direct instructions require either 2, 3, or 4 processor cycles for execution and, therefore, vary from 4.8 to 9.6μs in duration.

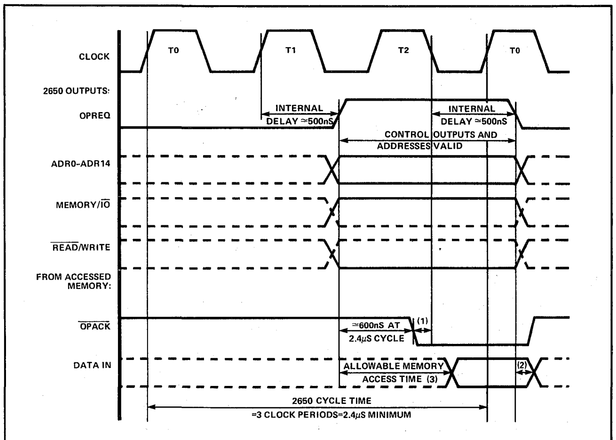
A timing diagram for a memory read cycle is shown in Figure 4. OPREQ (Operation Request) is the master control signal that coordinates all operations external to the processor. When true, OPREQ indicates that other output signals are valid. During a memory read cycle M/IO is in the M (Memory) state and R/W is in the R (Read) state. The address lines and the control lines become valid before OPREQ rises. The data to be read may be returned anytime after OPREQ becomes valid. An OPACK (Operation Acknowledge) should accompany the read data from the memory. The Data and OPACK signals should remain valid for 50 ns after OPREQ falls.

INPUT/OUTPUT INTERFACE

The 2650 microprocessor has a set of versatile I/O instructions and can perform I/O operations in a variety of ways. One-and two-byte I/O instructions are provided, as well as a special single-bit I/O facility. The I/O modes provided by the 2650 are designated as Data, Control, and Extended I/O.

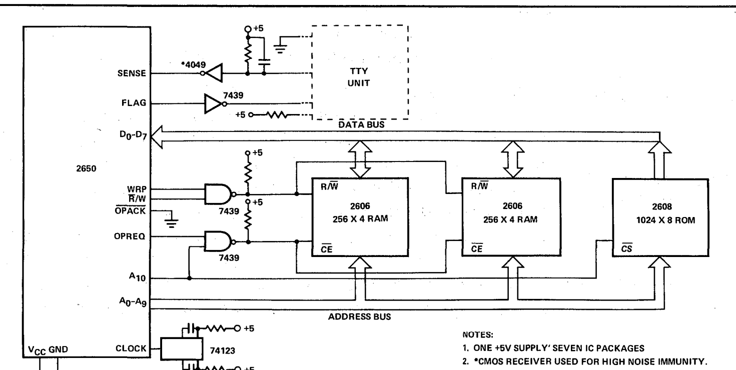
Data or Control I/O instructions are one byte long. Any general purpose register can be used as the source or destination. A special control line indicates if either a Data or Control instruction is being executed. Extended I/O is a two-byte read or write instruction. Execution of an extended I/O instruction will cause an 8-bit address, taken from the second byte of the instruction, to be placed on the low order eight address lines. The data, which can originate or terminate with any general purpose register, is placed on the data bus. This type of I/O can be used to simultaneously select a device and send data to it.

Memory reference instructions that address data outside of physical memory may also be used for I/O operations. When an instruction is executed, the address may be decoded by the I/O device rather than memory.



NOTES: (1) OPACK must go low at least 100nS before the trailing edge of T2 in order not to slow down the 2650.
(2) DATA IN signals must be valid for 50nS after the trailing edge of OPREQ.

Figure 4. MEMORY READ CYCLE TIMING



NOTES:
1. ONE +5V SUPPLY' SEVEN IC PACKAGES
2. *CMOS RECEIVER USED FOR HIGH NOISE IMMUNITY.

Figure 5. SEVEN PACKAGE MINIMAL SYSTEM

MEMORY INTERFACE

The memory interface consists of the address bus, the 8-bit data bus and several signals that operate in an interlocked or handshaking mode.

The Write Pulse signal is designed to be used as a memory strobe signal for any memory type. It has been particularly optimized to be used as the Chip Enable or Read/Write signal for the Signetics 2602 and 2606 RAMs.

INTERFACING — A MINIMAL SYSTEM EXAMPLE

The 2650 has been designed for low cost, easy interfacing, which is dramatically illustrated by a minimal system configuration shown in Figure 5. This system has a Teletype interface, 1024 bytes of ROM, and 256 bytes of RAM, yet requires only seven (7) standard integrated circuit packages. The ROM can contain a bootstrap loader and I/O driver programs for the Teletype. Other programs could reside in ROM or be read into RAM via the Teletype. An alternative to the 2608 N-Channel MOS ROM is the 82S115 Bipolar PROM which offers a 512 X 8 organization. Only one +5-volt power supply is required for this system. The advantages of conceptual simplicity and minimum system costs of the 2650 approach will be obvious to the system designer, particularly when compared to alternative microprocessor products.

INSTRUCTION SET

It may be seen from examination of the 2650 instruction set that there are many powerful instructions which are all easily understood and are typical of larger computers. There are one-, two-, and three-byte instructions as a result of the multiplicity of addressing modes. See Table 2 for a complete listing and Figure 6 for instruction formats.

Automatic incrementing or decrementing of an index register is available in the arithmetic indexed instructions. All of the branch instructions except indexed branching can be conditional.

Register-to-register instructions are one byte; register-to-storage instructions are two or three bytes long. The two-byte register-to-memory instructions are either immediate or relative addressing types.

Table 2.
INSTRUCTION SET

	MNEMONIC		OP CODE	FORMAT*	DESCRIPTION OF OPERATION	AFFECTS	CYCLES
LOAD/STORE	LOD	Z	000 000	1Z	Load Register Zero	CC (Note 1)	2
		I	000 001	2I	Load Immediate	CC (Note 1)	2
		R	000 010	2R	Load Relative	CC (Note 1)	3
		A	000 011	3A	Load Absolute	CC (Note 1)	4
	STR	Z	110 000	1Z	Store Register Zero (r ≠ 0)	CC (Note 1)	2
		R	110 010	2R	Store Relative	—	3
		A	110 011	3A	Store Absolute	—	4
ARITHMETIC	ADD	Z	100 000	1Z	Add to Register Zero w/wo Carry	C, CC (Note 1), IDC, OVF	2
		I	100 001	2I	Add Immediate w/wo Carry	C, CC (Note 1), IDC, OVF	2
		R	100 010	2R	Add Relative w/wo Carry	C, CC (Note 1), IDC, OVF	3
		A	100 011	3A	Add Absolute w/wo Carry	C, CC (Note 1), IDC, OVF	4
	SUB	Z	101 000	1Z	Subtract from Register Zero w/wo Borrow	C, CC (Note 1), IDC, OVF	2
		I	101 001	2I	Subtract Immediate w/wo Borrow	C, CC (Note 1), IDC, OVF	2
		R	101 010	2R	Subtract Relative w/wo Borrow	C, CC (Note 1), IDC, OVF	3
		A	101 011	3A	Subtract Absolute w/wo Borrow	C, CC (Note 1), IDC, OVF	4
	DAR		100 101	1Z	Decimal Adjust Register	CC (Note 2)	3
LOGICAL	AND	Z	010 000	1Z	AND to Register Zero (r ≠ 0)	CC (Note 1)	2
		I	010 001	2I	AND Immediate	CC (Note 1)	2
		R	010 010	2R	AND Relative	CC (Note 1)	3
		A	010 011	3A	AND Absolute	CC (Note 1)	4
	IOR	Z	011 000	1Z	Inclusive OR to Register Zero	CC (Note 1)	2
		I	011 001	2I	Inclusive OR Immediate	CC (Note 1)	2
		R	011 010	2R	Inclusive OR Relative	CC (Note 1)	3
		A	011 011	3A	Inclusive OR Absolute	CC (Note 1)	4
	EOR	Z	001 000	1Z	Exclusive OR to Register Zero	CC (Note 1)	2
		I	001 001	2I	Exclusive OR Immediate	CC (Note 1)	2
		R	001 010	2R	Exclusive OR Relative	CC (Note 1)	3
		A	001 011	3A	Exclusive OR Absolute	CC (Note 1)	4
COMPARE	COM	Z	111 000	1Z	Compare to Register Zero Arithmetric/Logical	CC (Note 3)	2
		I	111 001	2I	Compare Immediate Arithmetic/Logical	CC (Note 4)	2
		R	111 010	2R	Compare Relative Arithmetic/Logical	CC (Note 4)	3
		A	111 011	3A	Compare Absolute Artihmetic/Logical	CC (Note 4)	4
ROTATE	RRR		010 100	1Z	Rotate Register Right w/wo Carry	C, CC, IDC, OVF	2
	RRL		110 100	1Z	Rotate Register Left w/wo Carry	C, CC, IDC, OVF	2
BRANCH	BCT	R	000 110	2R	Branch On Condition True Relative	—	3
		A	000 111	3B	Branch On Condition True Absolute	—	3
	BCF	R	100 110	2R	Branch On Condition False Relative	—	3
		A	100 111	3B	Branch On Condition False Absolute	—	3
	BRN	R	010 110	2R	Branch On Register Non-Zero Relative	—	3
		A	010 111	3B	Branch On Register Non-Zero Absolute	—	3
	BIR	R	110 110	2R	Branch On Incrementing Register Relative	—	3
		A	110 111	3B	Branch On Incrementing Register Absolute	—	3

Table 2.

INSTRUCTION SET (Continued)

	MNEMONIC	OP CODE	FORMAT*	DESCRIPTION OF OPERATION	AFFECTS	CYCLES
BRANCH	BDR R	111 110	2R	Branch On Decrementing Register Relative	—	3
	BDR A	111 111	3B	Branch On Decrementing Register Absolute	—	3
	ZBRR	100 110 11	2ER	Zero Branch Relative, Unconditional	—	3
	BXA	100 111 11	3EB	Branch Indexed Absolute, Unconditonal (Note 5)	—	3
SUBROUTINE BRANCH/RETURN	BST R	001 110	2R	Branch To Subroutine On Condition True, Relative	SP	3
	BST A	001 111	3B	Branch To Subroutine On Condition True, Absolute	SP	3
	BSF R	101 110	2R	Branch To Subroutine On Condition False, Relative	SP	3
	BSF A	101 111	3B	Branch To Subroutine On Condition False, Absolute	SP	3
	BSN R	011 110	2R	Branch To Subroutine On Non-Zero Register, Relative	SP	3
	BSN A	011 111	3B	Branch To Subroutine On Non-Zero Register, Absolute	SP	3
	ZBSR	101 110 11	2ER	Zero Branch To Subroutine Relative, Unconditional	SP	3
	BSXA	101 111 11	3EB	Branch To Subroutine, Indexed, Absolute Unconditional (Note 5)	SP	3
	RET C	000 101	1Z	Return From Subroutine, Conditional	SP	3
	RET E	001 101	1Z	Return From Subroutine and Enable Interrupt, Conditional	SP, II	3
INPUT/OUTPUT	WRTD	111 100	1Z	Write Data	—	2
	REDD	011 100	1Z	Read Data	CC (Note 1)	2
	WRTC	101 100	1Z	Write Control	—	2
	REDC	001 100	1Z	Read Control	CC (Note 1)	2
	WRTE	110 101	2I	Write Extended	—	3
	REDE	010 101	2I	Read Extended	CC (Note 1)	3
MISC.	HALT	010 000 00	1E	Halt, Enter Wait State	—	2
	NOP	110 000 00	1E	No Operation	—	2
	TMI	111 101	2I	Test Under Mask Immediate	CC (Note 6)	3
PROGRAM STATUS	LPS U	100 100 10	1E	Load Program Status, Upper	F, II, SP	2
	LPS L	100 100 11	1E	Load Program Status, Lower	CC, IDC, RS, WC, OVF, COM, C	2
	SPS U	000 100 10	1E	Store Program Status, Upper	CC (Note 1)	2
	SPS L	000 100 11	1E	Store Program Status, Lower	CC (Note 1)	2
	CPS U	011 101 00	2EI	Clear Program Status, Upper, Masked	F, II, SP	3
	CPS L	011 101 01	2EI	Clear Program Status, Lower, Masked	CC, IDC, RS, WC, OVF, COM, C	3
	PPS U	011 101 10	2EI	Preset Program Status, Upper, Masked	F, II, SP	3
	PPS L	011 101 11	2EI	Preset Program Status, Lower, Masked	CC, IDC, RS, WC, OVF, COM, C	3
	TPS U	101 101 00	2EI	Test Program Status, Upper, Masked	CC (Note 6)	3
	TPS L	101 101 01	2EI	Test Program Status, Lower, Masked	CC (Note 6)	3

*FORMAT CODE: The number indicates the number of bytes. The letter(s) indicate the format type(s). See Fig. 6.

NOTES:
1. Condition code (CC1, CC0): 01 if positive, 00 if zero, 10 if negative.
2. Condition code is set to a meaningless value.
3. Condition code (CC1, CC0): 01 if RO > r, 00 if RO = r, 10 if RO < r.
4. Condition code (CC1, CC0): 01 if r > V, 00 if r = V, 10 if r < V.
5. Index register must be register 3 or 3'.
6. Condition code (CC1, CC0): 00 if all selected bits are 1s, 10 if **not** all the selected bits are 1s.

PROGRAM STATUS WORD

PSU

7	6	5	4	3	2	1	0
S	F	II	Not Used	Not Used	SP2	SP1	SP0

PSL

7	6	5	4	3	2	1	0
CC1	CC0	IDC	RS	WC	OVF	COM	C

S Sense
F Flag
II Interrupt Inhibit
SP2 Stack Pointer Two
SP1 Stack Pointer One
SP0 Stack Pointer Zero
CC1 Condition Code One
CC0 Condition Code Zero
IDC Interdigit Carry
RS Register Bank Select
WC With/Without Carry
OVF Overflow
COM Logical/Arith. Compare
C Carry/Borrow

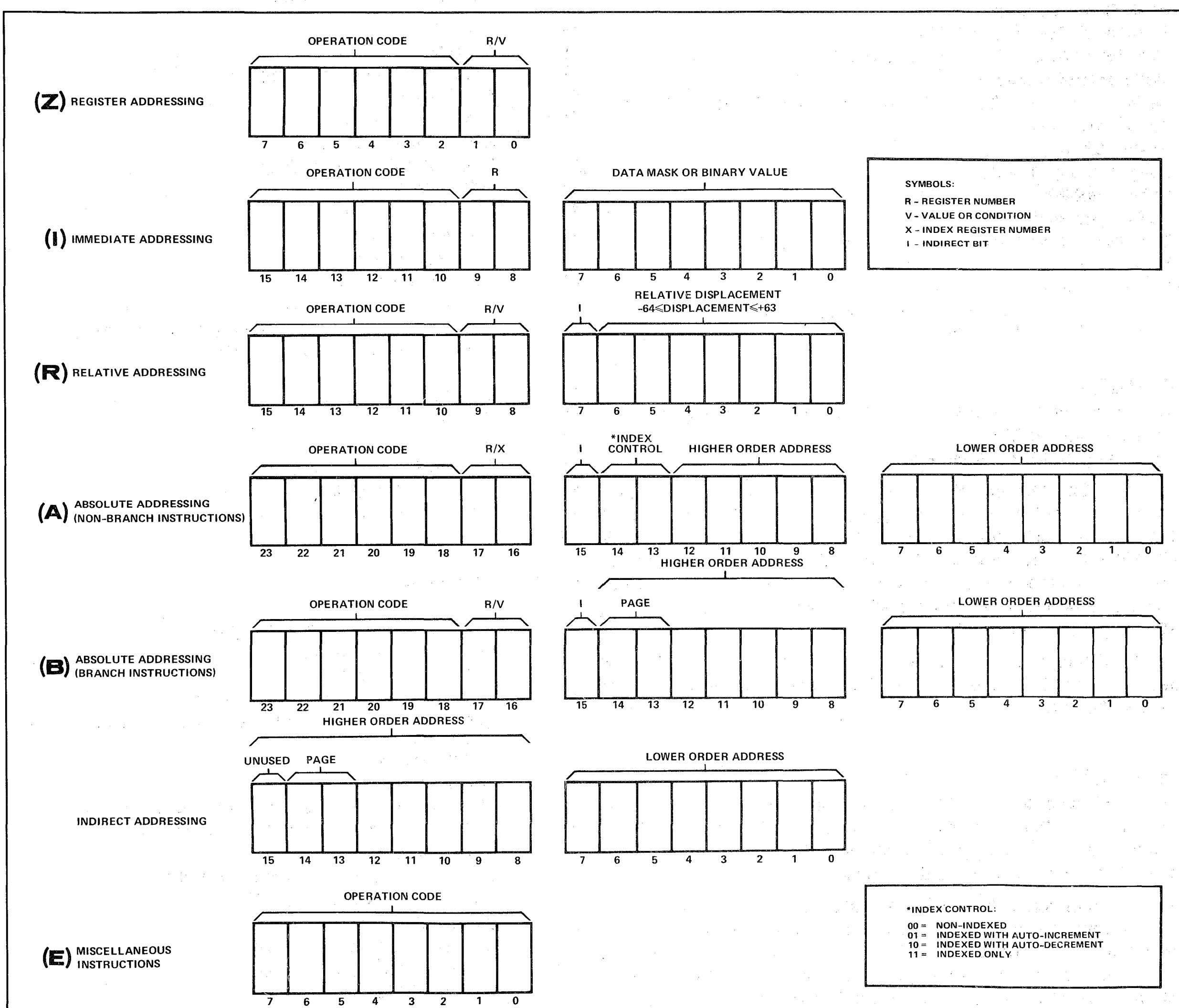


Figure 6. INSTRUCTION FORMATS

DESCRIPTION

The 2650PC1001 is a complete microcomputer on a single printed circuit board. The heart of this computer is Signetics' 2650 Microprocessor; a single chip, N-Channel MOS Integrated Circuit which contains the CPU and control sections of the classical general purpose computer architecture.

In addition to the Microprocessor, the 2650PC1001 contains both control and read/write memory, I/O ports, clock, and all the necessary buffering and interface circuits to permit data transfer both on and off the p.c.b. A block diagram of the system is shown in Figure 1.

FEATURES

- **2650 Microprocessor**
- **1k bytes of ROM with PIPBUG***
- **1k bytes of RAM (off-board expandable)**
- **1MHz crystal oscillator**
- **Serial I/O (either TTY 20mA current loop or RS232—selectable by jumper wire)**
- **2 eight-bit output ports**
- **2 eight-bit input ports**
- **DMA capability**
- **Led display indicators**
- **Data bus and address bus test points**
- **Buffered data and address outputs**
- **Single power supply (+5 volts)****

*Signetics Loader and Debugging Program. (See appl. note SS50)
**Assumes RS232 I/O port is not used.

MEMORY

The memory of the 2650PC1001 is divided into two segments:

a. ROM with PIPBUG
b. RAM (Read/Write Memory)

The Read-Only Memory (ROM) supplied with the card is the Signetics' 82S129 Field Programmable type (PROM). Eight of these 256 X 4 devices are arranged to provide a 1K X 8 memory array. The 265OPC1001 is supplied with the PIPBUG loader and debugger already programmed into the ROM. Since the devices are loaded into sockets, however, they can be easily replaced with other ROMs or PROMs programmed by the user.

The 1K X 8 array is constructed with Signetics' 2606 NMOS RAM devices. Since the 2606 is a 256 X 4 device, again 8 devices are used in the array.

SERIAL I/O

The serial I/O capability of the 2650PC1001 utilizes a unique serial I/O feature of the basic 2650 microprocessor. This feature allows serial data to be transferred directly into the 2650 under program control by using the sense and flag pins on the microprocessor.

Two types of serial I/O ports are available. The first is a teletype interface which can be directly connected to a teletype 20mA current loop. The second is an RS232 interface which provides a connection for voltage driven peripheral equipment. The selection of the particular interface to be used is made by connecting a jumper wire directly from the microprocessor flag and sense lines to the appropriate output port. If the RS232 interface is used, +12 and −12 volt supplies are required in addition to the +5 volt supply which operates the rest of the board.

PARALLEL I/O

Parallel I/O channels using the 2650's unique Non-Extended I/O mode are also provided. This mode allows a single byte instruction to select one of two distinct I/O devices. On the 2650PC1001, these two devices are represented by four separate data channels; two for reading and two for writing. The output (or write) channels are fully latched and buffered. The input (or read) channels are fully buffered. One read and one write channel represents a single I/O device. In addition to the Non-Extended I/O ports, the data and address buses, plus the appropriate control signals, are also available to provide the full extended I/O capability.

OTHER I/O

A complete listing of the I/O pins, plus a brief description of any I/O signal not detailed above, is as follows:

1,2	Ground
4-11	*Processor Data Bus*
12	Strobe to Enable Input Data Port
13	*D/C* Output
14	DMA Control Input
15	*Extended/Non-Extended* Output
16	*Interrupt Acknowledge* Output
17	*R/W* Output
18	*Write Pulse* Output
19	*Run/Wait* Output
20	*Operation Request* Output
21	*Memory/IO* Output
22	*Operation Acknowledge* Input
23	Clock Output (or Input if on-board clock not used)
24	Operation Request Input for DMA
25	*Reset* Input
26	*Interrupt Request* Input
27	*Pause* Input
28-32	Unused
33-47	*Address Bus*
48	+12 Volts for RS232
49	−12 volts for RS232
50	+5 volts
A, B	Ground
C	Not used
D-M	Non-Extended Output Port "D"
N	Clock to load data into Output Port "D"
P	TTY serial data Input (+)
R	TTY serial data Input (−)
S	TTY serial data Output pull up resistor (current loop +)
T	TTY serial data Output; TTL Level, open collector (current loop return)
U	RS232 ground
V	RS232 Output
W	TTY tape reader Output; TTL Level, open collector (+)
X	TTY tape reader Output pull up resistor (−)
Y	RS232 Input
Z	Clock to load data into Output Port "C"
a-h	Non-Extended Output Port "C"
j	Strobe to enable Input Port Control
k-u	Non-Extended Input Port "D"
v-$\bar{c}$	Non-Extended Input Port "C"
$\bar{d}$	+12 for RS232
$\bar{e}$	−12 for RS232
$\bar{f}$	+5 Volts

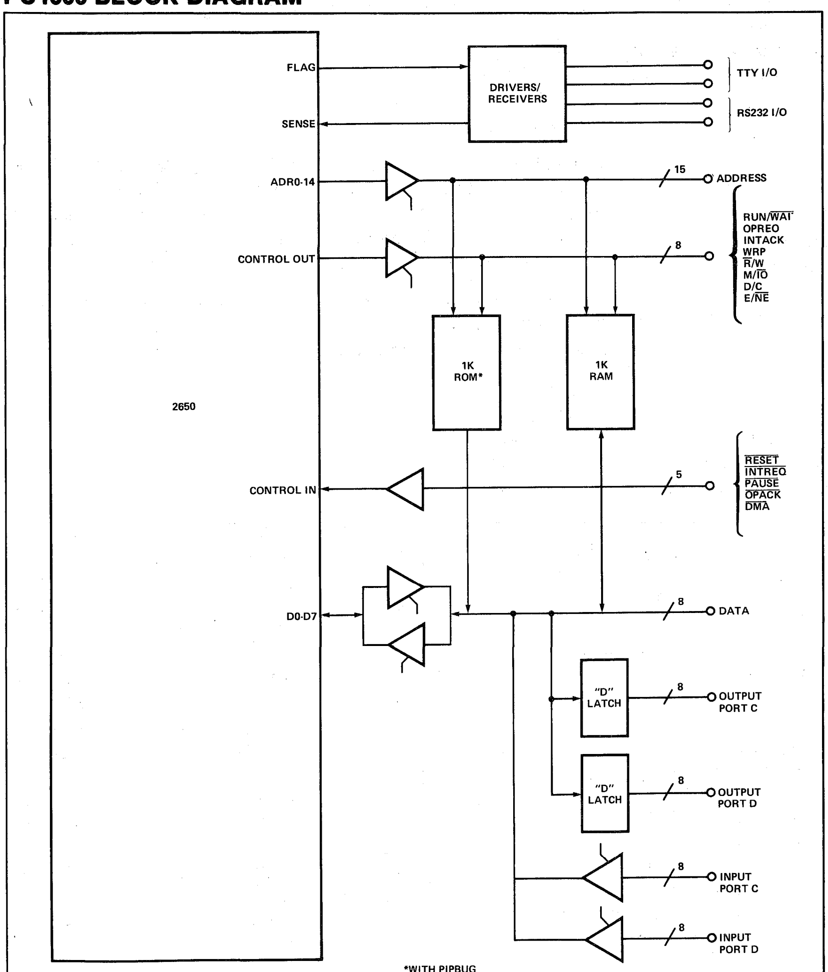
NOTE:
Italic items indicate buffered 2650 Microprocessor Outputs.

SUMMARY

The above is intended to provide a brief description of Signetics' 2650PC1001 Prototyping Board. More detailed information can be obtained from the following:

SS50	PIPBUG Application Note
SP50	2650PC1001 Manual (Detailed Description)
AS50	Serial I/O using Sense and Flag Application Note
2650BM1001	Basic 2650 Microprocessor Manual
	2650 Introductory Brochure

PC1000 BLOCK DIAGRAM



4K MEMORY CARD

DESCRIPTION

The 2650 PC2000 is a 4K Memory Card designed to be compatible with the 2650 microprocessor. It is composed of 32, 21L02 NMOS, 1K by 1 bit static RAM's, and organized in four groups of one kilobyte each. Decoding is provided to select one of the four groups and also distinguish the card in multi-card configurations. In a system application utilizing up to 8 cards (32K), each card is uniquely identified by hardwired jumpers. No external decoding is required.

The decoding logic is sectioned into two blocks. The first block determines if the address identifies that card as being part of the 8K page address. (The 2650 memory scheme is organized into 4 pages of 8K each.) The second block uniquely locates 1K bytes of memory on the board in the 8K bytes of memory of the selected page. Each 1K bank is individually selected by hardwired jumpers to the decoder.

FEATURES

- **Requires only single +5V supply**
- **Industry standard 21L02 memories**
- **Fully decoded for 32K memory organization**
- **Data bus buffered with tri-state drivers/receivers**
- **Accessable from microprocessor or DMA controller**
- **TTL compatible**
- **Dimensions are 8" X 6.875" with a 50 pin edge connector along the 8" dimension**
- **Typical power consumption of 4.5 watts**

SIGNAL DEFINITION

Memory control signals and address lines between the 2650 microprocessor and the 2650 PC2000 are indicated in the block diagram. The OPEX control line is reserved for use with DMA controllers. Its function is similar to that of the OPREQ line from the 2650. When either of these lines are true and a memory operation is specified (M/IO = High) the memory card is enabled to decode address lines AO through A14. When a bank is selected, the selected card control logic block allows the read-write line (R/W) and write pulse (WRP) to pass to the memory array and also enable the external data bus drivers. When the operation is complete the memory card responds with a true condition on OPACK.

JUMPER ADDRESS DECODING

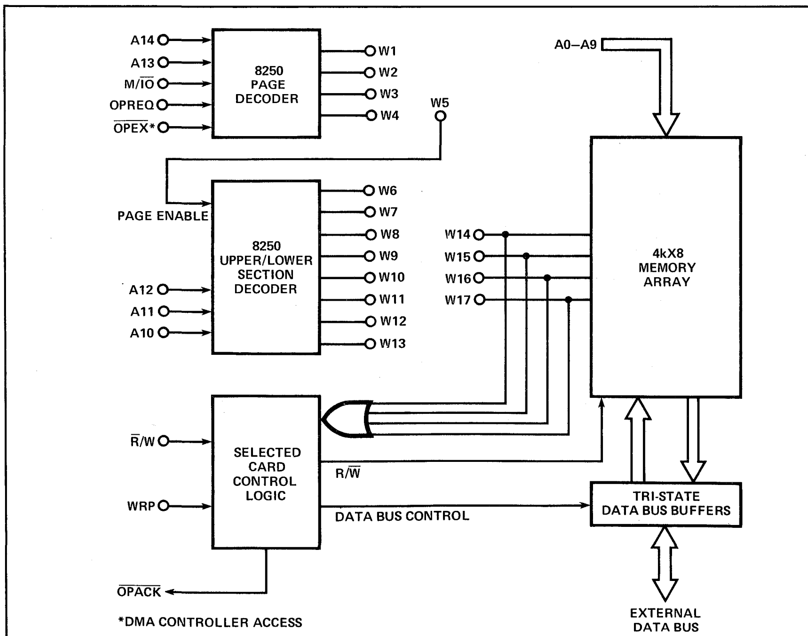
Jumpers are applied to designated plated-through holes identified by a 'Wn' mnemonic. To identify the card to be part of a particular page, jumper point W5 to one of the following:

WI for page 0
W2 for page 1
W3 for page 2
W4 for page 4

To locate each of the 1K bytes of the memory card in the selected memory page, four bank jumpers are required. The outputs of the decoder used to select one of eight 1K byte memory segments (W6-W13) must be connected to the selected 1K bytes of memory on the 2650 PC2000 (W14-W17).

Factory installed jumpers allow for immediate hook-up to a Demo System (DS1000/2000) which has 2K of memory. These jumpers have been hooked-up as follows:

W1 to W5 (page 0)
W8 to W14
W9 to W15
W10 to W16
W11 to W17



2650 PC2000 BLOCK DIAGRAM

2650 PC 2000 EDGE CONNECTOR

PIN	NAME	PIN	NAME
1,2,A,B	GROUND	34	ABUS13
4	DBUSO	35	ABUS12
5	DBUS1	36	ABUS14
6	DBUS2	37	ABUS9
7	DBUS3	38	ABUS10
8	DBUS4	39	ABUS8
9	DBUS5	40	ABUS7
10	DBUS6	41	ABUS6
11	DBUS7	42	ABUS5
17	R/W	43	ABUS3
18	WRP	44	ABUSO
20	OPREQ	45	ABUS1
21	M/IO	46	ABUS4
22	OPACK	47	ABUS2
24	OPEX	50,f	VCC +5V
33	ABUS11		

DESCRIPTION

The Demo System 2000 (2650 DS2000) is a hardware base for use with the 2650 CPU printed circuit board (PC1001) and allows the exercising of this card with user defined options. When the DS2000 is combined with a CPU board (PC1001) and a TTY, the user is equipped with everything he needs to exercise any of the software or hardware features of the 2650. The DS2000 has a built in power supply.

FEATURES

- **User defined expansion capability from connector supplying address, data and control lines.**
- **RS232 and TTY interface**
- **Two extended and two non-extended I/O ports**
- **Single step capability for program debugging**
- **Display of address bus, data bus and the two non-extended I/O ports**

CONNECTORS

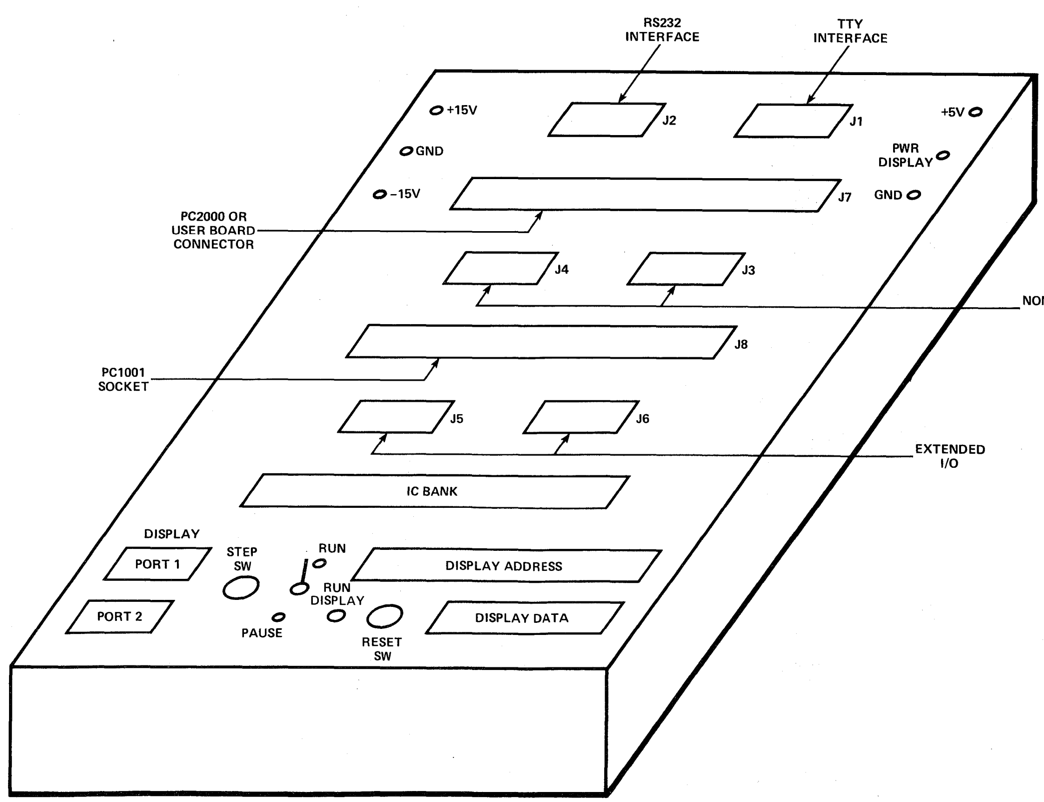
The 2650 CPU Board (PC1001) is inserted into the J8 connector to complete the demo system. The user printed circuit board is inserted into the J7 connector. Both connectors are the same type (100 Pin Amphenol, series 225) and the numbered pins of J7 and J8 have the same signals (except pin 12). The lettered pins of J7 (pins A through $\overline{g}$) are not used. The sockets and connectors of the DS2000 and their associated signals are provided in this data sheet.

DISPLAYS

The address and data bus led displays reflect the information on these buses during each OPREQ (beginning of an external operation). Latches store the information until another OPREQ is received. The two non-extended port displays represent data on channel C (port 2) and channel D (port 1) during the OPREQ for each I/O operation. A logic one on these displays will turn "on" the leds and a logic zero will turn them "off."

CONTROLS

The pause and step logic allows one instruction to be executed at a time by pushing the 'step' button when the Run/Pause switch is in the pause position. In this mode the Run/$\overline{\text{Wait}}$ display led will go off. The reset switch will reset the display latches and place all zeros in the 2650 instruction address register.



DS2000 HARDWARE BASE

MICROPROCESSOR

SIGNAL NAMES FOR CONNECTORS 17 AND 18

PIN NO.	FUNCTION (J7 & J8)	PIN NO.	FUNCTION (J8 ONLY)*
1	GND	A	GND
2	GND	B	GND
3	NC**	C	NC
4	$\overline{\text{DBUS0}}$	D	OPD 0
5	$\overline{\text{DBUS1}}$	E	OPD 1
6	$\overline{\text{DBUS2}}$	F	OPD 2
7	$\overline{\text{DBUS3}}$	H	OPD 3
8	$\overline{\text{DBUS4}}$	J	OPD 4
9	$\overline{\text{DBUS5}}$	K	OPD 5
10	$\overline{\text{DBUS6}}$	L	OPD 6
11	$\overline{\text{DBUS7}}$	M	OPD 7
12*	EIPD	N	COPD
13	D/$\overline{\text{C}}$	P	TTY SERIAL IN +
14	$\overline{\text{DMA}}$	R	TTY SERIAL IN −
15	E/$\overline{\text{NE}}$	S	TTY SERIAL OUT +
16	INTACK	T	TTY SERIAL OUT −
17	$\overline{\text{R}}$/W	U	RS232 GROUND
18	WRP	V	RS232 OUTPUT
19	RUN/$\overline{\text{WAIT}}$	W	TTY TAPE READER OUT +
20	OPREQ	X	TTY TAPE READER OUT −
21	M/$\overline{\text{IO}}$	Y	RS232 INPUT
22	$\overline{\text{OPACK}}$	Z	COPC
23	CLOCK	a	OPC 0
24	$\overline{\text{OPEX}}$	b	OPC 1
25	$\overline{\text{RESET}}$	c	OPC 2
26	$\overline{\text{INTREQ}}$	d	OPC 3
27	$\overline{\text{PAUSE}}$	e	OPC 4
28	NC	f	OPC 5
29	NC	g	OPC 6
30	NC	h	OPC 7
31	NC	j	EIPC
32	NC	k	IPD 0
33	ABUS 11	m	IPD 1
34	ABUS 13	n	IPD 2
35	ABUS 12	p	IPD 3
36	ABUS 14	r	IPD 4
37	ABUS 9	s	IPD 5
38	ABUS 10	t	IPD 6
39	ABUS 8	u	IPD 7
40	ABUS 7	r	IPC 0
41	ABUS 6	w	IPC 1
42	ABUS 5	x	IPC 2
43	ABUS 3	y	PIC 3
44	ABUS 0	z	IPC 4
45	ABUS 1	a	IPC 5
46	ABUS 4	b	IPC 6
47	ABUS 2	c	IPC 7
48	+12V	d	+12V
49	−12V	e	−12V
50	+5V	g	+5V

*J7 has no connections to these pins.
**NC = No Connection

EXTENDED INPUT/OUTPUT DIP SOCKETS

PIN NO.	FUNCTION J5	FUNCTION J6
1	$\overline{\text{DBUS 0}}$	ABUS 0
2	$\overline{\text{DBUS 1}}$	ABUS 1
3	$\overline{\text{DBUS 2}}$	ABUS 2
4	$\overline{\text{DBUS 3}}$	ABUS 3
5	$\overline{\text{DBUS 4}}$	ABUS 4
6	$\overline{\text{DBUS 5}}$	ABUS 5
7	$\overline{\text{DBUS 6}}$	ABUS 6
8	$\overline{\text{DBUS 7}}$	ABUS 7
9	OPACK	ABUS 8
10	M/$\overline{\text{IO}}$	ABUS 9
11	OPREQ	ABUS10
12	RUN/$\overline{\text{WAIT}}$	ABUS11
13	WRP	ABUS12
14	$\overline{\text{R}}$/W	ABUS13
15	INTACK	ABUS14
16	E/$\overline{\text{NE}}$	$\overline{\text{PAUSE}}$
17	$\overline{\text{DMA}}$	$\overline{\text{INTREQ}}$
18	D/$\overline{\text{C}}$	CLOCK

NON-EXTENDED INPUT/OUTPUT DIP SOCKETS

PIN NO.	FUNCTION J3		FUNCTION J4	
1	(Output Port C)	0	(Output Port D)	0
2	OPC	1	OPD	1
3	OPC	2	OPD	2
4	OPC	3	OPD	3
5	OPC	4	OPD	4
6	OPC	5	OPD	5
7	OPC	6	OPD	6
8	OPC	7	OPD	7
9	Clock Output Port	C	Clock Output Port	D
10	Enable Input Port	C	Enable Input Port	D
11	(Input Port C)	7	(Input Port D)	7
12	IPC	6	IPC	6
13	IPC	5	IPC	5
14	IPC	4	IPC	4
15	IPC	3	IPC	3
16	IPC	2	IPC	2
17	IPC	1	IPC	1
18	IPC	0	IPC	0

DESCRIPTION

The 2650 PC3000 is a basic text generating system requiring only six integrated circuits including one 2650 microprocessor. The serial communication link between the 2650 and the users terminal is accomplished with the flag and sense lines on the microprocessor. The 2650 PC3000 is used to control the storage of characters entered from a terminal with either a current loop or voltage swing capability (±7.5V min).

Control Characters allow the text to be printed out on the terminal with the capability for inserting unique characters at locations identified during text generation. When the text is printed out the entire text will be output unless a control character is detected. The microprocessor then stops the print-out and the operator enters the desired unique information. Another control character is then given to continue printing the text until all characters stored in memory are printed, or until another stop character is detected. The stop character is recorded in memory just like any other character; however, it is not printed during text print-out.

Additional control characters allow for the erasure of the previous character typed or the erasure of the entire memory.

FEATURES

- **Total of six IC packages**
- **Operates at +5V at a max of 500 ma**
- **Interface to either current loop or device capable of sending and receiving a minimum voltage swing of ±7.5 volts referenced to signal ground**
- **250 character storage capability**
- **Card size less than 3" X 4" with four screwed-on stand-offs at corners**
- **1 MHZ clock implemented with 74123 oneshot**
- **Variable baud rate between 110 and 300 baud by trimmer pot adjustment of clock**
- **PROM mounted in 24 pin socket**
- **Card edge connector supplied with each card**
- **Inputs provided for an external system reset.**

PART DESCRIPTIONS

2650	8-bit TTL compatible N-Channel Microprocessor incorporating a serial I/O Port. (See 2650 Hardware Specification Manual for complete description — 2650 BM1000.)
2606	1024-bit static MOS, TTL compatible RAM memory organized as 256 words by 4 bits/word.
82S115	4096-bit Bipolar TTL compatible PROM organized as 512 words by 8 bits/word.
N7426	Quad 2-input high voltage nand gate with open collector capable of driving voltage and current loop interfaces (20 ma maximum).
74123	Dual retriggerable monostable multivibrator with clear configured as a clock for 2650.
Potentiometer	Helipot series 91C, 50K, OHM 3/8" cermet trimming potentiometer.
PC Edge Connector	Ampnenol — 225-21021-401-117 Cinch — 251-10-30-160

Miscellaneous components consist of 11 (¼) watt and two (½) watt resistors, and two mica, one ceramic and one tantilum capacitor.

The following are required to make the board functional but are not supplied with the card:

RS232 type connector for voltage swing interface: DB25P or DB25S

Reset switch — (normally open, connected to +5V)

Power supplies: +5V
±15V

TERMINAL INTERFACE

VOLTAGE MODE TERMINAL CONNECTION

The voltage mode interface is very similar to the standard RS232 interface except that the "signal" ground cannot be connected to "protective" ground. When a Cinch type 25-pin connector (DB25P or DB25S) is used on an RS232 compatible terminal, the PC3000 should be connected as follows:

Voltage Mode Terminal Pin Description

DB25P (DB25S) Pin No.	PC3000 Edge Connector Pin No.	PC3000 Signal Name
1	No connection	—
3	6	VS OUT +
2	J	VS IN +
7	K	VS OUT — (Signal Gnd.)
5,6,8,20	Connect Together	—

On card jumper point 'A' to 'C' and point 'D' to 'E'.

CURRENT LOOP TERMINAL CONNECTION

When a terminal is used that employs current loop transmission techniques the four wires from the terminal should be connected to the corresponding four pins on the PC3000 card: TTY OUT +, TTY OUT −, TTY IN +, and TTY IN −.

On card jumper point 'A' to 'B' and point 'D' to 'F'.

PC3000 COMMAND SUMMARY

KEY	FUNCTION
Rubout (delete)	Erase last character in memory and echo the erased character. Additional preceding characters can be erased by continuing to depress the delete key.
Control and E	Erase entire memory.
Control and B	Used to indicate beginning of inserted message. Is not printed but stored in memory. Stops print-out when read from memory. Required once from each unique information entry.
Control and C	Continues print-out of memory after entry of unique information.
Control and P	Prints out contents of terminal memory.
Control and R	Software reset.

NOTE:
Bell will ring if any of the following are true.
1. Entering more than 250 characters in memory.
2. Requesting print-out of an empty buffer.
3. Attempting to delete more characters than there are in memory.

PC3000 CONNECTOR PIN ASSIGNMENT

PIN	FUNCTION	PIN	FUNCTION
1	GND	A	GND
2	+5	B	+5
3	+15	C	+15V
4	−15	D	−15
5	−	E	TTY IN−
6	VS OUT +	F	TTY OUT+
7	TTY IN+	H	TTY OUT−
8	−	J	VS IN+
9	RESET	K	VS OUT− (Signal Ground)
10	GND	L	GND

VS — Voltage Swing

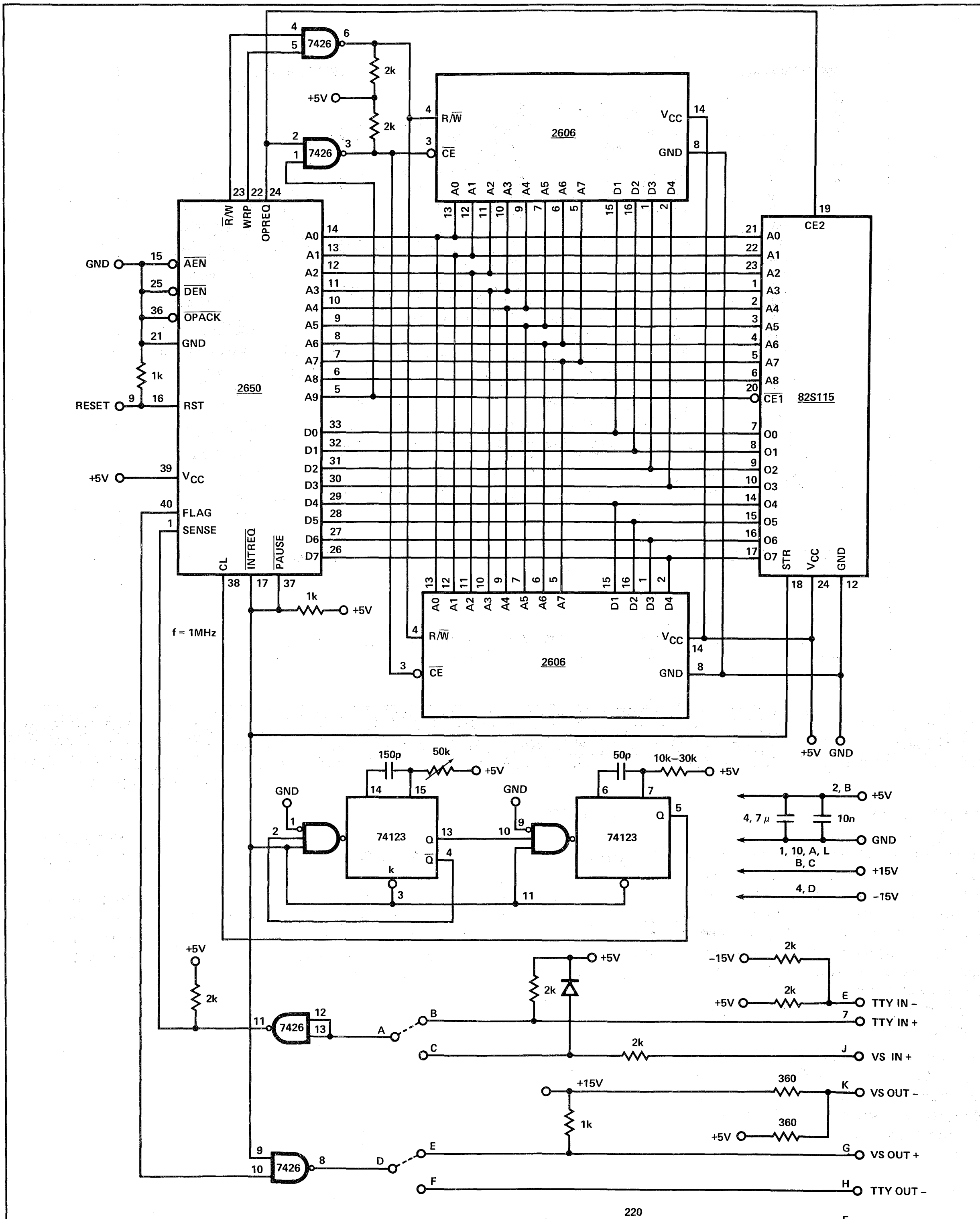
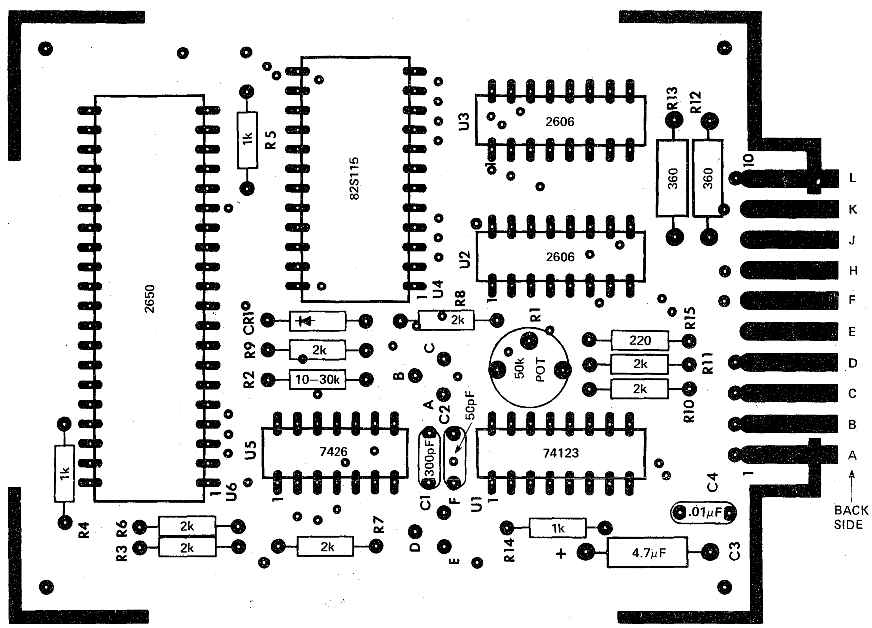


Figure 1 INTELLIGENT TYPEWRITER CONTROLLER



INTELLIGENT TYPEWRITER CONTROLLER BOARD LAYOUT

MICROPROCESSOR PROTOTYPING KIT — 2650 KT9000

2650 MICROPROCESSOR SERIES

DESCRIPTION

The KT9000 kit contains a 2650 microprocessor and enough chips to allow for the implementation of a small developmental system. Since the interface requirements of the 2650 are completely TTL compatible, no attempt has been made to limit the user's flexibility by dictating a fixed logic configuration. There is complete freedom in using standard SSI or MSI logic to adapt the microprocessor to the memory, I/O devices, or clock.

Several minimal system examples are presented to enable quick set up and evaluation. Other configurations to adapt to individual requirements should become evident from these examples.

PARTS LIST

PART NO.	QTY	DESCRIPTION	REFERENCE DATA SHEET
2650	1	CPU	—
2112	4	256 X 4 RAM	MOS Products
82S115I	1	4K PROM (Unprogrammed) 512 X 8	Bipolar Memories
8T31I	2	8-bit Bidirectional I/O Port	8000 Product
8T26B	4	Quad Bus DR/RREC	8000 Product
2650BM1000	1	Basic Manual	—

PARTS DESCRIPTIONS

2112: The 2112 is a static 1024-bit Random Access Memory organized as 256 words by 4 Bits/Word. It is fabricated with N-Channel, Silicon Gate, MOS technology and achieves an access time of less than 800 nanoseconds. No clocks are required, and the chip is powered from a single 5 volt source.

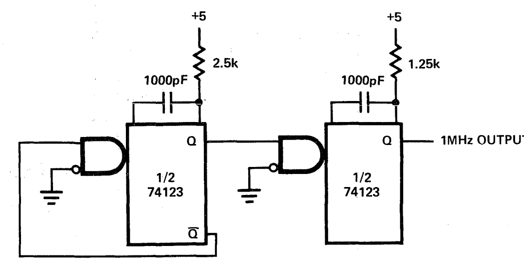
82S115I: The 82S115I is a 4096-bit Schottky-Clamped, Bipolar Read Only Memory, incorporating on-chip data output registers. It is field-programmable and fully TTL compatible with on-chip decoding and two chip enable inputs for ease of memory expansion. Inputs to the device are PNP transistors with a maximum current requirement of 100 μA.

8T31: The 8T31 is an 8-bit Bidirectional I/O Port designed to function as a general purpose I/O interface element. It consists of 8 clocked latches with two sets of bidirectional Inputs/Outputs. The capability exists for various hook-up schemes allowing master control from either the microprocessor or from the I/O device.

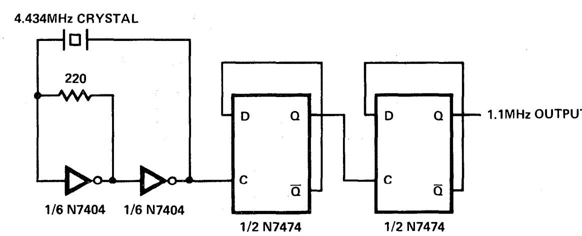
8T26B: The 8T26B consists of four pairs of inverting Tri-State Logic elements configured as a Quad Bus Drivers/Receivers with separate buffered receiver enable and driver enable lines. Both the driver and receiver gates have Tri-State outputs and low-current PNP inputs.

CIRCUIT EXAMPLES

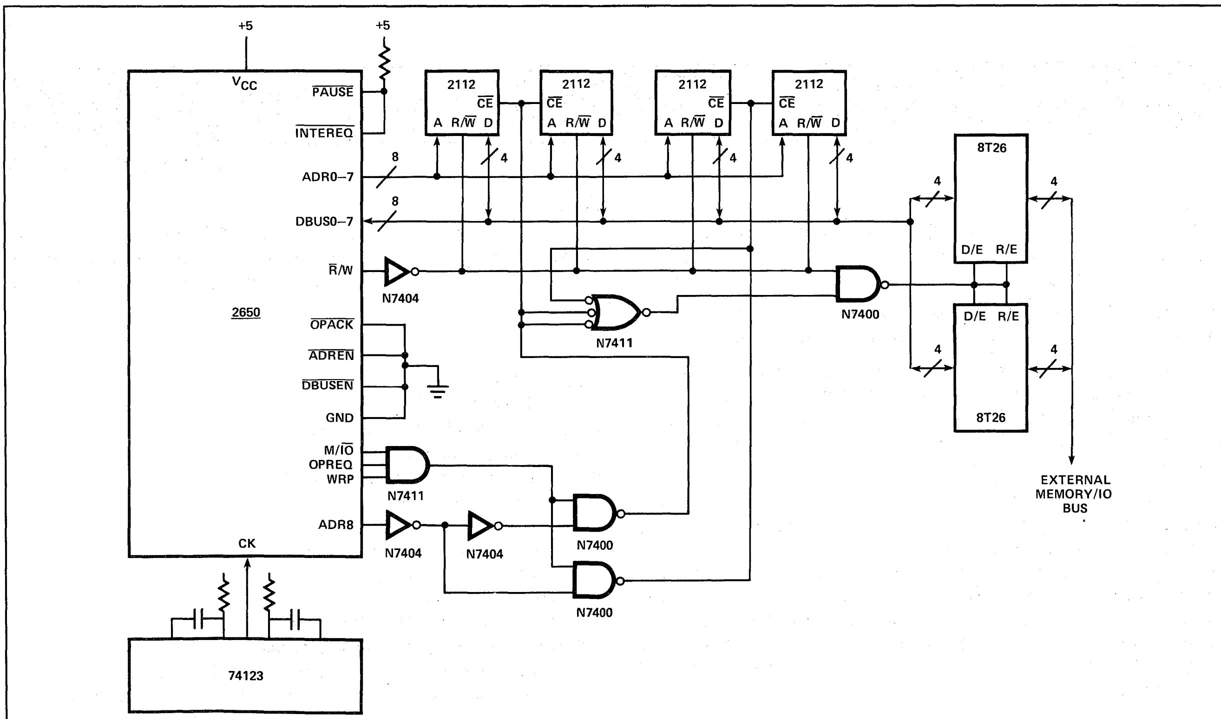
Two circuit configurations are presented to indicate a possible program checkout approach. The first figure is hooked up to allow the use of RAM for program debugging. The second figure represents a possible final system configuration with the program fixed in PROM. Both circuits use the 8T26's as bus buffers.



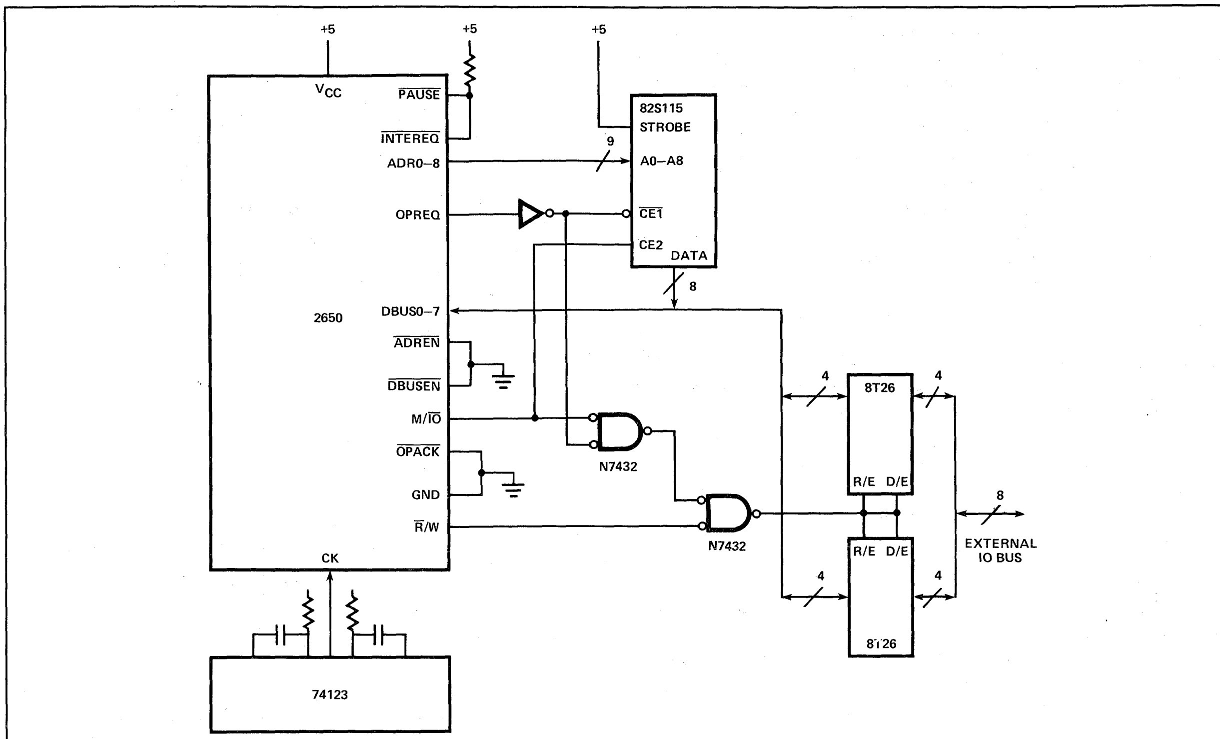
ONESHOT CLOCK OSCILLATOR CIRCUIT



CRYSTAL OSCILLATOR CIRCUIT



EXAMPLE OF INITIAL PROGRAM CHECKOUT CONFIGURATION



FINALIZED CONFIGURATION WITH PROGRAM FIXED IN PROM

2650 ASSEMBLER VERSION 3.2 — 2650 AS1000/1100

2650 MICROPROCESSOR SERIES

DESCRIPTION

The 2650 assembly language (PIPHASM) is a symbolic language designed specifically to facilitate the writing of programs for the Signetics 2650 microprocessor.

The AS1000 is configured to operate on 32-bit or larger machines and the AS1100 is configured to operate on 16-bit machines.

The 2650 assembler is a program which accepts symbolic source code as input and produces a listing and/or an object module "Hexadecimal" format compatible to the two tape punching programs PIPHTAP (for acceptance by PIPBUG), PIPSTAP (for PROM's) and also to the simulator, PIPSIM.

The assembler is written in standard Fortran IV and is approximately 1,250 Fortran card images in length. It is modular and may be executed in an overlay mode should memory restrictions make that necessary. It operates in a two pass mode to build a symbol table, to issue helpful error messages, produce an easily readable program listing and output a computer readable object module. This version of the assembler compiles into a 12K word load module on the PDP-11/40 (16 bit words) and executes under DOS (8K) within a 28K memory.

AVAILABILITY

The 2650 assembler is available on both NCSS and GE timeshare. It is also available from Signetics on 9 track magnetic tape written in EBCDIC in 80 character unblocked records at a density of 800 bpi.

FEATURES

- **Forward references**
- **Pseudo-Ops to aid programming**
- **Self-defining constants**
- **Symbolic machine operation codes**
- **Free format source code**
- **Syntax error checking**
- **Symbolic address assignment and references**
- **Data creation statements**
- **Storage reservation statements**
- **Assembly listing control statements**
- **Addresses can be generated as constants**
- **Character codes may be specified as ASCII or EBCDIC**
- **Comments and remarks may be encoded for documentation**

LANGUAGE REQUIREMENTS

I. INPUT REQUIREMENTS

Input to the assembler consists of a sequence of characters combined to form assembly language elements. These language elements include symbols, instruction mnemonics, constants and expressions which make up the individual program statements that comprise a source program.

A. Characters

Alphabetic:	A through Z
Numeric:	0 through 9
Special Characters:	blank
	(left parenthesis
	) right parenthesis
	+ add or positive value
	– subtract or negative value
	* asterisk
	' single quote
	, comma
	/ slash
	$ dollar sign
	< less than sign
	> greater than sign

B. Symbols

Symbols are formed from combination or characters. Symbols provide a convenient means of identifying program elements so they can be referenced by other elements.

C. Constants

A constant is a self-defining language element. Unlike a symbol, the value of a constant is its own "face" value and is invariant. Internal numbers are represented in 2's complement notation. There are two forms in which constants may be written: the Self-Defining Constant and the General Constant.

Self-Defining Constant

The self-defining constant is a form of constant which is written directly in an instruction and defines a decimal value.

General Constant

The general constant is also written directly in an instruction, but the interpretation of its value is dictated by a code character and delimited by quotation marks. Its form can be binary, octal, decimal, hexadecimal, EBCDIC or ASCII.

D. Expressions

An expression is an assembly language element that represents a value. It consists of a single term or combination of terms separated by arithmetic operators. A term may be a valid symbolic reference, a self-defining constant or a general constant.

II. FIELDS

A statement prepared for processing by the assembler is logically divided into four fields, as indicated below. They are free form and are separated by at least one blank character. The name must begin in logical column 1.

LABEL	OPERATION	OPERAND	COMMENTS
name	opcode	operand(s)	

Where:

LABEL FIELD	contains an optional label which the assembler will assign as the symbolic address of the first byte of the instruction.
OPERATION FIELD	contains any of the 2650 processor mnemonic operation codes as detailed in Appendix A, or any assembler Directive. This field may include an expression which specifies a register or value as required by the instruction. All symbols used in this field must have been previously defined, i.e., no symbolic forward references are allowed.
OPERAND FIELD	contains one or more operand elements such as indirect address indicator, operand expression, index register specification, auto-increment/auto-decrement indicator, constant specification, etc., depending on the requirements of the particular instruction.
COMMENTS FIELD	any characters following the argument field will be reproduced in the assembly listing without processing. The Comments Field must be separated from the argument field by at least one blank.

III. DIRECTIVES

There are eleven directives which the assembler will recognize. These assembler directives, although written much like processor instructions, are simply commands to the assembler instead of to the processor. They direct the assembler to perform specific tasks during the assembly process, but have no meaning to the 2650 processor. These assembler directives are:

- ORG — Set location counter
- EQU — Specify a symbol equivalence
- ACON — Define address constant
- DATA — Defines memory data
- RES — Reserve memory storage
- END — End of assembly
- EJE — Eject the listing page
- PRT — Printer control
- SPC — Space control
- TITL — Title
- PCM — Punch control

MICROPROCESSOR

DESCRIPTION

The 2650 Simulator (PIPSIM) is a Fortran IV program which allows a user to simulate the execution of his program without utilizing the 2650 processor. The simulator executes the 2650 program via host computer software by maintaining its own internal fortran storage registers to describe the 2650 program, the microprocessor registers, the ROM/RAM memory configuration, and the input data to be read dynamically from I/O devices. Inputs to the simulator are the object module (or the 2650 program in object format) produced by the 2650 assembler and a deck of user commands. The simulator can accommodate an object module of up to 8192 Bytes.

The output consists of a listing of the user's commands and a print out of both static and dynamic information as requested by the commands. The user may request traces of the processor status, dumps of the contents of memory, and recording of program timing statistics. Multiple simulations of the same program with different parameters may be executed during one simulation run.

The SM1000 is configured to operate on 32 bit or larger machines and executes under DOS (8K) within a 28K memory. The SM1100 is configured for 16 bit machines and compiles into a 16K word load module on a PDP-11/40.

AVAILABILITY

The 2650 Simulator is available on both NCSS and GE timeshare. It is also available from Signetics on a 9 track magnetic tape written in EBCDIC in 80 character unblocked records at a density of 800 bpi.

FEATURES

- **Cycle counter for timing estimates**
- **Instruction fetch break points**
- **Operand fetch break points**
- **Trace facilities**
- **Snapshot dumps**
- **Patching facility**
- **Statistical information generated**
- **Easy-to-use command language**
- **Optionally selected start and end addresses**
- **Simulated registers may be displayed while the simulation program is executed**
- **Simulated registers may be altered while the program is executing**
- **Maintains a 2K cell (easily modified to 8K) to simulate a read/write RAM**
- **Capability exists for configuring parts of simulator memory to look like ROM**
- **Incorporates a 200-byte first in, first out (FIFO) buffer to store the data read from a simulated input device**
- **Establishes initial program conditions**
- **Monitors execution sequences**

USER-COMMANDS

Commands specify how the program is to run and what data is to be recorded. The simulator accepts information in card image form. The entire card is read in Fortran 'A' format, and one command must be complete on one card. Comments may appear in any order within a command set.

The Signetics basic manual set (2650BM1000) contains a complete description of the user commands and the general operation of the simulator. Listed below is a summary of the available commands.

COMMAND NAME	PARAMETERS	DESCRIPTION
DUMP.	LOC, FWA-LWA (;....;LOC, FWA-LWA)	Display the area of memory, FWA-LWA, whenever the instruction at LOC executes.
REND	None	Execute the last simulation and terminate the entire run.
INPUT	VALUE (;....;VALUE)	Define the data to be read by simulated I/O instructions.
INSTR.	LOC (;....;LOC)	Display the processor state whenever the instruction at LOC executes.
LIMIT	NO	Specify the total number of instructions executed.
PATCH	LOC, VALUE (;....;LOC, VALUE)	Initialize each memory location, LOC, to VALUE.
REFER.	LOC (;....;LOC)	Display the processor state whenever the instruction at LOC is referenced by another instruction.
SETP.	LOC (,PSL=VALUE), (,PSU=VALUE)	Set the program status byte (lower and/or upper) to VALUE whenever the instruction at LOC executes.
SETR.	LOC (9, RO=VALUE)...(R6=VALUE)	Set the general purpose registers to VALUE whenever the instruction at LOC executes.
SROM	FWA-LWA	Specify the boundaries of Read-Only Memory.
START	LOC	Start the simulated program execution at LOC.
STAT	None	Display instruction statistics at end of program execution.
STOP.	LOC (;....;LOC)	Terminate the program execution when the instruction at LOC executes.
TEND	None	Execute the last simulation and prepare to read the User Commands for the next simulation.
TRACE.	FWA-LWA (;....;FWA-LWA)	Display the processor state whenever an instruction executes, which lies within the area of memory, FWA-LWA.

SIGNETICS HIGHER LEVEL LANGUAGE (PL/S)

DESCRIPTION
The Signetics higher level language is designed for use with the 2650 microprocessor. This language allows the programmer to reduce programming effort while retaining the control and efficiency of assembly language. It is written in ANSI standard Fortran IV and will execute on most machines without alteration. Programs written in this language tend to be self-documenting and are easily altered.

AVAILABILITY
The Signetics higher level language is available on both NCSS and GE timeshare. It is also available from Signetics on magnetic tape for 16 and 32-bit machines.

FEATURES
- **Written in free-form**
- **Adaptable to both 16 and 32-bit machines**
- **Block structured**
- **Employs procedure calls**
- **Byte and address data elements**
- **Based variables**
- **In line assembly language**
- **Macro capability**
- **Generates relocatable code supported by a relocating loader**
- **Includes PL/M as a subset**
- **Allows separate compilation of program modules**
- **Has improved control structure over PL/M**
- **Conditional compilation**
- **Compile time expression evaluation**

OVERVIEW OF THE LANGUAGE
The higher level language is a sequence of "Declarations" and "Executable Statements."

The declarations allow the programmer to control allocation of storage, define simple textual substitutions (Macros), and define procedures. The language is "Block Structured": Procedures may contain further declarations which control storage allocation and define other procedures.

The procedure definition facility of the language allows modular programming: A program can be divided into sections (e.g. teletype input, conversion from binary to decimal forms, and printing output messages). Each of these sections is written as a language procedure. Such procedures are conceptually simple, easy to formulate and debug, and easily incorporated into a large program. They may form a basis for a procedure library, if a family of similar programs is being developed. Procedures may be individually compiled.

The language handles two kinds of data, its two basic "Data Types": Byte and address. A byte variable or constant is one that can be represented as an 8-bit quantity; an address variable or constant is a 16-bit or double-byte quantity. The programmer can declare variable names to represent byte or address values. One can also declare vectors (or arrays) or type byte or address.

In general, executable statements specify the computational processes that are to take place. To achieve this, arithmetic, logical (Boolean), and comparison (relational) operators are defined for variables and constants of both types (BYTE and ADDRESS). These operators and operands are combined to form EXPRESSIONS, which resemble those of elementary algebra. Expressions are a major component of language statements.

A simple statement form is the assignment statement, which computes a result and stores it in a memory location defines by a variable name. Other statements in the language perform conditional tests and branching, loop control, and procedure invocation with parameter passing. The flow of program execution is specified by means of powerful control structures that take advantage of the block-structured nature of the language. Input and output statements read and write 8-bit values from and to input and output ports. Procedures can be defined which use these basic input and output statements to perform more complicated I/O operations.

A method of automatic text-substitution (more specifically, a "compile-time macor facility") is also provided. A programmer can declare a symbolic name to be completely equivalent to an arbitrary sequence of characters. As each occurrence of the name is encountered by the compiler, the declared character sequence is substituted, so the compiler actually processes the substituted character string instead of the symbolic name.

The compiler supports compile time expression evaluation and conditional compilation which allows selective compilation of code depending on an input parameter at compile time.

The language generates absolute and/or relocatable code. The relocatable modules may be linked by a powerful linkage editor at load time.

Additionally the language contains all machine independent features of the PL/M language as a subset, thereby enhancing portability of programs.

MICROCOMPUTER PROTOTYPE DEVELOPMENT SYSTEM (TWIN)

2650 MICROPROCESSOR SERIES

DESCRIPTION
The Signetics Microprocessor Prototype Development System is a modular system designed to support development and implementation of 2650 microcomputer systems.

A typical system consists of three hardware elements: a Prototype Development Computer (PDC), a floppy disk storage subsystem, and a system console (typically an ASR33 teletype). The PDC includes an integral MOS and bipolar PROM programmer and an in-circuit emulation/hardware debug facility. A wide range of PDC cards and system peripherals are available.

System software includes an Operating System, File Management, Debug Software, Text Editor, and 2650 Resident Macro Assembler. These programs provide the user with the tools to perform his software development easily and quickly. These software capabilities, together with the capacity and performance of the floppy disk subsystem, and the in-circuit emulation/hardware debug capability significantly reduces the time and cost of a microcomputer system development project.

The Signetics Microprocessor Prototype Development System introduces a unique new Multiprocessor architecture for prototyping systems. This architecture provides users with the benefits of maximum availability of common (user) memory space and a Master processor/Operating System that is isolated and independent from the user system even in the in-circuit emulation/hardware debug mode.

The Signetics Microprocessor Prototype Development System will have a long life cycle, since it is designed with the capability of supporting other Signetics microprocessors, additional peripherals and expanded software support and hardware debug capabilities.

HARDWARE FEATURES

Modular microprocessor prototype development system to support development, implementation and check out of 2650 microcomputer systems.

Powerful new Multiprocessor architecture provides maximum memory space to user and a protected environment for the Master processor/Operating System at all times.

Signetics 2650 microprocessor — 5 volt only, fully TTL compatible, 2.4us cycle time, easy to learn instruction set — is used for the Master and Slave microprocessors.

Hardware interfaces and software drivers provided for floppy disk storage subsystem, TTY, CRT terminal, paper tape reader, line printer and EIA RS232 terminals.

In-circuit emulation/hardware debug and powerful debug software provides extensive emulation and diagnostic facilities for the user system.

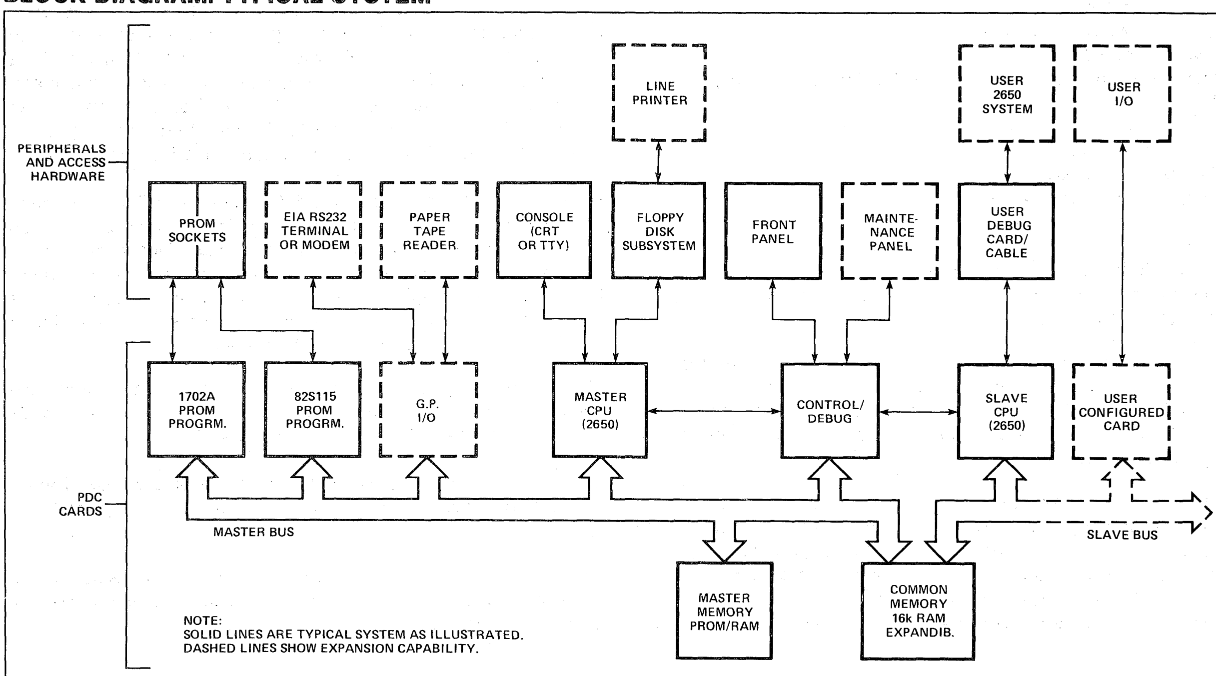
Integral MOS and bipolar PROM programmers.

User/Common memory of 16K bytes, expandable to 64K bytes.

Two universal bus structures with multiprocessor and DMA capabilities.

Eight level maskable priority interrupt system available to the user.

BLOCK DIAGRAM: TYPICAL SYSTEM



SOFTWARE FEATURES

System software provided with the Prototype Development System includes the Signetics Disk Operating System (SDOS), text editor, debug package, 2650 macroassembler, and linkage editor.

The Signetics Disk Operating System (SDOS) provides complete control over operation of all portions of the Prototype Development System. All functions relating to file handling, loading and execution are included, as well as provision for invoking the debug system and PROM programming functions.

The SDOS software has been designed to allow the user to create, edit, and assemble files; obtain object and listing outputs; load and execute programs; and through the debug system, check out programs in a most efficient manner.

SDOS provides a powerful procedure capability which gives the user the capability of creating powerful and customized operating system commands dynamically.

Programs may be read and written in either hexadecimal or SMS format.

The SDOS software provides a flexible input/output system which is organized through logical channels allowing the user to dynamically assign any logical channel to any physical device or file within the system. Thus, system I/O devices may be dynamically assigned using SDOS commands either from the console or from within a user's program.

SDOS assumes a dual CPU environment with one CPU designated as a master and the other as a slave. SDOS is written in 2650 Assembly Language and resides in a dedicated memory consisting of 2K PROM and 4K of RAM running under the master CPU.

SDOS will control a multidrive floppy disk subsystem (up to 8 drives), a line printer, a high speed paper tape reader and an ASR-33 TTY compatible console. Drivers are provided within SDOS for these I/O devices. In addition, the user may write his own driver for other peripheral devices and easily link them into SDOS system.

The Prototype Development System Resident Assembler translates symbolic 2650 assembly language instructions into appropriate machine language code. The Resident Assembler has full macro capability which is a powerful programming tool eliminating the need to rewrite similar sections of code repeatedly.

The Assembler is written in the Signetics Higher Level Language and produces either absolute object code or relocatable modules. The absolute object code produced is in hexadecimal format which may be loaded into the system for direct execution or may be converted by an SDOS command to SMS format for PROM or ROM programming.

The Linkage Editor program accepts relocatable modules produced by either the Macro Assembler or the Signetics Higher Level Language and creates an absolute object load module. This facility allows the modular construction of programs and prevents reassembling an entire program when modifications are made to one small section. True relocatability of object modules is a powerful feature previously found only on larger computer systems.

The Text Editor is a comprehensive software package which allows the user to enter and modify text files. The Text Editor is line oriented and accepts inputs from an input file, performs modifications in a work space and outputs the revised text to an output file.

The Debug System is a software program which will provide the user with run-time program debug capabilities within a hardware environment. It utilizes special hardware features built into the program development system to control the execution of the users program. User programs operating under the debug system will have dynamic program trace, breakpoint capabilities, memory modification capabilities, and status reporting on the memory, program, and internal processor status.

All of the above described software will be supplied in object format on either diskette or paper tape and is provided with each Prototype Development System.

PDC CARDS

MASTER CPU
- System Xtal Clock
- Master 2650
- UART/TTY Interface
- Real Time Clock
- Disk/Paper tape Port

CONTROL/DEBUG
- Debug Logic
- Master/Slave Interaction
- Interrupt Logic
- Front Panel Interface

SLAVE CPU
- Slave 2650
- User Cable Interface

MASTER MEMORY
- 4K-Byte Static NMOS RAM
- 2K-Byte 1702A Erasable PROM

COMMON MEMORY — 4K RAM
- 4K-Byte Static NMOS RAM

COMMON MEMORY — 16K RAM
- 16K-Byte Dynamic NMOS RAM

GENERAL PURPOSE I/O
- EIA Interface
- Four Output Ports
- Four Input Ports
- 8 Interrupt Lines

1702 PROM PROGRAMMER

82S115 PROM PROGRAMMER

USER CONFIGURABLE CARD
- For interfacing directly with users own I/O devices.

PERIPHERALS

FLOPPY DISK SUBSYSTEM
- Expandable to 8 drives

LINE PRINTER (optional)

HIGH SPEED PAPER TAPE READER (optional)

TELETYPE

CRT TERMINAL (optional)

AC POWER REQUIREMENTS

50Hz or 60Hz, 115/230 VAC, 150 watts

COMPATIBLE MEMORY AND INTERFACE PRODUCTS

The following list of memory and interface products are suitable for use with the 2650. These data sheets can be found in the appropriate section of this book.

2102-1	1024-bit Random Access Read/Write Static Memory
2680	4096-bit Read/Write Random Access Dynamic Memory
2606, 2606-1	256x4 Random Access Read/Write Static Memory
2608	1024x8 Static Read-Only Memory
8T26, 8T28	Tri-State Quad Bus Transceivers
8T31	8-bit Bidirectional Input-Output Port
9334	8-bit Addressable Latch
8T95 8T96 8T97 8T98	High Speed Hex Tri-State Buffers High Speed Hex Tri-State Inverters
82S09	576-bit Bipolar RAM(64x9)
82S10, 82S11	1024x1-bit Bipolar RAM-Open Collectors (82S10), Tri-State (82S11)
82S23, 82S123 ..	256-bit Bipolar Programmable ROM (32x8)
82S114	2048-bit Bipolar ROM (256x8 PROM)
82S115	4096-bit Bipolar ROM (512x8 PROM)
82S126, 82S129	1024-bit Bipolar Programmable ROM (256x4 PROM)
8204	2048-bit Bipolar ROM (256x8 ROM)
8205	4096-bit Bipolar ROM (512x8 ROM)
82S100/101	16x48x8 FPLA
1702A	2048-bit Static ROM (Erasable And Electrically Reprogrammable)

INTRODUCTION

The introduction of the Signetics Series 3000 Bipolar Microprocessor Chip Set has brought new levels of high performance to microprocessor applications not previously possible with MOS technology. Combining the Schottky bipolar N3001 Microprogram Control Unit (MCU) and N3002 Central Processing Element (CPE) with industry standard memory and support circuits, microinstruction cycle times of 100 nanoseconds are possible.

In the majority of cases, the choice of a bipolar microprocessor slice, as opposed to an MOS device, is based on speed or flexibility of microprogramming. Starting with these characteristics, the design of the Signetics Series 3000 Microprocessor has been optimized around the following objectives:

- Fast cycle time
- All memory and support chips are industry standard
- Cooler operation
- Lower total system cost

Furthermore, systems built with large-scale integrated circuits are much smaller and require less power than equivalent systems using medium and/or small scale integrated circuits.

The two components of the Series 3000 chip set, when combined with industry standard memory and peripheral circuits, allows the design engineer to construct high-performance processors and/or controllers with a minimum amount of auxillary logic. Features such as the multiple independent address and data buses, tri-state logic, and separate output enable lines eliminate the need for time-multiplexing of buses and associated hardware.

Each Central Processing Element represents a complete 2-bit slice through the data processing section of a computer. Several CPE's may be connected in parallel to form a processor of any desired Word length. The Microprogram Control Unit controls the sequence in which microinstructions are fetched from the microprogram memory (ROM/PROM), with these microinstructions controlling the step-by-step operation of the processor.

Each CPE contains a 2-bit slice of five independent buses. Although they can be used in a variety of ways, typical connections are:

Input M-bus:	Carries data from external memory
Input I-bus:	Carries data from input/output device
Input K-bus:	Used for microprogram mask or literal (constant) value input
Output A-bus:	Connected to CPE Memory Address Register
Output D-bus:	Connected to CPE accumulator.

As the CPE's are paralleled together, all buses, data paths, and registers are correspondingly expanded.

The microfunction input bus (F-bus) controls the internal operation of the CPE, selecting both the operands and the operation to be executed upon them. The arithmetic logic unit (ALU), controlled by the microfunction decoder, is capable of over 40 Boolean and binary operations as outlined in the FUNCTION DESCRIPTION section of the N3002 data sheet. Standard carry look-ahead outputs (X and Y) are generated by the CPE for use with industry standard devices such as the 74S182.

A typical processor configuration is shown in Figure 1. It should be remembered that in working with slice-oriented microprocessors, the final configuration may be varied to enhance speed, reduce component count, or increase data-processing capability. One method of maximizing a processor's performance is called pipelining. To accomplish this, a group of D-type flip-flops or latches (such as the 74174 Hex D-type Flip-Flop) are connected to the microprogram memory outputs (excluding the address control field AC_0 - AC_6) to buffer the current microinstruction and allow the MCU to overlap the fetch of the next instruction with the execution of the current one. The time saved in pipelining operations is the shorter of either the address set-up time to the microprogram memory (ROM/PROM) or the access time of the ROM/PROM. A convenient way of implementing pipelining is to use ROMs with on-board latches, such as the Signetics 82S115.

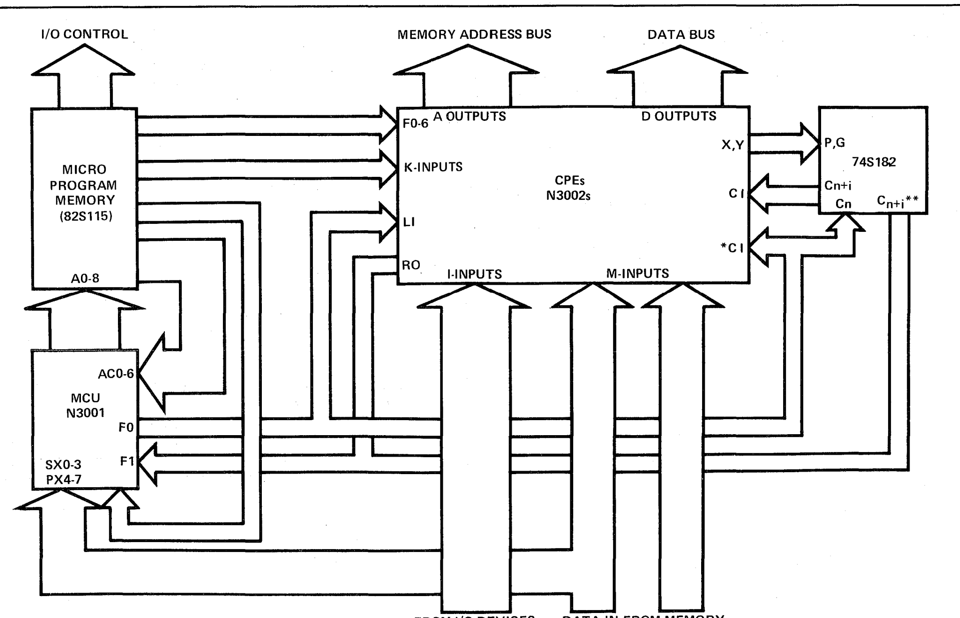


Figure 1: MICROCOMPUTER BLOCK DIAGRAM

MICROPROCESSOR

Figure 2 shows a typical microinstruction format using the 82S114 PROMs contained in the Signetics 3000 Microprocessor Designer's Evaluation Kit. Although this particular example is for a 48-bit word (6 PROMs), the allocation of bits for the mask (K-bus) and optional processor functions depends on the specific application of the system and the trade offs which the designer wishes to make.

In using the K-bus, it should be kept in mind that the K inputs are always ANDed with the B-multiplexer outputs into the ALU. Bit masking, frequently done in computer control systems, can be performed with the mask supplied to the K-bus directly from the microinstruction.

By placing the K-bus in either the all-one or all-zero condition (done with a single control bit in the microinstruction), the accumulator will either be selected or de-selected, respectively, in a given operation. This feature nearly doubles the amount of microfunctions in the CPE. A description of these various microfunctions can be found in the N3002 data sheet under the heading "FUNCTION DESCRIPTION" by referring to the K-bus conditions of all-ones (11) and all-zeros (00).

The MCU controls the sequence in which microinstructions are fetched from the microprogram memory (ROM/PROM). In its classical form, the MCU would use a next-address field in each microinstruction. However, the N3001 uses a modified classical approach in which the microinstruction field specifies conditional tests on the MCU bus inputs and registers. The next-address logic of the MCU also makes extensive use of a row/column addressing scheme, whereby the next address is defined by a 5-bit row address and 4-bit column address. Thus, from a particular address location, it is possible to jump unconditionally to any other location within that row or column, or conditionally to other specified locations in one operation. Using this method, the processor functions can be executed in parallel with program branches.

As an example of this flexibility, let us assume a disk controller is being designed. As part of the sequence logic, three bits of the disk drive status word must be tested and all three must be true in order to proceed with the particular sequencing operation. In any sequencing operation using a status word for conditional branch information, there are innumerable combinations of bits which must be tested throughout the sequencing operation. Using discrete logic techniques, this would involve several levels of gating.

However, the entire operation can be done in two microinstructions. First, the mask (K-bus) field in the microinstruction format is encoded with a one for each corresponding status bit to be tested and a zero for each bit to be discarded. The status word is input via the I-bus and ANDed with the K-bus mask using the CPE microfunction operation from F-Group 2, R-Group III. Assuming we are using low-true logic (TRUE = 0 Volts), we now test the result, which is located in the accumulator AC, for all zeros using the CPE microfunction operation from F-Group 5, R-Group III. Depending on the zero/non-zero status of AC, a one or zero will be loaded into the carryout CO bit. This bit can now be used as a condition for the next address jump calculation within the N3001 MCU. If the AC was zero (status word was true), we will jump to the next address within our controller sequence. If the AC was non-zero (status word not true), then a jump would be made back to the beginning of this two-microinstruction loop and the test sequence repeated until the status word (all three bits) is true.

Figure 3 shows a typical timing diagram for a system operating in the non-pipelined mode. Keep in mind that the maximum clock rate is dependent upon the total of propagation delay times plus required set-up times. It is at the designer's discretion to resolve the speed versus complexity tradeoffs.

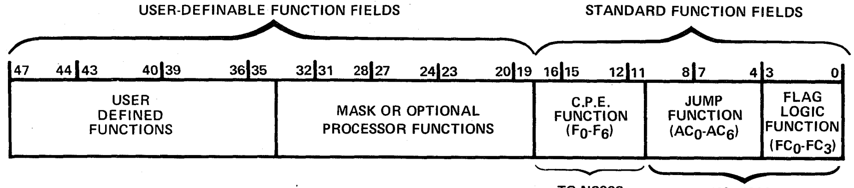


Figure 2: TYPICAL MICROINSTRUCTION FORMAT.
Note: The mask field need only be used during masking operations. At other times, it is entirely user definable.

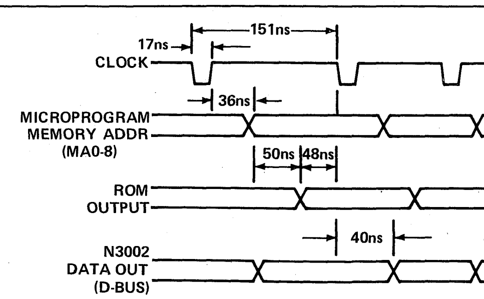


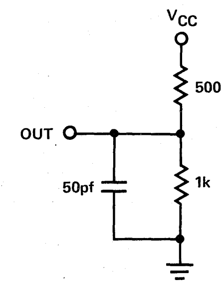
Figure 3: SYSTEM TIMING – NON-PIPELINED CONFIGURATION

ABSOLUTE MAXIMUM RATIONS*

Temperature Under Bias	0°C to +70°C
Storage Temperature	−60°C to +160°C
All Output and Supply Voltages	−0.5V to +7V
All Input Voltages	−1.0V to +5.5V
Output Currents	100mA

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may effect device reliability.

PARAMETER MEASUREMENT INFORMATION



NOTE: ALL RESISTORS VALUES ARE TYPICAL AND IN OHMS.

TEST CONDITIONS

Input pulse amplitude of 2.5 volts.

Input rise and fall times of 5ns between 1 volt and 2 volts.

Output load of 10mA and 50pF

Speed measurements are taken at the 1.5 volt level.

3001/3002 ELECTRICAL CHARACTERISTICS (T_A=0°C to 70°C)

PARAMETER	INPUT VOLTAGE									OUTPUT VOLTAGE					
	V_{IL} (V) LOW LEVEL			V_{IH} (V) HIGH LEVEL			V_C (V) INPUT CLAMP VOLTAGE			V_{OL} (V) LOW LEVEL			V_{OH} (V) HIGH LEVEL		
TEST CONDITIONS	V_{CC}=5.0V			V_{CC}=5.0V			V_{CC}=4.75 I_C=-5mA			V_{CC}=4.75V I_{OL}=10mA			V_{CC}=4.75V I_{OH}=-1mA		
DEVICE	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
N3001			0.8	2.0				-0.8	-1.0		0.35	0.45	MA0-MA8, ISE, FO	2.4	3.0
N3002			0.8	2.0				-0.8	-1.0	Except X & Y I_{OL}=16mA X and Y	0.3 0.35	0.45 0.50	2.4	3.0	

PARAMETER	INPUT CURRENT						OUTPUT CURRENT						POWER SUPPLY CURRENT		
	I_F (mA) LOAD			I_R (µA) LEAKAGE			I_{OS} (mA) SHORT CIRCUIT			I_O(Off)(µA) OFF-STATE			I_{CC} (mA) POWER SUPPLY CURRENT		
TEST CONDITIONS	V_{CC}=5.25V V_F=0.45V			V_{CC}=5.25V V_R=5.25V			V_{CC}=5.0V			V_{CC}=5.25V			V_{CC}=5.25V[2]		
DEVICE	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
N3001	CLK Input EN Input All Other Inputs	-0.075 -0.05 -0.025	-0.75 -0.50 -0.25	CLK EN Input All Other Inputs		120 80 40	MA0-MA8, ISE, FO -15	-28	-60	PR0-PR2, MA0-MA2,FO V_O=0.45V V_O=5.25V MA0-MA8,FO		-100 -100		170	240
N3002	F0-F6,CLK K0,K1,EA,ED I0,I,M0, M1,LI CI	-0.05 -0.85 -2.3	-0.25 -1.5 -4.0	F0-F6,CLK K0,K1,EA,ED I0,I1,M0, M1,LI CI		40 60 180	-15	-25	-60	 A0,A1,D0,D1 Only		-100 100		145	190

NOTES:

3001

1. Typical values are for T_A=25°C and 5.0 supply voltage.
2. EN input grounded, all other inputs and outputs open.

3002

1. Typical values are for T_A – 25°C and typical supply voltage.
2. CLK input grounded, other inputs open.

DESCRIPTION

The N3001 MCU is one element of a bipolar microcomputer set. When used with the 3002, 74S182, ROM or PROM memory, a powerful microprogrammed computer can be implemented.

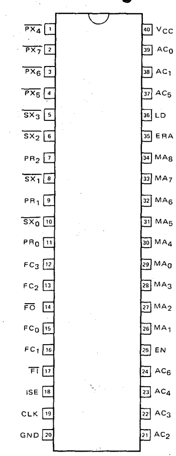
The 3001 MCU controls the fetch sequence of microinstructions from the microprogram memory. Functions performed by the 3001 include:

- Maintenance of microprogram address register
- Selection of next microinstruction address
- Decoding and testing of data supplied via several input busses
- Saving and testing of carry output data from the central processing (CP) array
- Control of carry/shift input data to the CP array
- Control of microprogram interrupts

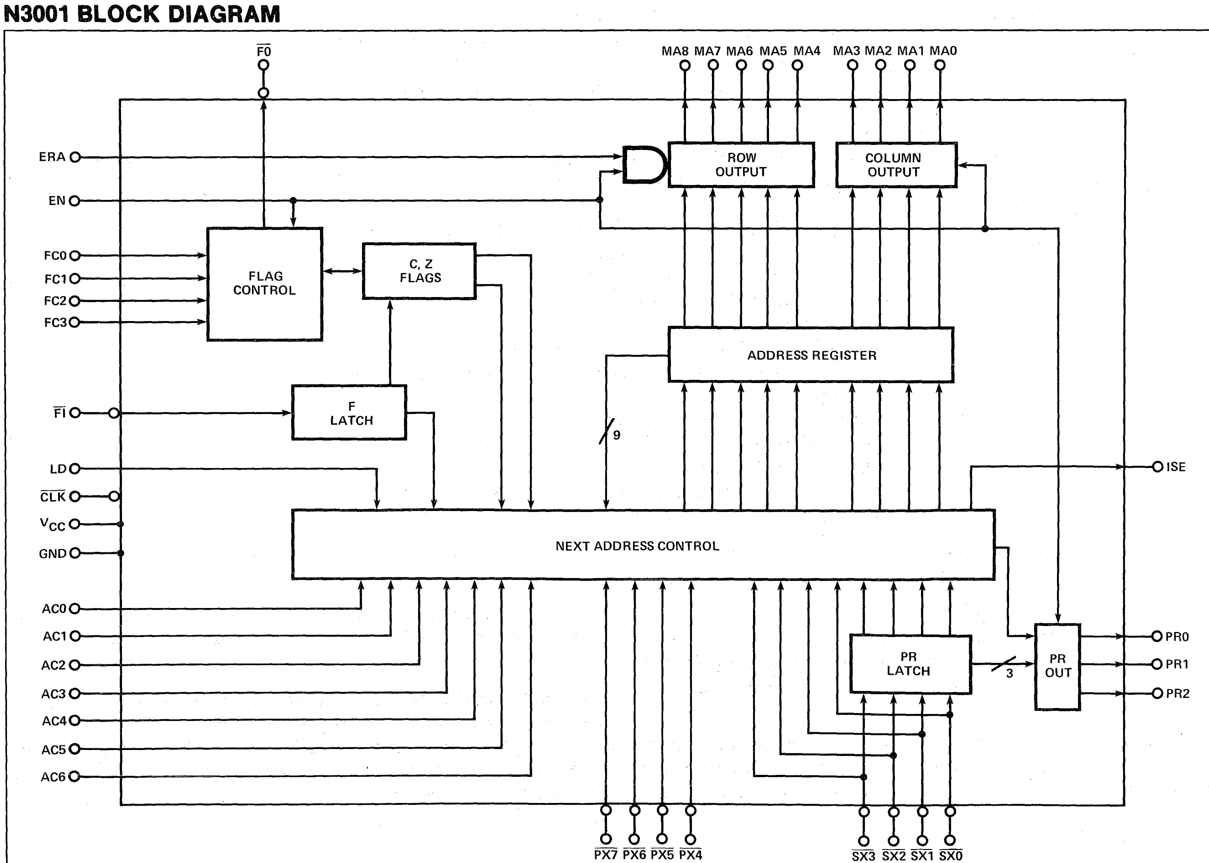
FEATURES

- **Schottky TTL process**
- **45ns cycle time (typ.)**
- **Direct addressing of standard bipolar PROM or ROM**
- **512 microinstruction addressability**
- **Advanced organization:**
    - **9-bit microprogram address register and bus organized to address memory by row and column**
    - **4-bit program latch**
    - **2 flag registers**
- **11 address control functions:**
    - **3 jump and test latch function**
    - **16 way jump and test instruction**
- **8 flag control functions:**
    - **4 flag input functions**
    - **4 flag output functions**

PIN CONFIGURATION



N3001 BLOCK DIAGRAM



PIN DESCRIPTION

PIN	SYMBOL	NAME AND FUNCTION	TYPE
1-4	$\overline{PX_4}$—$\overline{PX_7}$	Primary Instruction Bus Inputs Data on the primary instruction bus is tested by the JPX function to determine the next microprogram address.	Active LOW
5,6,8,10	$\overline{SX_0}$—$\overline{SX_3}$	Secondary Instruction Bus Inputs Data on the secondary instruction bus is synchronously loaded into the PR-latch while the data on the PX-bus is being tested (JPX). During a subsequent cycle, the contents of the PR-latch may be tested by the JPR, JLL, or JRL functions to determine the next microprogram address.	Active LOW
7,9,11	PR_0—PR_2	PR-Latch Outputs The PR-latch outputs (SX_0-SX_2) are synchronously enabled by the JCE function. They can be used to modify microinstructions at the outputs of the microprogram memory or to provide additional control lines.	Open Collector
12,13 15,16	FC_0—FC_3	Flag Logic Control Inputs The flat logic control inputs are used to cross-switch the flags (C and Z) with the flag logic input (FI) and the flag logic output (FO).	Active HIGH
14	$\overline{FO}$	Flag Logic Output The outputs of the flags (C and Z) are multiplexed internally to form the common flag logic output. The output may also be forced to a logical 0 or logical 1.	Active LOW Three-state
17	$\overline{FI}$	Flag Logic Input The flag logic input is demultiplexed internally and applied to the inputs of the flags (C and Z). Note: The flag input data is saved in the F-latch when the clock input (CLK) is low.	Active LOW
18	ISE	Interrupt Strobe Enable Output The interrupt strobe enable output goes to logical 1 when one of the JZR functions are selected (see Functional Description). It can be used to provide the strobe signal required by interrupt circuits.	Active HIGH
19	$\overline{CLK}$	Clock Input	
20	GND	Ground	
21—24 37—39	AC_0—AC_6	Next Address Control Function Inputs All jump functions are selected by these control lines.	Active HIGH
25	EN	Enable Input When in the HIGH state, the enable input enables the microprogram address, PR-latch and flag outputs.	
26—29	MA_0—MA_3	Microprogram Column Address Outputs	Three-state
30—34	MA_4—MA_8	Microprogram Row Address Outputs	Three-state
35	ERA	Enable Row Address Input When in the LOW state, the enable row address input independently disables the microprogram row address outputs. It can be used to facilitate the implementation of priority interrupt systems.	Active HIGH
36	LD	Microprogram Address Load Input When the active HIGH state, the microprogram address load input inhibits all jump functions and synchronously loads the date on the instructions busses into the microprogram register. However, it does not inhibit the operation of the PR-latch or the generation of the interrupt strobe enable.	Active HIGH
40	V_{CC}	+5 Volt Supply	

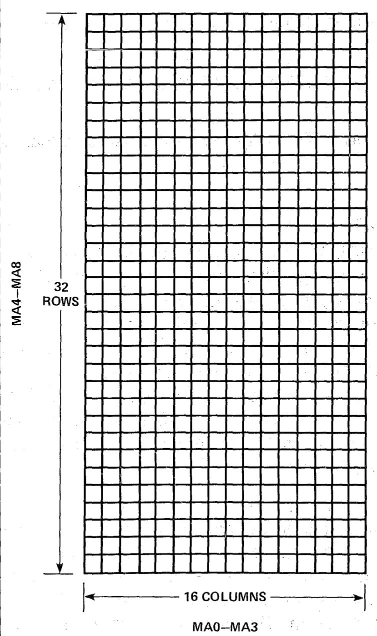
THEORY OF OPERATION

The MCU controls the sequence of microinstructions in the microprogram memory. The MCU simultaneously controls 2 flip-flops (C, Z) which are interactive with the carry-in and carry-out logic of an array of CPEs.

The functional control of the MCU provides both unconditional jumps to new memory locations and jumps which are dependent on the state of MCU flags or the state of the "PR" latch. Each instruction has a "jump set" associated with it. This "jump set" is the total group of memory locations which can be addressed by that instruction.

The MCU utilizes a two-dimensional addressing scheme in the microprogram memory. Microprogram memory is organized as 32 rows and 16 columns for a total of 512 words. Word length is variable according to application. Address is accomplished by a 9-bit address organized as a 5-bit row and 4-bit column address.

ADDRESSING ORGANIZATION



FUNCTIONAL DESCRIPTION

The following is a description of each of the eleven address control functions. The symbols shown below are used to specify row and column addresses.

SYMBOL	MEANING
row_n	5-bit next row address where n is the decimal row address.
col_n	4-bit next column address where n is the decimal column address.

UNCONDITIONAL ADDRESS CONTROL (JUMP) FUNCTIONS

The jump functions use the current microprogram address (i.e., the contents of the microprogram address register prior to the rising edge of the clock) and several bits from the address control inputs (AC0-AC6) to generate the next microprogram address.

MNEMONIC	FUNCTION DESCRIPTION
JCC	Jump in current column. AC_0—AC_4 are used to select 1 of 32 row addresses in the current column, specified by MA_0—MA_3, as the next address.
JZR	Jump to zero row. AC_0—AC_3 are used to select 1 of 16 column addresses in row_0, as the next address.
JCR	Jump in current row. AC_0—AC_3 are used to select 1 of 16 addresses in the current row, specified by MA_4—MA_8, as the next address.
JCE	Jump in current column/row group and enable PR-latch outputs. AC_0—AC_2 are used to select 1 of 8 row addresses in the current row group, specified by MA_7—MA_8, as the next row address. The current column is specified by MA_0—MA_3. The PR-latch outputs are asynchronously enabled.

FLAG CONDITIONAL ADDRESS CONTROL (JUMP/TEST) FUNCTIONS

The jump/test flag functions use the current microprogram address, the contents of the selected flag or latch, and several bits from the address control function to generate the next microprogram address.

MNEMONIC	FUNCTION DESCRIPTION
JFL	Jump/test F-latch. AC_0—AC_3 are used to select 1 of 16 row addresses in the current row group, specified by MA_8, as the next row address. If the current column group, specified by MA_3, is col_0—col_7, the F-latch is used to select col_2 or col_3 as the next column address. If MA_3 specifies column group col_8—col_{15}, the F-latch is used to select col_{10} or col_{11} as the next column address.
JCF	Jump/test C-flag. AC_0—AC_2 are used to select 1 of 8 row addresses in the current row group, specified by MA_7 and MA_8, as the next row address. If the current column group specified by MA_3 is col_0—col_7, the C-flag is used to select col_2 or col_3 as the next column address. If MA_3 specifies column group col_8—col_{15}, the C-flag is used to select col_{10} or col_{11} as the next column address.
JZF	Jump/test Z-flag. Identical to the JCF function described above, except that the Z-flag, rather than the C-flag, is used to select the next column address.

PX-BUS AND PR-LATCH CONDITIIONAL ADDRESS CONTROL (JUMP/TEST) FUNCTIONS

The PX-bus jump/test function uses the data on the primary instruction bus (PX_4—PX_7), the current microprogram address, and several selection bits from the address control function to generate the next microprogram address. The PR-latch jump/test functions use the data held in the PR-latch, the current microprogram address, and several selection bits from the address control function to generate the next microprogram address.

MNEMONIC	FUNCTION DESCRIPTION
JPR	Jump/test PR-latch. AC_0—AC_2 are used to select 1 of 8 row addresses in the current row group, specified by MA_7 and MA_8, as the next row address. The four PR-latch bits are used to select 1 of 16 possible column addresses as the next column address.
JLL	Jump/test leftmost PR-latch bits. AC_0—AC_2 are used to select 1 of 8 row addresses in the current row group, specified by MA_7 and MA_8, as the next row address. PR_2 and PR_3 are used to select 1 of 4 column addresses in col_4 through col_7 as the next column address.

JRL	Jump/test rightmost PR-latch bits. AC_0 and AC_1 are used to select 1 of 4 high-order row addresses in the current row group, specified by MA_7 and MA_8, as the next row address. PR_0 and PR_1 are used to select 1 of 4 possible column addresses in col_{12} through col_{15} as the next column address.
JPX	Jump/test PX-bus and load PR-latch. AC_0 and AC_1 are used to select 1 of 4 row addresses in the current row group, specified by MA_6—MA_8, as the next row address. PX_4—PX_7 are used to select 1 of 16 possible column addresses as the next column address. SX_0—SX_3 data is locked in the PR-latch at the rising edge of the clock.

FLAG CONTROL FUNCTIONS

The flag control functions of the MCU are selected by the four input lines designated FC_0—FC_3. Function code formats are given in "Flag Control Function summary".

The following is a detailed description of each of the eight flag control functions.

FLAG INPUT CONTROL FUNCTIONS

The flag input control functions select which flag or flags will be set to the current value of the flag input (FI) line.

Data on FI is stored in the F-latch when the clock is low. The content of the F-latch is loaded into the C and/or Z flag on the rising edge of the clock.

MNEMONIC	FUNCTION DESCRIPTION
SCZ	Set C-flag and Z-flag to FI. The C-flag and the Z-flag are both set to the value of FI.
STZ	Set Z-flag to FI. The Z-flag is set to the value of FI. The C-flag is unaffected.
STC	Set C-flag to FI. The C-flag is set to the value of FI. The Z-flag is unaffected.
HCZ	Hold C-flag and Z-flag. The values in the C-flag and Z-flag are unaffected.

FLAG OUTPUT CONTROL FUNCTIONS

The flag output control functions select the value to which the flag output (FO) line will be forced.

MNEMONIC	FUNCTION DESCRIPTION
FFO	Force FO to O. FO is forced to the value of logical O.
FFC	Force FO to C. FO is forced to the value of the C-flag.
FFZ	Force FO to Z. FO is forced to the value of the Z-flag.
FF1	Force FO to 1. FO is forced to the value of logical 1.

STROBE FUNCTIONS

The load function of the MCU is controlled by the input line designated LD. If the LD line is active HIGH at the rising edge of the clock, the date on the primary and secondary instruction busses, PX_4—PX_7 and SX_0—SX_3, is loaded into the microprogram address register. PX_4—PX_7 are loaded into MA_0—MA_3 and SX_0—SX_3 are loaded into MA_4—MA_7. The high-order bit of the microprogram address register MA_8 is set to a logical 0. The bits from the primary instruction bus select 1 of 16 possible column addresses. Likewise, the bits from the secondary instruction bus select 1 of the first 16 row addresses.

The MCU generates an interrupt strobe enable on the output line designated ISE. The line is placed in the active high state whenever a JZR to col_{15} is selected as the address control function. Generally, the start of a macroinstruction fetch sequence is situated at row_0 and col_{15} so the interrupt control may be enabled at the beginning of the fetch/execute cycle. The interrupt control responds to the interrupt by pulling the enable row address (ERA) input line low to override the selected next row address from the MCU. Then by gating an alternative next row address on to the row address lines of the microprogram memory, the microprogram may be forced to enter an interrupt handling routine. The alternative row address placed on the microprogram memory address lines does not alter the contents of the microprogram address register. Therefore, subsequent jump functions will utilize the row address in the register, and not the alternative row address, to determine the next microprogram address.

Note, the load function always overrides the address control function on AC_0—AC_6. It does not, however, override the latch enable or load sub-functions of the JCE or JPX instruction, respectively. In addition, it does not inhibit the interrupt strobe enable or any of the flag control functions.

ADDRESS CONTROL FUNCTION SUMMARY

		FUNCTION							NEXT ROW					NEXT COL			
MNEMONIC	DESCRIPTION	AC_6	5	4	3	2	1	0	MA_8	7	6	5	4	MA_3	2	1	0
JCC	Jump in current column	0	0	d_4	d_3	d_2	d_1	d_0	d_4	d_3	d_2	d_1	d_0	m_3	m_2	m_1	m_0
JZR	Jump to zero row	0	1	0	d_3	d_2	d_1	d_0	0	0	0	0	0	d_3	d_2	d_1	d_0
JCR	Jump in current row	0	1	1	d_3	d_2	d_1	d_0	m_8	m_7	m_6	m_5	m_4	d_3	d_2	d_1	d_0
JCE	Jump in column/enable	1	1	1	0	d_2	d_1	d_0	m_8	m_7	d_2	d_1	d_0	m_3	m_2	m_1	m_0
JFL	Jump/test F-latch	1	0	0	d_3	d_2	d_1	d_0	m_8	d_3	d_2	d_1	d_0	m_3	0	1	f
JCF	Jump/test C-flag	1	0	1	0	d_2	d_1	d_0	m_8	m_7	d_2	d_1	d_0	m_3	0	1	c
JZF	Jump/test Z-flag	1	0	1	1	d_2	d_1	d_0	m_8	m_7	d_2	d_1	d_0	m_3	0	1	z
JPR	Jump/test PR-latch	1	1	0	0	d_2	d_1	d_0	m_8	m_7	d_2	d_1	d_0	p_3	p_2	p_1	p_0
JLL	Jump/test left PR bits	1	1	0	1	d_2	d_1	d_0	m_8	m_7	d_2	d_1	d_0	0	1	p_3	p_2
JRL	Jump/test right PR bits	1	1	1	1	1	d_1	d_0	m_8	m_7	1	d_1	d_0	1	1	p_1	p_0
JPX	Jump/test PX-bus	1	1	1	1	0	d_1	d_0	m_8	m_7	m_6	d_1	d_0	x_7	x_6	x_5	x_4

NOTE:

d_n = Data on address control line n

m_n = Data in microprogram address register bit n

p_n = Data in PR-latch bit n

x_n = Data on PX-bus line n (active LOW)

f,c,z = Contents of F-latch, C-flag, or Z-flag, respectively

FLAG CONTROL FUNCTION SUMMARY

TYPE	MNEMONIC	DESCRIPTION	FC_1	0
	SCZ	Set C-flag and Z-flag to f	0	0
Flag	STZ	Set Z-flag to f	0	1
Input	STC	Set C-flag to f	1	0
	HCZ	Hold C-flag and Z-flag	1	1

TYPE	MNEMONIC	DESCRIPTION	FC_3	2
	FFO	Force FO to 0	0	0
Flag	FFC	Force FO to C-flag	0	1
Output	FFZ	Force FO to Z-flag	1	0
	FF1	Force FO to 1	1	1

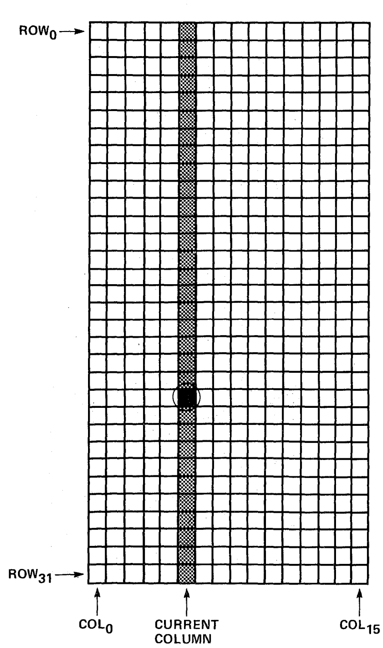
LOAD FUNCTION	NEXT ROW					NEXT COL			
LD	MA_8	7	6	5	4	MA_3	2	1	0
0	See Address Control Function Summary								
1	0	X_3	X_2	X_2	X_0	X_7	X_6	X_5	X_4

NOTE:
f = Contents of the F-latch
X_n = Data on PX- or SX-bus line n (active LOW)

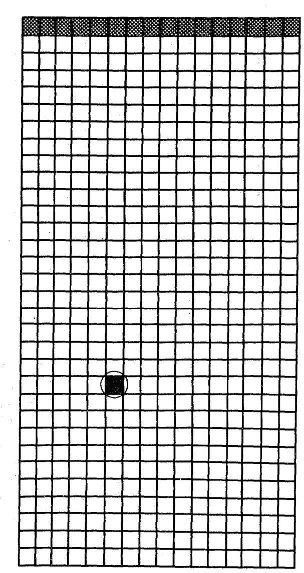
JUMP SET DIAGRAMS

The following ten diagrams illustrate the jump set for each of the eleven jump and jump/test functions of the MCU. Location 341 indicated by the circled square, represents one current row (row_{21}) and current column (col_5) address. The dark boxes indicate the microprogram locations that may be selected by the particular function as the next address.

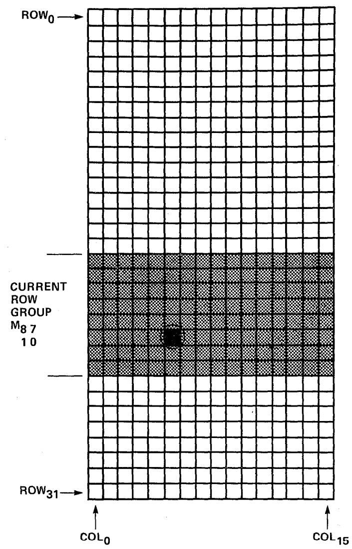
JCC
JUMP IN CURRENT COLUMN



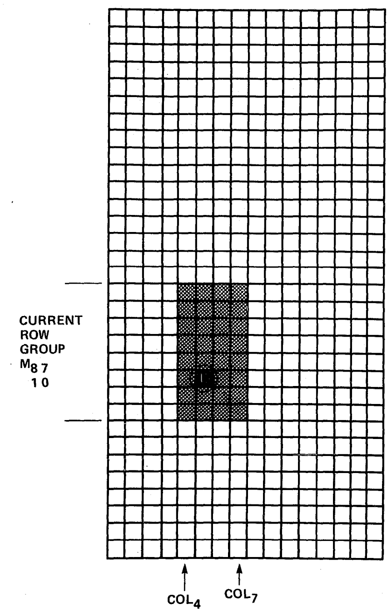
JZR
JUMP TO ZERO ROW



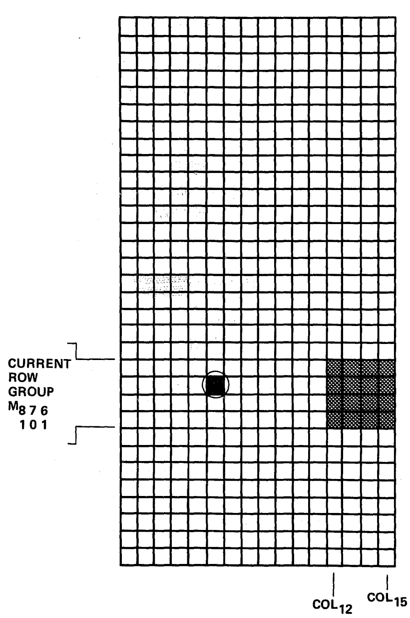
JPR
JUMP/TEST PR-LATCH



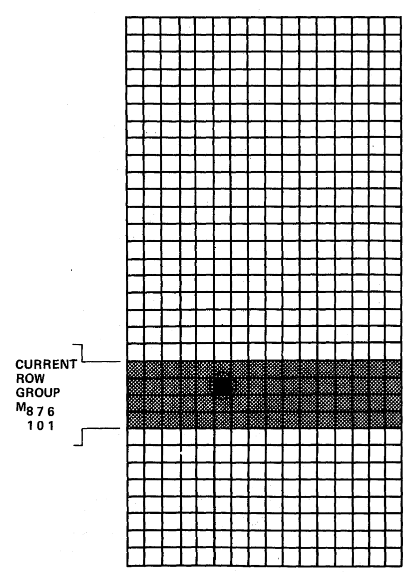
JLL
JUMP/TEST LEFT LATCH



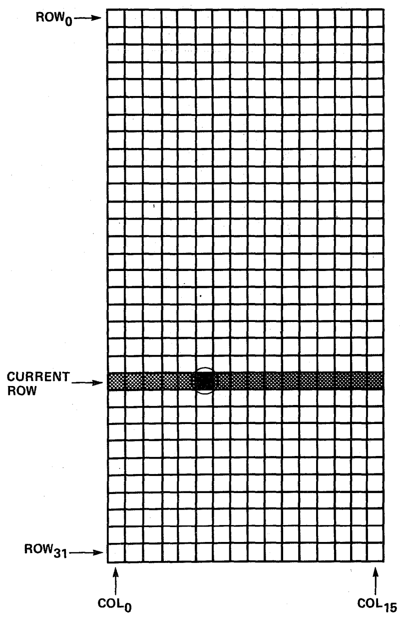
JRL
JUMP/TEST RIGHT LATCH



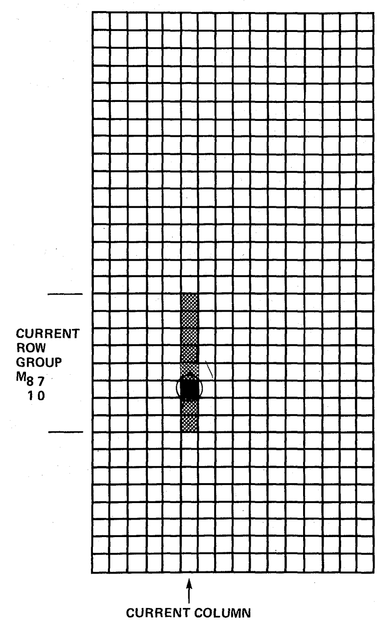
JPX
JUMP/TEST PX-BUS



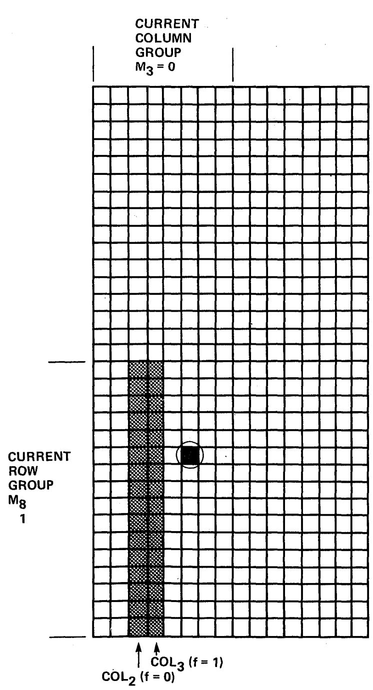
JCR
JUMP IN CURRENT ROW



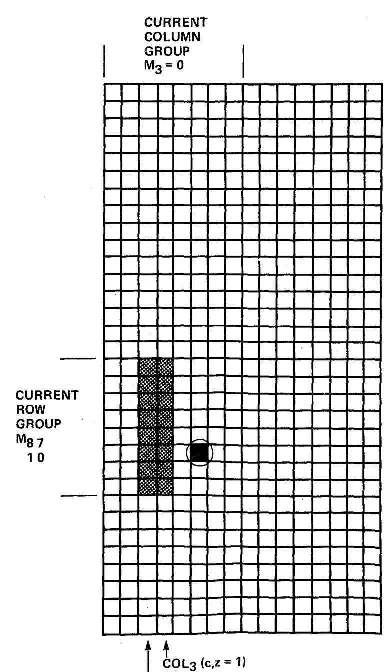
JCE
JUMP COLUMN/ENABLE



JFL
JUMP/TEST F-LATCH



JCF, JZF
JUMP/TEST C-FLAG
JUMP/TEST Z-FLAG

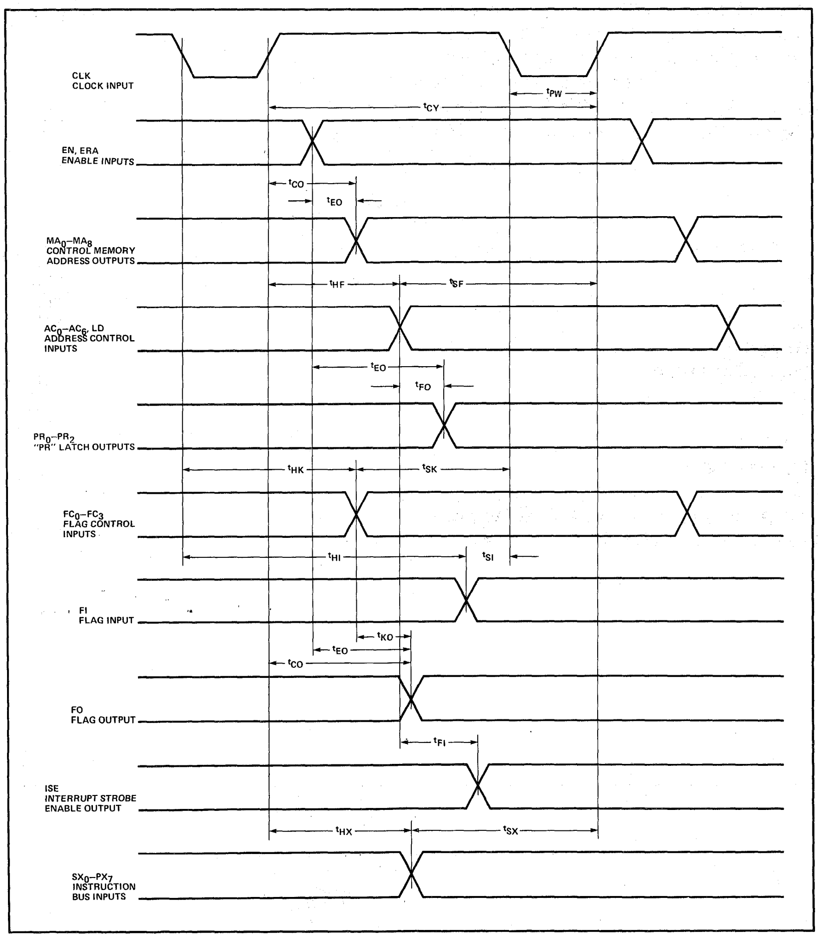


AC ELECTRICAL CHARACTERISTICS T_A=0°C to 70°C, V_{CC}=5.0V ± 5%

	PARAMETER	LIMITS MIN	TYP[1]	MAX	UNIT
t_{CY}	Cycle Time	60	45		ns
t_{WP}	Clock Pulse Width	17	10		ns
	Control and Data Input Set-Up Times:				
t_{SF}	LD, AC_0—AC_6 (Set to "1"/"0")	20	3/14		ns
t_{SK}	FC_0, FC_1	7	5		ns
t_{SX}	PX_4—PX_7 (Set to "1"/"0")	28	4/13		ns
t_{SI}	FI (Set to "1"/"0")	12	-6/0		ns
t_{SX}	SX_0 - SX_3	15	15		ns
	Control and Data Input Hold Times:				
t_{HF}	LD, AC_0—AC_6 (Hold to "1"/"0")	4	-3/-14		ns
t_{HK}	FC_0, FC_1	4	-5		ns
t_{HX}	PX_4—PX_7 (Hold to "1"/"0")	0	-4/-13		ns
t_{HI}	FI (Hold to "1"/"0")	16	6.5/0		ns
t_{NX}	SX_0-SX_3	0	-5		ns
t_{CO}	Propagation Delay from Clock Input (CLK) to Outputs (MA_0—MA_8, FO) (t_{PHL}/t_{PLH})		17/24	36	ns
t_{KO}	Propagation Delay from Control Inputs FC_2 and FC_3 to Flag Out (FO)		13	24	ns
t_{FO}	Propagation Delay from Control Inputs AC_0—AC_6 to Latch Outputs (PR_0—PR_2)		21	32	ns
t_{EO}	Propagation Delay from Enable Inputs EN and ERA to Outputs (MA_0—MA_8, FO, PR_0—PR_2)		17	26	ns
t_{FI}	Propagation Delay from Control Inputs AC_0—AC_6 to Interrupt Strobe Enable Output (ISE)		20	32	ns

NOTE:
1. Typical values are for T_A = 25°C and 5.0 supply voltage.

VOLTAGE WAVEFORMS



MICROPROCESSOR

BIPOLAR MICROPROCESSOR

DESCRIPTION

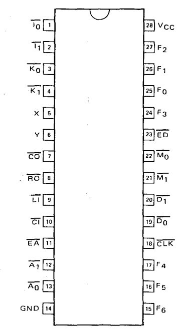
The N3002 Central Processing Element (CPE) is one part of a bipolar microcomputer set. The N3002 is organized as a 2-bit slice and performs the logical and arithmetic functions required by microinstructions. A system with any number of bits in a data word can be implemented by using multiple N3002s, the N3001 microcomputer control unit, the N74S182 carry look-ahead unit and ROM or PROM memory.

FEATURES

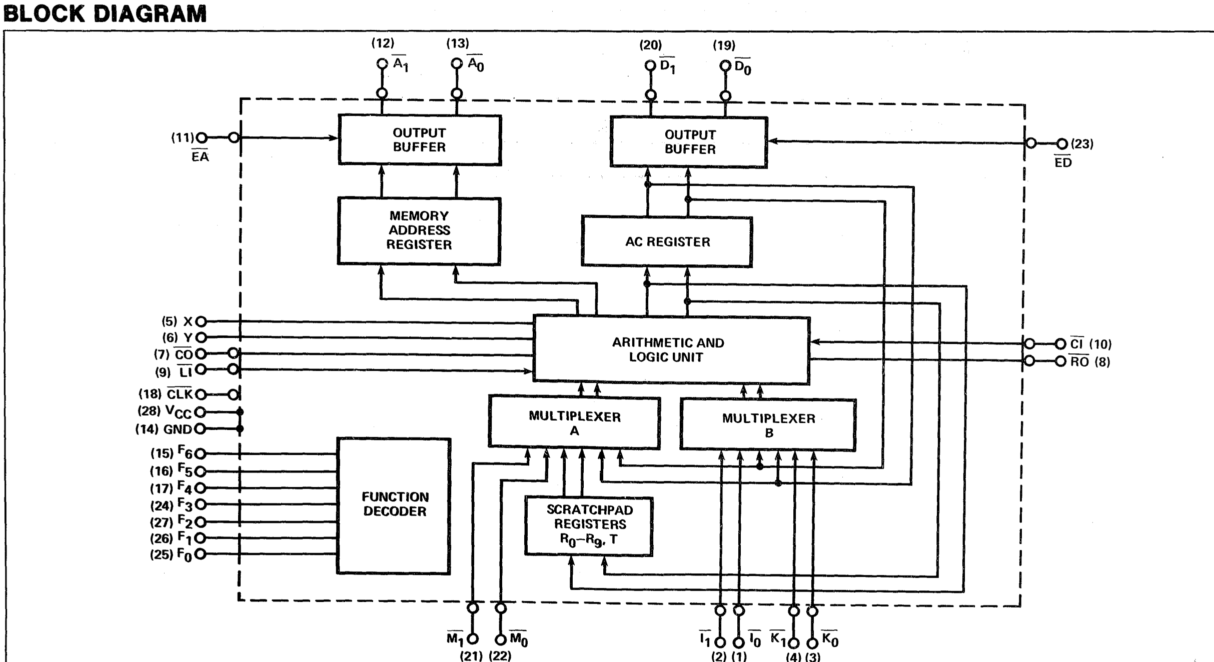
- **45ns cycle time (TYP.)**
- **Easy expansion to multiple of 2 bits**
- **11 general purpose registers**
- **Full function accumulator**
- **Useful functions include:**
  - **2's complement arithmetic**
  - **Logical and, or, not, exclusive-nor**
  - **Increment, decrement**
  - **Shift left/shift right**
  - **Bit testing and zero detection**
  - **Carry look-ahead generation**
  - **Masking via K-bus**
  - **Conditioned clocking allowing non-destructive testing of data in accumulator and scratchpad**
- **3 input busses**
- **2 output busses**
- **Control bus**

PIN CONFIGURATION

XL,I PACKAGE



BLOCK DIAGRAM



PIN DESCRIPTION

PIN	SYMBOL	NAME AND FUNCTION	TYPE
1,2	$\overline{I_0}$—$\overline{I_1}$	External Bus Inputs The external bus inputs provide a separate input port for external input devices.	Active LOW
3,4	$\overline{K_0}$—$\overline{K_1}$	Mask Bus Inputs The mask bus inputs provide a separate input port from the microprogram memory, to allow mask or constant entry.	Active LOW
5,6	X, Y	Standard Carry Look-Ahead Cascade Outputs The cascade outputs allow high speed arithmetic operations to be performed when they are used in conjunction with the 74S182 Look-Ahead Carry Generator.	Active HIGH
7	$\overline{CO}$	Ripple Carry Out The ripple carry output is only disabled during shift right operations.	Active LOW Three-state
8	$\overline{RO}$	Shift Right Output The shift right output is only enabled during shift right operations.	Active LOW Three-state
9	$\overline{LI}$	Shift Right Input	Active LOW
10	$\overline{CI}$	Carry Input	Active LOW
11	$\overline{EA}$	Memory Address Enable Input When in the LOW state, the memory address enable input enables the memory address outputs (A_0—A_1).	Active LOW
12—13	$\overline{A_0}$—$\overline{A_1}$	Memory Address Bus Outputs The memory address bus outputs are the buffered outputs of the memory address register (MAR).	Active LOW Three-state
14	GND	Ground	
15—17, 24—27	F_0—F_6	Micro-Function Bus Inputs The micro-function bus inputs control ALU function and register selection.	Active-HIGH
18	$\overline{CLK}$	Clock Input	
19—20	$\overline{D_0}$—$\overline{D_1}$	Memory Data Bus Outputs The memory data bus outputs are the buffered outputs of the full function accumulator register (AC).	Active LOW Three-state
21—22	$\overline{M_0}$—$\overline{M_1}$	Memory Data Bus Inputs The memory data bus inputs provide a separate input port for memory data.	Active LOW
23	$\overline{ED}$	Memory Data Enable Input When in the LOW state, the memory data enable input enables the memory data outputs (D_0—D_1).	Active LOW
28	V_{CC}	+5 Volt Supply	

SYSTEM DESCRIPTION

1. MICROFUNCTION DECODER AND K-BUS

Basic microfunctions are controlled by a 7-bit bus (F_0—F_6) which is organized into two groups. The higher 3 bits (F_4—F_6) are designated as F-Group and the lower 4 bits (F_0—F_3) are designated as the R-Group. The F-Group specifies the type of operation to be performed and the R-Group specifies the registers involved.

The F-Bus instructs the microfunction decoder to:
- Select ALU functions to be performed
- Generate scratchpad register address
- Control A and B multiplexer

The resulting microfunction action can be:
- Data transfer
- Shift operations
- Increment and decrement
- Initialize stack
- Test for zero conditions
- 2's complement addition and subtraction
- Bit masking
- Maintain program counter

2. A AND B MULTIPLEXERS

A and B multiplexers select the proper two operands to the ALU.

A multiplexer selects inputs from one of the following:
- M-bus (data from main memory)
- Scratchpad registers
- Accumulator

B multiplexer selects inputs from one of the following:
- I-bus (data from external I/O devices)
- Accumulator
- K-bus (literal or masking information from micro-program memory)

3. SCRATCHPAD REGISTERS

- Contains 11 registers (R_0—R_9, T)
- Scratchpad register outputs are multiplexed to the ALU via the A multiplexer
- Used to store intermediate results from arithmetic/logic operations
- Can be used as program counter

4. ARITHMETIC/LOGIC UNIT (ALU)

The ALU performs the arithmetic and logic operations of the CPE.

Arithmetic operations are:
- 2's complement addition
- Incrementing

- Decrementing
- Shift left
- Shift right

Logical operations are:
- Transfer
- AND
- Inclusive-OR
- Exclusive-NOR
- Logic complement

ALU operation results are then stored in the accumulator and/or scratchpad registers. For easy expansion to larger arrays, carry look-ahead outputs (X and Y) and cascading shift inputs (LI, RO) are provided.

5. ACCUMULATOR
- Stores results from ALU operations
- The output of accumulator is multiplexed into ALU via the A and B multiplexer as one of the operands

6. INPUT BUSES

M-bus: Data bus from main memory
- Accepts 2 bits of data from main memory into CPE
- Is multiplexed into the ALU via the A multiplexer

I-bus: Data bus from input/output devices
- Accepts 2 bits of data from external input/output devices into CPE
- Is multiplexed into the ALU via the B multiplexer

K-bus: A special feature of the N3002 CPE
- During arithmetic operations, the K-bus can be used to **mask** portions of the field being operated on
- Select or remove accumulator from operation by placing K-bus in all "1" or all "0" state respectively
- During non-arithmetic operation, the carry circuit can be used in conjunction with the K-bus for word-wise-OR operation for bit testing
- Supply literal or constant data to CPE

7. OUTPUT BUSES

A-bus and Memory Address Register
- Main memory address is stored in the memory address register (MAR)
- Main memory is addressed via the A-bus
- MAR and A-bus may also be used to generate device address when executing I/O instructions
- A-bus has Tri-State outputs

D-bus: Data bus from CPE to main memory or to I/O devices
- Sends buffered accumulator outputs to main memory or the external I/O devices
- D-bus has Tri-State outputs

FUNCTION DESCRIPTION

F GROUP	R GROUP	K BUS	NAME	EQUATION	DESCRIPTION
0	I	XX	—	$R_n + (AC \wedge K) + CI \rightarrow R_n, AC$	**Logically AND AC with the K-bus.** Add the result to R_n and carry input (CI). Deposit the sum in AC and R_n.
		OO	ILR	$R_n + CI \rightarrow R_n, AC$	Conditionally increment R_n and load the result in AC. Used to load AC from R_n or to increment R_n and load a copy of the result in AC.
		11	ALR	$AC + R_n + CI \rightarrow R_n, AC$	Add AC and CI to R_n and load the result in AC. Used to add AC to a register. If R_n is AC, then AC is shifted left one bit position.
0	II	XX	—	$M + (AC \wedge K) + CI \rightarrow AT$	**Logically AND AC with the K-bus.** Add the result to CI and the M-bus. Deposit the sum in AC or T.
		OO	ACM	$M + CI \rightarrow AT$	Add CI to M-bus. Load the result in AC or T, as specified. Used to load memory data in the specified register, or to load incremented memory data in the specified register.
		11	AMA	$M + AC + CI \rightarrow AT$	Add the M-bus to AC and CI, and load the result in AC or T, as specified. Used to add memory data or incremented memory data to AC and store the sum in the specified register.
0	III	XX	—	$AT_L \wedge (\overline{I_L \wedge K_L}) \rightarrow RO$ $LI \vee [(I_H \wedge K_H) \wedge AT_H] \rightarrow AT_H$ $[AT_L \wedge (I_L \wedge K_L)] \vee$ $[AT_H \vee (I_H \wedge K_H)] \rightarrow AT_L$	None
		OO	SRA	$AT_L \rightarrow RO \quad AT_H \rightarrow AT_L \quad LI \rightarrow AT_H$	Shift AC or T, as specified, right one bit position. Place the previous low order bit value on RO and fill the high order bit from the data on LI. Used to shift or rotate AC or T right one bit.
1	I	XX	—	$K \vee R_n \rightarrow MAR$ $R_n + K + CI \rightarrow R_n$	**Logically OR R_n with the K-bus.** Deposit the result in MAR. Add the K-bus to R_n and CI. Deposit the result in R_n.
		OO	LMI	$R_n \rightarrow MAR \quad R_n + CI \rightarrow R_n$	Load MAR from R_n. Conditionally increment R_n. Used to maintain a macro-instruction program counter.
		11	DSM	$11 \rightarrow MAR \quad R_n - 1 + CI \rightarrow R_n$	Set MAR to all one's. Conditionally decrement R_n by one. Used to force MAR to its highest address and to decrement R_n.

FUNCTION DESCRIPTION (Continued)

F GROUP	R GROUP	K BUS	NAME	EQUATION	DESCRIPTION
1	II	XX	—	$K \vee M \rightarrow MAR$ $M + K + CI \rightarrow AT$	**Logically OR the M-bus with the K-bus.** Deposit the result in MAR. Add the K-bus to the M-bus and CI. Deposit the sum in AC or T.
		OO	LMM	$M \rightarrow MAR \quad M + CI \rightarrow AT$	Load MAR from the M-bus. Add CI to the M-bus. Deposit the result in AC or T. Used to load the address register with memory data for macro-instructions using indirect addressing.
		11	LDM	$11 \rightarrow MAR$ $M - 1 + CI \rightarrow AT$	Set MAR to all ones. Subtract one from the M-bus. Add CI to the difference and deposit the result in AC or T, as specified. Used to load decremented memory data in AC or T.
1	III	XX	—	$(\overline{AT} \vee K) + (AT \wedge K) + CI \rightarrow AT$	**Logically OR the K-bus with the complement of AC or T, as specified.** Add the result to the logical AND of specified register with the K-bus. Add the sum to CI. Deposit the result in the specified register.
		OO	CIA	$\overline{AT} + CI \rightarrow AT$	Add CI to the complement of AC or T, as specified. Deposit the result in the specified register. Used to form the 1's or 2's complement of AC or T.
		11	DCA	$AT - 1 + CI \rightarrow AT$	Subtract one from AC or T, as specified. Add CI to the difference and deposit the sum in the specified register. Used to decrement AC or T.
2	I	XX	—	$(AC \wedge K) - 1 + CI \rightarrow R_n$	**Logically AND the K-bus with AC.** Subtract one from the result and add the difference to CI. Deposit the sum in R_n.
		OO	CSR	$CI - 1 \rightarrow R_n$ (See Note 1)	Subtract one from CI and deposit the difference in R_n. Used to conditionally clear or set R_n to all 0's or 1's, respectively.
		11	SDR	$AC - 1 + CI \rightarrow R_n$ (See Note 1)	Subtract one from AC and add the difference to CI. Deposit the sum in R_n. Used to store AC in R_n or to store the decremented value of AC in R_n.
2	II	XX	—	$(AC \wedge K) - 1 + CI \rightarrow AT$ (See Note 1)	**Logically AND the K-bus with AC.** Subtract one from the result and add the difference to CI. Deposit the sum in AC or T, as specified.
		OO	CSA	$CI - 1 \rightarrow AT$ (See Note 1)	Subtract one from CI and deposit the difference in AC or T. Used to conditionally clear or set AC or T.
		11	SDA	$AC - 1 + CI \rightarrow AT$ (See Note 1)	Subtract one from AC and add the difference to CI. Deposit the sum in AC or T. Used to store AC in T, or decrement AC, or store the decremented value of AC in T.
2	III	XX	—	$(I \wedge K) - 1 + CI \rightarrow AT$ (See Note 1)	**Logically AND the data of the K-bus with the data on the I-bus.** Subtract one from the result and add the difference to CI. Deposit the sum in AC or T, as specified.
		OO	CSA	$CI - 1 \rightarrow AT$	Subtract one from CI and deposit the difference in AC or T. Used to conditionally clear or set AC or T.
		11	LDI	$I - 1 + CI \rightarrow AT$	Subtract one from the data on the I-bus and add the difference to CI. Deposit the sum in AC or T, as specified. Used to load input bus data or decremented input bus data in the specified register.
3	I	XX	—	$R_n + (AC \wedge K) + CI \rightarrow R_n$	**Logically AND AC with the K-bus.** Add R_n and CI to the result. Deposit the sum in R_n.
		OO	INR	$R_n + CI \rightarrow R_n$	Add CI to R_n and deposit the sum in R_n. Used to increment R_n.
		11	ADR	$AC + R_n + CI \rightarrow R_n$	Add AC to R_n. Add the result to CI and deposit the sum in R_n. Used to add the accumulator to a register or to add the incremented value of the accumulator to a register.

MICROPROCESSOR

FUNCTION DESCRIPTION (Continued)

F GROUP	R GROUP	K BUS	NAME	EQUATION	DESCRIPTION
3	II	XX	—	$M + (AC \wedge K) + CI \rightarrow AT$	**Logically AND AC with the K-Bus.** Add the result to CI and the M-bus. Deposit the sum in AC or T.
		OO	ACM	$M + CI \rightarrow AT$	Add CI to M-bus. Load the result in AC or T, as specified. Used to load memory data in the specified register, or to load incremented memory data in the specified register.
		11	AMA	$M + AC + CI \rightarrow AT$	Add the M-bus to AC and CI, and load the result in AC or T, as specified. Used to add memory data or incremented memory data to AC and store the sum in the specified register.
3	III	XX	—	$AT + (I \wedge K) + CI \rightarrow AT$	**Logically AND the K-bus with the I-bus.** Add CI and the contents of AC or T, as specified, to the result. Deposit the sum in the specified register.
		OO	INA	$AT + CI \rightarrow AT$	Conditionally increment AC or T. Used to increment AC or T.
		11	AIA	$I + AT + CI \rightarrow AT$	Add the I-bus to AC or T. Add CI to the result and deposit the sum in the specified register. Used to add input data or incremented input data to the specified register.

FUNCTION TRUTH TABLE

FUNCTION GROUP	F_6	F_5	F_4
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1

REGISTER GROUP	REGISTER	F_3	F_2	F_1	F_0
I	R_0	0	0	0	0
	R_1	0	0	0	1
	R_2	0	0	1	0
	R_3	0	0	1	1
	R_4	0	1	0	0
	R_5	0	1	0	1
	R_6	0	1	1	0
	R_7	0	1	1	1
	R_8	1	0	0	0
	R_9	1	0	0	1
	T	1	1	0	0
	AC	1	1	0	1
II	T	1	0	1	0
	AC	1	0	1	1
III	T	1	1	1	0
	AC	1	1	1	1

SYMBOL	MEANING
I, K, M	Data on the I, K, and M busses, respectively
CI, LI	Data on the carry input and left input, respectively
CO, RO	Data on the carry output and right output, respectively
R_n	Contents of register n including T and AC (R-Group I)
AC	Contents of the accumulator
AT	Contents of AC or T, as specified
MAR	Contents of the memory address register
L, H	As subscripts, designate low and high order bit, respectively
$+$	2's complement addition
$-$	2's complement subtraction
$\wedge$	Logical AND
$\vee$	Logical OR
$\overline{\oplus}$	Exclusive-NOR
$\rightarrow$	Deposit into

NOTE:
1. 2's complement arithmetic adds 111 . . . 11 to perform subtraction of 000 . . . 01.

FUNCTION DESCRIPTION (Continued)

F GROUP	R GROUP	K BUS	NAME	EQUATION	DESCRIPTION
4	I	XX	—	$CI \vee (R_n \wedge AC \wedge K) \rightarrow CO$ $R_n \wedge (AC \wedge K) \rightarrow R_n$	**Logically AND the K-bus with AC.** Logically AND the result with the contents of R_n. Deposit the final result in R_n. Logically OR the value of CI with the word-wise OR of the bits of the final result. Place the value of the carry OR on the carry output (CO) line.
		00	CLR	$CI \rightarrow CO \quad O \rightarrow R_n$	Clear R_n to all O's. Force CO to CI. Used to clear a register and force CO to CI.
		11	ANR	$CI \vee (R_n \wedge AC) \rightarrow CO$ $R_n \wedge AC \rightarrow R_n$	Logically AND AC with R_n. Deposit the result in R_n. Force CO to one if the result is non-zero. Used to AND the accumulator with a register and test for a zero result.
4	II	XX	—	$CI \vee (M \wedge AC \wedge K) \rightarrow CO$ $M \wedge (AC \wedge K) \rightarrow AT$	**Logically AND the K-bus with AC.** Logically AND the result with the M-bus. Deposit the final result in AC or T. Logically OR the value of CI with the word-wise OR of the bits of the final result. Place the value of the carry OR on CO.
		00	CLA	$CI \rightarrow CO \quad O \rightarrow AT$	Clear AC or T, as specified, to all O's. Force CO to CI. Used to clear the specified register and force CO to CI.
		11	ANM	$CI \vee (M \wedge AC) \rightarrow CO$ $M \wedge AC \rightarrow AT$	Logically AND the M-bus with AC. Deposit the result in AC or T. Force CO to one if the result is non-zero. Used to AND M-bus data to the accumulator and test for a zero result.
4	III	XX	—	$CI \vee (AT \wedge 1 \wedge K) \rightarrow CO$ $AT \wedge (I \wedge K) \rightarrow AT$	**Logically AND the I-bus with the K-bus.** Logically AND the result with AC or T. Deposit the final result in the specified register. Logically OR CI with the word-wise OR of the final result. Place the value of the carry OR on CO.
		00	CLA	$CI \rightarrow CO \quad O \rightarrow AT$	Clear AC or T, as specified, to all O's. Force CO to CI. Used to clear the specified register and force CO to CI.
		11	ANI	$CI \vee (AT \wedge I) \rightarrow CO$ $AT \wedge 1 \rightarrow AT$	Logically AND the I-bus with AC or T, as specified. Deposit the result in the specified register. Force CO to one if the result is non-zero. Used to AND the I-bus to the accumulator and test for a zero result.
5	I	XX	—	$CI \vee (R_n \wedge K) \rightarrow CO$ $K \wedge R_n \rightarrow R_n$	**Logically AND the K-bus with R_n.** Deposit the result in R_n. Logically OR CI with the word-wise OR of the result. Place the value of the carry OR on CO.
		00	CLR	$CI \rightarrow CO \quad O \rightarrow R_n$	Clear R_n to all O's. Force CO to CI. Used to clear a register and force CO to CI.
		11	TZR	$CI \vee R_n \rightarrow CO$ $R_n \rightarrow R_n$	Force CO to one if R_n is non-zero. Used to test a register for zero. Also used to AND K-bus data with a register for masking and, optionally, testing for a zero result.
5	II	XX	—	$CI \vee (M \wedge K) \rightarrow CO$ $K \wedge M \rightarrow AT$	**Logically AND the K-bus with the M-bus.** Deposit the result in AC or T, as specified. Logically OR CI with the word-wise OR of the result. Place the value of the carry OR on CO.
		00	CLA	$CI \rightarrow CO \quad O \rightarrow AT$	Clear AC or T, as specified, to all O's. Force CO to CI. Used to clear the specified register and force CO to CI.
		11	LTM	$CI \vee M \rightarrow CO$ $M \rightarrow AT$	Load AC or T, as specified, from the M-bus. Force CO to one if the result is non-zero. Used to load the specified register from memory and test for a zero result. Also used to AND the K-bus with the M-bus for masking and, optionally, testing for a zero result.

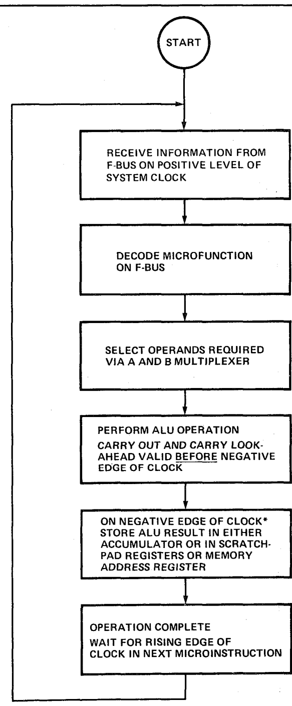
FUNCTION DESCRIPTION (Continued)

F GROUP	R GROUP	K BUS	NAME	EQUATION	DESCRIPTION
5	III	XX	—	$CI \vee (AT \wedge K) \rightarrow CO$ $K \wedge AT \rightarrow AT$	**Logically AND the K-bus with AC or T, as specified.** Deposit the result in the specified register. Logically OR CI with the word-wise OR of the result. Place the value of the carry OR on CO.
		OO	CLA	$CI \rightarrow CO \quad O \rightarrow AT$	Clear AC or T, as specified, to all O's. Force CO to CI. Used to clear the specified register and force CO to CI.
		11	TZA	$CI \vee AT \rightarrow CO$ $AT \rightarrow AT$	Force CO to one if AC or T, as specified, is non-zero. Used to test the specified register for zero. Also used to AND the K-bus to the specified register for masking and, optionally, testing for a zero result.
6	I	XX	—	$CI \vee (AC \wedge K) \rightarrow CO$ $R_n \vee (AC \wedge K) \rightarrow R_N$	Logically OR CI with the word-wise OR of the logical AND of AC and the K-bus. Place the result of the carry OR on CO. Logically OR R_n with the logical AND of AC and the K-bus. Deposit the result in R_n.
		OO	NOP	$CI \rightarrow CO \quad R_n \rightarrow R_n$	Force CO to CI. Used as a null operation or to force CO to CI.
		11	ORR	$CI \vee AC \rightarrow C_O$ $R_N \vee AC \rightarrow R_N$	Force CO to one if AC is non-zero. Logically OR AC with R_n. Deposit the result in R_n. Used to OR the accumulator to a register and, optionally, test the previous accumulator value for zero.
6	II	XX	—	$CI \vee (AC \wedge K) \rightarrow CO$ $M \vee (AC \wedge K) \rightarrow AT$	Logically OR CI with the word-wise OR of the logical AND of AC and the K-bus. Place the carry OR on CO. Logically OR the M-bus, with the logical AND of AC and the K-bus. Deposit the final result in AC or T.
		OO	LMF	$CI \rightarrow CO \quad M \rightarrow AT$	Load AC or T, as specified, from the M-bus. Force CO to CI. Used to load the specified register with memory data and force CO to CI.
		11	ORM	$CI \vee AC \rightarrow CO$ $M \vee AC \rightarrow AT$	Force CO to one if AC is non-zero. Logically OR the M-bus with AC. Deposit the result in AC or T, as specified. Used to OR M-bus with the AC and, optionally, test the previous value of AC for zero.
6	III	XX	—	$CI \vee (I \wedge K) \rightarrow CO$ $AT \vee (I \wedge K) \rightarrow AT$	Logical OR CI with the word-wise OR of the logical AND of the I-bus and the K-bus. Place the carry OR on CO. Logically AND the K-bus with the I-bus. Logically OR the result with AC or T, as specified. Deposit the final result in the specified register.
		OO	NOP	$CI \rightarrow CO \quad R_n \rightarrow R_n$	Force CO to CI. Used as a null operation or to force CO to CI.
		11	ORI	$CI \vee I \rightarrow CO$ $I \vee AT \rightarrow AT$	Force CO to one if the data on the I-bus is non-zero. Logically OR the I-bus to AC or T, as specified. Deposit the result in the specified register. Used to OR I-bus data with the specified register and, optionally, test the I-bus data for zero.
7	I	XX	—	$CI \vee (R_n \wedge AC \wedge K) \rightarrow CO$ $R_n \overline{\oplus} (AC \wedge K) \rightarrow R_n$	Logically OR CI with the word-wise OR of the logical AND of R_n and AC and the K-bus. Place the carry OR on CO. Logically AND the K-bus with AC. Exclusive-NOR the result with R_n. Deposit the final result in R_n.
		OO	CMR	$CI \rightarrow CO \quad \overline{R_n} \rightarrow R_n$	Complement the contents of R_n. Force CO to CI.
		11	XNR	$CI \vee (R_n \wedge AC) \rightarrow CO$ $R_n \overline{\oplus} AC \rightarrow R_n$	Force CO to one if the logical AND of AC and R_n is non-zero. Exclusive-NOR AC with R_n. Deposit the result in R_n. Used to exclusive-NOR the accumulator with a register.

FUNCTION DESCRIPTION (Continued)

F GROUP	R GROUP	K BUS	NAME	EQUATION	DESCRIPTION
7	II	XX	—	$CI \vee (M \wedge AC \wedge K) \rightarrow CO$ $M \overline{\oplus} (AC \wedge K) \rightarrow AT$	Logically OR CI with the word-wise OR of the logical AND of AC and the K-bus and M-bus. Place the carry OR on CO. Logically AND the K-bus with AC. Exclusive NOR the result with the M-bus. Deposit the final result in AC or T.
		00	LCM	$CI \rightarrow CO \quad \overline{M} \rightarrow AT$	Load the complement of the M-bus into AC or T, as specified. Force CO to CI.
		11	XNM	$CI \vee (M \wedge AC) \rightarrow CO$ $M \overline{\oplus} AC \rightarrow AT$	Force CO to one if the logical AND of AC and the M-bus is non-zero. Exclusive-NOR AC with the M-bus. Deposit the result in AC or T, as specified. Used to exclusive-NOR memory data with the accumulator.
7	III	XX	—	$CI \vee (AT \wedge I \wedge K) \rightarrow CO$ $AT \overline{\oplus} (I \wedge K) \rightarrow AT$	Logically OR CI with the word-wise OR of the logical AND of the specified register and the I-bus and K-bus. Place the carry OR on CO. Logically AND the K-bus with the I-bus. Exclusive-NOR the result with AC or T, as specified. Deposit the final result in the specified register.
		00	CMA	$CI \rightarrow CO \quad \overline{AT} \rightarrow AT$	Complement AC or T, as specified. Force CO to CI.
		11	XNI	$CI \vee (AT \wedge I) \rightarrow CO$ $I \overline{\oplus} AT \rightarrow AT$	Force CO to one if the logical AND of the specified register and the I-bus is non-zero. Exclusive-NOR AC with the I-bus. Deposit the result in AC or T, as specified. Used to exclusive-NOR input data with the accumulator.

MICROCYCLE TIMING SEQUENCE



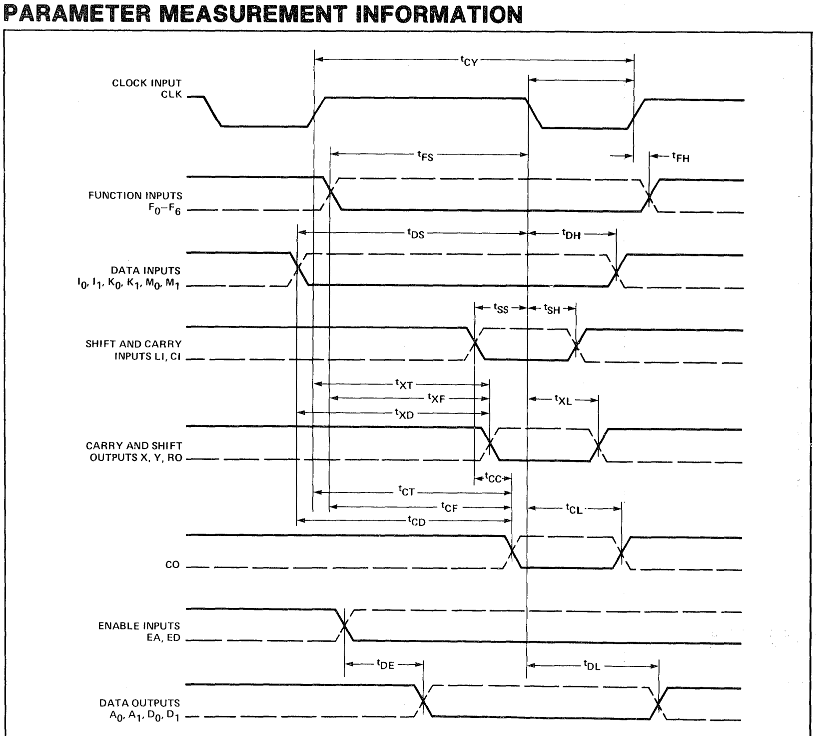
*SYSTEM CLOCK MAY BE OMITTED THROUGH EXTERNAL GATING IN ORDER TO USE CARRY, SHIFT OR CARRY LOOK-AHEAD CIRCUIT TO PERFORM NON-DESTRUCTIVE TEST ON DATA IN ACCUMULATOR OR IN SCRATCHPAD REGISTERS.

SWITCHING CHARACTERISTICS $T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 5\%$

SYMBOL	PARAMETER	MIN	TYP[1]	MAX	UNIT
t_{CY}	Clock Cycle Time	70	45		ns
t_{WP}	Clock Pulse Width	17	10		ns
t_{FS}	Function Input Set-Up Time (F_0 through F_6)	48	-23→35		ns
	Data Set-Up Time:				
t_{DS}	$I_0, I_1, M_0, M_1, K_0, K_1$	40	12→29		ns
t_{SS}	LI, CI	21	0→7		ns
	Data and Function Hold Time:				
t_{FH}	F_0 through F_6	4	0		ns
t_{DH}	$I_0, I_1, M_0, M_1, K_0, K_1$	4	-28→-11		ns
t_{SH}	LI, CI	12	-7→0		ns
	Propagation Delay to X, Y, RO from:				
t_{XF}	Any Function Input		28	41	ns
t_{XD}	Any Data Input		16→20	33	ns
t_{XT}	Trailing Edge of CLK		33	48	ns
t_{XL}	Leading Edge of CLK	13	18→40	73	ns
	Propagation Delay to CO from:				
t_{CL}	Leading Edge of CLK	16	24→44	84	ns
t_{CT}	Trailing Edge of CLK		30→40	56	ns
t_{CF}	Any Function Input		25→35	52	ns
t_{CD}	Any Data Input		17→23	44	ns
t_{CC}	CI (Ripple Carry)		9→13	20	ns
	Propagation Delay to A_0, A_1, D_0, D_1 from:				
t_{DL}	Leading Edge of CLK		17→25	40	ns
t_{DE}	Enable Input ED, EA		10→12	20	ns

NOTE:
1. Typical values are for $T_A = 25°C$ and typical supply voltage.

PARAMETER MEASUREMENT INFORMATION



OBJECTIVE SPECIFICATION

8X01-A,F

DESCRIPTION

The CRC Generator/Checker circuit is used to provide an error detection capability for serial digital data handling system. The serial data stream is divided by a selected polynomial and the division remainder is transmitted at the end of the data stream, as a Cyclic Redundancy check character (CRCC). When the data is received, the same calculation is performed. If the received message is error-free, the calculated remainder should satisfy a predetermined pattern. In most cases, the remainder is zero except in the case where Synchronous Data Link Control type protocols are used whereby the correct remainder is checked for 1111000010111000 (x^0 - x^{15}).

8 polynomials are provided and can be selected via a 3-bit control bus. Popular polynomials such as CRC-16 and CCITT are implemented. Polynomials can be programmed to start with either all zeros or all ones.

Automatic right justification for polynomials of degree less than 16 is provided.

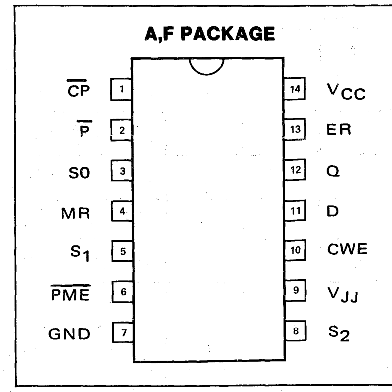
FEATURES

- **I^2L technology**
- **TTL inputs/outputs**
- **10 MHz (max) data rate**
- **total power dissipation = 175 mw (max)**
- **Vcc = 5.0V**
- **V_{JJ} = 1.0V**
- **separate preset and reset controls**
- **SDLC specified pattern match**
- **Automatic right justification**

TYPICAL APPLICATIONS

- **Floppy and other disc systems**
- **Digital cassette and cartridge systems**
- **Data communication systems**

PIN CONFIGURATION



FUNCTIONAL DESCRIPTION

The CRC Generator/Checker circuit provides a means of detecting errors in a serial data communications environment. A binary message can be interpreted as a binary polynomial H(x). This polynomial can be divided by a generator polynomial P(x) such that H(x) = P(x) Q(x) + R(x) whereby Q(x) is the quotient and P(x) is the remainder. During transmission, the remainder is appended to the end of the message as check bits. For a given message, a unique remainder is generated. Hardware implementation of division is simply a feedback shift register with exclusive OR gating. Subtraction and addition in modulo 2 is implemented by the exclusive OR function. The number of shift register stages is equal to the degree of the divisor polynomial.

Table 1 shows the polynomials implemented in the CRC circuit. Each polynomial can be selected via the three-bit polynomial control inputs S_0, S_1 and S_2. To generate the check bits, the data stream is entered via the Data (D) input, using the HIGH to LOW transition of the Clock ($\overline{CP}$) input. This data is gated with the most significant output (Q) of the register, and controls the exclusive OR gates. The Check Word Enable (CWE) must be held HIGH while the data is being entered. After the last data bit is entered, the CWE is brought LOW and the check bits are shifted out of the register and appended to the data bits using external gating.

To check an incoming message for errors, both the data and check bits are entered through the D input with the CWE input held HIGH. The 8X01 is not in the data path, but only monitors the message. The Error output becomes valid after the last check bit has been entered into the 8X01 by a HIGH to LOW transition of $\overline{CP}$. If no detectable errors have occurred during the data transmission, the resultant internal register bits are all LOW and the Error output (ER) is LOW. If a detectable error has occurred, ER is HIGH. ER remains valid until the next HIGH to LOW transition of $\overline{CP}$ or until the device has been Preset or Reset. $\overline{PME}$ must be HIGH if ER output is used to reflect all zero result.

For data communications using the Synchronous Data Link Control protocol (SDLC), the 8X01 is first preset to all ones before any accumulation is done. This applies to both transmitter and receiver. A special pattern of 1111000010111000 (x^0 - x^{15}) is used in place of all zeroes during receiving for valid message check. $\overline{PME}$ is incorporated to select this option. If $\overline{PME}$ is LOW during the last bit time of the message, ER output is LOW if result matches this special pattern. When ER if HIGH, error has occurred

A HIGH level on the Master Reset (MR) input asynchronously clears the register. A LOW level on the Preset ($\overline{P}$) input asynchronously sets the entire register if the control code inputs specify a 16-bit polynomial; in the case of the 12 or 8-bit check polynomials only the most significant 12 or 8 register bits are set and the remaining bits are cleared.

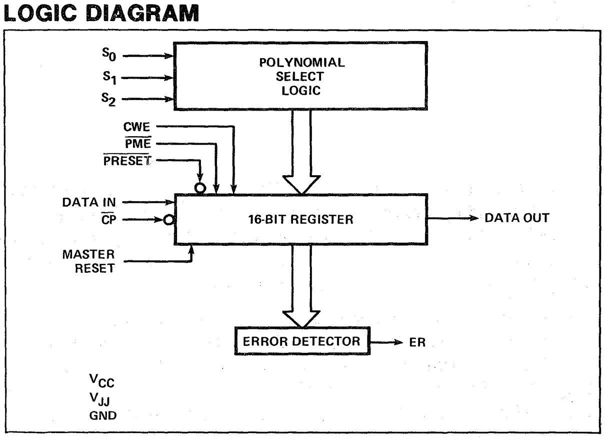
RECOMMENDED OPERATING CONDITIONS

PARAMETER		LIMITS MIN	TYP	MAX	UNITS
V_{CC}	Supply voltage	4.75	5.0	5.25	V
I_{JJ}	Supply current	40		100	mA

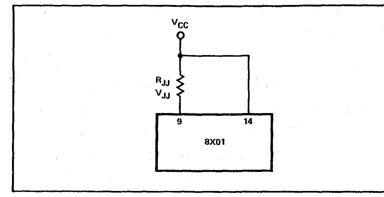
S_0, S_1, S_2	Polynominal Select Inputs
D	Data Input
$\overline{CP}$	Clock (operates on HIGH to LOW transition) Input
CWE	Check Word Enable
$\overline{P}$	Preset (active LOW) input
MR	Master Reset (active HIGH) input
Q	Data Output
ER	Error (active HIGH) output
$\overline{PME}$	Pattern match enable (active LOW)

SELECT CODE			POLYNOMIAL	REMARKS
S_2	S_1	S_0		
L	L	L	$X^{16}+X^{15}+X^{2}+1$	CRC-16
L	L	H	$X^{16}+X^{14}+X+1$	CRC-16 REVERSE
L	H	L	$X^{16}+X^{15}+X^{13}+X^{7}+X^{4}+X^{2}+X^{1}+1$	
L	H	H	$X^{12}+X^{11}+X^{3}+X^{2}+X+1$	CRC-12
H	L	L	$X^{8}+X^{7}+X^{5}+X^{4}+X+1$	
H	L	H	$X^{8}+1$	LRC-8
H	H	L	$X^{16}+X^{12}+X^{5}+1$	CRC-CCITT
H	H	H	$X^{16}+X^{11}+X^{4}+1$	CRC-CCITT REVERSE

LOGIC DIAGRAM

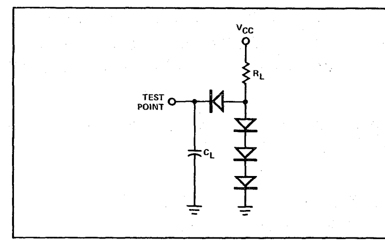


I^2L INJECTOR CURRENT SOURCE

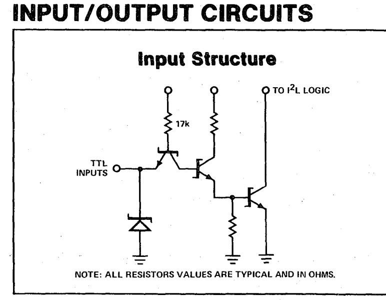


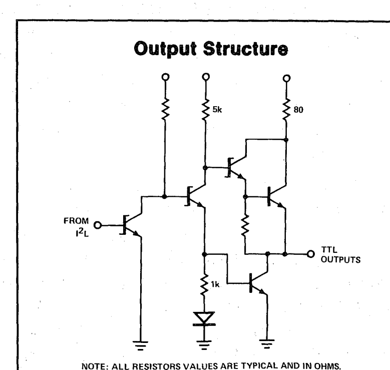
$$R_{JJ}=\frac{V_{CC}-V_{JJ}}{I_{jj}}=\frac{(5.0-0.5)V}{60mA}$$
$$=\frac{4.15V}{60mA}=700\Omega$$

TEST CIRCUIT



INPUT/OUTPUT CIRCUITS





DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (UNLESS OTHERWISE NOTED)

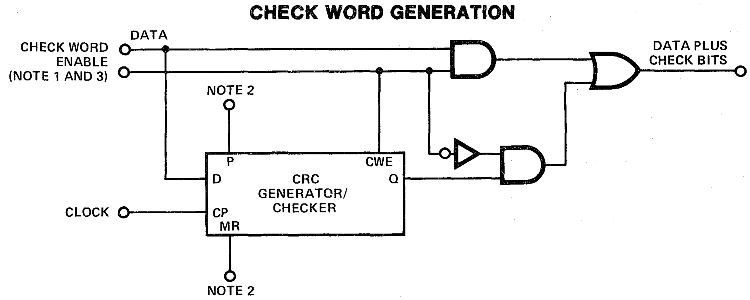
PARAMETER		TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
V_{IH}	Input high voltage		2.0			v
V_{IL}	Input low voltage				0.8	v
	Input clamp diode voltage	Vcc = MIN, I_{IN} = 18mA			-1.5	v
V_{OH}	Output high voltage	Vcc = MIN, I_{OH} = 400μA	2.7			v
V_{OL}	Output low voltage	Vcc = MIN, I_{OL} = 8mA			0.5	v
I_{1H}	Max. input current	Vcc = MAX			0.1	mA
I_{1H}	Input high current	Vcc = MAX, V_{1N} = 2.7v		1.0	2.0	μA
I_{IL}	Input low current	Vcc = MAX, V_{IN} = 0.4v			-0.36	mA
I_{OS}	Output short circuit current	Vcc = MAX, V_{OUT} = 0v	-10		-42	mA
I_{JJ}	Supply current	Vcc = MAX, Inputs open		60	100	mA
I_{CC}	Vcc = MAX, Inputs open			10	18	mA

OBJECTIVE SPECIFICATION 8X01-A,F

SWITCHING CHARACTERISTICS (T_A = 25°C, I_{JJ} = 60mA)

PARAMETER		TEST CONDITIONS		LIMITS V_{CC}=5V			LIMITS V_{CC}=4.5V		UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
$t_wCP(L)$	Clock Pulse Width (low)	Fig.2	30						ns
t_sD	Setup Time, Data to Clock	Fig. 5		60	75				ns
t_sCWE	Setup Time, CWE to Clock	Fig. 5		45	65				ns
t_n	Hold Time, Data, CWE to Clock	Fig. 5 C_L = 15pF		0					ns
$t_wP(L)$	Preset Pulse Width (Low)	Fig. 3	40						ns
$t_wMR(H)$	Master Reset Pulse Width (High)	Fig. 5	40						ns
t_{REC}	Recovery Time, MR, Preset to Clock	Fig. 3,4		60	90				ns
f_{max}	Maximum Clock Frequency						8	10	MHz
t_{PLH}, t_{PHL}	Propagation Delay Clock, MR, Preset to Data Output	Fig. 2,3,4 C_L = 15pf					80	95	ns
t_{PLH}, t_{PHL}	Propagation Delay Clock, MR, Preset to Error Output	C_L = 15pf					110	125	ns

Fig. 2
CHECK WORD GENERATION



NOTES:
1. Check word Enable is HIGH while data is being clocked, LOW during transmission of check bits.
2. 8X01 must be reset or preset before each computation
3. CRC check bits are generated and appended to data bits.

Fig. 3
PROPAGATION DELAYS $\overline{CP}$ TO Q AND $\overline{CP}$ TO ER

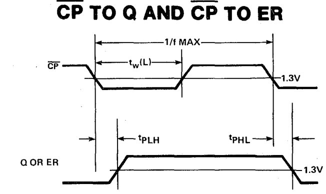


Fig. 4
PROPAGATION DELAYS, $\overline{P}$ TO Q AND ER PLUS RECOVERY TIME P TO $\overline{CP}$

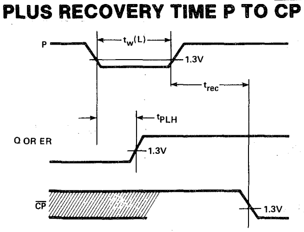


Fig. 5
PROPAGATION DELAYS, MR TO Q AND ER PLUS RECOVERY TIME, MR TO $\overline{CP}$

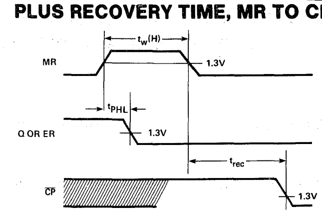
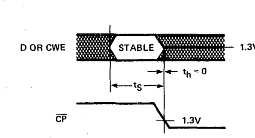


Fig. 6
SET UP AND HOLD TIMES D TO $\overline{CP}$ and CWE TO $\overline{CP}$



OBJECTIVE SPECIFICATION

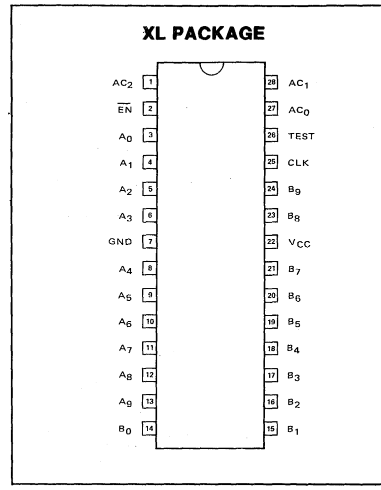
DESCRIPTION

The Signetics 8X02 is a Low-Power Schottky LSI device intended for use in high performance microprogrammed systems to control the fetch sequence of microinstructions. When combined with standard ROM or PROM, the 8X02 forms a powerful microprogrammed control section for computers, controllers, or sequenced logic.

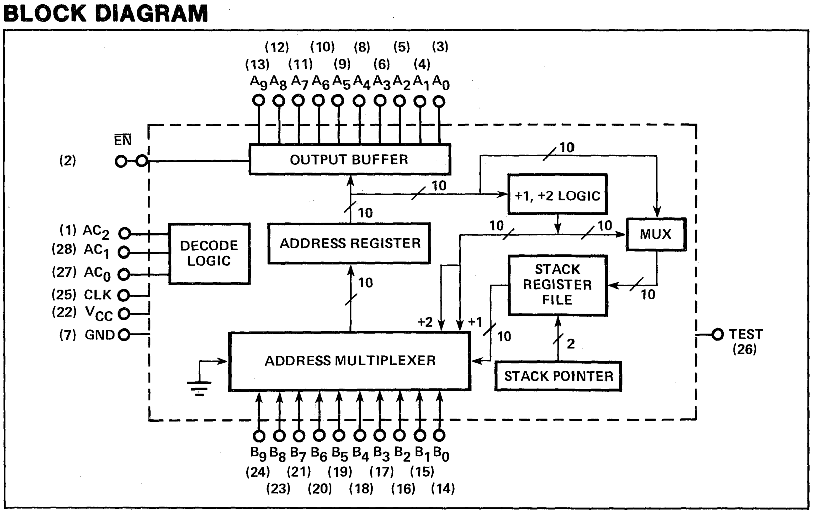
FEATURES

- **Low-power Schottky process**
- **50ns cycle time (TYP)**
- **1024 microinstruction addressability**
- **N-way branch**
- **4-level stack register file (LIFO type)**
- **Automatic push/pop stack operation**
- **"Test & skip" operation on test input line**
- **3-bit command code**
- **Tri-state buffered outputs**
- **Auto-reset to address 0 during power-up**
- **Conditional branching, pop stack, & push stack**
- **Positive edge trigger (low-to-high transition)**

PIN CONFIGURATION



BLOCK DIAGRAM



PIN DESCRIPTION

PIN	SYMBOL	NAME AND FUNCTION	TYPE
	$A_0 - A_9$	Microprogram Address Outputs	Three-state Active HIGH
	$AC_0 - AC_2$	Next Address Control Function Inputs All addressing control functions are selected by these command lines.	Active HIGH
	$B_0 - B_9$	Branch Address Inputs Determines the next address of an N-way branch when used with the BRANCH TO SUBROUTINE (BSR) or BRANCH ON TEST (BRT) command.	Active HIGH
	$\overline{EN}$	Enable Input When in the LOW state, the Microprogram Address Outputs are enabled.	Active LOW
	CLK	Clock Input All resisters are triggered on the LOW-to-HIGH transition of the clock.	
	TEST	Test Input Used in conjunction with four NEXT ADDRESS CONTROL FUNCTION commands to effect conditional skips, branches, and stack operations.	Active HIGH
	GND	Ground	
	V_{CC}	+5 Volt Supply	

FUNCTIONAL DESCRIPTION

The Signetics 8X02 Control Store Sequencer is an LSI device using Low Power Schottky technology and is intended for use in high performance microprogrammed applications. When used alone, the 8X02 is capable of addressing up to 1k words of microprogram. This may be expanded to any microprogram size by conventional paging techniques.

The Address Register consists of ten D-type, edge-triggered flip-flops with a common clock. A new address is entered into the Address Register on the LOW-to-HIGH transition of the clock. The next address to be entered into the Address Register is supplied via the Address Multiplexer.

The Address Multiplexer is a five-input device that is used to select either the branch input, +1 adder, +2 adder, stack register file, or ground (all zeros) as the source of the next microinstruction address. The proper multiplexer channel is automatically selected via the Decode Logic according to the Address Control Function Input and Test Input line.

The +1, +2 logic is used to increment the present contents of the Address Register Register by one or two, depending on the function input command. Thus, the next address to the Control Store ROM/PROM may be either the current address plus one (N+1) or the current address plus two (N+2). If the same Microprogram Address is to be used on successive occasions, the clock to the 8X02 must simply be disabled; therefore, no new address is loaded into the Address Register.

The Stack File Register is used to provide a return address linkage whenever a subroutine or loop is executed. The 4X10 stack operates in a last-in, first-out (LIFO) mode, with the stack pointer always pointing to the next address to be read. Operation of the stack pointer is automatically controlled by the Address Control Function Inputs. Since the stack is four words deep, up to four loops and/or subroutines may be nested.

The branch input is a ten-bit field of direct inputs to the multiplexer which can be selected as the next control store address. Using the appropriate branch command, an N-way branch is possible where N is the address of any micro-instruction within the 1024 word microcode page. Likewise, the RESET command is a special case of an N-way branch in which the multiplexer selects an all zeros input, forcing the next microinstruction address to be ZERO.

The Test Input line is used in conjunction with the conditional execution of four Address Control Function commands. When the Test Input if false (LOW), the sequencer simply increments to the next address (N+1). When it is true (HIGH), the sequencer executes a branch as defined by the input command, thereby transferring control to another portion of the microprogram.

All Address Output lines of the 8X02 are three-state buffered outputs with a common enable line ($\overline{EN}$). When the Enable line is HIGH, all outputs are placed in a high-impedance state, and external access to the control store ROM/PROM is possible. This allows a preprogrammed set of microinstructions to be executed from external or built-in test equipment (BITE), vectored interrupts, and Writable Control Store if implemented.

NEXT ADDRESS CONTROL FUNCTION

MNEMONIC	DESCRIPTION	FUNCTION $AC_{2\ 1\ 0}$	TEST	NEXT ADDRESS	STACK	STACK POINTER
TSK	Test & skip	0 0 0	False True	Current + 1 Current + 2	N.C. N.C.	N.C. N.C.
INC	Increment	0 0 1	X	Current + 1	N.C.	N.C.
BLT	Branch to Loop if test input true	0 1 0	False True	Current + 1 Stack reg file	X POP (read)	Decr Decr
POP	POP stack	0 1 1	X	Stack reg file	POP (read)	Decr
BSR	Branch to subroutine if test input true	1 0 0	False True	Current + 1 Branch addr.	N.C. PUSH (Curr+1)	N.C. Incr
PLP	Push for looping	1 0 1	X	Current + 1	PUSH (Curr Addr)	Incr
BRT	Branch if test input true	1 1 0	False True	Current + 1 Branch addr.	N.C. N.C.	N.C. N.C.
RST	Set micro-program addr. output to zero	1 1 1	X	All O's	N.C.	N.C.

X = Don't care
N.C. = No change

MICROPROCESSOR

FUNCTIONAL DESCRIPTION

The following is a description of each of the eight Next Address Control Functions (AC_2 - AC_0)

MNEMONIC	FUNCTION DESCRIPTION
TSK	AC_{2-0}=000: TEST & SKIP Perform test on TEST INPUT LINE. If test is FALSE (LOW): Next Address=Current Address +1; Stack Pointer unchanged If test is TRUE (HIGH): Next Address=Current Address +2 (i.e. Skip next microinstruction); Stack Pointer unchanged
INC	AC_{2-0}=001: INCREMENT Next Adress=Current Address + 1 Stack Pointer unchanged
BLT	AC_{2-0}=-010: BRANCH TO LOOP IF TEST CONDITION TRUE. Perform test on TEST INPUT LINE. If test is FALSE (LOW): Next Address=Current Address+1; Stack Pointer decremented by 1 If test is TRUE (HIGH): Next Address=Address from Stack Register File (POP); Stack Pointer decremented by 1
POP	AC_{2-0}=011: POP STACK Next Address=Address from Stack Register File (POP) Stack Pointer decremented by 1
BSR	AC_{2-0}=100: BRANCH TO SUBROUTINE IF TEST CONDITION TRUE. Perform test on TEST INPUT LINE. If test is FALSE (LOW): Next Address=Current Address +1; Stack Pointer unchanged If test is TRUE (HIGH): Next Address=Branch Address Input (B_{0-9}); Stack Pointer incremented by 1 PUSH (write) Current Address +1→Stack Register File
PLP	AC_{2-0}=101: PUSH FOR LOOPING Next Address=Current Address +1 Stack Pointer incremented by 1 PUSH (write) Current Address→Stack Register File
BRT	AC_{2-0}=110: BRANCH ON TEST CONDITION TRUE Perform test on TEST INPUT LINE. If test is FALSE (LOW): Next Address=Current Address +1; Stack Pointer unchanged If test is TRUE (HIGH): Next Address=Branch Address Input (B_{0-9}); Stack Pointer unchanged
RST	AC_{2-0}=111: RESET TO ZERO Next Address=0 Stack Pointer unchanged

ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
V_{CC}	Power Supply Voltage	+7	Vdc
V_{IN}	Input Voltage,	+5.5	Vdc
V_O	Off-State Output Voltage	+5.5	Vdc
T_A	Operating Temperature Range	0° to +70°	°C
T_{stg}	Storage Temperature Range	-65° to +150°	°C

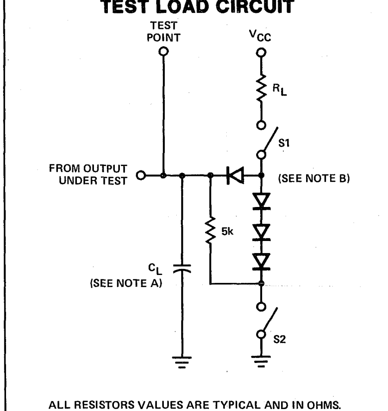
ELECTRICAL CHARACTERISTICS $0°C \leq +70°C$, $4.75V$, $V_{CC} \leq 5.25V$

PARAMETER		TEST CONDITIONS	LIMITS MIN	TYP[1]	MAX	UNIT
V_{IH}	High level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
V_I	Input clamp voltage	$V_{CC} = 4.75V$, $I_I = -18mA$			-1.5	V
V_{OH}	High-level output voltage	$V_{CC} = 4.75V$, $I_{OH} = -2.6mA$	2.4			V
V_{OL}	Low-level output voltage	$V_{CC} = 4.75V$, $I_{OL} = 8mA$			0.5	V
I_I	Input current at maximum Input voltage	$V_{CC} = 5.25V$, $V_I = 5.5V$			100	μA
I_{IH}	High-level input current	$V_{CC} = 5.25V$, $V_I = 2.7V$				
	$AC_0 - AC_2$, $\overline{EN}$, TEST				40	μA
	$B_0 - B_9$				20	μA
	CLK				60	μA
I_{IL}	Low-level input current	$V_{CC} = 5.25V$, $V_I = 0.4V$				
	AC_0—AC_2, $\overline{EN}$, TEST				-0.72	mA
	B_0—B_9				-0.36	mA
	CLK				-1.08	mA
I_{OS}	Short-circuit output current	$V_{CC} = 5.25V$	-20		-100	mA
I_{OZH}	High-Z state output current	$V_{OUT} = 2.7V$			20	μA
I_{OZL}	High-Z state output current	$V_{OUT} = 0.4V$			-20	μA
I_{CC}	Supply current	$V_{CC} = 5.25V$		130	155	mA

NOTE:
1. All typical values are at $V_{CC} = 5V$, $T_A = 25°C$.

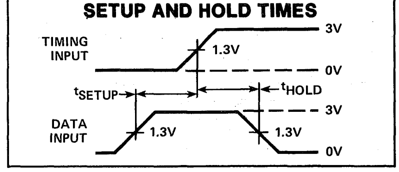
PARAMETER MEASUREMENT INFORMATION

TEST LOAD CIRCUIT

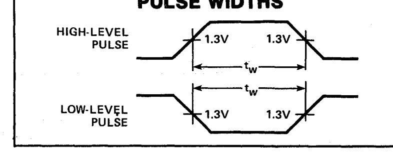


NOTES:
A. C_L includes probe and jig capacitance.
B. All diodes are 1N916 or 1N3064.
C. R_L = 2k, C = 15pF.

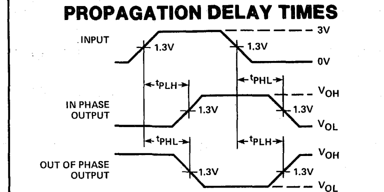
VOLTAGE WAVEFORMS SETUP AND HOLD TIMES



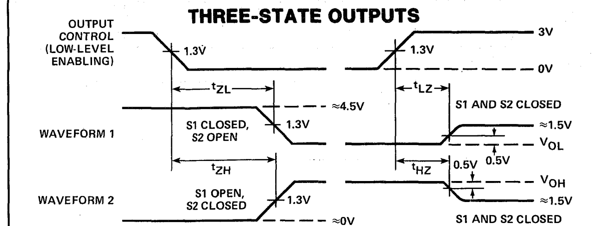
VOLTAGE WAVEFORMS PULSE WIDTHS



VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES THREE-STATE OUTPUTS



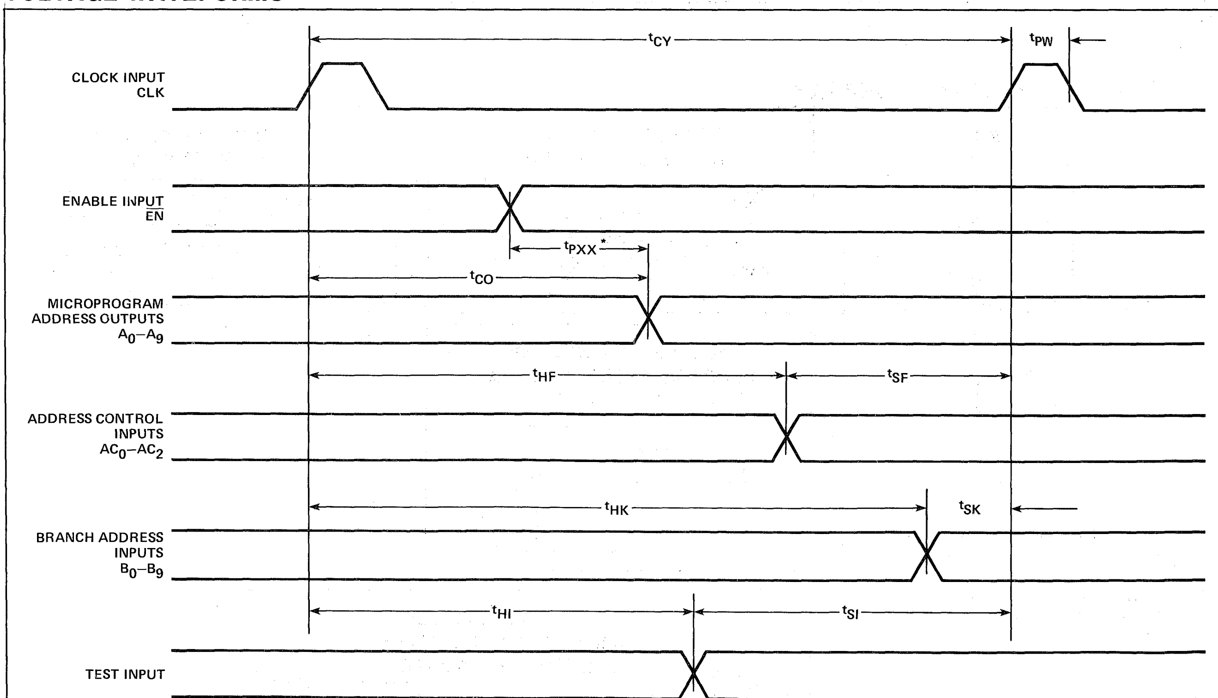
MICROPROCESSOR

SWITCHING CHARACTERISTICS T_A = 0°C to 70°C, V_{CC} = 5.0V + 5%

PARAMETER		LIMITS MIN	TYP[1]	MAX	UNIT
t_{CY}	Cycle Time	57	44		ns
t_{PW}	Clock Pulse Width	25	19		ns
	Propagation Delay from Enable Input ($\overline{EN}$) to Outputs (A_0—A_9)				
t_{PHZ}	("1" to High Impedance)		7	10	ns
t_{PLZ}	("0" to High Impedance)		10	13	ns
t_{PZH}	(High Impedance to "1")		14	19	ns
t_{PZL}	(High Impedance to "0")		21	27	ns
t_{CO}	Propagation Delay from Clock Input (CLK) to Outputs (A_0—A_9)		27	34	ns
	Control and Data Input Set-up Times:				
t_{SF}	AC_0—AC_2	31	24		ns
t_{SK}	B_0—B_9	13	10		ns
t_{SI}	TEST	31	24		ns
	Control and Data Input Hold Times:				
t_{HF}	AC_0—AC_2	26	20		ns
t_{HK}	B_0—B_9	0	0		ns
t_{HI}	TEST	26	20		ns

NOTE:
1. Typical values are for T_A = 25°C and V_{CC} = +5.0 volts.

VOLTAGE WAVEFORMS



* t_{pxx} = t_{phz}, t_{plz}, t_{pzh} and t_{pzl} as applicable

OBJECTIVE SPECIFICATION

8X03 - B,F • 8X04 - B,F

DESCRIPTION

In magnetic tape systems, data is recorded onto the tape in parallel fashion i.e. one bit of each word is recorded on a separate track. Due to the inherent properties of magnetic tape and the misalignment of read heads, data skewing can occur during data recovery period. Systems using high speed drive and high density recording technique, data skewing can indeed become a problem. The Deskew FIFO is designed specifically to perform this data synchronization Function.

The 8X03/04 consists of all the necessary logic for one track of information. Two inputs are provided for each track. Associated with each input are 16 bits of storage. Both inputs are clocked by one common clock. For data recorded using Group-Coded Recording technique, one input is used for input data and the other input used for storing error information associated with each track. For other recording technique such as phase-encoding only one input is needed.

Data is clocked into the first available cell addressed by the write address counter. After each Write cycle, the Write Address Counter is updated and points to the next available cell. During a Read cycle, the Read Address Counter points to the cell where the first bit of data is written in. At the end of the Read cycle, the Read Address Counter is updated to point at the next available cell. Constant comparison is made between the Read and Write Address Counter and status flags of, ¼ full, ½ full, ¾ full and full are brought out to the user.

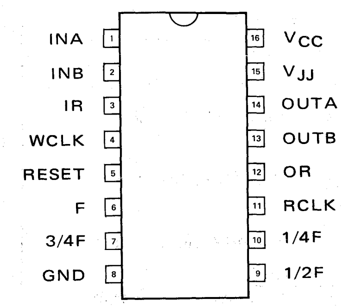
Cascading to longer words can be accomplished with no external circuitry required. When in the cascading mode, data is stored in the first available cell of the first chip, then transferred to the first available of the second chip and so on. Output is thus always available from the last stage of the last chip.

FEATURES

- **I^2L technology**
- **10 MHz typical data rate**
- **16 pin DIP package**
- **300 mA max current requirement**
- **TTL compatible input and outputs**
- **Asynchronous read, write**
- **Open collector outputs**
- **Passive-pullup data outputs**
- **Fully cascadable**
- **8X03**
  15V input/output Breakdown Voltage
- **8X04**
  5.5V input/output Breakdown Voltage

PIN CONFIGURATION

B,F PACKAGE



SIGNAL DEFINITION

I_A, I_B	Data inputs	Non-inverting
I_R	Input ready-follows WCLK Low when FIFO is full (mainly used as cascading clock)	
WCLK	Write clock	Active high
O_A, O_B	Output data	Non-inverting (O C)
OR	Output ready Low when FIFO is empty (mainly used as cascading clock)	Active high (O C)
RCLK	Read clock	Active high
¼,½F,¾F,F	Status flags	Active high (O C)
MR	Master reset MR resets read & write Address counters to predetermined states. Data stored will not be altered.	Active high

SWITCHING CHARACTERISTICS (T_A = 25°C)

PARAMETER		TEST CONDITIONS	LIMITS MIN	TYP	MAX	UNITS
t_{WIR}	Write clock to input ready				40	ns
t_{WOR}	Write clock to output ready	**			150	ns
t_{DOUT}	Write clock to data out	**			150	ns
t_{FLAG}	Write clock to full flag output				150	ns
t_R	Read clock to data out				90	ns
	Read clock to empty flag				120	ns
	Master reset to output ready	C_L = 15pf			100	ns
	Non-cascaded mode					
	Maximum write data rate			10		MHz
	Maximum read data rate			10		MHz
	Cascaded mode					
	Maximum write data rate			5		MHz
	Maximum read data rate			5		MHz

** Only when FIFO is empty.

RECOMMENDED OPERATING CONDITIONS

(I_{JJ} = 200 mA ± 10%)

PARAMETER		LIMITS MIN	TYP	MAX	UNITS
WRITE CYCLE					
W_{PW}	Write clock pulse width		30		ns
t_{WS1}	Input data setup time	0			ns
t_{WS0}		20			ns
t_{WH1}	Input data hold time	40			ns
t_{WH0}		60			ns
F_W	Maximum input data rate		10		MHz
READ CYCLE					
R_{PW}	Read clock pulse width		60		ns
F_R	Maximum read frequency		10		MHz
MR_{PW}	Master reset pulse width		30		ns

ABSOLUTE MAXIMUM RATING OVER OPERATING FREE-AIR TEMPERATURE RANGE

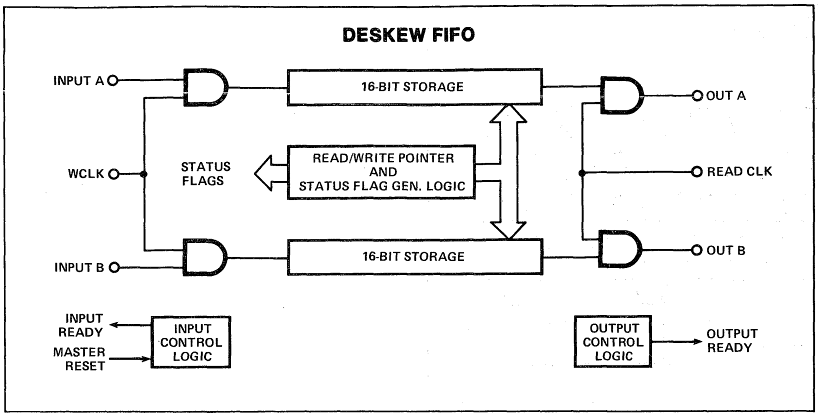
(UNLESS OTHERWISE NOTED)

PARAMETER		LIMITS MIN	TYP	MAX	UNITS
I_{JJ}	Supply current			275	mA
V_{IN}	Input voltage (8X03)			15	V
	(8X04)			5.25	V
	Off-state (high level) Voltage applied to Open collector outputs				
	(8X03)			15	V
	(8X04)			5.25	V
	Storage temperature	-65		+150	°C

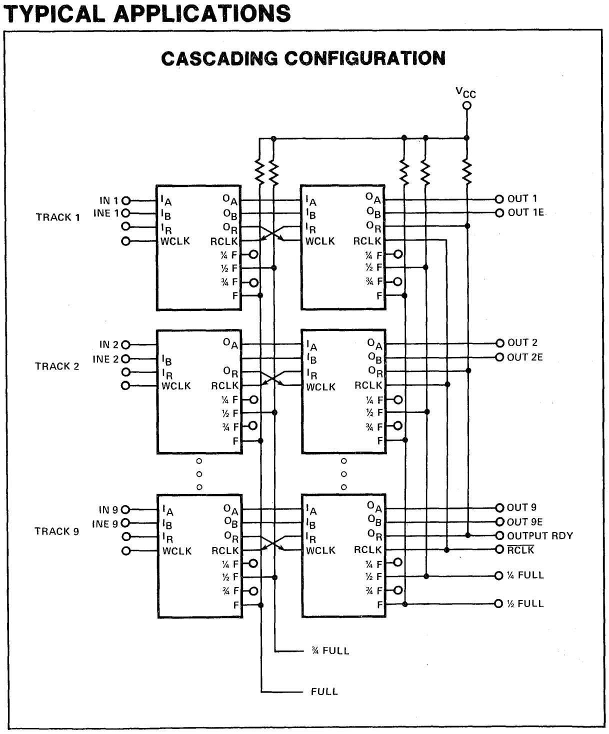
DC CHARACTERISTICS OVER RECOMMENDED OPERATING CONDITIONS

PARAMETER		TEST CONDITIONS	LIMITS MIN	TYP	MAX	UNITS
8X03						
V_{TH}	Input threshold voltage			2.4		V
I_{IL}	Low level input current	V_{IN} = 0.4V			1	mA
I_{IH}	High level input current	V_{IN} = 10V			100	μA
I_I	Input current at max. voltage	V_{IN} = 13V			500	μA
V_{OH}	High level output voltage	I_{OH} = -5ma	7			V
V_{OL}	Low level output voltage	I_{OL} = 2ma			0.4	V
I_{OUT}	Output reverse current (For open collector outputs)	V_{OUT} = 13V			750	μA
I_{CC}	Supply current				60	mA
I_{JJ}			100	105	300	mA
I_{OS}	Short circuit current (Data outputs)	V_{OUT} = 0V			11	mA
8X04						
V_{IH}	High level input voltage		2			V
V_{IL}	Low level input voltage				0.8	V
I_I	Input current @ maximum input voltage	V_{IN} = 2.4V			200	μA
V_{OH}	High level output voltage (Data outputs)	I_{OUT} = -2.5ma	2.7			V
V_{OL}	Low level output voltage	I_{OUT} = 8ma			0.4	V
I_{OUT}	Output reverse current (Open collector outputs)	V_{OUT} = 5.25V			250	μA
I_{CC}	Supply current				50	mA
I_{JJ}			100	165	300	mA
I_{OS}	Short circuit current	V_{OUT} = OV			5	μA

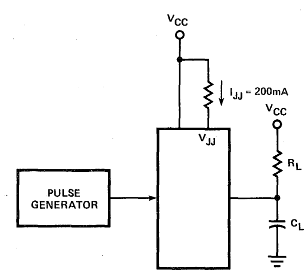
BLOCK DIAGRAM



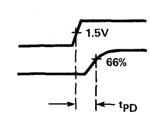
TYPICAL APPLICATIONS



TEST CIRCUITS

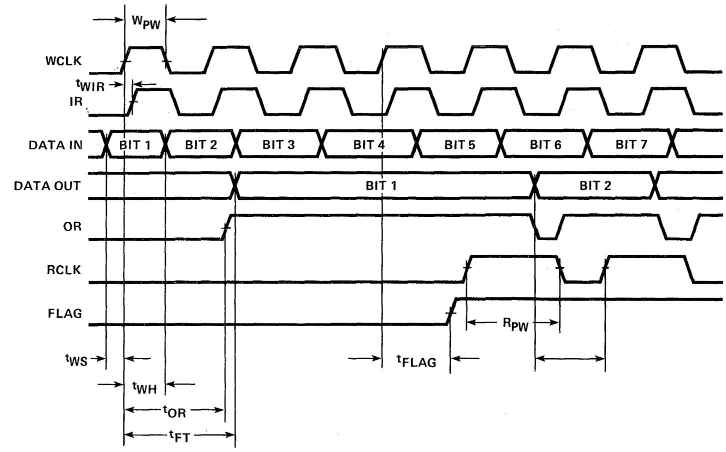


	8X03	8X04
R_L	3KΩ	1KΩ
V_{CC}	13V	5V

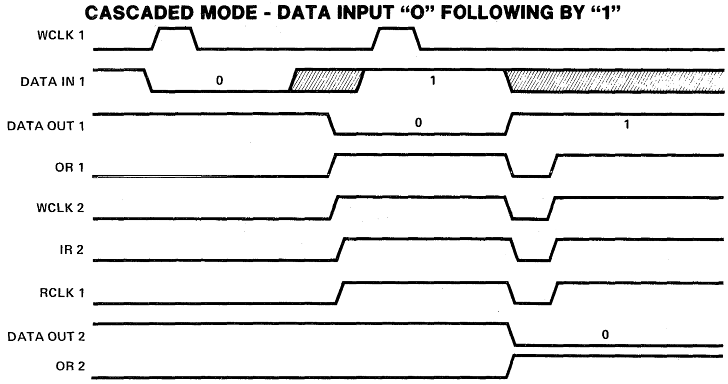


WAVEFORMS

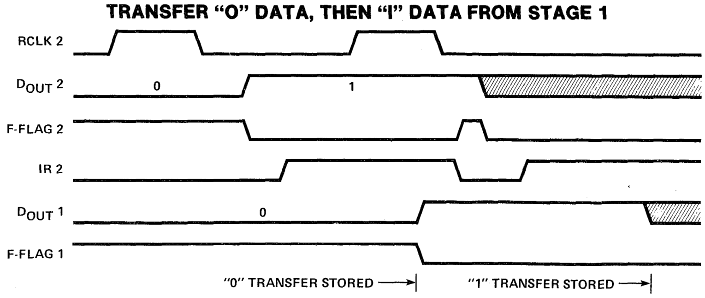
DESKEW FIFO TIMING DIAGRAM



CASCADED MODE - DATA INPUT "O" FOLLOWING BY "1"



CASCADED MODE-BOTH STAGES FULL, READ "O" DATA THEN "I" DATA FROM 2ND STAGE. TRANSFER "O" DATA, THEN "I" DATA FROM STAGE 1



DESCRIPTION

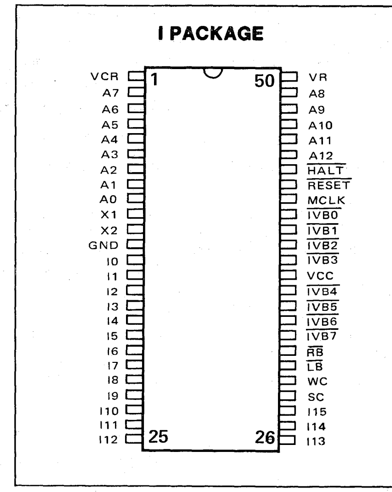
The Signetics 8X300 Interpreter is a monolithic, high-speed micro-processor implemented with bipolar Schottky technology. As the central processing unit, CPU, it allows 16-bit instructions to be fetched, decoded and executed in 300 nanoseconds. A 300 nanosecond instruction cycle requires maximum memory access of 85 nanoseconds, and maximum I/O device access of 40 nanoseconds.

Interpreter instructions operate on 8-bit, parallel data. Logic is distributed along the data path within the Interpreter. Input data can be rotated and masked before being subject to an arithmetic or logical operation; and output data can be shifted and merged with the input data, before being output to external logic. This allows 1- to 8-bit I/O and data memory fields to be accessed and processed in a single instruction cycle.

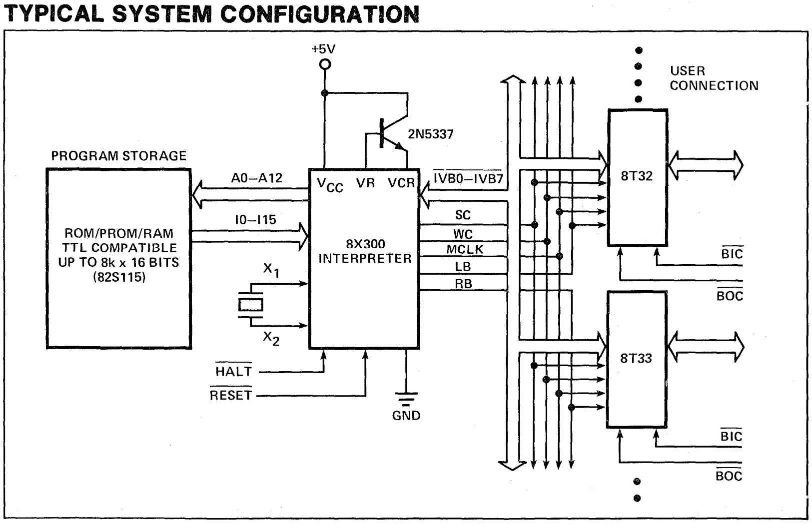
FEATURES

- **225 ns instruction decode and execute delay (with Signetics 8T32/33 I/O port).**
- **Eight 8-bit working registers.**
- **Single instruction access to 1-bit, 2-bit, 3-bit . . . or 8-bit field on I/O bus.**
- **Separate instruction address, instruction, and I/O data busses.**
- **On-chip oscillator.**
- **Bipolar Schottky technology.**
- **TTL inputs and outputs.**
- **Tri-state output on I/O data bus.**
- **+5 volt operation from 0° to 70°C.**

PIN CONFIGURATION



TYPICAL SYSTEM CONFIGURATION



PIN DESCRIPTION

PIN	SYMBOL	NAME AND FUNCTION	TYPE
2-9,45-49	A0-A12:	Instruction address lines. A high level equals "1." These outputs directly address up to 8192 words of program storage. A12 is least signigicant bit.	Active high
13-28	I0-I15:	Instruction lines. A high level equals "1." Receives instructions from Program Storage. I_{15} is least significant bit.	Active high
33-36,38-41	$\overline{IVB0}$-$\overline{IVB7}$	Interface Vector (IV) Bus. A low level equals "1." Bidirectional tri-state lines to communicate with I/O devices. $\overline{IVB7}$ is least significant bit.	Three-state Active low
42	MCLK:	Master Clock. Output to clock I/O devices, and/or provide synchronization for external logic	
30	WC:	Write Command. High level output indicates data is being output on the IV Bus.	Active high
29	SC:	Select Command. High level output indicates that an address is being output on the IV Bus.	Active high
31	$\overline{LB}$:	Left Bank. Low level output to enable one of two sets of I/O devices (LB is the complement of RB).	Active low
32	$\overline{RB}$:	Right Bank. Low level output to enable one of two sets of I/O devices (RB is the complement of LB).	Active low
44	$\overline{HALT}$:	Low level is input to stop the Interpreter.	Active low
43	$\overline{RESET}$:	Low level is input to initialize the Interpreter.	Active low
10-11	X1,X2:	Inputs for an external frequency determining crystal. May also be interfaced to logic or test equipment.	
50	VR	Reference Voltage to Pass Transistor.	
1	VCR	Regulated Output Voltage from Pass Transistor	
37	VCC:	5V power connection.	
12	GND:	Ground.	

PROGRAM STORAGE INTERFACE

Program Storage is typically connected to the A0-A12 (A12 is least signigicant bit) and I0-I15 signal lines. An address output on A0-A12 identifies one 16-bit instruction word in program storage. The instruction word is subsequently input on I0-I15 and defines the interpreter operations which are to follow.

The Signetics 82S115 Prom, or any TTL compatible memory, may be used for program storage.

I/O DEVICES INTERFACE

An 8-bit I/O bus, called the Interface Vector (IV) data bus, is used by the Interpreter to communicate with two fields of I/O devices. The complementary $\overline{LB}$ and $\overline{RB}$ signals identify which field of the I/O devices is selected.

Both I/O data and I/O address information can be output on the IV bus. The SC and WC signals are typically used to distinguish between I/O data and I/O address information as follows:

SC	WC	
1	0	I/O address is being output on IV bus
0	1	I/O data is being output on IV bus
0	0	I/O data is expected on the IV bus, as input to the Interpreter
1	1	Not generated by the Interpreter

The Signetics 82sxxx series RAM, and the 8T32/33 may be attached to the IV bus. (See Application Book)

INTERPRETER ARCHITECTURE AND OPERATION SUMMARY

Figure 1 provides a diagram of Interpreter internal architecture, and Table 1 summarizes Interpreter registers.

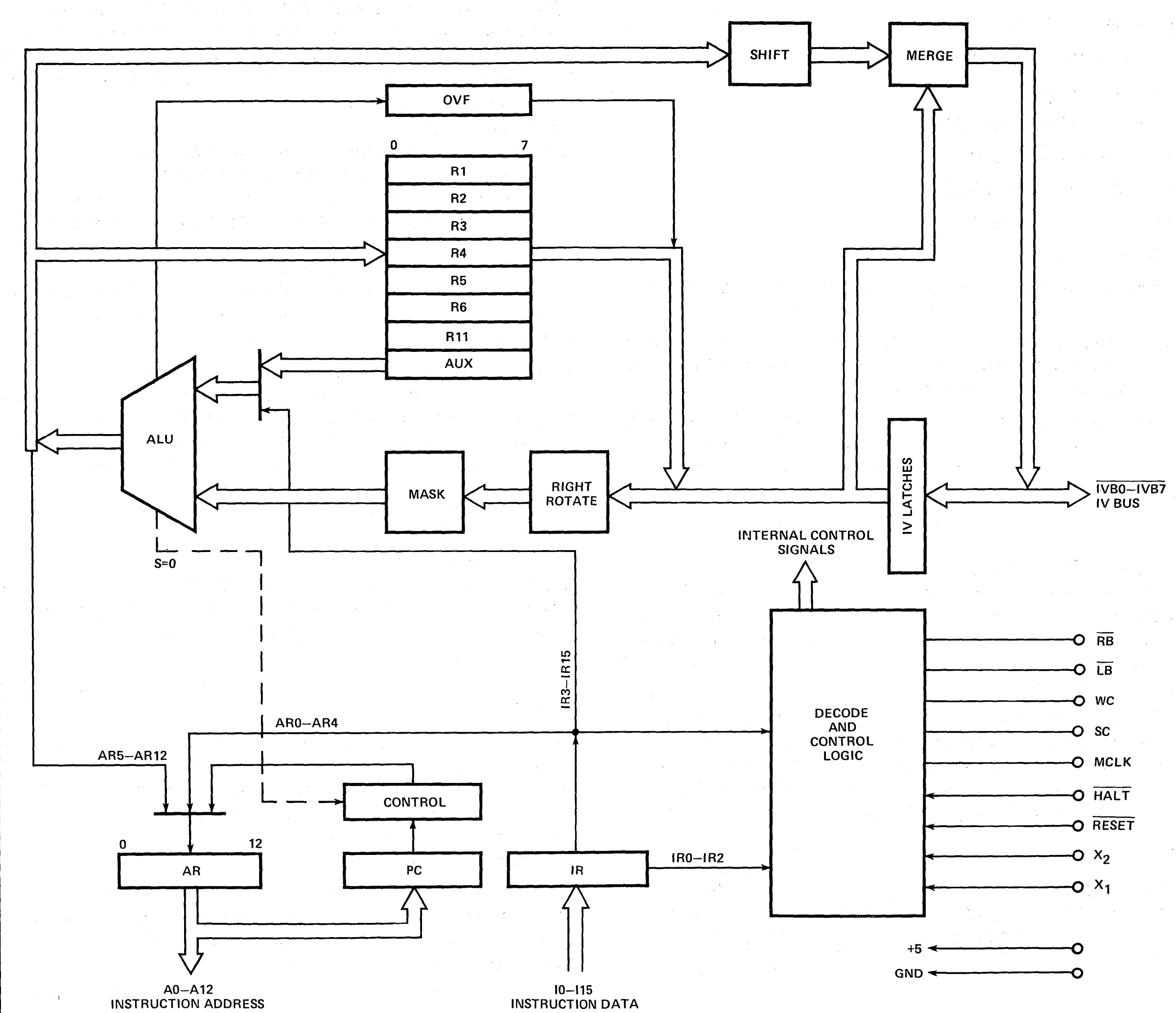


Figure 1

Interpreter Architecture

Table 1
INTERPRETER INTERNAL REGISTERS

Programmable Registers (all 8 bits):

AUX—General working register. Contains second term for arithmetic or logical operations.

R1 —General Working register.

R2 —General working register.

R3 —General working register.

R4 —General working register.

R5 —General working register.

R6 —General working register.

R11 —General working register.

Other Registers:

Address Register (AR) —A 13-bit register containing the address of the current instruction.

OVF—The least-significant bit of this register is used to reflect overflow status resulting from the most recent ADD operation (see Instruction Set Summary).

Program Counter (PC) —Normally contains the address of the current instruction and is incremented to obtain the next instruction address.

Instruction Register (IR)—Holds the 16-bit instruction word currently being executed.

INSTRUCTION CYCLE

Each interpreter operation is executed in one instruction cycle, which may be as short as 300ns. The Interpreter generates MCLK to synchronize external logic to the instruction cycle. Instruction cycles are subdivided into quarter cycles. MCLK is an output during the last quarter cycle.

During the third quarter cycle of an instruction, an address is output on A0-A12, identifying the location in program storage of the next instruction word. This instruction word defines the next instruction, which must be input on I0-I15 during the first quarter cycle of the next instruction cycle (see Figure 2).

INST. AND IV BUS DATA INPUT	DATA PROCESSING	ADDR. AND IV BUS CHANGING	ADDR. AND IV BUS DATA VALID MCLK = HIGH
← ¼ cycle →	← ¼ cycle →	← ¼ cycle →	← ¼ cycle →

Figure 2
INSTRUCTION CYCLE

Instruction Set Summary

The 16-bit instruction word input on I0-I15 is decoded by the instruction decode logic to implement events that are to occur during the remainder of the instruction cycle. Generally the 16-bit instruction word is decoded as follows:

Bit Position	0 1 2	3 … 15
	Instruction Class	Operand(s) Specification

A detailed usage of the 13 "operand(s) specification" bits is given in following sections.

Three operation code bits allow for eight instruction classes. The eight instruction classes are summarized in Table 2. Each entry is referred to as an "instruction class" because the unique architecture of the Interpreter allows a number of powerful variations to be specified by the thirteen operand(s) specification bits. A complete description of instruction formats and some instruction examples are provided in the Applications Guide.

Data Processing

The Interpreter architecture includes eight 8-bit working registers, an arithmetic logic unit (ALU), an overflow register, and the 8-bit IV Bus. Internal 8-bit data paths connect the registers and IV Bus to the ALU inputs, and the ALU output to the registers and IV Bus. Data processing logic is distributed along these internal 8-bit data paths. Rotate and mask logic precedes the ALU on the data entry path. Shift and merge logic follows the ALU on the data output path. All four sets of logic can operate on eight data bits in a single instruction cycle. (See Figure 1)

When less than eight bits of data are specified for output to the IV bus by the ALU, the data field (shifted if necessary) is inserted into the prior contents of the IV bus latches. The IV bus latches contain data input at the start of an instruction. This data in the IV bus latches will be specified in the instruction as a) IV bus source data or b) data from an automatic read when the IV bus is specified as a destination. Therefore, IV bus bit positions outside an inserted bit field are unmodified.

Data Addressing

Sources and destinations of data are specified using a 5-bit octal number, as shown in Table 3. The source and/or destination of data to be operated upon is specified in a single instruction word.

Referring to Table 1, the Auxiliary register (address 00) is the implied source of the second argument for ADD, AND or XOR operations.

IVL and IVR are write-only registers used only as a destination. They have addresses and are treated as registers, but in reality they do not exist. When IVL is specified as a destination or the D field = $20\text{-}27_8$, then $\overline{LB}$= 'low', $\overline{RB}$ = 'high' are generated; when IVR is specified as a destination or the D field = $30\text{-}37_8$, then $\overline{RB}$ = low, $\overline{LB}$ = 'high' are generated.

When IVL or IVR is specified as the destination in an instruction, SC is also activated and data is placed on the IV bus. If IVL or IVR is specified as a source of data, the source data is all zeros.

INSTRUCTION SEQUENCE CONTROL

The Address Register and Program Counter are used to generate addresses for accessing an instruction. The Address Register is used to form the instruction address, and in all but three instructions (XEC, NZT, and JMP) the address is copied into the Program Counter. The instruction address is formed in one of three ways:

1. For all instructions but the JMP, XEC, and a satisfied NZT, the Program Counter is incremented by one and placed in the Address Register.
2. For the JMP instruction, the full 13-bit address field from the JMP instruction is placed into the Address Register and copied into the Program Counter.
3. For the XEC and NZT instructions, the high order 5- or 8-bits of the Program Counter are combined with 8- or 5-lower-order bits of ALU output (XEC or NZT) and placed in the Address Register. For the NZT instruction, it is also copied into the Program Counter.

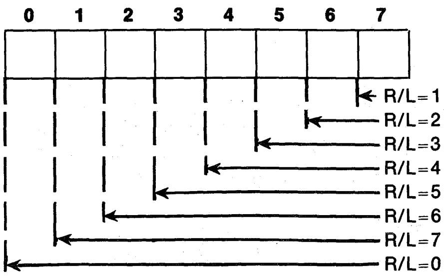
TABLE 2
INSTRUCTION SET SUMMARY

INSTRUCTION MNEMONIC	OP CODE	FORMATS	DESCRIPTION	I/O CONTROL SIGNALS	INSTRUCTION CYCLE: INSTRUCTION INPUT AND DATA PROCESSING	INSTRUCTION CYCLE: ADDRESS/IV BUS OUTPUT
MOVE	0	Register to Register 0 2 3 7 8 10 11 15 [0 | S | R/L | D] S≠07,17,20-37$_8$ D≠10,20-37$_8$	(S)→D Move contents of register specified by S to register specified by D. Right rotate contents of register S by R/L places before operation.	SC= WC= LB/RB=	0 0 1 if D=17	1 if D=07,17 0 1 if D=17
		IV Bus to Register: 0 2 3 7 8 10 11 15 [0 | S | R/L | D] S=20-37$_8$ D≠10,20-37$_8$	Move right rotated IV bus (source) data specified by S to register specified by D. R/L specifies the length of source data with most significant bits set to zero.	SC= WC= LB/RB= LB/RB=	0 0 0 if S=20-27 1 if S=30-37	1 if D=07,17 0 1 if D=17 1 if D=17
		Register to IV Bus: 0 2 3 7 8 10 11 15 [0 | S | R/L | D] S≠07,17,20-37$_8$ D=20-37$_8$	Move contents of register specified by S to the IV bus. Before placement on IV bus, data is shifted as specified by D, and R/L bits merged with existing IV bus data.	SC= WC= LB/RB= LB/RB=	0 0 x x	0 1 0 if D=20-27 1 if D=30-37
		IV Bus to IV Bus: 0 2 3 7 8 10 11 15 [0 | S | R/L | D] S=20-37$_8$ D=20-37$_8$	Move right rotated IV bus data (sources) specified by S to the IV bus. Before placement on IV bus, data is shifted or specified by D and R/L specifies the legnth of source data and of destination data merged with existing IV bus data.	SC= WC= LB/RB= LB/RB=	0 0 0 if S=20-27 1 if S=30-37	0 1 0 if D=30-37 1 if D=30-37
ADD	1	SAME AS MOVE	(S) plus (AUX) → D Same as MOVE but contents of AUX ADDed to the source data. If carry from most significant bit then OVF=1, otherwise OVF=0		SAME AS MOVE	
AND	2	SAME AS MOVE	(S) ∧ (AUX) → D Same as MOVE but contents of AUX ANDed with source data.		SAME AS MOVE	
XOR	3	SAME AS MOVE	(S) ⊕ (AUX) → D Same as MOVE but contents of AUX exclusive ORed with source data.		SAME AS MOVE	
XEC	4	Register Immediate: 0 2 3 7 8 15 [4 | S | I] S≠07,17,20-37$_8$ I=000-377$_8$	Execute instruction at current page address offset by I + (S). EXECute the instruction at the address determined by catenating 5 high order bits of PC with the 8 bit sum of I and register specified by S. PC is not incremented.	SC= WC= LB/RB	0 0 x	0 0 x
		IV Bus Immediate: 0 2 3 7 8 10 11 15 [4 | S | R/L | I] S=20-37$_8$ I=00-37$_8$	EXECute the instruction at the address determined by catenating 8 high order bits of PC with the 5 bit sum of I and rotated IV bus data (source) specified by S. R/L specifies length of source data with most significant bits set to zero. PC is not incremented.	SC= WC= LB/RB= LB/RB=	0 0 0 if S=20-27 1 if S=30-37	0 0 x x

MICROPROCESSOR

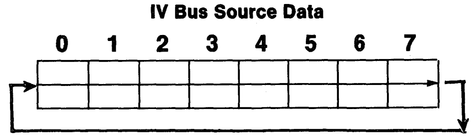
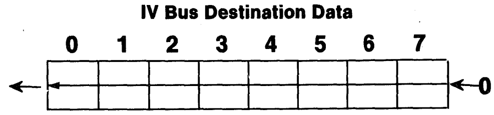
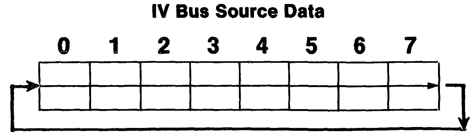
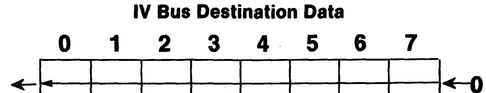
TABLE 2
INSTRUCTION SET SUMMARY

INSTRUCTION MNEMONIC	OP CODE	FORMATS	DESCRIPTION	I/O CONTROL SIGNALS	←INSTRUCTION CYCLE→	
					INSTRUCTION INPUT AND DATA PROCESSING	ADDRESS/IV BUS OUTPUT
NZT	5	Register Immediate: 0 2 3 7 8 15 | 5 | S | I | S≠07,17,20-37_8 I=000-377_8	If (S) ≠ 0, jump to current page address offset by I; otherwise PC + 1 → PC If contents of register specified by S is Non Zero then Transfer to address determined by catenating 5 high order bits of PC with I; otherwise increment PC.	SC= $\overline{WC}$= $\overline{LB}$/RB=	0 0 x	0 0 x
		IV Bus Immediate: 0 2 3 7 8 10 11 15 | 5 | S | R/L | I | S=20-37_8 I=00-37_8	If right rotated IV bus data (source) is Non Zero then Transfer to address determined by catenating 8 high order bits of PC with I; otherwise increment PC.	SC= $\overline{WC}$= $\overline{LB}$/RB= $\overline{LB}$/RB=	0 0 0 if S=20-27 1 if S=30-37	0 0 x x
XMIT	6	Register Immediate: 0 2 3 7 8 15 | 6 | D | I | D≠20-37_8 I=000-377_8	Transmit I → D TRANSMIT and store 8 bit binary pattern I to register specified by D.	SC= $\overline{WC}$= $\overline{LB}$/RB=	0 0 x	1 if D=07,17 0 1 if D=17
		IV BUS IMMEDIATE 0 2 3 7 8 10 11 15 | 6 | D | R/L | I | D=20-37_8 I=00-37_8	TRANSMIT binary pattern I to IV bus. Before placement on IV bus, literal I is shifted as specified by D and R/L bits merged with existing IV bus data.	SC= $\overline{WC}$= $\overline{LB}$/RB= $\overline{LB}$/RB=	0 0 x x	0 1 0 if S=20-27 1 if S=30-37
JMP	7	Address Immediate: 0 2 3 15 | 7 | A | A=00000-17777_8	Jump to Program Address A JUMP to program storage address A. A is stored in the address register (AR).	SC= $\overline{\ }$ WC=$\overline{LB}$/RB	0 0 x	0 0 x



**IV BUS DATA
LENGTH SPECIFICATION**

**TABLE 3
DATA SOURCE/DESTINATION ADDRESS**

S AND/OR D FIELD SPECIFICATION (OCTAL)	SOURCE/DESTINATION
00	Auxiliary Register (AUX)
01 to 06	Work registgers (R1 to R6) respectively
07	IVL write-only register (destination only)
10	Overflow status (OVF) — source only
11	Working register (R11)
17	IVR write-only register (destination only)
2N (N=0,1,2, 3,4,5,6,7)	a. If a source, IV bus data right rotated (7 — N) bits and masked (specified by R/L). $\overline{LB}$='low' and $\overline{RB}$='high' generated. **IV Bus Source Data**  b. If a destination, IV bus data left shifted (7 — N) bits and merged (specified by R/L). $\overline{LB}$='low' and $\overline{RB}$='high' generated. **IV Bus Destination Data** 
3N (N=0,1,2, 3,4,5,6,7)	a. If a source, IV bus data right rotated (7 — N bits and masked (specified by R/L). $\overline{LB}$='high' and $\overline{RB}$='low' generated. **IV Bus Source Data**  b. If a destination, IV bus data left shifted (7 — N) bits and merged (specified by R/L). $\overline{LB}$='high' and $\overline{RB}$='low' generated. **IV Bus Destination Data** 

SYSTEM DESIGN USING THE INTERPRETER

Designing hardware around the 8X300 Interpreter reduces to selecting a program storage devicer (ROM, PROM, etc.), selecting I/O devices (IV BYTE, MULTIPLEXERS, RAM, etc.), selecting clock mode (system driven or crystal controlled) and interfacing the Interpreter to these components, as shown in Figure 3.

SYSTEM CLOCK

The Interpreter has an integrated oscillator which generates all necessary clock signals. The oscillator is designed to connect directly to a series resonant quartz crystal via pins X1 and X2. The crystal resonant frequency, f, is related to the desired cycle time, T, by the relationship f=2/T. For a 300 ns system, f=6.667 MHz.

In lower speed applications where the cycle time need not be precisely controlled, a capacitor may be connected between X1 and X2 to drive the oscillator. If cycle time is to be varied, X1 and X2 should be driven from complementary outputs of a pulse generator. Figure 4 shows a typical configuration. For systems where the Interpreter is to be driven from a master clock, the X1 and X2 lines may be interfaced to TTL logic as shown in Figure 5.

CRYSTAL CHARACTERISTICS

Type:	Fundamental mode, series resonant
Impedance at Fundamental:	35 ohms maximum
Impedance at harmonics and spurs:	50 ohms minimum

HALT, RESET SIGNALS

$\overline{\text{HALT}}$:

A low level at the $\overline{\text{HALT}}$ input causes the Interpreter to stop processing after completion of the current instruction (end of quarter cycle when MCLK is high). $\overline{\text{HALT}}$ does not inhibit MCLK or affect any internal registers. Normal operations begins with the next complete instruction cycle after the $\overline{\text{HALT}}$ input goes high.

$\overline{\text{RESET}}$:

A low level at the $\overline{\text{RESET}}$ input sets the program counter and address register to zero and inhibits MCLK. $\overline{\text{RESET}}$ must be applied for at least one full instruction cycle to insure both registers are cleared. MCLK occurs on first instruction cycle and normal operation begins with the second instruction cycle after the $\overline{\text{RESET}}$ input goes high.

EXAMPLE:

A specific example of a control system, using the 8X300 Interpreter — four 8T32/33 IV Bytes, and two 82S215 ROMs is shown in Figure 3. Only eight components are required to build this system which contains 512 words of program storage, 32 TTL I/O connection points, and operates at a 300-ns instruction cycle time.

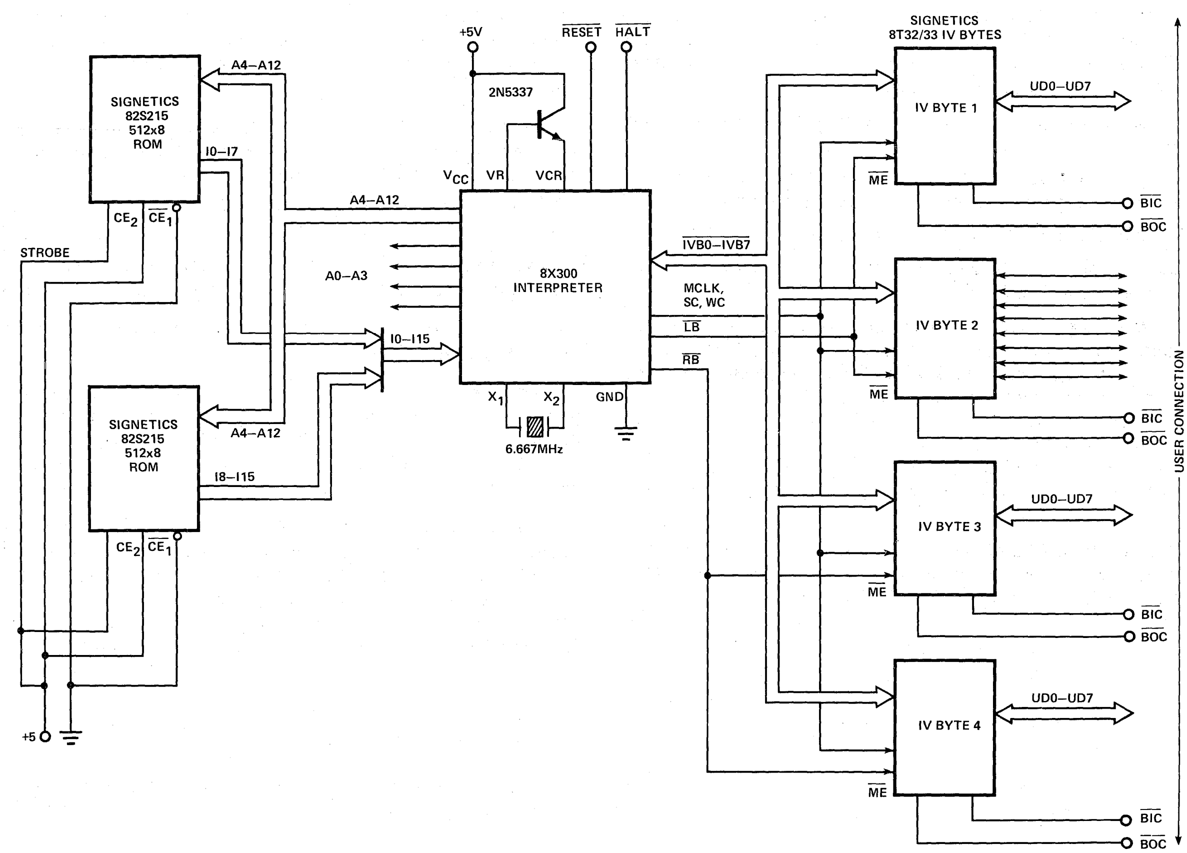
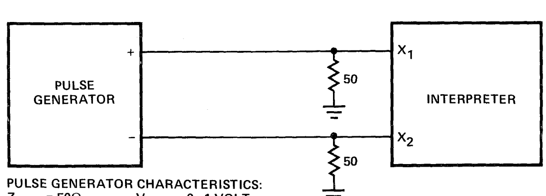


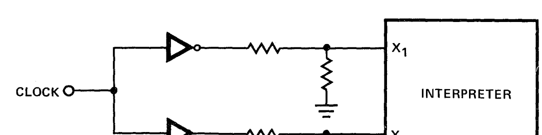
FIGURE 3
EXAMPLE OF CONTROL SYSTEM



PULSE GENERATOR CHARACTERISTICS:
$Z_{OUT} = 50\Omega$ V_{OUT} = 0–1 VOLT
RISETIME ≤ 10ns SKEW ≤ 10ns
COMPLEMENTARY OUTPUTS

NOTE: ALL RESISTORS VALUES ARE TYPICAL AND IN OHMS.

FIGURE 4
CLOCKING WITH A PULSE GENERATOR



TTL DRIVER CHARACTERISTICS:
RISETIME AND FALLTIME ≤ 10ns
SKEW BETWEEN COMPLEMENTARY OUTPUTS ≤ 10ns

FIGURE 5
CLOCKING WITH TTL

SYSTEM TIMING

The system instruction cycle time is determined by program storage access time, I/O register data/control delays, and Interpreter propagation delays. Instruction cycle time is normally constrained by two major propagation delay paths:

1. Program storage access time + instruction -to- address stable delay **or**

   Program storage access time + I/O control input delay + I/O device access time, + IV Bus to address stable delay

II. I/O control input delay + I/O device access time.

These propagation path delay times must be consistent with the Interpreter internal clock times.

Interpreter internal clock intervals occur every quarter cycle of a complete instruction cycle. The Interpreter output MCLK is high during the last quarter cycle of every instruction cycle. Interpreter input operations (instruction data, IV Bus data) occur during the first two quarter cycles (INPUT PHASE). Interpreter output operations (address, IV Bus data) occur during the last two quarter cycles (OUTPUT PHASE). Figure 6 illustrates typical timing waveforms for an instruction cycle. Interpreter propagation delays are shown in Figure 6.

Propagation path II delay time must be less than one quarter cycle. Interpreter delay times which are applicable are: MCLK TO SC/WC INPUT CONTROL and MCLK TO LB/RB INPUT CONTROL. These delays occur during the first part of the first quarter cycle as shown in Figure 6 and correspond to I/O control input delays.

The maximum I/O device access time is the difference between one quarter cycle time and the I/O control input delay. Using the delay values, the required I/O device access time is determined by the following equations:

35ns + I/O device access $\leq$ ¼(cycle time) EQ1

25ns + I/O device access $\leq$ ¼(cycle time) EQ2

For a 300-ns instruction cycle time, I/O device access times must be less than 40ns and 50ns respectively. The Signetics 8T32/33 IV Byte is an I/O register which satisfies the I/O device access time constraints.

Propagation path I determines the allowable program storage access time for a given instruction cycle time. The program storage access time is the smaller of these two equations:

Program storage access $\leq$ cycle time — instruction to address stable EQ3

Program storage access $\leq$ cycle time — (I/O device access + I/O control input delay $\leq$ IV Bus to address stable delay) EQ4

Therefore, a cycle time of 300 ns requires a program storage access time of 85ns or less.

Tradeoffs can be made between I/O device access time and program storage access time. If the I/O device access and program storage access times are less than the limits determined in equations EQ1,EQ2 and EQ3, then EQ4 can be used to trade I/O device and program storage access times.

Propagation delays during the OUTPUT PHASE usually do not limit instruction cycle times. MCLK is normally used to control data entry into I/O devices on the IV Bus during the last two quarter cycles. The user must insure that data set-up time requirements of I/O devices are satisfied. Data output on the IV Bus will be stable for the duration of MCLK if the I/O device access time and instruction cycle time satisfy the following equation:

I/O device access + I/O control input delay + ½(cycle time) $\leq$ MCLK to IV Bus stable delay.

If the above inequality is not satisfied, the IV Bus data may be changing during MCLK.

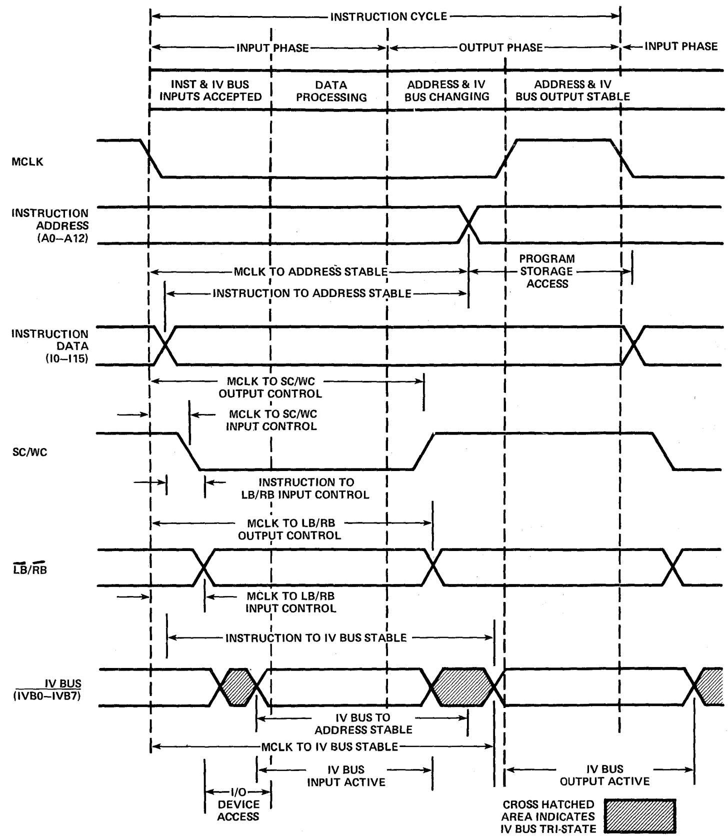


Figure 6
TYPICAL INSTRUCTION CYCLE TIMING

ABSOLUTE MAXIMUM RATINGS

Supply Voltage V_{CC} 7V
Logic Input Voltage 5.5V
Crystal Input Voltage 2V

AC ELECTRICAL CHARACTERISTICS

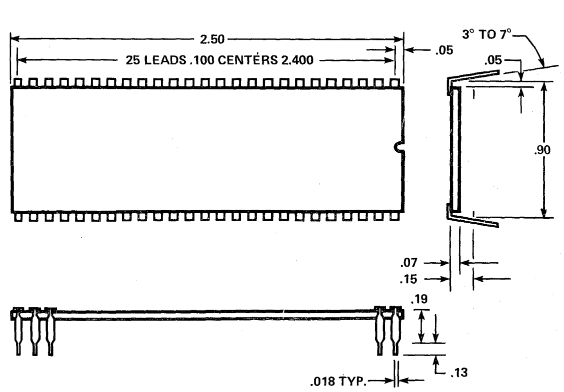
DELAY DESCRIPTION	PROPAGATION DELAY LIMIT	CYCLE TIME LIMIT
X1 falling edge to MCLK falling edge		
MCLK to SC/WC input control	25ns	
MCLK to SC/WC output control *		.5(CYC) + 25ns
INSTRUCTION to $\overline{LB}$/RB input control	35ns	
MCLK to $\overline{LB}$/RB input control	35ns	
MCLK to $\overline{LB}$/RB output control		.5 (CYC) + 35ns
INSTRUCTION to IV BUS stable	225ns	
MCLK to IV BUS stable	225ns	
IV BUS input stable to IV BUS output stable	150ns	
INSTRUCTION to ADDRESS stable	215ns	
MCLK to ADDRESS stable	215ns	.5 (CYC) + 40ns
IV BUS to ADDRESS stable	140ns	
MCLK falling edge to $\overline{HALT}$ falling edge	¼(CYC)—40ns (max)	
MCLK falling edge to $\overline{HALT}$ rising edge	¼(CYC)—40ns	
MCLK falling edge to $\overline{RESET}$ falling edge	½(CYC) (max)	
$\overline{RESET}$ rising edge to first MCLK	0 to 1 CYC (max)	

Limits apply for V_{CC} = 5V ≤ 5% and 0°C ≤ T_A ≤70°C.
Loading on ADDRESS outputs ≤ 100pF and other outputs ≤ 300pF
*IV Bus outputs remain Hi Z for at least 20ns after SC/WC output control

DC ELECTRICAL CHARACTERISTICS

PARAMETER	TEST CONDITIONS	LIMITS MIN	TYP	MAX	UNITS
V_{IH} High-level input voltage					
X1, X2		.6			V
All others		2			V
V_{IL} Low-level input voltage					
X1, X2				.4	V
All others				.8	V
V_{CL} Input clamp voltage (Note 1)	V_{CC} = 4.75V I_I = -10mA			-1.5	V
I_{IH} High-level input current					
X1, X2	V_{CC} = 5.25V V_{IH} = .6V		2700		μA
All others	V_{CC} = 5.25V V_{IH} = 4.5V		<1	50	μA
I_{IL} Low-level input current					
$\overline{\text{X1, X2}}$	V_{CC} = 5.25V		-2500		μA
IVBO-7	V_{IL} = .4V V_{CC} = 5.25V		-140	-200	μA
I0-I15	V_{IL} = .4V V_{CC} = 5.25V		-880	-1600	μA
$\overline{\text{HALT}}$, $\overline{\text{RESET}}$	V_{IL} = .4V V_{CC} = 5.25V V_{IL} = .4V		-230	-400	μA
V_{OL} Low-level output voltage					
A0-A12	V_{CC} = 4.75V I_{OL} = 4.25mA		.35	.55	V
All others	V_{CC} = 4.75V I_{OL} = 16mA		.35	.55	V
V_{OH} High-level output voltage	V_{CC} = 4.75V I_{OH} = 3mA	2.4			V
I_{OS} Short circuit output current (Note 2)	V_{CC} = 5.25V	-30		-140	mA
V_{CC} Supply voltage		4.75	5	5.25	V
I_{CC} Supply current	V_{CC} = 5.25V		300	450	mA

NOTES:
1. Crystal inputs X1 and X2 do not have clamp diodes.
2. Only one output may be grounded at a time.
3. (Limits apply for V_{CC} = 5V ± 5% and 0°C<T_A<70°C unless specified otherwise.)



INTERPRETER PACKAGE DIMENSIONS

mitrel

6

MILrel 38510/833 PROGRAM

The Signetics MILrel 38510/883 Program is organized to provide a broad selection of processing options, structured around the most commonly requested customer flows. The Program is designed to provide our customers:

- Five standard processing flows to help minimize the need for custom specs.
- Cost savings realized by using standard processing flows in lieu of custom flows.
- Better delivery lead times by minimizing spec negotiation time, plus allows customers to buy product off-the-shelf or in various stages of production rather than waiting for devices started specifically to custom specs.

The following explains the five different processing options available to you. Special device marking clearly distinguishes the type of screening performed and examples of product marking are included here for your reference.

1) JAN Qualified:

JAN Qualified product is designed to give you the optimum in quality and reliability. The JAN processing level is offered as the result of the government's product standardization programs, and is monitored by the Defense Electronic Supply Center (DESC), through the use of industry-wide procedures and specifications.

JAN Qualified products are manufactured, processed and tested in a government certified facility to MIL-M-38510, and appropriate device slash sheet specifications. Design documentation, lot sampling plans, electrical test data and qualification data for each specific part type has been approved by the Defense Electronic Supply Center (DESC) and products appear on the DESC Qualified Products List. (QPL-38510)

Group B testing, per MIL-STD-883 Method 5005 is performed on each six weeks of production on each slash sheet for each package type. Group C, per MIL-STD-883, Method 5005 is performed every ninety days for each slash sheet.

In addition to the common specs used throughout the industry for processing and testing, JAN Qualified products also possess a requirement for a standard marking to be used throughout the I.C. industry. Table 1 explains JAN part numbers and an example, using a 5400 device, illustrates how this marking appears on a circuit package.

2) JAN Processed:

This option is extremely useful when the reliability and screening of a JAN device is required, however, Signetics is not listed on the QPL for the product needed. Processing is performed to MIL-STD-883, Method 5004 and product is 100% electrically tested to the appropriate JAN slash sheet.

MARKING:

M38510/ (applicable slash sheet, device class, package symbolization for a JAN processed 5400F device would appear as follows:

S AAAA ← Date Code
M38510/
00104
BCB

Do Not confuse this marking with a fully qualified JAN device. This is a JAN equivalent. (Note: Differences between package marking - "J" is missing from the M38510 and manufacturer's code is not symboled on the package).

Group B and C data for JAN processed and the other MILrel processing levels which follow, consists of Group B testing performed per MIL-STD-883, Method 5005, every one hundred eighty days minimum by package type and Group C per MIL-STD-883, Method 5005, is run every ninety days on each wafer processing family.

3) JAN Rel:

Processing to this option is ideal when no JAN slash sheets are released on devices required. Product is processed to MIL-STD-883, Method 5004, and is 100% electrically tested to industry data sheets. (Specific parameters required by a customer may also be included).

MARKING:

M38510/ (industry part number, device class, case outline and lead finish designators.) Package symbolization for a 5400F device ordered with JAN Rel processing would appear as follows:

S AAAA ← Date Code
M38510/
5400 BCB

4) /883B:

This is a lower priced version of the JAN Rel option described above. Processing is identical with the only exceptions being that DC electrical testing over the temperature range and AC electrical testing at room temperature are performed on a sample basis instead of 100%.

MARKING:

Signetics part number and package /883B (or /883C for Class C devices). Package symbolization for a 5400F processed to /883B criteria would appear as follows:

S AAAA ← Date Code
S5400F
/883B

5) Mil Temp.:

If you need a Military temp. range device, but do not require all the high reliability screening performed in the other proccessing options, our Mil-Temp. product is ideal. Mil-Temp parts are the standard full Mil-Temperature range product guaranteed to a 1% AQL to the Signetics data sheet parameters.

MARKING:

Symbolization on these devices consist of the Signetics part number and package only. Again using our 5400F as an example, package marking for a Mil-Temp. device would appear as follows:

S AAAA ← Date Code
S5400F

Table 1
JAN 38510 PART NUMBERS — WHAT THEY MEAN

The following chart is offered for your reference to help take some of the mystery out of JAN part number marking. For an example, we will take the marking for a 5400F processed to JAN and explain its meaning, as well as other options.

JM38510 /001 04 B C B

MILITARY DESIGNATOR	DETAIL SPECIFICATION	DEVICE TYPE	DEVICE CLASS	CASE OUTLINE	LEAD FINISH
Calls Out MIL-M-38510 JAN IC The "J" in the marking is very important. If it's not there it's not a JAN DEVICE. *DO NOT* be confused by JAN equivalents marked M38510.	Refers to detail Slash sheet spec 001,002,003----- A Slash sheet detail spec will usually represent a family of devices with similar functions. i.e. the /001 detail spec represents many positive NAND gates such as the 5400, 5401, 5403, 5410, 5420, & 5430 etc. The /002 detail spec on the other hand represents many flip flop functions such as the 5472, 5473, 54107, 5476, 5474, 5470 and so on for the rest of the slash sheets.	Refers to a specific Part Type under the detail spec. This, plus the detail spec # will denote a part type. i.e.: detail dev. generic spec + type = type 001 01 = 5430 001 02 = 5420 001 03 = 5410 **001 04 = 5400** detail dev. generic spec + type = type 002 01 = 5472 002 02 = 5473 002 03 = 54107 and so on for the rest of the slash sheets.	Device Class Calls out Processing to either Class A **B** or C of MIL-STD-883	This Code denotes the package i.e: A = ¼" x ⅛" flat pak B = ¼" x ⅛" flat pak **C = ¼" x ¾" 14 PIN dual-in-line** D = ¼" x ⅜" flat pak 14 pin E = ¼" x ¾" 16 PIN dual-in-line F = ¼" x ⅜" flat pak 16 pin G = 8 lead metal can H = ¼" x ¼" 10 PIN flat pak I = ⅜" x ½" 10 lead metal can J = ½" x 1¼" 24 pin dual-in-line K = ⅜" x ½" 24 pin flat pak L = ⅜" x ½" 24 PIN flat pak Z = ¼" x ⅜" 24 PIN flat pak	A = Kovar or alloy 42 with Hot solder Dip **B = Kovar or alloy 42 with tin plate** C = Kovar or alloy with gold plate

Actual Marking for our 5400F as it appears on the device.

S AAAA ← Date Code
JM38510
00104
BCB
DKB ← Signetics manufacturers code (Per Mil-M-38510)

Table 2
MIL-M-38510/MIL-STD-883 PROCESSING LEVELS

TEST	MIL-STD-883 METHOD	CLASS A	CLASS B	CLASS C
Internal Visual (Preseal)	2010.2	Cond A	Cond B	Cond B
Stabilization Bake	1008.1 (24 hr min.)	Cond C	Cond C	Cond C
Temperature Cycling	1010.1	Cond C	Cond C (note 1)	Cond C (note 1)
Constant Acceleration	2001.1	Cond E Y2 then Y1 plane	Cond E Y1 plane	Cond E Y1 plane
Seal A. Fine Leak B. Gross Leak	1014.1 (Note 3)	 Cond A or B Cond C2	 Cond A or B Cond C2	 Cond A or B Cond C2
Visual inspection	1010.1 (note 2)	Required	Required	Required
Critical Electrical Parameters (pre burn-in)	Subgroup A-1 (note 4)	Read and Record	Optional	Not Required
Burn-in Test	1015.1, $T_A=+125°C$	240 hours min.	160 hours min.	Not Required
Critical Electrical Parameters (post Burn-in)	Subgroup A-1 (note 4)	Read and Record	Not Required	Not Required
Signetics FAILURE CRITERIA		PDA 5%	PDA 10%	Not Required
Reverse Bias Burn in (note 7)	1015.1, $T_A=+150°C$ t = 72 hours	Cond A or C	Not Required	Not Required
Critical Electrical Parameters (post burn-in)	Subgroup A-1 (note 4)	Read and Record	Required	Not Required
Final Electrical Test Parameters	Perform 100% go-no-go measurements of subgroup A parameters (note 4)	Subgroups A1, A2, A3, A9, Functional tests, truth table when applicable (A7)	Subgroups A1, A2, A3, A9, Functional tests, truth table when applicable (A7)	Subgroup A1, functional tests, truth table when applicable (A7)
Radiographic Inspection	2012.1	Yes	Not Required	Not Required
Quality Conformance Inspection (note 9)	5005	Class A	Class B	Class C
External Visual	2009.1	Yes	Yes	Yes

NOTES:
(1) Class B and Class C may be subjected to thermal shock, Method 1011.1, Cond. A, as an alternate.
(2) The visual examination of Method 1010.1 may be performed at the end of each environmental screen test or at the end of the screening sequence.
(3) Test is not applicable to solid molded devices.
(4) Detailed tests, conditions, and limits applicable to each subgroup are given in the Signetics data sheet ELECTRICAL CHARACTERISTICS table. See Table 3 for the corresponding Group A tests of MIL-STD-883.
(5) All test equipment calibrated to meet requirements of MIL-Q-9858 and MIL-C-45662.
(6) The individual MIL-STD-883 Test Methods are, in many cases, designed to "stand alone" as a sole screen or sole Group B environmental sampling test. But since 5004.3 specifies a screening series or flow, some of the measurements, etc., specified in an individual Test Method are not intended to be performed in the screening series, provided they are performed at the conclusion of the screening sequence.
(7) Required only when specified in the applicable procurement document. For this stress, as many input and output junctions as possible are reversed biased.
(8) Group A per 5005. Generic Data available for Groups B and C on Devices produced to Class B and C. (See MILrel Generic Data).

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Table 3
MIL-STD-883 GROUP A ELECTRICAL TESTS

MIL-STD-883A GROUP A SUBGROUP	TEST DESCRIPTION
A1	Static tests at 25°C
A2	Static tests at maximum rated operating temperature
A3	Static tests at minimum rated operating temperature
A4	Dynamic tests at 25°C*
A5	Dynamic tests at maximum rated operating temperature*
A6	Dynamic tests at minimum rated operating temperature*
A7	Functional tests at 25°C
A8	Functional tests at maximum and minimum rated operating temperatures
A9	Switching tests at 25°C
A10	Switching tests at maximum rated operating temperature
A11	Switching tests at minimum rated operating temperature

*Applicable only to Signetics Analog Products

MILrel GENERIC DATA

MILrel GENERIC DATA

Signetics has a new program for those customers who require qualification data on their products. This program allows our customers to obtain reliability information without the necessity of running Groups B, C and D inspections for their particular purchase order. It provides for the customer something that has not been readily available before in the semiconductor industry in that all Mil-Rel Generic Data is controlled and audited by both Government Inspection and Quality Assurance.

Signetics MILrel Generic Data is generated by the Military Products Division. The data is compiled from 1) Jan qualification lots, and 2) Data generated by qualification lots run for other reliability programs.

A MILrel Generic family is defined as consisting of *die function* and *package type* families.

A Generic die function lot qualifies a ninety day manufacturing period and a representative package type qualifies a one hundred and eighty day manufacturing period.

MILrel Generatic Data:

- Allows our customers to qualify Signetics products based on existing qualification data performed at Signetics.
- Allows our customers to reduce costs and improve deliveries.
- Provides assurance that all Signetics die function families and packages meet JAN and customer reliability requirements.
- Provides an attributes summary to the customer backed by lot identity and traceabillity.

When ordering just ask for "Signetics MILrel Generic Data".

The following is a list of products, packages and processing levels available in full Military temperature range. Data sheet pages for each product are included in the last column for your easy reference.

DEVICE	JAN M38510 SLASH SHEET	QPL STATUS JAN QUALIFIED +		JAN PROCESSED		JAN REL/883 MIL TEMP		DATA SHEET REF PAGE
		DIP	FLAT PACK	DIP	FLAT PACK	DIP	FLAT PACK	
Logic								
5400	/00104	I	I	F	W	F	W	53
5401	/00107	I	I	F	W	F	W	53
5402	/00401	I	I	F	W	F	W	54
5403	/00109	I	—	F	—	F	—	55
5404	/00105	I	I	F	W	F	W	55
5405	/00108	I	I	F	W	F	W	56
5406	/00801	Coming	—	F	W	F	W	56
5407	/00803	Coming	—	F	W	F	W	57
5408	/01601	I	I	F	W	F	W	57
5409	/01602	I	I	F	W	F	W	58
5410	/00103	I	I	F	W	F	W	58
5411	None	—	—	—	—	F	W	59
5412	/00106	—	—	—	—	—	—	59
5413	/15101	Coming	—	Coming	—	F	W	60
5414	/15102	Coming	—	Coming	—	F	W	60
5416	/00802	Coming	—	F	W	F	W	62
5417	/00804	Coming	—	F	W	F	W	62
5420	/00102	I	I	F	W	F	W	62
5421	None	—	—	—	—	F	W	63
5423	/00402	—	—	—	—	—	—	—
5425	/00403	—	—	—	—	—	—	—
5426	/00805	II	—	F	—	F	—	64
5427	/00404	Coming		F	W	F	W	65
5428	None	—	—	—	—	F	W	65
5430	/00101	I	I	F	W	F	W	66
5432	None	—	—	—	—	F	W	66
5433	None	—	—	—	—	F	W	67
5437	/00302	I	I	F	W	F	W	67
5438	/00303	I	I	F	W	F	W	68
5439	None	—	—	—	—	F	W	68
5440	/00301	I	I	F	W	F	W	69
5442	/01001	I	I	F	W	F	W	69
5443	/01002	I	I	F	W	F	W	70
5444	/01003	I	I	F	W	F	W	71
5445	/01004	Coming	—	F	W	F	W	72
5446	/01006	Coming	—	Coming	—	F	W	73
5447	/01007	Coming	—	Coming	—	F	W	74
5448	/01008	Coming	—	Coming	—	F	W	76
5449	/01009	—	—	—	—	—	—	—
5450	/00501	I	I	F	W	F	W	77
5451	/00502	I	I	F	W	F	W	77
5453	/00503	I	I	F	W	F	W	79
5454	/00504	I	I	F	W	F	W	80
5460	None	—	—	—	—	F	W	81
5470	/00206	I	I	F	W	F	W	84
5472	/00201	I	I	F	W	F	W	85
5473	/00202	I	I	F	W	F	W	86
5474	/00205	I	I	F	W	F	W	87
5475	/01501	I	I	F	W	F	W	88
5476	/00204	I	I	F	W	F	W	90
5477	/01502	—	I	—	W	—	W	91
5479	/00207	—	—	—	—	—	—	91

+ Per QPL -38510-22 Dated 12 Jan 76.

DEVICE	JAN M38510 SLASH SHEET	QPL STATUS JAN QUALIFIED +		JAN PROCESSED		JAN REL/883 MIL TEMP		DATA SHEET REF PAGE
		DIP	FLAT PACK	DIP	FLAT PACK	DIP	FLAT PACK	
5480	None	—	—	—	—	F	W	92
5482	/00601	—	—	—	—	—	—	—
5483	/00602	I	I	F	W	F	W	93
5485	/15001	II	II	F	W	F	W	95
5486	/00701	I	I	F	W	F	W	97
5490	/01307	Coming	—	Coming	—	F	W	100
5491	None	—	—	—	—	F	W	102
5492	/01301	Coming	—	Coming	—	Coming	—	102
5493	/01302	I	Coming	F	W	F	W	104
5494	None	—	—	—	—	F	W	106
5495	/00901	I	—	F	—	F	—	106
5496	/00902	I	I	F	W	F	W	108
54100	None	—	—	—	—	F	W	111
54107	/00203	I	—	F	—	F	—	116
54109	None	—	—	—	—	F	W	118
54116	/01503	Coming	—	I	—	I	—	123
54121	/01201	I	I	F	W	F	W	124
54122	/01202	—	—	—	—	—	—	128
54123	/01203	I	I	F	W	F	W	129
54125	/15301	Coming	—	Coming	—	F	W	130
54126	/15302	Coming	—	Coming	—	F	W	131
54128	None	—	—	—	—	F	W	131
54132	/15103	Coming	—	Coming	—	F	W	132
54145	/01005	Coming	—	Coming	—	F	W	136
54147	*/15601	Coming	—	Coming	—	F	W	137
54148	*/15602	Coming	—	Coming	—	F	W	138
54150	/01401	II	—	I	Q	I	Q	140
54151	/01406	Coming	—	F	W	F	W	142
54152	None	—	—	—	—	F	W	143
54153	/01403	I	I	F	W	F	W	145
54154	*/15201	Coming	—	—	—	I	Q	146
54155	*/15202	Coming	—	—	—	F	W	147
54156	*/15203	Coming	—	—	—	F	W	148
54157	/01405	I	I	F	W	F	W	149
54158	None	—	—	—	—	F	W	150
54160	/01303	I	I	F	W	F	W	152
54161	/01306	I	I	F	W	F	W	153
54162	/01305	I	I	F	W	F	W	156
54163	/01304	I	I	F	W	F	W	160
54164	/00903	I	—	F	—	F	—	162
54165	/00904	Coming	—	Coming	—	F	W	164
54166	None	—	—	—	—	F	W	167
54170	*/01801	—	—	—	—	F	—	169
54174	/01701	I	I	F	W	F	W	174
54175	/01702	II	II	F	W	F	W	175
54180	/01901	II	II	F	W	F	W	178
54181	/01101	Coming	—	I	—	I	—	178
54182	/01102	II	II	F	W	F	W	183
54190	None	—	—	—	—	F	W	184
54191	None	—	—	—	—	F	W	187
54192	/01308	Coming	—	Coming	—	F	W	190
54193	/01309	Coming	—	Coming	—	F	W	192
54194	/00905	II	II	F	W	F	W	196
54195	/00906	II	II	F	W	F	W	197
54198	None	—	—	—	—	I	Q	203
54199	None	—	—	—	—	I	Q	206
54279	None	—	—	—	—	F	W	221

*Slash sheets not released as of date of this publication.

+ Per QPL -38510-22 Dated 12 Jan 76.

DEVICE	JAN M38510 SLASH SHEET	QPL STATUS JAN QUALIFIED +		JAN PROCESSED		JAN REL/883 MIL TEMP		DATA SHEET REF PAGE
		DIP	FLAT PACK	DIP	FLAT PACK	DIP	FLAT PACK	
54298	None	—	—	—	—	F	W	228
54H00	/02304	I	I	F	W	F	W	53
54H01	/02306	I	Coming	F	W	F	W	54
54H04	/02305	I	I	F	W	F	W	55
54H05	None	—	—	—	—	F	W	56
54H08	/15501	Coming	—	F	—	F	W	57
54H10	/02303	I	I	F	W	F	W	58
54H11	/15502	Coming	—	F	—	F	W	59
54H20	/02302	I	I	F	W	F	W	62
54H21	/15503	Coming	—	F	—	F	W	63
54H22	/02307	I	Coming	F	W	F	W	64
54H30	/02301	I	I	F	W	F	W	66
54H40	/02401	Coming	II	F	W	F	W	69
54H50	/04001	I	I	F	W	F	W	77
54H51	/04002	I	I	F	W	F	W	77
54H52	None	—	—	—	—	F	W	78
54H53	/04003	I	I	F	W	F	W	79
54H54	/04004	I	I	F	W	F	W	80
54H55	/04005	I	I	F	W	F	W	81
54H60	None	—	—	—	—	F	W	82
54H61	None	—	—	—	—	F	W	82
54H62	None	—	—	—	—	F	W	82
54H71	None	—	—	—	—	F	W	84
54H72	/02201	I	I	F	W	F	W	85
54H73	/02202	I	I	F	W	F	W	86
54H74	/02203	I	I	F	W	F	W	87
54H76	/02204	I	I	F	W	F	W	90
54H101	/02205	II	II	F	W	F	W	111
54H102	None	—	—	—	—	F	W	112
54H103	/02206	II	II	F	W	F	W	114
54H106	None	—	—	—	—	F	W	115
54H108	None	—	—	—	—	F	W	117
54LS00	/30001	II	II	F	W	F	W	53
54LS01	None	—	—	—	—	F	W	54
54LS02	+/30301	Coming	—	Coming	—	F	W	54
54LS03	/30002	II	II	F	W	F	W	55
54LS04	/30003	II	II	F	W	F	W	55
54LS05	/30004	II	II	F	W	F	W	56
54LS08	*/31004	Coming	—	Coming	—	F	W	57
54LS09	None	—	—	—	—	F	W	58
54LS10	/30005	II	II	F	W	F	W	58
54LS11	*/31001	Coming	—	Coming	—	F	W	59
54LS12	/30006	II	II	F	W	F	W	59
54LS13	None	—	—	—	—	F	W	60
54LS14	None	—	—	—	—	F	W	60
54LS15	*/31002	Coming	—	Coming	—	F	W	61
54LS20	/30007	II	II	F	W	F	W	62
54LS21	*/31003	Coming	—	Coming	—	F	W	63
54LS22	/30008	II	II	F	W	F	W	64
54LS26	None	—	—	—	—	F	W	64
54LS27	*/30302	Coming	—	Coming	—	F	W	65
54LS28	None	—	—	—	—	F	W	65
54LS30	/30009	II	II	F	W	F	W	66
54LS32	*/30501	Coming	—	Coming	—	F	W	66
54LS33	None	—	—	—	—	F	W	67
54LS37	*/30202	Coming	—	Coming	—	F	W	67

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DEVICE	JAN M38510 SLASH SHEET	QPL STATUS JAN QUALIFIED +		JAN PROCESSED		JAN REL/883 MIL TEMP		DATA SHEET REF PAGE
		DIP	FLAT PACK	DIP	FLAT PACK	DIP	FLAT PACK	
54LS38	*/30203	Coming	—	Coming	—	F	W	68
54LS40	*/30201	Coming	—	Coming	—	F	W	69
54LS42	None	—	—	—	—	Coming	—	69
54LS51	*/30401	Coming	—	Coming	—	F	W	77
54LS54	*/30402	Coming	—	Coming	—	F	W	80
54LS55	None	—	—	—	—	F	W	81
54LS73	None	—	—	—	—	F	W	86
54LS74	None	—	—	—	—	F	W	87
54LS75	None	—	—	—	—	F	W	88
54LS76	None	—	—	—	—	F	W	90
54LS78	None	—	—	—	—	F	W	91
54LS83A	None	—	—	—	—	Coming	—	93
54LS85	*/31101	Coming	—	Coming	—	Coming	—	95
54LS86	*/30502	Coming	—	Coming	—	F	W	98
54LS90	None	—	—	—	—	F	W	100
54LS92	None	—	—	—	—	F	W	102
54LS93	None	—	—	—	—	F	W	104
54LS95B	*/30603	Coming	—	Coming	—	Coming	—	106
54LS96	*/30604	Coming	—	Coming	—	Coming	—	108
54LS107	None	—	—	—	—	F	W	116
54LS109	None	—	—	—	—	F	W	118
54LS112	None	—	—	—	—	F	W	119
54LS113	None	—	—	—	—	F	W	121
54LS114	None	—	—	—	—	F	W	122
54LS122	None	—	—	—	—	Coming	Coming	128
54LS123	None	—	—	—	—	Coming	Coming	129
54LS125	None	—	—	—	—	Coming		130
54LS126	None	—	—	—	—	Coming	Coming	131
54LS132	None	—	—	—	—	F	W	132
54LS136	None	—	—	—	—	F	W	134
54LS138	None	—	—	—	—	F	W	134
54LS139	None	—	—	—	—	F	W	135
54LS145	None	—	—	—	—	Coming		136
54LS151	None	—	—	—	—	F	W	142
54LS153	None	—	—	—	—	F	W	145
54LS154	None	—	—	—	—	Coming		146
54LS157	None	—	—	—	—	F	W	149
54LS158	None	—	—	—	—	F	W	150
54LS161	None	—	—	—	—	Coming		153
54LS163	None	—	—	—	—	F	W	160
54LS164	*/30605	—	—	—	—	F	W	162
54LS170	None	—	—	—	—	F	W	169
54LS173	None	—	—	—	—	Coming		—
54LS174	None	—	—	—	—	F	W	174
54LS175	None	—	—	—	—	F	W	175
54LS181	*/30801	Coming	—	Coming	—	I	Q	178
54LS190	None	—	—	—	—	F	W	184
54LS191	None	—	—	—	—	F	W	187
54LS192	None	—	—	—	—	F	W	190
54LS193	None	—	—	—	—	F	W	192
54LS194	*/30601	Coming	—	Coming	—	Coming	—	195
54LS195	*/30602	Coming	—	Coming	—	Coming	—	197
54LS196	None	—	—	—	—	Coming	—	200
54LS197	None	—	—	—	—	Coming	—	201
54LS221	None	—	—	—	—	F	W	210
54LS251	None	—	—	—	—	F	W	212

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		DIP	FLAT PACK	DIP	FLAT PACK	DIP	FLAT PACK	
54LS253	None	—	—	—	—	F	W	214
54LS257	None	—	—	—	—	Coming	—	215
54LS258	None	—	—	—	—	Coming	—	216
54LS260	None	—	—	—	—	F	W	217
54LS261	None	—	—	—	—	F	W	218
54LS266	*/30303	Coming		Coming		F	W	220
54LS279	None	—	—	—	—	Coming	—	221
54LS283	None	—	—	—	—	Coming	—	222
54LS290	None	—	—	—	—	Coming	—	223
54LS293	None	—	—	—	—	Coming	—	225
54LS365	None	—	—	—	—	Coming	—	—
54LS366	None	—	—	—	—	Coming	—	—
54LS367	None	—	—	—	—	Coming	—	—
54LS368	None	—	—	—	—	Coming	—	—
54LS375	None	—	—	—	—	Coming	—	—
54LS386	None	—	—	—	—	F	W	230
54LS670	None	—	—	—	—	F	W	230
54S00	/07001	II	II	F	W	F	W	53
54S02	/07301	Coming	—	Coming	—	F	W	54
54S03	/07002	Coming	—	F	W	F	W	55
54S04	/07003	Coming	—	F	W	F	W	55
54S05	/07004	Coming	—	F	W	F	W	56
54S08	None	—	—	—	—	F	W	57
54S09	None	—	—	—	—	F	W	58
54S10	/07005	Coming	—	F	W	F	W	58
54S11	*/08001	Coming	—	Coming	—	F	W	59
54S15	*/08002	Coming	—	Coming	—	F	W	61
54S20	/07006	Coming	—	F	W	F	W	62
54S22	/07007	Coming	—	F	W	F	W	64
54S30	/07008	—	—	—	—	—	—	66
54S32	None	—	—	—	—	F	W	66
54S37	None	—	—	—	—	F	W	67
54S38	None	—	—	—	—	—	—	68
54S40	/07201	Coming	—	Coming		F	W	69
54S51	/07401	Coming	—	F	W	F	W	77
54S64	/07402	Coming	—	F	W	F	W	80
54S65	/07403	Coming	—	F	W	F	W	83
54S74	/07101	Coming	—	F	W	F	W	87
54S85	*/08201	Coming	—	Coming	—	F	None	95
54S86	/07501	Coming	—	Coming	—	F	W	98
54S112	/07102	Coming	—	F	W	F	W	119
54S113	/07103	Coming	—	F	W	F	W	121
54S114	/07104	Coming	—	F	W	F	W	122
54S133	/07009	Coming	—	F	W	F	W	132
54S134	/07010	Coming	—	F	W	F	W	133
54S135	/07502	—	—	F	—	—	—	133
54S138	*/07701	—	—	—	—	—	—	134
54S139	*/07702	—	—	—	—	—	—	135
54S140	/08101	Coming	—	Coming	—	F	W	—
54S151	*/07901	Coming	—	Coming	—	F	W	142
54S153	*/07902	Coming	—	Coming	—	F	W	145
54S157	*/07903	Coming	—	Coming	—	F	W	149
54S158	*/07904	—	—	—	—	—	—	150
54S174	/07105	—	—	—	—	—	None	174

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DEVICE	JAN M38510 SLASH SHEET	QPL STATUS JAN QUALIFIED + DIP	QPL STATUS JAN QUALIFIED + FLAT PACK	JAN PROCESSED DIP	JAN PROCESSED FLAT PACK	JAN REL/883 MIL TEMP DIP	JAN REL/883 MIL TEMP FLAT PACK	DATA SHEET REF PAGE
54S175	/07106	—	—	—	—	—	None	—
54S181	*/07801	Coming	—	Coming	—	I	None	—
54S182	*/07802	—	—	—	—	F	None	—
54S194	*/07601	—	—	—	—	—	None	—
54S195	*/07602	—	—	—	—	—	—	—
54S251	*/07905	—	—	—	—	Coming	—	—
54S253	None	—	—	—	—	F	W	—
54S257	*/07906	—	—	—	—	Coming	None	—
54S258	*/07907	Coming	—	Coming	—	F	None	—
54S260	None	—	—	—	—	F	W	—
54S280	*/07703	Coming	—	Coming	—	Coming	—	—
8200	None	—	—	—	—	I	Q	255
8201	None	—	—	—	—	I	Q	255
8202	None	—	—	—	—	I	Q	255
8203	None	—	—	—	—	I	Q	255
8230	None	—	—	—	—	F	W	259
8231	None	—	—	—	—	F	W	259
8232	None	—	—	—	—	F	W	259
8233	None	—	—	—	—	F	W	262
8234	None	—	—	—	—	F	W	262
8235	None	—	—	—	—	F	W	262
8241	None	—	—	—	—	F	W	264
8242	None	—	—	—	—	F	W	264
8243	None	—	—	—	—	I	—	247
8250	*/15204	Coming	—	Coming	—	F	W	271
8251	*/15205	Coming	—	Coming	—	F	W	271
8252	*/15206	Coming	—	Coming	—	F	W	271
8260	None	—	—	—	—	I	Q	275
8261	None	—	—	—	—	F	W	278
8262	None	—	—	—	—	F	W	280
8263	None	—	—	—	—	I	Q	282
8264	None	—	—	—	—	I	Q	282
8266	None	—	—	—	—	F	W	285
8267	None	—	—	—	—	F	W	285
8269	None	—	—	—	—	F	W	291
8270	None	—	—	—	—	F	W	292
8271	None	—	—	—	—	F	W	292
8273	None	—	—	—	—	F	W	297
8274	None	—	—	—	—	F	W	298
8275	None	—	—	—	—	F	W	300
8280	None	—	—	—	—	F	W	306
8281	None	—	—	—	—	F	W	306
8284	None	—	—	—	—	I	Q	318
8285	None	—	—	—	—	I	Q	318
8288	None	—	—	—	—	F	W	321
8290 (54196)	None	—	—	—	—	F	W	323
8291 (54197)	None	—	—	—	—	F	W	323
8292	None	—	—	—	—	F	W	328
8293	None	—	—	—	—	F	W	330
8808	None	—	—	—	—	F	W	—
8815	None	—	—	—	—	F	W	—
8816	None	—	—	—	—	F	W	—
8819	None	—	—	—	—	F	W	—
8822	None	—	—	—	—	F	W	—
8824	None	—	—	—	—	F	W	—
8825	None	—	—	—	—	F	W	—

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DEVICE	JAN M38510 SLASH SHEET	QPL STATUS JAN QUALIFIED + DIP	QPL STATUS JAN QUALIFIED + FLAT PACK	JAN PROCESSED DIP	JAN PROCESSED FLAT PACK	JAN REL/883 MIL TEMP DIP	JAN REL/883 MIL TEMP FLAT PACK	DATA SHEET REF PAGE
8828	None	—	—	—	—	F	W	—
8829	None	—	—	—	—	F	W	—
8840	None	—	—	—	—	F	W	—
8848	None	—	—	—	—	F	W	—
8855	None	—	—	—	—	F	W	—
8859	None	—	—	—	—	I	Q	—
8870	None	—	—	—	—	F	W	—
8875	None	—	—	—	—	F	W	—
8879	None	—	—	—	—	F	W	—
8880	None	—	—	—	—	F	W	107
8881	None	—	—	—	—	F	W	—
8885	None	—	—	—	—	F	W	—
8889	None	—	—	—	—	F	W	—
8890	None	—	—	—	—	F	W	—
8891	None	—	—	—	—	F	W	—
8H16	None	—	—	—	—	F	W	—
8H21	None	—	—	—	—	F	W	—
8H22	None	—	—	—	—	F	W	—
8H70	None	—	—	—	—	F	W	—
8H80	None	—	—	—	—	F	W	—
8H90	None	—	—	—	—	F	W	—
8T01	None	—	—	—	—	F	W	—
8T04	None	—	—	—	—	F	W	17
8T05	None	—	—	—	—	F	W	21
8T06	None	—	—	—	—	F	W	23
8T09	None	—	—	—	—	F	W	26
8T10	None	—	—	—	—	F	W	30
8T13	None	—	—	—	—	F	W	33
8T14	None	—	—	—	—	F	W	35
8T18	None	—	—	—	—	F	W	43
8T37	None	—	—	—	—	F	W	89
8T80	None	—	—	—	—	F	W	83
8T90	None	—	—	—	—	F	W	84
9300	/15901	Coming	—	Coming	—	F	W	232
9308 (54116)	/01503	Coming	—	I	—	I	—	—
9309	/01404	I	I	F	W	F	W	—
9310	None	—	—	—	—	F	W	—
9316	None	—	—	—	—	F	W	—
9322 (54157)	/01405	I	I	F	W	F	W	—
9324	/15002	—	—	—	—	—	—	—
9602	None	—	—	—	—	F	W	—
MOS								
2102-4	None	—	—	—	—	F	I	—
2102-6	None	—	—	—	—	F	I	—
LINEAR								
LM101	None	—	—	—	—	F	T	56
LM101A	/10103	Coming	—	Coming	—	F	T	60
LM107	None	—	—	—	—	F	T	69
LM108	None	—	—	—	—	F	T	72
LM108A	/10104	—	—	—	—	F	T	80

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MILrel

DEVICE	JAN M38510 SLASH SHEET	QPL STATUS JAN QUALIFIED +		JAN PROCESSED		JAN REL/883 MIL TEMP		DATA SHEET REF PAGE
		DIP	FLAT PACK	DIP	FLAT PACK	DIP	FLAT PACK	
SE510	None	—	—	—	—	F	—	106
SE511	None	—	—	—	—	F	—	107
SE555	*/10901	Coming	—	Coming	—	F	T	158
SE556	*/10902	Coming	—	Coming	—	F	—	162
SE567	None	—	—	—	—	F	T	282
μA709	None	—	—	—	—	F	T	89
μA709A	None	—	—	—	—	F	T	—
μA710	/10301	—	—	—	—	F	T	202
μA711	/10302	—	—	—	—	F	K	203
μA723	/10201	—	—	—	—	F	L	117
μA733	/10301	—	—	—	—	F	K	172
μA741	/10101	Coming	—	Coming	—	F	T	93
μA747	/10102	Coming	—	Coming	—	F	K	96
μA748	None	—	—	—	—	F	T	101
MC1558	None	—	—	—	—	F	T	87

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BIPOLAR MEMORIES

DEVICE	JAN M38510 SLASH SHEET	QPL STATUS JAN QUALIFIED +		JAN PROCESSED		JAN REL/883 MIL TEMP		DATA SHEET REF PAGE
		DIP	FLAT PACK	DIP	FLAT PACK	DIP	FLAT PACK	
3101A	None	—	—	—	—	F	—	10
54S200	None	—	—	—	—	F	—	208
54S201	None	—	—	—	—	F	—	209
54S301	None	—	—	—	—	F	—	233
82S09	None	—	—	—	—	I	—	19
82S10	None	—	—	—	—	F	—	20
82S11	None	—	—	—	—	F	—	20
82S16	None	—	—	—	—	F	—	16
82S17	None	—	—	—	—	F	—	16
82S23	None	—	—	—	—	F	—	33
82S25	None	—	—	—	—	F	—	20
82S100	None	—	—	—	—	F	—	59
82S101	None	—	—	—	—	F	—	59
82S114	None	—	—	—	—	I	—	49
82S115	None	—	—	—	—	—	—	49
82S123	None	—	—	—	—	F	—	33
82S126	*/00201	Coming	—	Coming	—	F	—	43
82S129	*/00202	Coming	—	Coming	—	F	—	43
82S130	None	—	—	—	—	F	—	46
82S131	None	—	—	—	—	F	—	46
82S215	None	—	—	—	—	I	—	49
82S226	None	—	—	—	—	F	—	25
82S229	None	—	—	—	—	F	—	25
82S230	None	—	—	—	—	Coming	—	27
82S231	None	—	—	—	—	Coming	—	27

All MILrel products are also available to die form.
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CROSS REFERENCE
JAN PART NUMBERS TO INDUSTRY PART TYPE

JAN /NO.	PART TYPE	JAN /NO.	PART TYPE	JAN /NO.	PART TYPE	JAN/NO.	PART TYPE
M38510/ 00101	5430	M38510/ 01202	54122	M38510/ 02503	54L193	M38510/ 05302	4019A
00102	5420	01203	54123	02504	93L10	05303	4030A
00103	5410	01301	5492	02505	93L16	05401	4008A
00104	5400	01302	5493	02601	54L86	05501	4009A
00105	5404	01303	54160	02701	54L02	05502	4010A
00106	5412	01304	54163	02801	54L95	05503	4049A
00107	5401	01305	54162	02802	54L164	05504	4050A
00108	5405	01306	54161	02803	93L28	05505	4041A
00109	5403	01307	5490	02804	93L00	05601	4017A
00201	5472	01308	54192	02805	76L70	05602	4018A
00202	5473	01309	54193	02806	54L91	05603	4020A
00203	54107	01401	54150	02901	54L42	05604	4022A
00204	5476	01402	9312	02902	54L43	05605	4024A
00205	5474	01403	54153	02903	54L44	05701	4006A
00206	5470	01404	9309	02904	54L46	05702	4014A
00207	5479	01405	54157 (9322)	02905	54L47	05703	4015A
00301	5440	01406	54151	02906	76L42A	05704	4021A
00302	5437	01501	5475	02907	93L01	05705	4031A
00303	5438	01502	5477	03001	15930	05801	4016A
00401	5402	01503	54116 (9308)	03002	15935	06001	10501
00402	5423	01504	9314	03003	15936	06002	10502
00403	5425	01601	5408	03004	15946	06003	10505
00404	5427	01602	5409	03005	15962	06004	10506
00501	5450	01701	54174	03101	932	06005	10507
00502	5451	01702	54175	03102	944	06006	10509
00503	5453	01801	54170	03103	957	06101	10531
00504	5454	01901	54180	03104	958	06102	10631
00601	5482	02001	54L30	03105	933	06103	10576
00602	5483	02002	54L20	03201	951	06104	10535
00603	9304	02003	54L10	03301	945	07001	54S00
00701	5486	02004	54L00	03302	948	07002	54S03
00801	5406	02005	54L04	03303	950	07003	54S04
00802	5416	02006	54L01/	03304	9093	07004	54S05
00803	5407		54L03	04001	54H50	07005	54S10
00804	5417	02101	54L71	04002	54H51	07006	54S20
00805	5426	02102	54L72	04003	54H53	07007	54S22
00901	5495	02103	54L73	04004	54H54	07008	54S30
00902	5496	02104	54L78	04005	54H55	07009	54S133
00903	54164	02105	54L74	04101	54L51	07010	54S134
00904	54165	02201	54H72	04102	54L54	07101	54S74
00905	54194	02202	54H73	04103	54L55	07102	54S112
00906	54195	02203	54H74	04104	54L54	07103	54S113
01001	5442	02204	54H76	04201	54L121	07104	54S114
01002	5443	02205	54H101	04202	54L122	07105	54S174
01003	5444	02206	54H103	05001	54011A	07106	54S175
01004	5445	02301	54H30	05002	4012A	07201	54S40
01005	54145	02302	54H20	05003	4023A	07301	54S02
01006	5446	02303	54H10	05101	4013A	07401	54S51
01007	5447	02305	54H04	05102	4027A	07402	54S64
01008	5448	02306	54H01	05201	4000A	07403	54S65
01009	5449	02307	54H22	05202	4001A	07501	54S86
01101	54181	02401	54H40	05203	4002A	07502	54S135
01102	54182 (9342)	02501	54L90	05204	4025A	07601	54S194
01201	54121	02502	54L93	05301	4007A	07602	54S195

CROSS REFERENCE
JAN PART NUMBERS TO INDUSTRY PART TYPE

JAN/NO.	PART TYPE	JAN/NO.	PART TYPE	JAN/NO.	PART TYPE	JAN/NO.	PART TYPE
M38510/ 07701	54S138	M38510/ 10404	55115	M38510/ 15602	54148	M38510/ 30003	54LS04
07702	54S139	10405	55113	15603	9318	30004	54LS05
07703	54S280	10406*	7831	15701	9338	30005	54LS10
07801	54S181	10407*	7832	15801	9321	30006	54LS12
07802	54SS182	10501	μA733	15802	9317	30007	54LS20
07901	54S12151	10601	LM102	15901	9300	30008	54LS22
07902	54S153	10602	LM110	15902	9328	30009	54LS30
07903	54S157	10701*	μA7805	16001	9334	30201*	54LS40
07904	54S158	10702*	μA7812	20101*	MCM5303	30202*	54LS37
07905	54S251	10703*	μA7815		(64 X 8 Prom o.c.)	30203*	54LS38
07906	54S257	10704*	μA7824	20102*	MCM5304	30301*	54LS02
07907	54S258	10801*	MH0026		(64 x 8 Prom)	30302*	54LS27
08001	54S11	10901*	555	20201*	82S126	30303*	54LS266
08002	54S15	10902*	556		(256 x 4 Prom o.c.)	30401*	54LS51
08101	54S140	15001	5485	20202*	82S129	30402*	54LS54
08201*	54S85	15002	9324		(256 x 4 Prom t.s.)	30501*	54LS32
10101	μA741	15101	5413	23001*	93410	30502*	54LS86
10102	μA747	15102	5414		(256 x 1 RAM o.c.)	30601*	54LS194
10103	LM101A	15103	54132	2302 *	5531	30602*	54LS195
10104	LM108A	15201	54154		(256 x 1 RAM t.s.)	30603*	54LS95
10105	LM2101A	15202	54155	23501*	2680	30604*	54LS96
10106	LH2108A	15203	54156		(85°C 4K RAM)	30605*	54LS164
10107	LM118	15204	8250	23502*	TMS4050	30606*	54LS295
10201	μA723	15205	8251		(85°C 4K RAM)	30607*	54LS395
10301	μA710	15206	8252	23503*	2680	30801*	54LS181
10302	μA711	15301	54125		(100°C 4K RAM)	31001*	54LS11
10303	LM106	15302	54126	23504*	TMS4050	31002*	54LS15
10304	1M111	15501	54H08		(100°C 4K RAM)	31003*	54LS21
10401	55107	15502	54H11	30001	54LS00	31004*	54LS08
10402	55108	15503	54H21	30002	54LS03	31101*	54LS85
10403	55114	15601	54147				

*Slash sheets not released as of date of this publication.

RELIABILITY 7

I. STANDARD COMMERCIAL PRODUCT RELIABILITY

"Signetics Product Reliability Report R363"* dated June 1975 represents the foundation upon which product reliability philosophy emanates at Signetics. The report differentiates product reliability from product quality. A summation of 13 years (1962 to 1975) of product reliability data is represented by the report. Excerpts from the report are presented herein.

Failure Rate Packets* exist for all Signetics Products. Once per quarter life test data generated from various reliability programs (including SURE II) is summarized and added to existing die process family life test data thereby resulting in updated I.C. failure rate calculations. At the present time, 10 such "Failure Rate Packets" covering 18 Die Process Families exist to provide current failure rate calculations/quotations.

Quarterly SURE II Summaries* containing all recently completed SURE II Die Process Qualification and SURE II Package Qualification Tests exist by which to monitor current product reliability performance to tests which meet or exceed MIL-STD-883A, Method 5005.3 requirements.

Reliability Reports* covering specific topics such as PROM Reliability, Dual Level Metallization Time-Temperature and Current Density Results, etc. are also available as compliments to the items above.

II. SURE II (PRODUCT RELIABILITY QUALIFICATION PROGRAM)

SURE II Bulletin 5005* details the philosophy and procedures used for the **S**ystematic **U**niformity and **R**eliability **E**valuation (SURE II) Program. SURE II is a Signetics in-house qualification program designed to continually qualify all Signetics Die Process Families and all Package/Assembly Families to tests which meet or exceed the most recent military microelectronic test programs (MIL-STD-883A, Method 5005.3 and MIL-M-38510). SURE II is provided at no cost to the customer. Excerpts from Bulletin 5005 are presented herein.

III. SUPR II (100% Screening Program for Commercial/Industrial Products)

SUPR II* the **S**ignetics **U**pgraded **P**roduct **R**eliability (SUPR) Program is designed to provide integrated circuits of a higher level of quality and reliability than is available with standard commercial product. SUPR II products are available as Level A or Level B products. The SUPR II Brochure is presented herein.

IV. MILrel 38510/883 Program (100% Screening Program for Hi-Rel/Mil Products)

MILrel 38510/883 Program — The Signetics MILrel 38510/883 Program is designed to provide integrated circuits of a Military/Hi-Rel grade of product quality and reliability. The program is organized to provide a broad selection of processing options, structured around the most commonly requested customer flows. The MILrel 38510/883 Program is presented herein.

*The reader may obtain a copy of this publication by contacting the

Signetics QRA Department
Signetics Corporation
811 E. Arques Avenue
Sunnyvale, California 94086
(408) 739-7700

SIGNETICS PRODUCT RELIABILITY REPORT R363 JUNE, 1975*

FOREWORD

13 Years of Reliability Data, Over 2000 Lots, over 100,000 Devices, Over 575,000,000 Actual Device hours

All Signetics Products are Represented and Uniquely Delineated

SECTION 1 (Summary of Signetics Product Reliability and Reliability Philosophy)

History of Reliability Testing at Signetics

Signetics Philosophy Regarding Reliability

Questions and Answers to Key Reliability Concerns (Section 1.3)

Primary Manufacturing Factors Affecting Reliability (Table 1-2)

SECTION 2 (Understanding the Failure Rate vs. Acceleration Factor vs. Activation Energy Relationship and Log Normal Life Distributions)

Reliability Terms and Definitions (Failure Rate Equation, Bathtub Curve, Infant Mortality, Acceleration Factor, Arrhenius Equation, Activation Energies, Log Normal Life Distribution, etc.)

Pitfalls to Taking Assessed Failure Rates at Face Value

Failure Rate Acceleration Factor vs. Temperature Graphs — Signetics and Others (Figure 2-2)

SECTION 3 (Signetics Life Test Results and Assessed Failure Rates)

Life Test Data from 1962 to April 1975

Die Process Family Failure Rates (Table 3-5)

Failure Rate Predictions per MIL-HDBK-217B, An Alternate Method (Table 3-7)

SECTION 4 (Signetics SURE Program Package Qualification Results)

January 1963 to December 1969 Results (Table 4-1)

January 1970 to December 1974 Results (Table 4-2)

SECTION 5 (Plastic Molded Integrated Circuits)

Plastic Encapsulant Manufacturing Considerations (Table 5-1)

Plastic Product Accelerated Environmental Test Results (Tests Beyond the Scope of Section 4)

Plastic Product vs. Hermetic Product Application Considerations (Table 5-19)

SECTION 6 (100% Screening vs. Reliability Improvement)

The Use of Screening as a **Possible** Enhancement of Product Reliability

Reliability Improvement Factors VIA Screening (Table 6-5, Section 6.3)

SECTION 7 (SURE II — The Signetics 883A Reliability Program)

Signetics has an Ongoing Product Qualification Program called "SURE II"

Obtain a Copy of Bulletin 5005, "SURE II — Signetics 883A Reliability Program"

*Highlights and excerpts from report. All references to Tables, Sections, and Figures are with respect to the same as they appear in report R363. The excerpts were extracted intact so that a one to one relationship exists with the information contained in report R363.

ANSWERS TO SOME OF THE MORE FREQUENTLY ASKED RELIABILITY QUESTIONS

The following subsection presents the most frequently asked questions about I.C. reliability. The foundation for each answer can be found elsewhere in this report.

How should accelerated stresses be chosen? The stresses chosen should relate to realistic operating conditions, relate to legitimate failure mechanisms which can be accelerated (while not introducing new failure mechanisms), and be designed to limit physical destruction of the device so that failure analysis is possible. Section 2 lists several other concepts which Signetics believes are fundamental to the proper interpretation and understanding of accelerated stress results.

What are the assessed failure rate levels for Signetics Products? The present day bipolar technology failure rates for standard non-pre-screened products range from 0.021% to 0.00049% per 1000 hours at 25°C ambient at 60% confidence. Similarly the MOS technology failure rates range from 0.031% to 0.0035% per 1000 hours. The reader is urged to study Section 3 and understand the variables and limitations that apply to the die process family failure rates of Table 3-5. The reader should also review Table 3-7, for an alternate method of determining failure rates. It behooves the system analyst to know as much as possible about the limitations to existing I.C. failure rates so that the best system failure rate prediction can be made based on the application and environment.

How does one determine the current assessed failure rate for a specific product based on Signetics Data? Signetics life test data and failure rates are organized by die process families. Given such a request, the data for the appropriate die process family is provided. (Internal to Signetics, the QRA representative locates the fab process code corresponding to the specific product via referencing the Product Master File. Once the die process family is determined, the corresponding failure rate is known). These data can then be applied directly as failure rates for the specific device in question.

Are Signetics products continuing to show a downward trend in failure rates? Yes and no. Figure 3.1 shows that bipolar technology products showed a downward trend for the six years that calculations were made between and including 1963 to 1970. The cumulative failure rate curve of 1975 has many new technologies as well as shorter stress times added to it. Considering all the "noise" in the failure rate calculations the failure rates appear to have leveled off. However, if one uses the acceleration factors derived from the 1970 failure rate curve and applies them to DTL/TTL life test data generated from 1971 to 1975, the resulting 25°C failure rate is less than that "demonstrated" at 25°C in 1970. Signetics believes that a 25°C ambient assessed failure rate at the 0.00 OX% (i.e. 0.0001%, 0.0002%, etc.) per 1000 hour level will be extremely difficult to improve in the 1970's. One must keep in mind, however, that due to increasing complexities, the actual failure rate per discrete component is decreasing drastically.

What are the dominant life test failure mechanisms? Signetics has found that accelerated testing at a junction temperature >150°C for prolonged times leads to gold-aluminum intermetallic failure at the bond. Except for that mechanism, Signetics believes that the assessed failure rates are influenced by random defects rather than systematic failures to which reliability physics could be applied and solutions found.

What is the longest life test that Signetics has run? The longest life test is still in process as a demonstration in the front lobby of Signetics in Sunnyvale, California. The "VIP'S" (very important parts) consist of 111 pre-production DTL circuits which have been operating since 1962. Their history is shown in Table 3-1.

How do the temperature acceleration factors that Signetics uses to assess failure rates compare to others used by the industry? Figure 2-2, shows that the Signetics Failure Rate Acceleration Factor vs Temperature Graph can be interpreted as slightly conservative when compared to other available graphs.

What can be said about the integrity of Signetics packages and assembly techniques? Signetics packages are capable of routinely passing the class B LTPD requirements of MIL-STD-883 method 5005. Typically, they are also capable of meeting class A LTPD requirements. See Section 4.

How do plastic package failure rates compare to "hermetic" package failure rates? Based on extensive relatively dry environment life tests (i.e. operating systems on the production floor, HTOL, HTRB, and HTSL), Signetics has found the Silicone, Epoxy Novolac I, and Hermetic package failure rates to be the same (within experimental uncertainty). Refer to Tables 5-2 and 5.3.

What are the primary constraints placed on plastic molded product applications? Junction temperatures must be kept below 150°C to avoid excessive gold-aluminum intermetallic formation as well as bond wire grain growth, both contributing to bond failures. Prolonged exposures in environments approaching 85°C ambient and 85% R.H. should be avoided. These environments are extreme. In more typical applications, problems do not exist as testified to by the millions of plastic I.C.'s that have been used in all types of applications for many years. Refer to Section 5.

How does 100% Screening Affect I.C. Failure Rates? There is no simple answer to the question of screening effectiveness for a specific application. Usually the system application and MTBF (Mean Time Between Failure) requirements together with a good history of confirmed reject failure modes dictate what type of screening if any should be done. As a general guide, Signetics does reference MIL-HDBK-217B and has calculated reliability improvement factors as shown in Table 6-6.

What effect does radiation have on Signetics I.C. performance? Per Table 1-1A, DTL circuits operate satisfactorily while being subjected to transient radiation of $2.5X10^8$ Rads/Sec. or a slow neutron flux of $.2X10^{11}$ neutrons/cm^2. Per Table 6-7, TTL circuits are capable of satisfactory operation during transient gamma radiation in excess of $1X10^8$ Rads/Sec. The TTL circuits are also capable of sustaining $1X10^{13}$ neutrons/cm^2 without significant permanent damage due to the neutron radiation.

Does Signetics have an ongoing Qualification Program for standard products? Yes, its called the SURE II Program. A copy of the SURE II Bulletin 5005 dated March 1975 is available as a complement to this report. Also section 7 of this report contains a brief description of the SURE II/883A Reliability Program.

Table 1-2A
PRIMARY MANUFACTURING FACTORS WHICH HAVE A POTENTIAL IMPACT ON I.C. RELIABILITY (1)

PRIMARY MANUFACTURING FACTORS (POSSIBLY AFFECTING RELIABILITY)	POSSIBLE RELIABILITY IMPACT	APPLICABLE IN PROCESS CONTROLS
I. Wafer Related Factors A. Bulk Considerations 1. Power vs thermal resistance vs T_J (Usually milliwatt range power requirements are easily accommodated by suitable heat-sink packages) 2. Current Non-Uniformity due to: a. Emitter geometry and size variations b. Dopant diffusion variations (emitter resistivity, effective base width, large fields due to diffusion fronts and junction curvature.) c. Silicon lattice defects (dislocations, diffusion damage, oxidation damage)	1. "Hot Spot" formation 2. "Second breakdown" phenomenon 3. Excessive AL-Si eutectic formation. Alloy shorts through junction. 4. Increased carrier generation/recombination due to lattice defect propagation.	1. Starting Slice (Orientation, resistivity, thickness, bow, taper) 2. Mechanical Polish (taper, thickness, surface finish, dislocations) 3. Epitaxial Deposition (thickness, resistivity, stacking faults) 4. Diffusion (Furnace control via V/I uniformity, registration, diffusion depth, resistivity, electrical tests)
B. Passivation Considerations 1. Thermal oxide dielectric strength a. Oxide contamination affect. Top side phosphosilicate glass (PSG) "gettering". b. Oxide thickness and uniformity 2. Junction coverage (passivation!). Latteral diffusion vs contract openings. 3. Thermal oxide and PSG charges a. Qss, surface state charge density (Intrinsic to Si-$Si0_2$ interface for 200A°. Related to ionic Si in oxide. Post assembly stresses <300°C have little affect) b. N_{ST}, fast surface state charge density at Si-$Si0_2$ due to lattice disruption. (Distort C-V plots, anneals at 500°C reduce levels to $\leq 10^{10} cm^{-2}$). c. Qo, mobile ionic impurity charge density. Na is the primary culprit. (K, Li, organics etc. are other possibilities, but seldom found. The usually large negative ions are not a problem in $Si0_2$). Na @ 127°C, 10V gate bias, redistributes 100% across 5.5KA° of oxide in 10 minutes. d. Qs', traps space charge density in $Si0_2$ introduced by radiation generating electron-hole pairs which separate if gate bias exists. Anneal at 300°C cures traps. e. Oxide surface charges "extended gate affect". (Δ R.H. of 40% to 90% produces Δ Sheet resistance of 10^{18} ohms to 10^{15} ohms). Also includes propagation along the interface of two insulators under influence of electric field. f. Polarization of glass — dipole affect. $\pm V_G$ produces $\pm \Delta$ C-V during polarization.	1. Direct metal to silicon shorts, resistive paths. 2. Static discharge susceptibility (increases with low series input resistance and high parallel resistance or junction BV) 3. $Si0_2$ + AL producing AL_20_3 plus Si which can short. 4. Parametric degradation (ΔV_T, Δh_{FE}, ΔBV, ΔI_L etc. due to depletion, inversion, and carrier generation sites)	1. Oxidation (thickness, pinholes, cleanliness via C-V plots and element detection) 2. Photoresist (Dimensions, alignment, etch completeness, rinse completeness) 3. Glass Density (Measure of porosity) 4. Control of Qss via proper oxidation ambient and temperature control.
4. Phosphorous doped thermal oxide (emitter doping cycle) and PSG anomalies. a. Glass cracking (Low P_20_5) b. Unattached P in glass (High P_20_5) c. Lack of sufficient gettering (Low P_20_5) d. Negative oxide/glass slopes if phosphorous concentration increases towards the Si surface. (Faster etching in areas of high concentration). e. PSG Porosity	1. Cracked glass vs DLM 2. Phosphorous leach out of glass forming phosphoric acid in presence of H_20 which attacks metal. 3. Parametric instability 4. Aluminum "microcracks" over oxide/glass steps. 5. Trapped etchants (H_3PO_4).	1. PSG deposition procedure. 2. P_20_5 content 3. PSG annealing procedures 4. Visual and SEM inspections. 5. Pinhole detection
C. Metallization Considerations 1. Metal-Si contact and "via" (AL-AL) contact integrity 2. Stripe cross sectional area (Current capability) 3. Grain size. 4. Deposition contamination 5. "Peeling" Aluminum (Non-Adherence to $Si0_2$) 6. Oxide/Glass step coverage (Especially Collector). 7. Interrelationship of metal to glass (Glass chemical and mechanical properties and possible affect on microcracks, migration, corrosion, and bondability of metal).	1. Δ ohmic contact resistance 2. AL migration (Safe for $J<2x10^5$ A/cm^2) 3. Al "microcracks" at step 4. Metal corrosion (Oxide retards) 5. Poor bondability 6. Parametric instability	1. Target/source coverage and purity. Evaporator control. 2. Thickness measurement 3. Alloy Cycle 4. SEM. 5. C-V plots 6. "Scotch Tape Pull Test" 7. Bond Pull
II. Package and Assembly Related Factors A. Wafer scribe, break, die plating. (Silicon microcracks, conductive particles, contamination - especially moisture related). B. Die Attach (Die Size - area/thickness-dependent) 1. Alloy (Si-Au eutectic, Solder reflow) a. Amount of "wetting" b. Void formation due to diffusion reactions c. Ductility (Thermal stress relief)	1. Parametric instability 2. Loose conductive particles after assembly 3. Die "pop off" 4. Δ thermal resistance 5. Δ electrical resistance	1. Visual Inspections 2. Inert handling procedure 3. Die pry

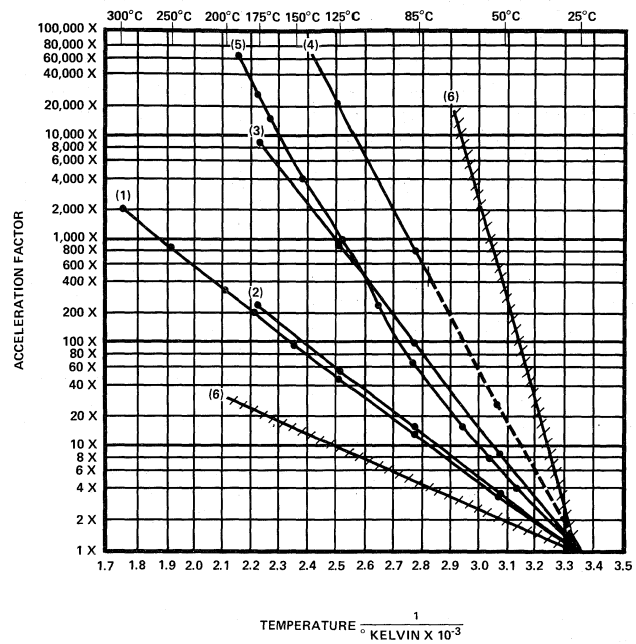
Table 1-2B
PRIMARY MANUFACTURING FACTORS HAVING A POTENTIAL IMPACT ON I.C. RELIABILITY (1)

PRIMARY MANUFACTURING FACTORS (POSSIBLY AFFECTING RELIABILITY)	POSSIBLE RELIABILITY IMPACT	APPLICABLE IN PROCESS CONTROLS
C. Bonding (Requires proper pad layout and die orientation) 1. Thermocompression Gold Wire Bonding (Gold wire is work hardened during wire drawing then stress relieved for suitable characteristics. Ball bonds, stitch bonds-via capillary, and wedge bonds-via wedge tool can be made.) a. Amount of bond deformation b. Wire gain growth c. Intermetallics (Au-Al) d. Wire sag 2. Ultrasonic Aluminum Wire Bonding (Wire is hardened for handling via silicon etc. addition). a. Ductility b. Intermetallics (Au-Al) at package. c. Bond deformation d. Wire dress	1. Bond lift off (under bonding) 2. Au - Al interdiffusion (Kirckendall voids, "purple" plague) producing a. weak bonds b. resistive bonds Keep time temperature product low and do not exceed 150°C for long time periods after assembly. 3. Wire breakage in span during thermal and mechanical stress. 4. Both Au and Al wire lose strength above 150°C 5. Wire to wire shorts or wire to die shorts.	1. Post bond visual for workmanship 2. Au and Al wire (size, tensile strength, % elongation, composition, visual) 3. Thermocompression Bonds a. Capillary cleanliness and temperature b. Bonding area temperature (≥ 300°C). c. Force (60-150g depending upon wire size etc.) and dwell time (ms range). d. Ball formation vs Wire Melt vs New Structure 4. Bond pull data and analysis of break mode.
D. Non-Plastic "Hermetic" Packages. Intent is to maintain a dry (dew point ≪0°C) inert inner atmosphere. 1. Common to Hermetic Packages a. Plating integrity (Nickel, gold, tin). Thickness, coverage, adherence, resistance to oxidation and chemicals, solderability. b. Die attach and bond integrity (Cavity Plating) c. External lead integrity (presence of stress cracks prior to plating, ductility, and material strength) 2. Metal Can (H_{2O} < 10PPM attainable) a. Glass to lead seal integrity. 3. Ceramic Packages With Reflow Alloy Lid Seal (H_20 ≪ 200 PPM. Dew Point ≪ −35°C is attainable).	1. Corrosion of Al wire and die metallization. 2. Corrosion of external leads. 3. External lead fatigue. 4. Inability to withstand chemical, thermal and mechanical environmental stresses. (Ref. Mil-Std-883A) 5. Parametric instability.	1. Fine leak test(10^{-6} to 10^{-8} atm cc/sec) 2. Gross leak test (For < 10^{-5} atm cc/sec) 3. Header bondability and discoloration. 4. Inner package atmosphere analysis. 5. Dye Penetrant 6. Die pry and bond pull
4. Ceramic Packages with top side lid frit seal plus Cerdip and Cerpac (Ceramic base and ceramic lid sealed via solder glass which also supports lead frame). The solder glass technology is based on the glass-ceramic phenomena of nucleation and crystalization (devitrification) of a lead-zinc-borate glass. (H_{20} ≤ 200 PPM, Dew point ≤ −35°C is attainable). a. Lack of high initial heating rates (for high fluidity and mass transport in glassy phase) or lack of slow cooling rates (To minimize thermal shock) during lid seal. b. Proper glass binder control to achieve minimum of voids in glass (< 5%). c. Reliability hazard of tin dipping the leads after lid seal (thermal shock potential) at the "user end". d. Water retention of certain glass binders (used in glassing operation). e. Die attach to printed glass-gold film. f. Susceptibility of the sealing glass to be attacked or become conductive in various plating and cleaning solutions. g. Contaminant free oxidizing environment (Can not use N_2) for lid seal.	1. Problems previously mentioned in prior box. 2. Lead to lead shorts on cerdip and cerpac due to P_b reduction and formation of lead balls. 3. User handling, fixturing and mounting procedures are important in maintaining seal integrity.	1. DTA characterization of sealing glass. 2. Torque test to ≥ 20 in-lb on lid. Averages of ≥ 40 in-lb are typical. 3. Proper Seal Profile. Time/temperature accumulation and oxidizing atmosphere are critical to determining devitrification life. 4. Glass Thickness on Lids. 5. Dye penetrant and other controls mentioned in prior box. 6. Proper electroplating procedures.
E. Plastic Packages Refer to Section 5, Table 5-1	Refer to Section 5, Table 5-1	Refer to Section 5, Table 5-1

NOTES:

(1) Many of the concepts expressed in table 1-2 were extracted from an article by Peattie, Adams, Carrell, George and Valek titled "Elements Of Semiconductor — Device Reliability" which appeared in Proceedings of the IEEE, Vol. 62, No. 2, February, 1974. The concepts are applicable to present day I.C. manufacturing.

Figure 2-2
FAILURE RATE ACCELERATION FACTOR vs TEMPERATURE GRAPHS — SIGNETICS AND OTHERS



NOTES:

(1) Calculated from the Signetics Failure Rate vs Temperature Graph of Figure 3.2. Signetics uses acceleration factors of 15(for 85°C), 50(for 125°C), 100(for 150°C), 200(for 175°C), 350(for 200°C), 970(for 250°C) and 2100(for 300°C) to relate to 25°C equivalent ambient temperature. The 25°C to 125°C segment of the graph is based primarily on operating life data. The segment of the graph above 125°C is based on high temperature storage data. The graph equates to an "activation energy" Ea =0.41 eV.

(2) Calculated from MIL-HDBK-217B, 20 September, 1974, Table 2.1.5-4 for ΠT_1 vs T_J values. The graph equates to an "activation energy" E_A=0.41 eV and is applicable to all bipolar digital (except ECL) in the normal mode of operation.

(3) Calculated from MIL-HDBK-217B, 20 September, 1974, Table 2.1.5-4 for ΠT_2 vs T_J values. The graph equates to an "activation energy" E_A=0.70 eV and is applicable to all Mos, all Linear, and bipolar ECL devices in the normal mode of operation.

(4) Calculated from MIL-STD-883A, 15 November 1974, Figures 1005-4 and 1015-1 by extrapolating the time temperature regression graph from 78°C back to 25°C. The MIL-STD-883A graph is the Bell Telephone Laboratories Graph (Specification A-B-689143, 16 January 1974 etc.) and as such applies to storage and operating T_J values and primarily surface inversion failure mechanisms. The graph equates to an "activation energy" E_A = 1.02 eV.

(5) This curved graph is the result of plotting the "rule of thumb" that failure rates (hence acceleration factors) double for every + Δ 10°C.

(6) All competitor data (available to Signetics) produced graphs falling within these two boundaries. The two boundaries equate to "activation energies" of E_A = 0.23 eV (for lower graph) and E_A = 1.92 eV.

Table 3-5
SIGNETICS I.C. FAILURE RATES CALCULATED FROM THE DATA OF TABLES 3-3 AND 3-4

DESCRIPTION OF SURE DIE PROCESS FAMILIES 1971 TO 1975	SURE FAB PROCESS CODES	EXAMPLE OF A TYPICAL DEVICE	COMBINED (HTOL & HTSL) 25°C EQUIVALENT (1)			λ (25°C) IN % PER 1000 HOURS (2)		
			DEVICE HOURS	# FAILURES CAT.	# FAILURES DEG.	BASED UPON CAT. AND DEG. FAILURES	BASED UPON CATASTROPHIC FAILURES (3)	BASED UPON DIE RELATED CAT. FAILURES
T^2L & DTL, Gold Doped Slow Speed High/Low Voltage	A,A1,B1,J	SE 124 FLIPFLOP	181,868,000	0	1 (1)	0.0011	0.00049	0.00049
T^2L & DTL, Gold Doped Fast Speed Low Voltage	C1,C2,C5,CA CB,D,C6	7400 GATE	619,788,320	6 (5)	4 (4)	0.0019	0.0012	0.0010
Schottky, Std. Aluminum SLM and DLM	R2,S2,X1,X2 X6,X7,Z1	86 S 62 PARITY G	115,275,000	5 (2)	1 (1)	0.0062	0.0054	0.0027
Schottky, Silicide SLM and DLM	R4,S4,X3,X4	82 S 10 1K RAM	19,900,000	3 (0)	0	0.021	0.021	0.0045
Low Pwr. Schottky, Silicide, Ion Implantation, SLM/DLM	P4, V3	74L S 74 FLIPFLOP	141,100,000	2 (0)	0	0.0022	0.0022	0.00064
PROMS, Std. Non-Schottky T^2L C1 Process Plus Nichrome	E2C1, C3	8223 PROM	14,373,800	1 (1)	0	0.0063	0.0063	0.0063
PROMS, Std. Aluminum Schottky DLM Plus Nichrome Fuses	R5, X5	82 S 115 4K PROM	18,290,000	0	0	0.0050	0.0050 (4)	0.0050
ECL, Std. Aluminum Contacts SLM and DLM	Q1, Y1, Y2	10131 FLIPFLOP	180,700,000	0	5 (5)	0.0035	0.0005	0.0005
ECL, Std. Aluminum Contacts, Washed Emitter, SLM and DLM	U2	10145 RAM	30,200,000	0	0	0.003	0.003	0.003
ECL, Silicide, Washed Emitter, SLM and DLM	U4	10164 MULTIPLX	117,000,000	3 (2)	0	0.0035	0.0035	0.0026
Linear, High Voltage	M,ME,MX,PX R, P, M1	μA741 OP.AMP	172,779,000	4 (3)	3 (2)	0.0048	0.0030	0.0024
Linear, Medium Voltage	E,EX,EX2 QX,Q2	565 PLL	25,600,000	0	0	0.0035	0.0035	0.0035
Linear, Low Voltage	B,B2,C,H,K L/L1/L3,W,W1	556 TIMER	43,200,000	0	0	0.0021	0.0021	0.0021
TOTAL FOR BIPOLAR TECHNOLOGIES			1,680,074,120	24 (13)	14 (13)	0.0023	0.0015	0.00084
DMOS, Double Diffused MOS. N-Channel, Ion Implanted	L21A/B/C M2D2/3/4	SD 301 FET	26,450,000	0	0	0.0035	0.0035	0.0035
CMOS, Complimentary MOS, Ion Implanted, Metal Gate	C2K	4011 GATE	91,519,000	4 (4)	4 (4)	0.010	0.0056	0.0056
NMOS, MOS Silicon Gate, LOW Voltage, N-Channel, Ion Implt	N3A C2N	2602 1K RAM	26,860,450	0	2 (2)	0.012	0.004	0.004
NMOS, MOS Silicone Gate High Voltage, N-Channel, Ion Implt	N3B	2604 4K RAM	5,920,000	0	0	0.015	0.015	0.015
PMOS, MOS Silicon Gate Low Voltage P-Channel	K3A C2G	2580 8K ROM	84,535,000	9 (7)	5 (5)	0.018	0.011	0.0098
PMOS, MOS Silicon Gate High Voltage P-Channel	K3B C2T	1103 1K RAM	8,955,720	2 (2)	0	0.031	0.031	0.031
TOTAL FOR MOS TECHNOLOGIES			243,240,170	15 (13)	11 (11)	0.0113	0.0068	0.0059
TOTAL FOR BIPOLAR AND MOS TECHNOLOGIES			1,923,314,290	39 (26)	25 (24)	0.0034	0.0021	0.0014

NOTES:

(1) The Signetics Failure Rate Acceleration Factor vs. Temperature Graph (Figure 2-2) was used to calculate the T_A=25°C equivalent device hours. The catastrophic failures are defined as opens, shorts or non-functional parts. All other "failures" are defined as degradational. The total number of catastrophic and degradational failures are listed without parentheses. The quantity within the parentheses refers to those failures which appear to be related to die failure mechanisms (i.e. assembly and package related failure mechanisms are not included in the in-parentheses quantities).

(2) The failure rates are calculated at 60% confidence and are based upon the combined (HTOL and HTSL) 25°C Equivalent data shown.

(3) Signetics recommends using the failure rate values of this column (more typical of real life). When using these failure rate values, it is important to realize that the failure rates are constantly changing as more data becomes available. Of additional importance is the fact that the failure rates are somewhat influenced by assembly and packaging failure mechanisms. which are random and not unique to a particlar die process family.

(4) To date over 9 billion fused link hours and over 9 billion unfused link hours have been accumulated producing an MTBF (Inverse of Failure Rate) of 9.4 $\times 10^9$ hours for both fused and unfused links.

Table 3-7

FAILURE RATE PREDICTIONS PER MIL-HDBK-217B, 20 SEPTEMBER 1974, "RELIABILITY PREDICTION OF ELECTRONIC EQUIPMENT"

		FAILURE RATE PREDICTIONS PER MIL-HDBK-217B										
1975 SURE II DIE PROCESS FAMILY	FAMILY DESCRIPTION	ARBITRARY CANDIDATE DEVICE TYPES	F.R. PREDICT MODEL(1)	PARAMETERS PER FAILURE RATE EQUATION (1): N (2)	Π_Q (3)	Π_L (4)	Π_E (5)	Π_T (6)	C_1 (1)	C_2 (1)	λ_p F/10^6HR	λ %F/10^3HR
I TTL/DTL	Gold doped, Slow speed High/Low Voltage	SE 124, DTL FLIP FLOP	1. a.	G= 4	150	1	0.2	0.17	.0033	.0064	0.276	0.0276
II TTL/DTL	Gold Doped, Fast speed Low Voltage	7400, QUAD 2-IMPUT NAND GATE	1. a.	G= 4	150	1	0.2	0.17	.0033	.0064	0.276	0.0276
		74147, 10 LINE TO 4 LINE DECODER	1. a.	G= 31	150	1	0.2	0.33	.013	.013	1.034	0.1034
III Schottky	Std. Aluminum Schottky SLM or DLM	82 S 62, 9 BIT PARITY GEN.	1. a.	G= 10	150	1	0.2	0.17	.0061	.0089	0.423	0.0423
IV Schottky	Silicide Schottky, Single Level Metal	74 S 40, DUAL 4-INPUT NAND BUFFER	1. a.	G= 2	150	1	0.2	0.17	.0021	.0050	0.204	0.0204
	(SLM) or Dual Level Metal (DLM)	82 S 10, 1024x1 BIPOLAR RAM	1. d.	B= 1024	150	1	0.2	0.33	.13	.049	7.91	0.791
V Low Power Schottky	Silicide Schottky, Ion Implantation, SLM or DLM	74L S 74, DUAL FLIP FLOP	1. a.	G= 12	150	1	0.2	0.17	.0069	.0095	0.461	0.0461
VI BIPOLAR MEMORY	Std. Aluminum Schottky DLM plus Ni-Cr Fuses	82 S 23, 32x8 BIPOLAR PROM	1. d.	B= 256	150	1	0.2	0.33	.032	.012	1.94	0.194
PROMS		82 S 115, 512x8 BIPOLAR PROM	1. d.	B= 4096	150	1	0.2	0.33	.17	.070	10.52	1.052
VII ECL	Standard Silicide, ECL, SLM or DLM	10109, DUAL 4/5-INPUT OR/NOR GATE	1. a.	G= 4	150	1	0.2	0.24	.0033	.0064	0.311	0.0311
VIII ECL	Silicide, Washed Emitter, ECL, SLM/ DLM	10164, 8 LINE TO 1 LINE MULTIPLXR	1. a.	G= 12	150	1	0.2	0.24	.0069	.0095	0.533	0.0533
IX Linear	Higher Voltage Process	μA741 Operational Amplifier	1. b.	T= 20	150	1	0.2	0.24	.0055	.013	0.588	0.0588
X Linear	Medium Voltage Process	565, PHASE LOCKED LOOP	1. b.	T= 28	150	1	0.2	0.24	.0071	.016	0.735	0.0735
XI Linear	Low Voltage Process	556, DUAL TIMER	1. b.	T= 46	150	1	0.2	0.24	.010	.021	0.99	0.099
XII DMOS	Double Diffused MOS, N-Channel, Ion Implntd	SD 301, DUAL GATE DMOS FET	1. b.	T= 2	150	1	0.2	0.24	.0016	.0056	0.226	0.0226
XIII CMOS	CMOS, Ion Implanted, Metal Gate	4011, QUAD 2-IMPUT NAND GATE	1. a.	G= 4	150	1	0.2	0.24	.0033	.0064	0.311	0.0311
XIV NMOS	MOS Silicon Gate, Low Voltage N Channel,	2602, 1024x1 STATIC RAM	1. d.	B= 1024	150	1	0.2	0.76	.13	.049	16.29	1.629
	Ion Implantation	2650, 8 BIT MICROPROCESSOR	1. c.	G= 1300	150	1	0.2	0.76	9.35	3.52	1171.5	117.15
XV NMOS	MOS Silicon Gate, High Volt N-Chan, Ion Implnt	2604, 4096x1 DYNAMIC RAM	1. d.	B= 4096	150	1	0.2	0.76	.30	.12	37.8	3.78
XVI PMOS	MOS Silicon Gate, Low Voltage P	2521, DUAL 128 BIT STATIC S.R.	1. d.	B= 256	150	1	0.2	0.76	.056	.020	6.98	.698
	Channel	2580, 2048x4 STATIC ROM	1. d.	B= 8192	150	1	0.2	0.76	.26	.11	32.94	3.294
XVII PMOS	MOS Silicon Gate, High Voltage P Channel	1103, 1024x1 DYNAMIC RAM	1. d.	B= 1024	150	1	0.2	0.76	.13	.049	16.29	1.629

(1) $\lambda p = \lambda T + \lambda M = \Pi_L \Pi_Q (C_1 \Pi T + C_2 \Pi E)$. The overall device failure rate λ p (Failures/10^6Hours) is composed of the failure rate component λ T due to time degradation causes (represents degradation mechanisms which are accelerated by temperature and electrical bias; composed largely of phenomena which follow the Arrhenius type rate acceleration) plus the failure rate component λ M due to mechanical causes (application environment induces direct or indirect failure mechanisms from mechanical stresses such as stresses set up by thermal expansion). The ΠT (temperature acceleration factor),C_1 and C_2 (circut complexity factors) values are related to device technology/circut complexity and their values are computed from Section 2.1 of MIL-HDBK-217 B for one of the following four classes of devices:
   a. Monolithic Bipolar and NMOS, PMOS, CMOS Digital (SSI/MSI, Gates $\leq$ 100, Transistors $\leq$ 400).
   b. Monolithic Bipolar and DMOS Linear.
   c. Monolithic Bipolar and NMOS, PMOS, CMOS Digital (LSI).
   d. Monolithic Bipolar and NMOS, PMOS, CMOS Memories (RAMS, ROMS, PROMS, and $\geq$ Dual 8 Bit Shift Registers).

(2) N = # of gates (G), assume 4 transistors/gate, for 1.a. or 1.c.; N=# transistors (T) for 1.b.; N=# bits (B) for 1.d.

(3) Π_Q = Quality factor can be 1, 2, 5, 10, 16 or 150. 150 was chosen to coincide with commercial (non-military standard) parts.

(4) Π_L = Learning factor can be 1 or 10. 1 was chosen to relate to products for which production conditions/controls have stabilized.

(5) Π_E = The applicable environmental factor can be 0.2, 1.0,4.0,5.0,6.0 or 10.0. 0.2 chosen to reflect a ground benign environment.

(6) Π_T = Temperature acceleration factor based on T_J=25°C (ambient) + 10°C (or 25°C). 10°C used for #transistors $\leq$ 120.

Table 4-1

SUMMARY OF ALL SURE ENVIRONMENTAL RESULTS (PACKAGE QUALIFICATIONS TESTS) — JANUARY 1963 TO DECEMBER 1969

SURE PACKAGE FAMILY DESCRIPTIONS	RESULTS BY SUBGROUP (TOTAL QTY FAILURES/TOTAL QTY OF DEVICES) (1)													
	LTPD = 15		LTPD = 15		LTPD = 15		LTPD = 15		LTPD = 15		LTPD = 15		LTPD = 10	
	B1	(2)	B2	(2)	B3	(2)	B4	(2)	B5	(2)	B6	(2)	B7	(2)
Metal Cans (K, T)	0/330	—	3/330	1-4A 2-2D	0/330	—	0/330	—	0/330	—	2/880	2-1C	0/880	—
Plastic Dip, Silicone (A, B)	0/615	—	14/653	13-1C 1-2D	0/615	—	0/615	—	0/615	—	5/1640	3-1C 1-3C 1-3A 1-4A	3/1640	1-2B 1-1C 1-2A
Dip-Cerdip (F)	0/45	—	0/45	—	0/45	—	2/64	2-3F	0/45	—	0/120	—	1/120	1-2B
Flatpac — Glass, Kovar Lid/Glass To Kovar Seal (G, J)	0/1530	—	3/1540	1-2D 1-4A 1-4B	2/1530	1-4A 1-3E	3/1549	3-3F	2/1540	2-3I	9/3994	2-2E 3-2A 1-3E 1-2B 1-1B 1-1C	5/4078	3-2A 1-2B 1-1C
Flatpac — Ceramic Body/ Glass Seal at Leads, Ceramic Lid/Glass Seal (Q)	0/30	—	1/40	1-1C	0/30	—	1/40	1-3F	0/30	—	1/80	1-1C	0/80	—
Flatpac-Ceramic Body, Alloy Seal (P, R)	0/20	—	0/20	—	0/20	—	0/20	—	0/20	—	0/60	—	0/40	—
TOTAL % REJECTS	0% 0/2570		0.799% 21/2628		0.078% 2/2570		0.229% 6/2618		0.077% 2/2580		0.266% 18/6774		0.132% 9/6802	
% LOTS WITHOUT REJECTS	100% 171/171		93% 158/171		99% 169/171		98% 168/171		99% 169/171		90% 152/169		95% 162/171	

NOTES:

(1) Explanation of Subgroups (Per MIL-S-19500 and MIL-STD-750; Reference SURE Bulletin 5001)
- B1: Physical Dimensions
- B2: DC Parameters, Solderability, Temperature Cycling (10 cycles), Thermal Shock (5 cycles), Moisture Resistance (10 days), End Point Electricals with Drift Criteria Applied.
- B3: DC Parameters, Mechanical Shock (1500g), Vibration Fatigue (30g), Vibration Variable Frequency (30g), Acceleration (30,000g), End Point Electricals with Drift Criteria Applied.
- B4: Terminal Strength, Hermeticity (Small Leak & Large Leak)
- B5: Salt Atmosphere (24 hours)
- B6: DC Parameters, Storage Life (1000 hours $T_A \geq 150°C$), End Point Electricals with Drift Criteria Applied.
- B7: DC Parameters, Operating Life (1000 hours, $T_A = 125°C$, Dynamic Conditions), End Point Electricals with Drift Criteria Applied.

(2) The results of failure analysis are shown via code X-YZ where X is the quantity of failures with mechanism YZ. The YZ mechanisms are defined as follows:
1. Bond Problems
   - A. Bond Degradation (Intermetallics)
   - B. Poor Bond Adherence (Substd. Bonds)
   - C. Broken Bond Wires (At the Die or Package)
2. Die Problems
   - A. Oxide Defects (Shorts, Pits, Voids)
   - B. Junction (Leakage) Degradation
   - C. Mask or Diffusion Defects
   - D. Aluminum Metallization (Cracked, Thin, Voided)
   - E. Cause Unknown, Electrical Degradation
3. Assembly and Package Problems
   - A. Aluminum Metal Scratches
   - B. Die Chips or Cracks
   - C. Wire Shorts to Die or Package
   - D. Wire Breakage (In the Span)
   - E. Lifted Die From Attach Pad
   - F. Hermetic Seal (Fine or Gross)
   - G. External Lead Broken
   - H. Cracked Package
   - I. Pitted Leads/Lead Corrosion
4. Miscellaneous
   - A. Failures Not Analyzed
   - B. Aluminum Corrosion (Moisture Ingression, etc. Could be Die Fab, Package or Assembly Related)

Table 4-2

SUMMARY OF ALL SURE ENVIRONMENTAL RESULTS (PACKAGE QUALIFICATION TESTS) — JANUARY 1970 TO DECEMBER 1974

	RESULTS BY SUBGROUP (TOTAL QTY FAILURES/TOTAL QTY OF DEVICES) (1)															
SURE PACKAGE	LTPD = 15		LTPD = 15		LTPD = 15		LTPD = 15		LTPD = 15		LTPD = 15		LTPD = 15		LTPD = 5(3)	
FAMILY DESCRIPTIONS	B1	(2)	B2	(2)	B3	(2)	B4	(2)	C1	(2)	C2	(2)	C3	(2)	C4	(2)
Plastic Dips, Epoxy (V,A,B, AA,BA, N, XF)	0/105	—	0/105	—	0/105	—	0/105	—	0/105	—	0/105	—	0/105	—	0/315	—
Plastic Dip, Silicone (V,A,B, XA, XC, N)	0/165	—	0/165	—	0/172	—	3/222	3-4A	15/277	5-4A 5-4B 1-1B 4-1C	4/228	4-4B	0/165	—	3/445	1-2C 2-2E
Plastic Dip, APT/PILL (AH)	0/120	—	0/120	—	0/120	—	1/130	1-3G	0/120	—	0/120	—	0/120	—	0/340	—
Flatpac-Ceramic Body/ Glass Seal at Leads, Ceramic Lid/Glass Seal (Q)	0/225	—	0/225	—	0/225	—	0/225	—	1/235	1-4B	0/225	—	1/235	1-3G	0/640	—
Flatpac-Cerpac (W)	0/210	—	0/210	—	0/210	—	2/229	2-3G	0/210	—	0/210	—	0/210	—	2/605	1-2E 1-2B
Flatpac-Glass, Kovar Lid/ Glass to Kovar Seal (J)	0/270	—	0/270	—	0/270	—	0/270	—	1/280	1-4A	0/269	—	3/299	1-31 2-4A	0/730	—
Flatpac-Ceramic Body, Alloy Seal (P,R)	0/30	—	0/30	—	0/30	—	0/30	—	0/30	—	2/49	2-4A	3/82	3-31	0/80	—
DIP — Cerdip (F)	0/322	—	0/322	—	0/322	—	13/411	8-3F 5-3G	12/418	7-3F 3-4A 1-1A 1-2A	0/322	—	0/322	—	2/885	1-2E 1-2C
DIP — Ceramic Body, Metal Lid/Alloy Seal (L)	0/210	—	0/210	—	0/210	—	0/210	—	1/210	1-3H	3/210	3-3C	0/210	—	1/590	1-4A
DIP- Ceramic Body, Ceramic Lid/Glass Seal (I_ A, INC)	0/45	—	0/45	—	0/45	—	0/45	—	3/55	1-3F 1-2B 1-2E	2/45	2-1C	0/45	—	0/135	—
Solid Header With Mounting Holes (DA)	0/30	—	0/30	—	0/30	—	0/30	—	1/30	1-3B	0/30	—	0/30	—	2/90	1-3A 1-3B
Metal Cans (T,TA,DB,DC, DE, L, K)	0/150	—	0/150	—	0/150	—	1/160	1-4A	0/150	—	1/150	1-1C	0/150	—	0/430	—
TOTAL % REJECTS	0% 0/1882		0% 0/1882		0% 0/1889		0.97% 20/2067		1.60% 34/2120		0.61% 12/1963		0.36% 7/1973		0.19% 10/5285	
% LOTS WITHOUT REJECTS	100% 125/125		100% 125/125		100% 125/125		90% 113/125		86% 107/125		95% 118/125		97% 121/125		92% 115/125	

NOTES:

(1) Explanation of Subgroups (Per MIL-STD-883 Groups B and C Environmental Tests. Reference SURE Bulletin 5001A of June 1970). The numbers in parentheses refer to MIL-STD-883 Methods.

- B1 = Physical Dimensions (2008), Cond. A
- B2 = Marking Permanency (2008), Cond. B; Visual and Mechanical (2008), Cond. B; Bond Strength (2011), Cond. D
- B3 = Solderability (2003), 260°C ± 10°C
- B4 = Lead Fatigue (2004), Cond. B2; 10 × Visual; Hermeticity (1014), Fine-Cond. A or B and Gross-Cond. C
- C1 = Pre-Test Electrical Parameters; Thermal Shock (1011), Cond. C, 15 cycles, −65°C to 150°C; Temperature cycle (1010), Cond. C, 10 cycles, −65°C to 150°C; Hermeticity (1014), Fine-Cond. A or B and Gross-Cond. C; Moisture Resistance (1004); Vibration and Initial Conditioning Omitted; End Point Electrical Parameters Recorded, 25°C D.C. and Functional.
- C2 = Pre-Test Electrical Parameters; Mechanical Shock (2002), Cond. B, 1500G's; Vibration Variable Frequency (2007), Cond. A (20G pk); Constant Acceleration (2001), Cond. E (30 KG); End Point Electrical Parameters Recorded, 25°C D.C. and functional.
- C3 = Salt Atmosphere (1009), Cond. A, Omit Initial Conditioning; 10 × Visual Inspection
- C4 = Pre-Test Electrical Parameters; High Temperature Storage (1008), T_A = 150°C, + = 1000 hours; End Point Electrical Parameters Recorded, 25°C D.C. and Functional. Drift criteria applied.

Note that the Hermeticity Test does not apply to solid molded packages.

(2) The results of failure analysis are shown via code X-YZ where X is the quantity of failures with mechanism YZ. The YZ mechanisms are defined as follows:

1. Bond Problems
   - A. Bond Degradation (Intermetallics)
   - B. Poor Bond Adherence (Substd. Bonds)
   - C. Broken Bond Wires (At the Die or Package)
2. Die Problems
   - A. Oxide Defects (Shorts, Pits, Voids)
   - B. Junction (Leakage) Degradation
   - C. Mask or Diffusion Defects
   - D. Aluminum Metallization (Cracked, Thin, Voided)
   - E. Cause Unknown, Electrical Degradation
3. Assembly and Package Problems
   - A. Aluminum Metal Scratches
   - B. Die Chips or Cracks
   - C. Wire Shorts to Die or Package
   - D. Wire Breakage (In the Span)
   - E. Lifted Die From Attach Pad
   - F. Hermetic Seal (Fine or Gross)
   - G. External Lead Broken
   - H. Cracked Package
   - I. Pitted Leads/Lead Corrosion
4. Miscellaneous
   - A. Failures Not Analyzed
   - B. Aluminum Corrosion (Moisture Ingression, etc. Could be Die Fab, Package, or Assembly Related).

(3) Changed from a LTPD of 15 to a LTPD of 5 in 1973.

Table 5-1
ENCAPSULANT VS RELIABILITY VS "MANUFACTURING" CONSIDERATIONS

PLASTIC ENCAPSULANT CONSIDERATIONS (COMPOSITION, PROPERTIES, PROCESSING)	APPLICABLE RELIABILITY CONSIDERATIONS (1)	POSSIBLE MANUFACTURING INTERACTIONS (2)
I. Chemical Composition 1. Resin (Type and Hardener) 2. Catalyst 3. Mold Release 4. Flame retardant System 5. Filler (Type, Amount and Particle Size Distribution) II. Chemical — Physical Properties 1. Thermal Stability 2. Impurities (Ionic Conductance and PH of water extract, Total Halogens, Total Metallic Impurities). III. Thermomechanical Properties 1. Thermal Expansion Coeficients ($\alpha 1$, $\alpha 2$) 2. Glass Transition Temperature (T_G) IV. Thermal Conductivity V. Mechanical and Electrical Properties 1. Molded Material 2. Post Cured Material VI. Process Conditions Affecting Package Properties 1. Preheating 2. Encapsulant Flow Characteristics. 3. Molding (Temperature, time, and pressure). 4. Post molding curing (Temperature and time). 5. Finish Operations (Deflash, cutapart, lead bend, lead dipping/plating).	1. Dry environment parametric stability (leakage current, threshold voltage, bond resistance, etc.) a. Evolution of contaminants during molding and cure. (Mobile ionic impurities, polar organic groups, etc.) b. Post cure thermal degradation of encapsulant. 2. Humid environment parametric stability (measure of the encapsulants ability to resist water absorption by the bulk material or moisture ingression along the leadframe/bond wire/ encapsulant interfaces.) a. Electrolytic metal (usually aluminum) corrosion. b. Leach of contaminants producing "extended gate" affect, conductive glass, depletion/inversion or accumulation of silicon surface. c. Decrease in encapsulant electrical resistance. 3. Effect of thermomechanical stress of encapsulant on the bond/bond wire system. (Room, "window", and hot opens or shorts). a. Wire grain growth ("Creep"). b. Decrease in bond strength. c. Wire to wire shorts ("Wire Sweep" related). d. Wire to die shorts. 4. Flammability	1. Die Process Technology (Sensitivity to contaminants and corrosion) a. Gold doped bipolar digital. b. Non-gold doped bipolar digital. c. Bipolar linear. d. NMOS, PMOS, DMOS, CMOS 2. Glass Integrity a. Porosity b. Phosphorous leach c. Gettering ability 3. Metal Integrity a. Retarding effect of oxidized metal on metal corrosion b. Grain size, etc. 4. Bond Integrity Factors of table 1-2 paragraph II. C. 5. Lead frame a. Material b. Plating

NOTES:
(1) Typical Signetics reliability "tools" include
a. HTOL or HTRB (85°C or 125°C), and HTSL (150°C) to evaluate the electrical compatibility of the encapsulating material in a dry environment.
b. Temperature humidity stresses (85°C and 85% R.H., 121°C and 100% R.H., cyclic 25°C to 65°C with 80 to 98% R.H.) with or without electrical bias.
c. Power Cycle (P_D max and either a5 min. or a10 min. cycle), Temperature cycle (0 to 125°C, −55°C to 125°C, −65°C to 150°C), and thermal shock (0 to 100°C, −55°C to 125°C, −65°C to 150°C).
(2) Refer to Table 1-2 for a more comprehensive coverage of "manufacturing" factors.

Table 5-19
A GENERAL COMPARISON OF EPOXY DIP TO CERDIP APPLICATION CONSIDERATIONS

APPLICATION OR PERFORMANCE CONSIDERATION	GENERAL COMPARISON (1)		COMMENTS
	EPOXY DIP	CERDIP	
Cost	Lower	Higher	
Failure Rate for Steady State non-Humid Environment	Same (0.0024% / 1000 Hour)	Same (0.0024% / 1000 hour)	Refer to Section 5.3 and Table 5.2 for details
Thermal Resistance (Effect on T_J During Operation)	Usually Higher	Standard	Medium Power Plastic Packages with a θ_{JA} comparable to CerDip are available
Storage Temperature (Maximum Rating)	150°C	200°C	E-Dip Limited by Au-Al bonding system and epoxy thermal stability.Ref. Sec. 5.1
Temperature Limit for Reverse Bias Stresses	≤125°C	150°C	E-Dip≤125°C to keep T_J≤150°C for extended stress times.
Resistance to Mechanical Abuse	High Strength Encapsulant	Package Strength is related to the seal area	CerDips could lose their hermetic seal with abnormal handling, board insertion, etc.
Mechanical Shock Mechanical Vibration Constant Acceleration	Solid Package	Cavity Package	BOTH packages easily meet SURE subgroup C2 requirement of Table 4-2. (Refer to Section 5.6 also)
Salt Atmosphere (For Lead Corrosion)	Same	Same	BOTH packages have Alloy 42 leadframes. CerDip has tin plated, E-Dip has solder dipped leads. See Subgroup C-3 of Table 4-2.
Thermal Shock, 15~,-65 to 150°C Temperature Cycle, 10~, -65 to 150°C, Moisture Resistance, 10 days	Excellent	Good	See Subgroup C-1 of Table 4-2. The possibility of CerDip loosing hermetic seal increases slightly with larger seal areas.
Extended Power Cycle, 5 min/cycle $\Delta T_J \doteq 80°C$.	No Bond Problems at 20,000 cycles	No Bond Problems Expected at 10,000 cycles	Refer to figure 5-3 for E-Dip. See note (2) for Cerdip.
Extended Temperature Cycle (Expected Safe Performance Levels)	4000 cyc, 0 to 125°C 1000 cyc, -55 to 125°C 500 cyc, 0 to 150°C	200 cycles, -55 to 125°C	For E-Dip, concern is bond integrity. Refer to figure 5-3 for E-Dip. For CerDip, concern is loss of hermetic seal (3).
Extended Thermal Shock (Expected Safe Performance Levels)	2000 Shocks, 0 to 100°C 1000 Scks, -55 to 125°C 250 Scks, -65 to 150°C	200 Shocks, 0 to 100°C	For E-Dip, concern is bond integrity. Refer to figure 5-4 for E-Dip, for CerDip concern is hermetic seal loss (3)
Extended Temperature (85°C) Humidity (85% R.H.) with 5V Bias. (Expected Performance)	2000 Hour, 2% Rejects (4)	Hermetic	For E-Dip, refer to figure 5-1, CerDip will also fail if hermetic seal is lost.
Pressure Cooker, 30 PSIA (15 PSIG), 121°C (Expected Performance)	24 hour, 0% Rejects 96 hour, 2% rejects (4)	Hermetic	For E-Dip, refer to figure 5-2. CerDip will also fail if hermetic seal is lost.

NOTES:

(1) Refer to Table 1-2 and Table 5-1 for an overview of manufacturing factors and encapsulant considerations vs. potential impact on I.C. Reliability. CerDip packages have a glass seal at the leadframe and use ultrasonic aluminum wire bonding. The Epoxy Dip packages use Novolac I encapsulant and thermocompression gold wire bonding.

(2) A November 30, 1970 NASA (MSFC) Report, TMX-64566, showed that 2N2222A transistors (vendor unknown) with 1 mil aluminum ultrasonic bonded wire can develop 5.8 CUM.% bond failures (at the heel of the bond) after 10,000 cycles (0% at 8,000 cycles) of 6 minute power cycles of ΔPd = 500mW, ΔIc = 50mA. The aluminum wire in air can be expected to see a higher temperature than the gold wire which is surrounded by epoxy. Aluminum wire lead movement caused by Joulian heating (I^2R) and die power dissipation can result in fatigue if excessive microcrack/tool marks exist.

(3) Signetics packages were tested to and passed 200 cycles of -65°C to 150°C thermal shock. However, a report by W. T. Fitch, "The Degradation of Bonding Wires and Sealing Glasses with Extended Thermal Cycling", appearing in the April 1975 13th Annual Proceedings Reliability Physics, states that 0 to 100°C thermal shock tests performed on CerDip packages from 6 vendors showed one vendor having a 50% hermetic seal failure problem after 110 shocks. Seal integrity is related to the amount of extended thermal shock testing.

(4) Refer to Section 5-4 for an interpretation of these reject levels.

100% SCREENING AFFECT ON I.C. FAILURE RATES

Considering the various screening flows, the failure mechanisms, the lot to lot variations, etc., it is extremely difficult to predict with any certainty to what extent a specific screen will improve product reliability. If general criteria are required, Signetics suggests using MIL-HDBK-217B, "Reliability Prediction Of Electronic Equipment", Table 2.1.5-1 Π_Q Quality Factors. Since Π_Q is a direct multiplier in the failure rate equations of MIL-HDBK-217B, Table 2.1.5-1 of the MIL-HDBK can be translated as shown in Table 6-6.

Table 6-6
MIL-HDBK-217B RELIABILITY IMPROVEMENT FACTORS VIA SCREENING

RELIABILITY IMPROVEMENT FACTOR	SCREENING LEVEL USED (Quality Level)	EXAMPLE OF A SIGNETICS PRODUCT
1	Commercial part with no screening beyond the manufacturer's regular quality asurance practices.	N7400A
9 (1)	SIGNETICS SUPR II Level A (1)	S N7400A
9.4	MIL-M-38510, Class C (JAN)	JM38510/XXXXXCZZ
15	Manufacturer equivalent of MIL-STD-883, METHOD 5004, Class B	S5400F/883B
25 (1)	SIGNETICS SUPR II Level B (1)	S-B N7400A
30	MIL-STD-883, Method 5004, Class B	M38510/5400BZZ
75	MIL-M-38510, Class B (JAN)	JM38510/XXXXXBZZ
150	MIL-M-38510, Class A (JAN)	-----

NOTE:
(1) These Reliability Improvement Factors and associated Screening Levels are not from MIL-HDKB-217B but rather from the Signetics Upgraded Reliability (SUPR II) Program for commercial and industrial products. These are approximate Reliability Improvement Factors which Signetics has estimated for these two screening levels.

SURE II - THE SIGNETICS 883A RELIABILITY PROGRAM

SURE II BULLETIN 5005

Bulletin 5005 dated March, 1975 and titled "SURE II The Signetics 883A Reliability Program Covering All Product Lines" details the philosophy and procedures used for the SURE II in-house qualification program designed to continually qualify all Signetics die process families and all Signetics package families. Bulletin 5005 contains three sections.

Section 1: 100% Product Screen Tests and Lot Acceptance Tests

Section 2: Signetics SURE II/883A Reliability Program

Section 3: Optional High Reliability Screening

Bulletin 5005 is available as a separate publication and as such is not reproduced here. However, a few excerpts from Bulletin 5005 which are considered basic to understanding the ongoing Signetics SURE II Program are included here for quick reference purposes.

What is SURE II For?

SURE II provides fingertip data that demonstrates the reliability of Signetics Products. Data summaries from each SURE II Qualification Test are available for customer inquiries. Quarterly comprehensive summaries are also available for customer inquiries.

SURE II allows the customer to qualify Signetics products based upon testing at Signetics. This is a cost effective approach as it allows many customers to use the same qualification results.

SURE II provides assurance that all Signetics Fab Processes meet established reliability standards on a continual basis.

SURE II provides assurance that all Signetics Packages meet established reliability standards on a continual basis.

SURE II provides the basic attributes data quoted in Product Reliability Reports and is used for failure calculations.

SURE II provides variables data on key drift parameters (as well as additional parameters) for all storage and operating life tests. This data is available for inspection at Signetics and can be obtained at a nominal fee.

A Brief Description of SURE II Procedures

For 1975, grouping of similar die processes and similar packages at Signetics resulted in 27 unique generic families to be qualified periodically. Throughout 1975, 88 unique qualification tests were scheduled. The number of generic families can and will change from year to year as new fab processes and packages are introduced and old ones obsoleted. A description of each of the 27 unique generic families for 1975 as well as the candidate products that were scheduled throughout the year are shown in Tables 2.5, 2.6, and 2.7. Similar generic family descriptions and schedules of products to be sampled on the SURE II program will be available at the start of each new year.

For die process family qualifications, a representative device from each generic die process family is evaluated once every 90 days (4 times a year) per Table 2.1. Post stress failures are defined via the criteria of Table 2.4. References to additional Tables within Tables 2.1 and 2.4 refer to additional tables contained in Bulletin 5005.

Similarly, a representative device (representative package with a common die for electrical testing) from each generic package family is evaluated bi-annually per Table 2.2 or Table 2.3. References to additional tables within Tables 2.2 and 2.3 refer to additional tables contained in Bulletin 5005.

Table 2.1

SIGNETICS SURE II PROGRAM FOR DIE PROCESSES (REFERENCING MIL-STD-883A, GROUP C)

MIL-STD-883A GROUP C SUBGROUP	TEST DESCRIPTION	MIL-STD-883A METHOD	CONDITIONS	LTPD
—	Pre Test Electrical Parameters	—	Subgroup A1 & A4 or A7 as applicable. Refer to Table 1.3	
—	High Temperature Storage End Point Electrical Parameters FAILURE CRITERIA	1008.1 Note 2	Test Condition C. $T_A = 150°C$, t=1000 hours. Subgroups A1 & A4 or A7 as applicable. Refer to Table 2.4	λ=5
C1	High Temperature Operating Life End Point Electrical Parameters FAILURE CRITERIA	1005.1 Note 2	Test Condition D or E as applicable. $T_A = +125°C$ or $+85°C$ as applicable. t=1000 hours. Subgroups A1 & A4 or A7 as applicable Refer to Table 2.4	λ=5

Table 2.2

SIGNETICS SURE II PROGRAM FOR HERMETIC PACKAGES (PER MIL-STD-883A, GROUP B & D)

MIL-STD-883A GROUP B & D SUBGROUP	TEST DESCRIPTION	MIL-STD-883A METHOD	CONDITIONS	LTPD/MAX. ACC.
D1	Physical Dimensions	2016	Attributes data per appropriate Signetics package outline	15
B1 B2 B3	Resistance to Solvents Internal Visual and Mechanical Bond Strength	2015 2014 2011.1	 No Photograph Test Condition D	3 devices/no failure 1 device/no failure 15 (10 devices min.)
 B4	Stabilization Bake Solderability	1008.1 2003.1	Condition B, 160 hours minimum. Solder Temperature 260°C ± 10°C	Note 1 15 (3 devices min.)
D2	Lead Integrity Seal a. Fine b. Gross	2004.1 1014.1 Note 2	Test Condition B_2 Test Condition A Test Condition C	15
D3	Thermal Shock Temperature Cycle Moisture Resistance Seal a. Fine b. Gross Visual Examination End Point Electrical Parameters	1011.1 1010.1 1004.1 1014.1 Note 3 Note 2	15 cycles, Test Condition C, +150°C to −65°C 10 cycles, Test Condition C, 150°C to −65°C Test Condition A Test Condition C Subgroups A1 & A4 to A7 as applicable. Refer to Table 1.3	 15
D4	Mechanical Shock Vibration Variable Frequency Constant Acceleration Seal a. Fine b. Gross Visual Examination End Point Electrical Parameters	2002.1 2007 2001.1 1014.1 Note 3 Note 2	Test Condition B Test Condition A Test Condition E Test Condition A Test Condition C Subgroups A1 & A4 or A7 as applicable. Refer to Table 1.3	15
D5	Salt Atmosphere	1009.1	Test Condition A	15

NOTES:
(1) Preconditioning of Solderability sample satisfies the time/temperature requirement of Class B screening (Burn-in).
(2) Only electrically and/or hermetically acceptable parts (as applicable) are to be subjected to this test subgroup.
(3) Visual examination shall be in accordance with Method 1010.1 or 1011.1 at a magnification 5X to 10X.
(4) All test equipment calibrated to meet requirements of MIL-Q-9858A and MIL-C-45662A.

Table 2.3
SIGNETICS SURE II PROGRAM FOR PLASTIC PACKAGES (REFERENCING MIL-STD-883A, GROUP B & D)

MIL-STD-883A GROUP B & D SUBGROUP	TEST DESCRIPTION	MIL-STD-883A METHOD	CONDITIONS	LTPD/MAX. ACC.
D1	Physical Dimensions	2016	Attributes data per appropriate Signetics package outline	15
B1 B2	Resistance to Solvents Internal Visual and Mechanical	2015 2014	 No Photograph	3 devices/no failure 1 device/no failure
B4	Stabilization Bake Solderability	1008.1 2003.1	Condition B, 160 hours min. Solder Temperature 260°C ± 10°C	Note 1 15 (3 devices min)
D2	Lead Integrity	2004.1	Test Condition B_2	15
D3	Pre Test Electrical Parameters Thermal Shock, Extended End Point Electrical Parameters	 1011.1	Subgroup A7 & Thermal Scan. Note 2 200 cycles, Test Condition C, +150°C to −65°C Subgroup A7 & Thermal Scan. Note 2	5 10 for TO-220
D3	Pre Test Electrical Parameters Temperature Cycle, Extended End Point Electrical Parameters	 1010.1	Subgroup A7 & Thermal Scan. Note 2 1000 cycles, Test Condition B, 125°C to −55°C Subgroup A7 & Thermal Scan. Note 2	5 10 for TO-220
D3	Moisture Resistance End Point Electrical Parameters	1004.1 Note 3	Subgroup A1 & A4 or A7 as applicable. Refer to Table 1.3	15
D4	Mechanical Shock Vibration Variable Frequency Constant Acceleration End Point Electrical Parameters	2002.1 2007 2001.1 Note 3	Test Condition B Test Condition A Test Condition E Subgroup A1 & A4 or A7 as applicable. Refer to Table 1.3	15
D5	Salt Atmosphere End Point Electrical Parameters	1009.1 Note 3	Test Condition A Subgroup A1 & A4 or A7 as applicable. Rèfer to Table 1.3	15
—	Pressure Cooker End Point Electrical Parameters	— Note 3	96 hours, 30 PSIA, Note 4 Subgroup A1, A4 or A7 as applicable. Refer to Table 1.3	10
—	Temperature-Humidity, Note 5 End Point Electrical Parameters	— Note 3	85° C/85% R.H. with bias ≤5 volts, t = 2000 hours Subgroup A1, A4 or A7 as applicable. Refer to Table 1.3	10/2

NOTES:
(1) Preconditioning of solderability sample satisfies the time/temperature requirement of Class B screening (Burn-in).
(2) Refer to Table 1.3 for subgroup A7 definition. Thermal Scan refers to a test that monitors bond continuity continuously over the temperature range of 25°C to 125°C.
(3) Where endpoint measurements are required, only electrically acceptable parts to same measurement criteria are subjected to the prior stresses.
(4) 24 hours 30 PSIA for TO-220
(5) Not applicable to TO-220

TABLE 2.4
SIGNETICS SURE II FAILURE CRITERIA FOR DIE PROCESS FAMILIES

LOGIC - DTL AND TTL	
Parameter	ΔLimit
"1" Input Current	5X initial value or 25% of limit, whichever is greater
"1" Output Voltage	±20% of initial value
"O" Input Current	±20% of initial value
"O" Output Voltage	±100mV
I_{CC} (Supply Current)	±20% of initial value

ECL (EMITTER COUPLED LOGIC)	
Parameter	ΔLimit
"1" Input Current	±20% of initial value or ±35μA, whichever is greater
"1" Output Voltage	±20% of initial value or ±25mV, whichever is greater
"O" Input Current	±20% of initial value or ±15μA, whichever is greater
"O" Output Voltage	±20% of initial value or ±45mV, whichever is greater
I_E (Supply Current)	±20% of initial value

LOGIC - SCHOTTKY AND LOW POWER SCHOTTKY	
Parameter	ΔLimit
"1" Input Current	5X initial value, or 25% of limit, whichever is greater
"O" Input Current	±20% of initial value
"1" Output Voltage	±20% of initial value
"O" Output Voltage	±100 mV
VOS (Offset Voltage)	±10% of initial value
I_{CC} (Supply Current)	±20% of initial value

MOS (N-CHANNEL, P-CHANNEL, AND COMPLIMENTARY)	
Parameter	ΔLimit
Input & Clock Leakage	5X initial value or ±100nA, whichever is greater
"O" Input Voltage	±20% of initial value
"1" Input Voltage	±20% of initial value
"O" Output Voltage	±20% of initial value
"1" Output Voltage	±20% of initial value
I_{DD} or I_{CC} (Supply Current)	±20% of initial value

DMOS (DOUBLE DIFFUSED MOS)	
Parameter	ΔLimit
V_T	±30% of initial value or ±200mV, whichever is greater
Rds (on)	±20% of initial value
BV_{DS}	±20% of initial value
I_D(off)	5X initial value or ±100nA, which is greater

NOTES:
(1) All products are tested to subgroups A1, A4, or A7 as applicable. Refer to Table 1.3. The detailed tests, conditions and limits applicable to each product are listed in the Signetics Data Book ELECTRICAL CHARACTERISTICS table. All parameters must meet the min/max limits as well as the Δ limits shown.
(2) All fusible products (PROM's) are programmed prior to stress and fuse patterns verified after stress.

TABLE 2.4 (Continued)
SIGNETICS SURE II FAILURE CRITERIA FOR DIE PROCESS FAMILIES

	Linear/Analog Product Family — Parameter Δ Limits									
Applicable Parameter	Operational and Differential Amplifiers	Sense Amplifer	Video & RF/IF Amplifers	Comparators	Consumer Communications Circuits & Function Gen (1)	Timers	Voltage Regulators	Phase Locked Loops	Per. Interface Circuits (2)	Gas Table Decoder/ Drivers
Power Supply or Quiescent current	±20% of initial value	±20% of initial value	±20% of initial value	±20% of initial value	±20% of initial value	±20% of initial value	±20% of initial value	±20% of initial value	±20% of initial value	±20% of initial value
Input Offset Voltage (Vio)	±1mV			±1mV						
Input Bias Current (I in)		±30% of initial value								
Input Threshold Voltage (V_T)		±1mV								
Voltage Gain			±20% of initial value	±20% of initial value						
Output Voltage						±0.20 volts	±20% of initial value			
Initial Accuracy						±1% (absolute value				
Trigger Voltage						±0.10 volts				
High Level Output Voltage (VOH)		±20% of initial value							20% of initial value	
Low Level Output Voltage (VOL)		±100mV							±100mV	
High Level Input Current (IIH)		≥5X initial value or > ± 5μA							≥ 5X initial value or > ± 5μA	≥ 5X initial value or > ± 5μA
Low Level Input Current (IIL)		± 20% of initial value							± 20% of initial value	± 20% of initial value
Output Leakage Current (IOH)										±300nA
Output Breakdown Voltage										± 20% of initial value
Center Frequency of Oscillation								± 10% of initial value		

NOTES:
(1) Radios, Receivers, Modulators, Demodulators, Detectors
(2) MOS Clock Drivers, Line Drivers, Line Receivers
(3) All products are tested to subgroups A1, A4, or A7 as applicable. Refer to Table 1.3. The detailed tests, conditions and limits applicable to each product are listed in the Signetics Data Book ELECTRICAL CHARACTERISTICS Table. All parameters must meet the min/max limits as well as the Δ limits shown.

Table 2.5

1975 SURE II QUALIFICATION PROGRAM - DIE PROCESS FAMILIES - DEFINITIONS AND SCHEDULE

SURE Family	Family Description	SURF Fab Process Codes	Candidate Device Types	Quarter I		Quarter II		Quarter III		Quarter IV	
				Device	Date (2)	Device	Date (2)	Device	Date (2)	Device	Date (2)
I	Gold Doped	A	7490, 74121, 7420,	7420	2-17-75						
TTL	Slow Speed		8T16								
DTL	High/Low	A1	7426			7426	5-12-75				
	Voltage	B1	8T80					8T80	8-18-75		
		J	SE124							SE124	12-8-75
II	Gold Doped	C1	8242, 74175, 74H76,					74175	9-29-75		
TTL	Fast Speed		8233, 7474, 8293								
DTL	Low Voltage	C2	74193, 74164							74193	11-24-75
		C5	7406, 7416, 7407,								
			7417								
		CA	74107								
		CB	74160, 74161			74161	6-2-75				
		D	74147, 74148	74147	3-3-75						
III	Std. Aluminum	R2	82S226**					82S226	7-1-75		
Schottky	Schottky, Single	S2	C2272 (82S09)**								
	Level Metal (SLM)	X2	C2237, 3207A***								
	or Dual Level		521***, 522***								
	(DLM)	X7	82S62**	82S62	3-10-75					82S62	10-6-75
		Z1	8204*, 8205**,			8205	4-1-75				
			8208**								
		X1	3207***			3207	4-1-75				
		X6	527***, 529***								
IV	Silicide Schottky	R4	82S25**								
Schottky	(SLM) or (DLM)	S4	82S16**, 82S17**,	82S10	2-3-75						
			82S09B**, 82S10**								
		X3	54S00, 54S40			54S00	5-19-75			54S40	11-3-75
		X4	54S112					54S112	8-25-75		
V	Silicide Schottky,	P4	10144*								
LS	Ion Implantation	V3	74LS00, 74LS74	74LS00	2-10-75	74LS74	4-21-75	74LS40	8-4-75	74LS20	11-24-75
	(SLM) or (DLM)		74LS40, 74LS20								
VI	Std. Aluminum	R5	82S23, 82S123,	82S23	2-3-75	82S115	4-8-75	82S130	7-8-75	82S126	10-13-75
Bipolar	Schottky, DLM,		82S126, 82S129,								
Memory	plus Ni:Cr fuses		82S114, 82S115,								
			82S130, 82S27								
VII	Standard Silicide,	Y3	10105, 10109, 10110	10109	2-24-75			10110	9-1-75		
ECL	ECL	Y4	10131, 10133, 10191			10133	5-26-75			10131	12-22-75
	(SLM) or (DLM)										
VIII	Silicide, Washed	U4	10141, 10145,	10141	2-17-75	10145	4-28-75	10160	7-28-75	10164	11-17-75
ECL	Emitter, ECL		10160, 10164								
	(SLM) or (DLM)										
IX	High Voltage	M	LM311							LM311	11-17-75
Linear	Process	ME	DM8880								
		MX	μA723, μA723	μA723	2-17-75					μA741	12-1-75
		PX	536					536	8-11-75		
		R	LM108			LM108	5-5-75				
X	Medium Voltage	E	565, 566, 562			565	4-21-75				
Linear	Process	EX	545, 532	545	3-17-75			532	7-1-75		
		EX2	μA78L00								
		QX	μA7800							μA7800	10-20-75
		Q2	LM109								
XI	Low Voltage	B	μA711								
Linear	Process	B2	75453			75453	6-9-75				
		C	DM8880								
		H	7524							7524	12-22-75
		K	μA733								
		L	556, 567, μA758	556	3-10-75	567	6-2-75	μA758	9-22-75		
		W	CG388, CG451								
XII	Double Diffused	L21A	SD5000, SD211			SD5000	4-7-75	SD211	7-14-75		
DMOS	MOS, N-Channel	L21B	SD6000, SD303	SD6000	2-10-75					SD303	10-27-75
	Ion Implanted	L21C	SD301								
XIII	CMOS, Ion Implanted	C2K	4015, 4050, 4528	4015	2-24-75	4050	4-28-75	4528	7-21-75	4014	11-10-75
CMOS	Metal Gate		4014, 4027, 4025								
XIV	MOS Silicon Gate	N3A	2602, 2606, 2608,	2602B	2-24-75	2602F	6-9-75	2602B	9-15-75	2602F	12-15-75
MOS	Low Voltage N		2650								
	Channel, Ion Implant										

Table 2.5 (Continued)
1975 SURE II QUALIFICATION PROGRAM - DIE PROCESS FAMILIES - DEFINITIONS AND SCHEDULE

SURE Family	Family Description	SURF Fab Process Codes	Candidate Device Types	Quarter I		Quarter II		Quarter III		Quarter IV	
				Device	Date (2)	Device	Date (2)	Device	Date (2)	Device	Date (2)
XV MOS	MOS Silicon Gate High Voltage N Channel, Ion Implant	N3B	2604	2604	3-3-75 (3)	(4)		2604	7-21-75	(4)	
XVI MOS	MOS Silicon Gate Low Voltage P Channel	K3A	2518, 2521, 2522, 2525, 2532, 2533 2580	2521	3-10-75	2533	5-5-75	2580	9-8-75	2525	12-29-75
XVII MOS	MOS Silicon Gate High Voltage P Channel	K3B	1103, 2504, 2527	1103	3-17-75 (3)	1103	4-14-75	2504	7-7-75	1103	10-27-75

NOTES:
(1) SURE Die Quals involve N ≥ 45 to HTSL, N ≥ 45 to HTOL, R & R Pre and Post . 1000 hours.
(2) The date refers to scheduled start date.
(3) A developmental test is scheduled in lieu of a SURE Qual test.
(4) This family has only one device and thus requires qualification every six months.
* This device is included in the ECL product line even though fabricated per die process family shown.
** This device is included in the Bipolar Memory product line even though fabricated per die process family shown .
*** This device is included in the Linear product line even though fabricated per die process family shown.

Table 2.6
1975 SURE II QUALIFICATION PROGRAM - PLASTIC PACKAGES - DEFINITIONS AND SCHEDULE

SURE PACKAGE FAMILY	DESCRIPTION	PACKAGES IN FAMILY (CODE DESIGNATION)	1975 SCHEDULE			
			QUARTERS I & II		QUARTERS III & IV	
			PACKAGE	DATE (1)	PACKAGE	DATE (1)
I	Plastic Dip (Epoxy)	V— 8 lead N—24 lead A—14 lead XF—28 lead B—16 lead AA—14 lead Medium Power BA—16 lead Medium Power	A	3-10-75	V	7-1-75
II	Plastic Dip (Silicone)	V— 8 lead XA—18 lead A—14 lead SC—22 lead B—16 lead N—24 lead	B	3-10-75	XA	8-4-75
III	Plastic Power, Flange Mounted	TO-220 3 lead	TO-220	6-2-75	TO-220	10-27-75

(1) The date refers to scheduled package qualification start date.

Table 2.7

1975 SURE II QUALIFICATION PROGRAM - HERMETIC PACKAGE - DEFINITIONS AND SCHEDULE

SURE PACKAGE FAMILY	DESCRIPTION	PACKAGES IN FAMILY (CODE DESIGNATION)	1975 SCHEDULE			
			QUARTERS I & II		QUARTERS III & IV	
			PACKAGE	DATE (1)	PACKAGE	DATE (1)
I	(Q) Flatpac-Ceramic Body/Glass Seal at Leads/Ceramic Lid/ Glass Seal	QF—10 lead QH—14 lead QJ—16 lead QN—24 lead	QH	5-19-75	QN	7-14-75
II	(W) Flatpac-Cerpac	WF—10 lead WH—14 lead WJ—16 lead	WH	3-17-75	WJ	8-25-75
III	(F) Dip-Cerdip	FH—14 lead, SSI or MSI FJ—16 lead, SSI or MSI or LSI FN—24 lead	FH (SSI)	3-31-75	FJ (LSI)	9-15-75
IV	(I) Dip-Ceramic Body/ Metal Lid/Alloy Seal	IE—8 lead IM—22 lead IH—14 lead INB—24 lead IJ—16 lead IQ—28 lead IK—18 lead IW—40 lead	IJ	4-7-75	INB	10-6-75
V	(I) Dip-Ceramic Body/ Ceramic Lid/Glass Seal	IEA—8 lead IMA—22 lead IHA—14 lead INC—24 lead IJA—16 lead IQA—28 lead IKA—18 lead IWA—40 lead	IJA	4-21-75	INC	11-10-75
VI	Solid Header With Mounting Holes	DA—2 lead TO-3	DA	5-12-75	DA	12-1-75
VII	Metal Can	T-8 lead TO-5, 200 mil diameter TA-8 lead TO-5, 230 mil diameter DB-3 lead, TO-5 Solid Header DC-4 lead TO-46 DE-4 lead TO-72 L-10 lead TO-5 Tall Can K-10 lead TO-5 Short Can	K	3-3-75	TA	12-15-75

(1) The date refers to scheduled package qualification start date.

SIGNETICS SUPR II

FOR ANALOG, LOGIC, MEMORY AND MOS PRODUCTS

Signetics' Upgraded Product Reliability (SUPR) program is designed to provide industrial manufacturers with integrated circuits of a higher level of quality and reliability than is available with standard commercial product. Improvements in quality and reliability will result in significant cost savings to the integrated circuit user by:

Eliminating the need for incoming electrical inspection
Eliminating the need for outside testing laboratories
Reducing in-process inventory
Reducing P.C. board rework
Simplifying system check-out
Reducing warranty repair work
Reducing field service calls
Reducing customer dissatisfaction

SUPR II is a corporate program covering a comprehensive selection of device types in ceramic, metal can and plastic packages from all of Signetics' product groups.

Logic (TTL, Schottky TTL, low power Schottky TTL, CMOS)
Analog (industrial, consumer and interface)
Bipolar memory (ROMs, RAMs, PROMs)
MOS (ROMs, RAMs and Microprocessors)

SUPR II OPTIONS

SUPR II combines both quality and reliability improvements by imposing more stringent controls and raising inspection criteria at all stages of manufacturing and testing. Two levels of quality and reliability are offered, each tailored to different user needs.

LEVEL A — Cost/Effective Program

Improved in-process controls and tighter inspection levels, are combined with thermal stressing and high temperature testing to insure the maximum improvement in quality and reliability which can be achieved at nominal cost.

Highlights of Level A processing include:

MIL-STD-883 die and preseal visual inspection criteria
MIL-STD-883 thermal shock preconditioning
100% D.C. testing
100% high temperature testing
The tightest commercial outgoing inspection criteria in the industry

LEVEL B — Maximum Reliability Program

SUPR II Level B provides the maximum level of reliability which can be achieved at costs compatible with the needs of manufacturers of industrial equipment.

Level B processing provides in addition to all the steps of Level A:

100% burn-in to MIL-STD-883A test conditions equivalent to 168 hours at 125°C

SUPR II procedures have been developed as a result of Signetics' many years of supplying integrated circuits to the exacting requirements of large mainframe computer, automotive, industrial and military customers.

Your local Signetics sales office or distributor can supply details of device types currently included in the SUPR II program.

QUALITY AND RELIABILITY

Quality and Reliability are two important measurements of a products merit. "Quality" provides information concerning the probability of faulty I.C.s existing in a given lot arriving at your plant, while "Reliability" is a measurement of how well an initially good part will remain so over time.

1. IMPROVING QUALITY

Some percentage of defective devices will always exist in any lot of mass produced items. The number of defective units received by the customers can be reduced by the use of tightened inspection criteria at the vendors outgoing quality control station.

A good example of the savings which can be achieved by purchasing tighter inspection levels is given in Figure 1. Here we are comparing the various levels of inspection (AQL) available for device functionality and its impact on the number of P.C. boards which must be reworked during system manufacturing. Using the standard commercial AQL on functionality of 1.0%, at 120 integrated circuit packages per board, typically more than 90% of boards will require rework. At 0.15% AQL, rework is reduced to 25%, and at 0.1%, typically over 12% rework is required.

AQL LEVELS ON FUNCTIONALITY VERSUS BOARD REWORK RATES

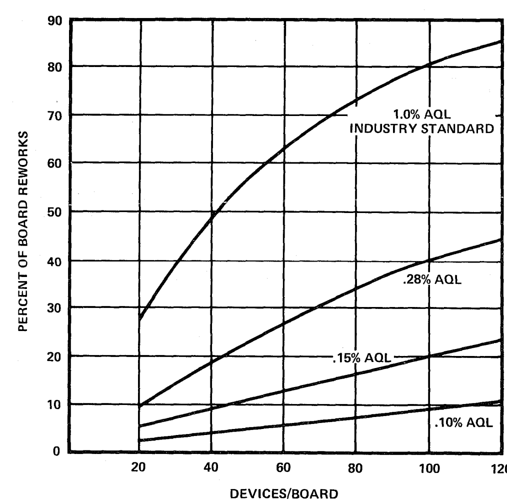


Figure 1

2. IMPROVING RELIABILITY

Reliability is a measurement of how well a device that meets all electrical requirements initially will continue to operate over the life of a system. In general, if an integrated circuit is going to fail, it will occur during the early stages of its life. The SUPR II program employs improved manufacturing screens to identify potential defects that would result in early operational failure together with stresses which subject the circuit to conditions equivalent to an accelerated period of actual use.

QUALITY VERSUS RELIABILITY

Quality and Reliability are two measurements which are often mistakenly used interchangeably.

The interrelation between the two only occurs in the steps the I.C. vendor takes to improve them. Thus controls designed to enhance the long term reliability of a device may also help reduce the number of marginal devices produced. It is important to realize that a shipment of circuits of high quality (few defects), may possibly be of low reliability (high failure rate). Signetics' SUPR II program addresses both of these attributes.

HOW DO INTEGRATED CIRCUIT FAILURES OCCUR

Results of a three years failure analysis performed on Signetics product returned from board check-out, systems check-out, field usage, environmental life tests, etc., revealed the pattern shown in Figure 2.

FAILURE ANALYSIS DATA SUMMARY

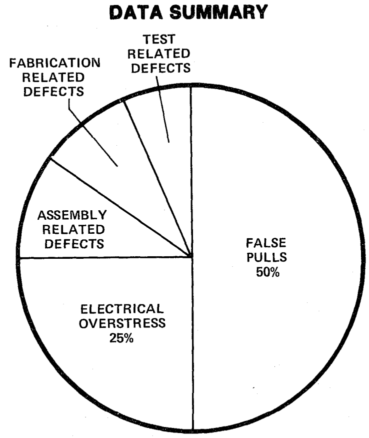


Figure 2

50% of the devices were found to be electrically good. They are attributed to being "false pulls" that occur during normal trouble shooting at the board and system levels.

25% of the devices were damaged by electrical overstress. Causes for electrical overstress are incorrect insertion, board shorts between device pins, power supply transients, poor handling techniques, etc.

The remaining 25% were verified to be true failures. These occur as a result of an in-process manufacturing defect or a test escape. The failure mechanisms were grouped into three major categories: Wafer fabrication, assembly and packaging, and test problems. Table I shows the SUPR II program process flows and AQL guarantees designed to reduce the number of failures resulting from this category of defects.

Table I.

Failure Mechanisms	Causes	SUPR II Control
Fabrication Related	Die Metalization or Oxide Defects Mechanical Scratches Contamination	SEM Monitor Die Visual Stabilization Bake (Plastic only) Burn-in (Option)
Assembly Related	Bonding, Wire, Package and Seal Defects	Preseal Visual Thermal Shock Stabilization Bake Hermeticity (Non Plastic) Hot-Rail Testing (Plastic Only)
Test Related	Test Escapes Specification Errors	AQL Guarantees High Temperature Testing

INFANT MORTALITY FAILURES

The relative failure rate for a given lot of standard commercial integrated circuits over a period of time after delivery to a customer is illustrated in Figure 3.

Failure rates are most severe during the first few months of operating life. This is known as the "infant mortality" phase. Beyond this time, a very low failure rate can be expected until the old age or "wear-out" phase is reached.

A system manufacturer has various alternate approaches to solving problems arising from infant failures. He can ship his system to the end customer and repair field failure as they occur. He can operate the system in-house for this period. Or he can purchase devices which have already been preconditioned to eliminate most of the weak units. Each customer must choose the most cost effective method for his particular business. A considerable number of the reliability defects which cause early failures are eliminated by the manufacturing control and preconditioning steps of SUPR II Level A processing. More persistent defects can be accelerated by the use of "burn-in" techniques. The "burn-in" processing of SUPR II, Level B effectively allows the system manufacturer to ship his equipment at point 3 on the failure rate curve. SUPR II Level B processing is generally only applicable to systems where a field failure is extremely expensive or hazardous.

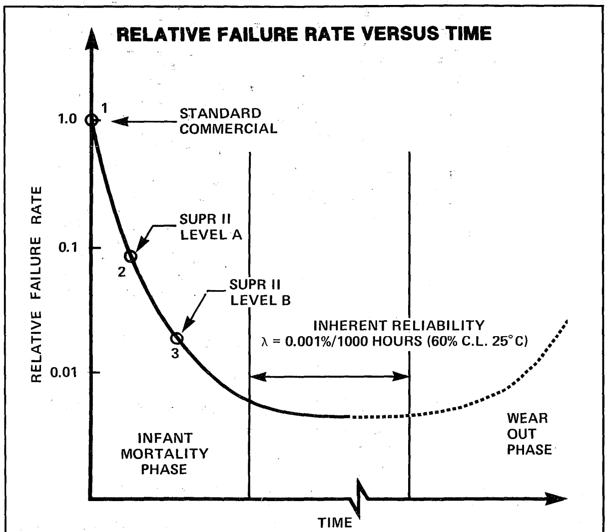


Figure 3

WHAT IS BURN-IN?

"Burn-in" consists of placing the integrated circuit in an oven at a high temperature for a specified period of time. During this period, electrical power is supplied to the device.

This process is designed to accelerate the aging of a device beyond the infant mortality life stage. After burn-in, integrated circuits should have a very low failure rate. There are a number of ways of burning-in a device. Signetics' program is based upon a MIL-STD 883A regression curve which provides options based upon temperature levels versus time. From the curve, a program designed around an accelerated temperature that will provide an equivalent test to 168 hours at 125°C is utilized.

BURN-IN CONDITIONS

Test data accumulated on Signetics devices indicates that point 3 on Figure 3 can be reached with a burn-in equivalent to 168 hours at 125°C.

MIL-STD-883A, Method 1015 describes a number of different conditions for integrated circuit burn-in. For SUPR II Level B, Signetics has selected Condition F. This is an accelerated burn-in derived from military programs which uses a high temperature reversed bias condition together with a temperature-time regression curve. This allows the flexability of using a higher temperature to reduce the time required in the oven.

Figure 4 shows the MIL-STD-883A curve normalized to 25°C. It can be seen that every hour at 125°C is equivalent to 2.5 x 10^4 hours (or approximately 3 years) at 25°C. Similarly, 21 hours at 155°C is equivalent to 168 hours at 125°C.

Signetics SUPR II Level B burn-in preconditioning is performed at an appropriate point on this curve to provide the same reliability assurance as 168 hours at 125°C. The shorter time allows maximum utilization of equipment resulting in cost effective pricing for the commercial market place. In addition, delivery lead times can be reduced significantly.

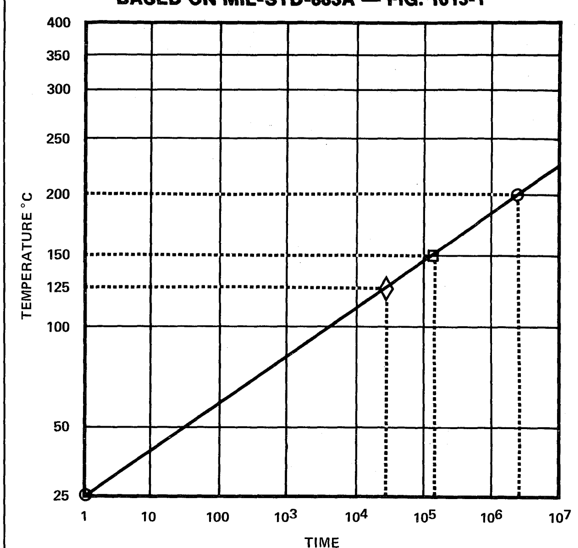


Figure 4

HOW TO ORDER

Your local Signetics distributor or sales office can advise price and availability of SUPR II integrated circuits.

Many Signetics distributors will be able to supply some of the more popular devices processed to Level A off the shelf. Level B devices are built to order. SUPR II prices are quoted as adders to the standard commercial device price. Product should be ordered by the same procedure as is outlined for standard I.C.s in the Signetics Catalog with the addition of the identifier for the desired level of SUPR II processing.

EXAMPLE. To order a plastic 7400 TTL circuit:

N	7400	A	SUPR II-B
TEMPERATURE RANGE	PART IDENTIFICATION	14 PIN PLASTIC PACKAGE	SUPR II LEVEL B PROCESSING

SUPR II PROGRAM PROCESS FLOWS

Figure 5 shows the generalized process flow for all Signetics integrated circuits purchased to the SUPR II program. Each product group (Analog, Bipolar Memory, Logic and MOS) may follow slightly different procedures dictated by the specific device characteristics. Each of these steps has been designed to provide the most comprehensive program for upgraded quality and reliability in the integrated circuit industry.

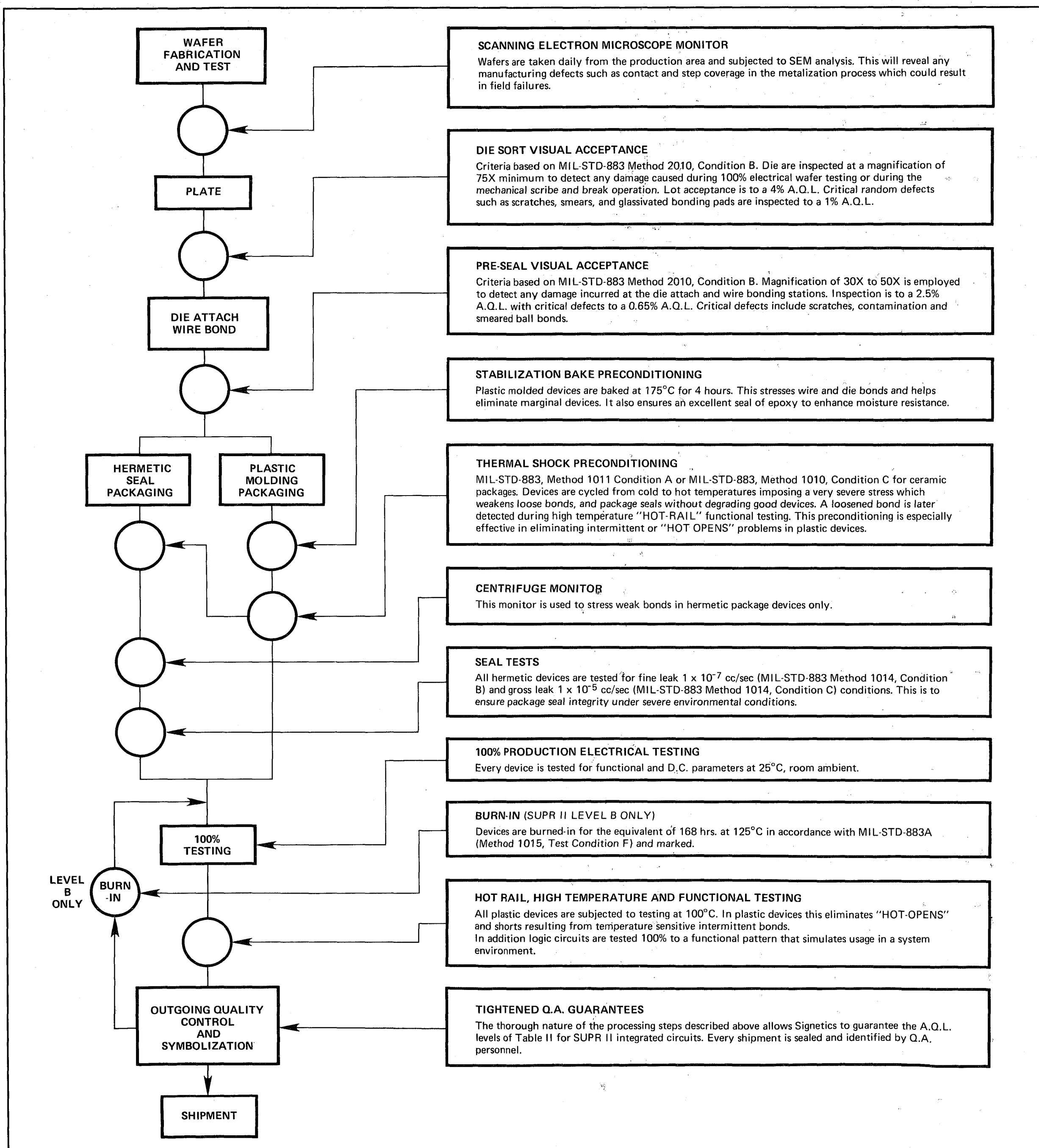


Figure 5

Table II
SUPR II AQL GUARANTEES

		ANALOG		BIPOLAR MEMORY		LOGIC		MOS/LSI	
		PLASTIC	CERAMIC METAL CAN	PLASTIC	CERAMIC METAL CAN	PLASTIC	CERAMIC METAL CAN	PLASTIC	CERAMIC METAL CAN
HOT OPENS	100°C	0.015%	—	0.015%	—	0.015%	—	0.015%	—
FUNCTIONALITY (NOTE 1)	25°C	0.15	0.15	0.25	0.25	0.10	0.10	0.25	0.25
	HIGH TEMPERATURE	0.25	0.25	—	—	0.10	0.10	0.25	0.25
D.C. PARAMETRIC	25°C	0.25	0.25	0.65	0.65	0.65	0.65	0.65	0.65
	OVER TEMPERATURE	0.65	0.65	0.65	0.65	0.65	0.65	0.65	0.65
A.C. PARAMETRIC	25°C	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0
MECHANICAL	MAJOR	0.25	0.25	0.25	0.25	0.25	0.25	0.25	0.25
	MINOR	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0
SEAL TEST (CERAMIC METAL CAN ONLY)	FINE LEAK 1×10^{-7} cc/s	N/A	1.0	N/A	1.0	N/A	1.0	N/A	1.0
	GROSS LEAK 1×10^{-5} cc/s	N/A	0.65	N/A	0.65	N/A	0.65	N/A	0.65

NOTE 1:

To insure AQL levels tighter than 0.65% on D.C. parameters usually requires continual correlation of test equipment between customer and vendor to avoid test interpretation problems. If the objective is to reduce system rework costs, functional operation of a device (does it switch or toggle in the system) is often more critical than the absolute value of a parameter. For this reason SUPR II focuses attention on tightened AQLs on functionality.

For analog devices, D.C. parameters, such as input current and offset voltages, tend to be more critical to system operation than for logic devices. A 0.25% AQL is therefore offered on analog D.C. parameters, with the realization that careful attention must be paid to establishing correlation at the customer's incoming inspection.

signetics

PACKAGES 8

PACKAGES

INTRODUCTION

The following information applies to all packages unless otherwise specified on individual package outline drawings.

GENERAL:

1. Dimensions shown are metric units (millimeters), except those in parentheses which are English units (inches).
2. Lead spacing shall be measured within this zone.
3. Tolerances non-cumulative.
4. Thermal resistance values are determined by utilizing the linear temperature dependence of the forward voltage drop across the substrate diode in a digital device to monitor the junction temperature rise during known power application across VCC and ground. The values are based upon 120 mils square die for plastic packages and a 90 mils square die in the smallest available cavity for hermetic packages. All units were solder mounted to P.C. boards, with standard stand-off, for measurement.

PLASTIC ONLY:

5. Lead material: Alloy 42 or equivalent, solder dipped.
6. Body material: Plastic
7. Round hole in top corner denotes lead No. 1.
8. Body dimensions do not include molding flash.

HERMETIC ONLY:

9. Lead material:
   a. Alloy 52 - gold plated, tin plated, or solder dipped.
   b. ASTM alloy F-15 (KOVAR) or equivalent - gold plated, tin plated, or solder dipped.
   c. ASTM alloy F-30 (Alloy 42) or equivalent - tin plated.
   d. ASTM alloy F-15 (KOVAR) or equivalent - gold plated.
   e. ASTM alloy F-15 (KOVAR) or equivalent - tin plated.
10. Body Material:
    a. 1010 Steel - nickel plated or tin plate over nickel.
    b. Eyelet, ASTM alloy F-15 or equivalent - gold or tin plated.
    c. Eyelet, ASTM alloy F-15 or equivalent - gold or tin plated, glass body.
    d. Ceramic with glass seal at leads.
    e. BeO ceramic with glass seal at leads.
    f. Ceramic with ASTM alloy F-15 or equivalent.
11. Lid Material:
    a. 1010 steel, nickel plated, or tin-plate over nickel, weld seal.
    b. Nickel or tin plated nickel, weld seal.
    c. Ceramic, glass seal.
    d. ASTM alloy F-15 or equivalent, gold plated.
12. Signetics symbol, angle cut, or lead tab denotes Lead No. 1.
13. Recommended minimum offset before lead bend.
14. Maximum glass climb .010 inches.
15. Maximum glass climb or lid skew is .010 inches.
16. Typical four places.

STANDARD DUAL-IN-LINE PLASTIC PACKAGES

NO. OF LEADS	PACKAGE CODE	θ_{ja}/θ_{jc}(°C/W)	DESCRIPTION[1]	PAGE
8	V	162/65		3
14	A	150/65	T0-116/M0-001	3
16	B	137/53	M0-001	3
18	XA	135/53		3
20	NL[2]	135/53		3
22	XC	120/53		3
24	N	116/53	M0-015	4
28	XF	116/53	M0-015	4
40	NW[2]	110/50	M0-015	4

PLASTIC POWER PACKAGES

NO. OF LEADS	PACKAGE CODE	θ_{ja}/θ_{jc}(°C/W)	DESCRIPTION[1]	PAGE
3	S	200/70	T0-92	4
3	U	75/3	T0-220	4
3 + GND	GB[2]	95/15	Single-In-Line (SIL)	5
4 + GND	GC[2]	95/15	Single-In-Line (SIL)	5
12 + GND	PH/PHA	95/15	Batwing	5
14	AA[3]	95/33	Butterfly	5
16	BA[3]	95/33	Butterfly	5
18	XAA[2]	90/26	Butterfly	5
20	NLA[2]	90/26	Butterfly	6
24	NA[3]	60/23	Butterfly	6
28	XL[3]	56/21	Butterfly	6

HERMETIC PACKAGES

METAL HEADERS

NO. OF LEADS	PACKAGE CODE	θ_{ja}/θ_{jc}°C/mW	DESCRIPTION	PAGE
2	DA	TBD	T0-3 Solid Header	7
3	DB	TBD	T0-39 Solid Header, Short Can	7
4	DC	TBD	T0-72 Solid Header	7
4	DE	TBD	T0-72 Glass Filled Header	7
8	T	.150/.025	T0-99 Header (.200 Dia.)	8
10	K	.150/.025	T0-100 Header, Short Can	8
10	L	.150/.025	T0-100 Header, Tall Can	8

FLAT PACKS

10	WF	.240/.050	Flat Ceramic	9
14	WH	.205/.050	Flat Ceramic	9
16	WJ	.200/.050	Flat Ceramic	9
16	RJ	.133/.030	Flat Ceramic, Bed Base	9
24	WN	.155/.040	Flat Ceramic	9
10	QF	.230/.055	Flat Ceramic	9
14	QH	.185/.045	Flat Ceramic	10
16	QJ	.170/.045	Flat Ceramic	10
24	QN	.155/.044	Flat Ceramic	10
10	QFA	.230/.055	Flat Ceramic Laminate	10
14	QHA	.185/.045	Flat Ceramic Laminate	10
16	QJA	.170/.045	Flat Ceramic Laminate	10
24	QNA	.155/.044	Flat Ceramic Laminate	11

CERDIP FAMILY

14	FH	.110/.030	Dual-In-Line Ceramic	11
16	FJ	.100/.030	Dual-In-Line Ceramic	11
18	FK	.093/.027	Dual-In-Line Ceramic	11
22	FM	.075/.027	Dual-In-Line Ceramic	11
24	FN	.060/.026	Dual-In-Line Ceramic	12

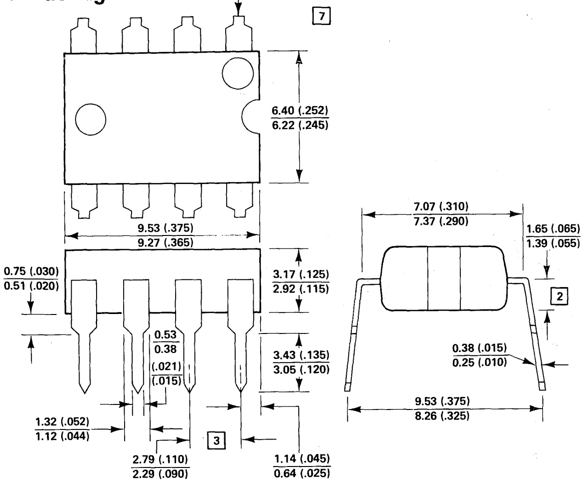
LAMINATED CERAMIC, SIDE BRAZED LEAD PACKAGES

8	IEA	.100/.030	Dip Laminate	12
14	IHA	.095/.025	Dip Laminate	12
16	IJA	.090/.025	Dip Laminate	12
18	IKA	.088/.025	Dip Laminate	12
22	IMA	.080/.025	Dip Laminate	13
24	INC	.065/.025	Dip Laminate	13
28	IQA	.060/.025	Dip Laminate	13
40	IWA	.055/.025	Dip Laminate	13

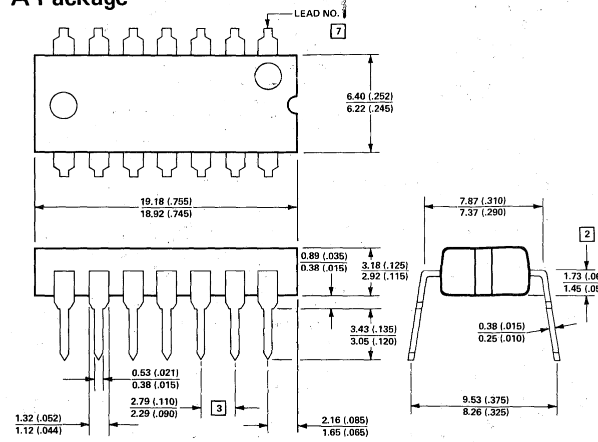
NOTES:
1. Dual-In-Line packages unless otherwise described.
2. Package not yet available; scheduled for 1976 release.
3. Package outline is the same as corresponding standard Dual-In-Line package with identical number of leads.

PLASTIC: Standard Dual-In-Line

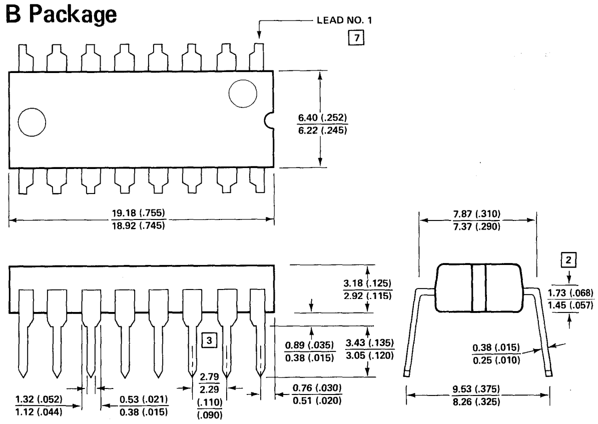
V Package



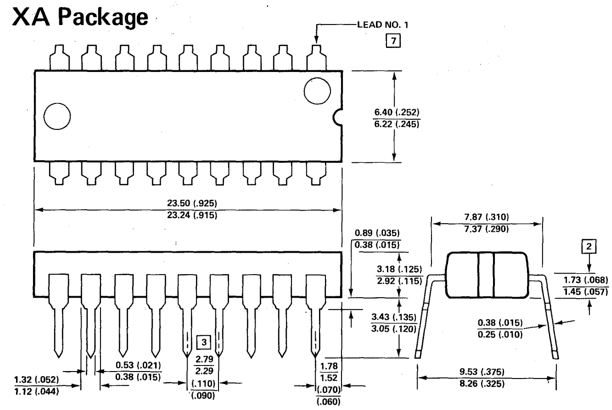
A Package



B Package



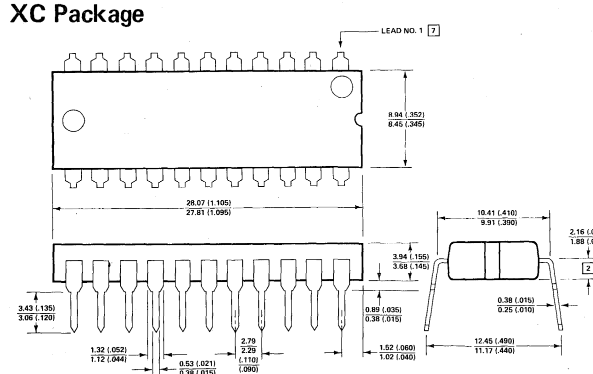
XA Package



NL Package

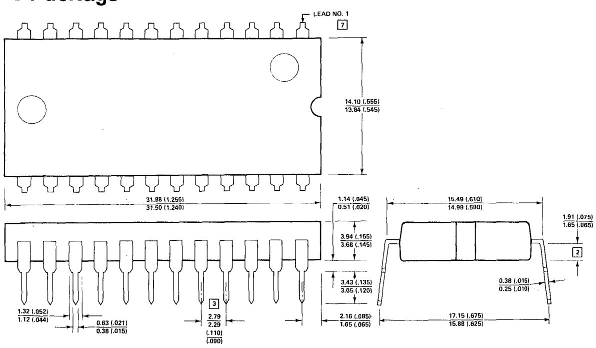
Package not yet available
Scheduled for 1976 release

XC Package

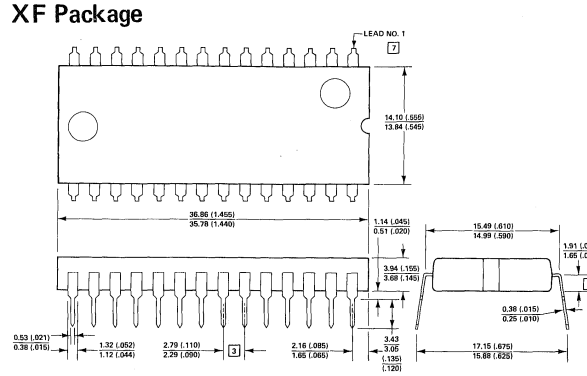


PLASTIC: Standard Dual-In-Line (cont' d.)

N Package



XF Package

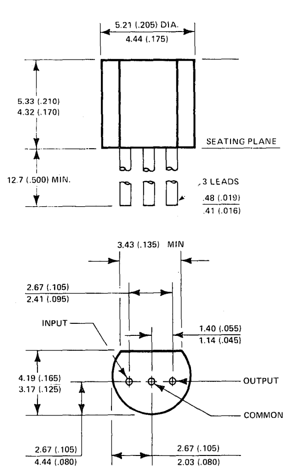


NW Package

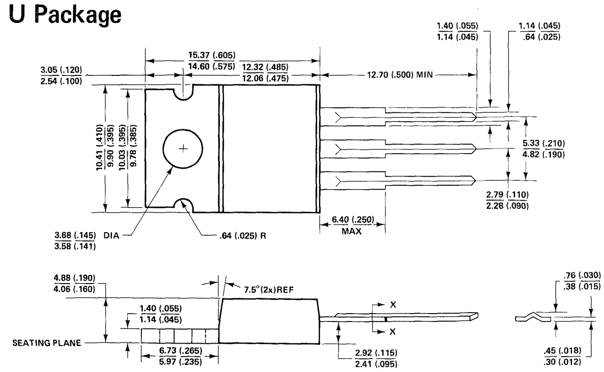
Package not yet available
Scheduled for 1976 release

PLASTIC: Power

S Package



U Package



NOTE: 1. LEAD MATERIAL – COPPER, NICKEL PLATED, SOLDER DIPPED.

PLASTIC: Power (cont' d.)

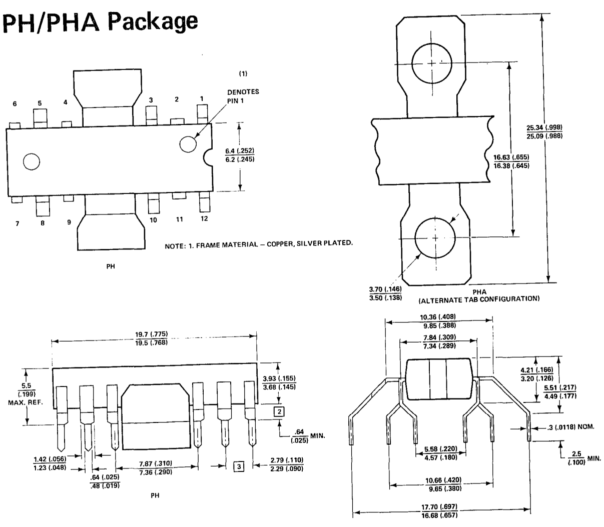
GB Package

Package not yet available
Scheduled for 1976 release

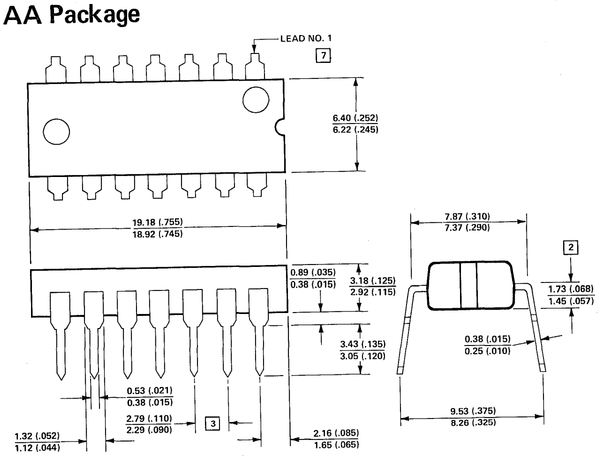
GC Package

Package not yet available
Scheduled for 1976 release

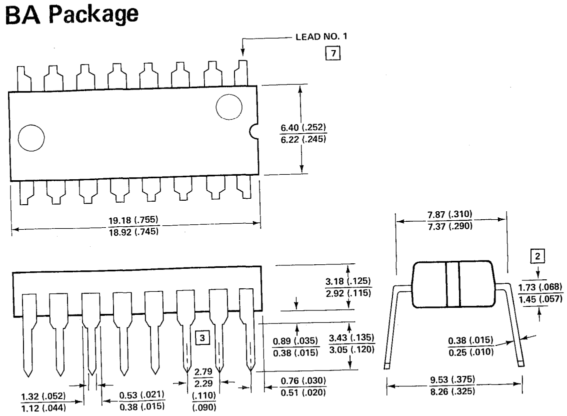
PH/PHA Package



AA Package



BA Package



XAA Package

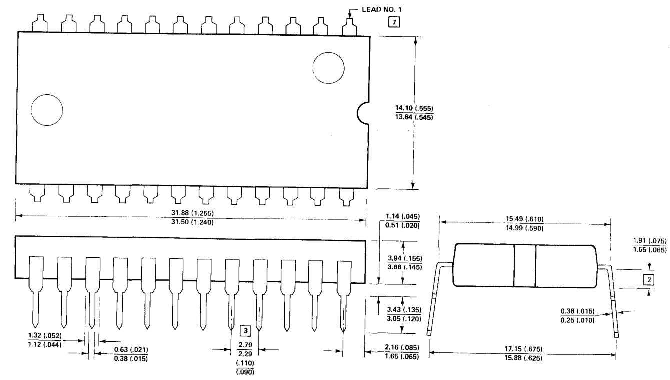
Package not yet available
Scheduled for 1976 release

PLASTIC: Power (cont' d.)

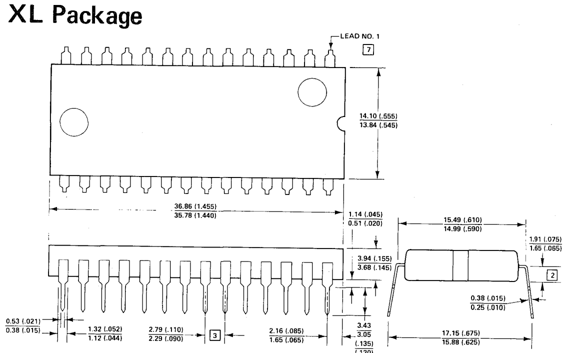
NLA Package

Package not yet available
Scheduled for 1976 release

NA Package



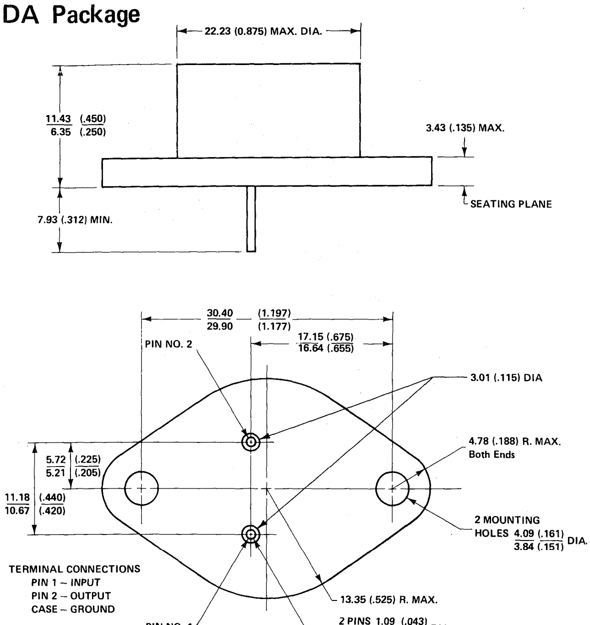
XL Package



PACKAGES

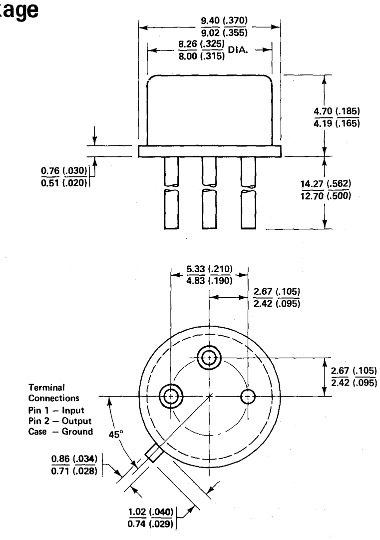
HERMETIC: Metal Headers

DA Package



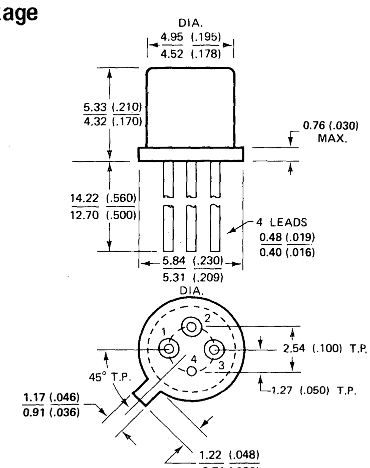
CONSTRUCTION NOTES: 9a, 10a, 11a

DB Package



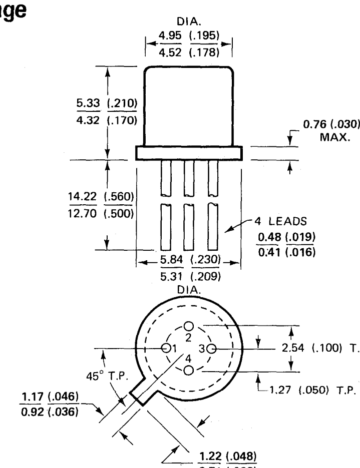
CONSTRUCTION NOTES: 9b, 10b, 11b

DC Package



CONSTRUCTION NOTES: 9b, 10b, 11b

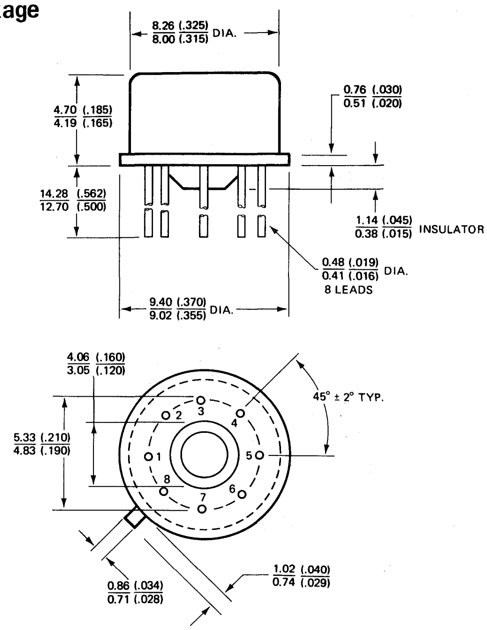
DE Package



CONSTRUCTION NOTES: 9b, 10b, 11b

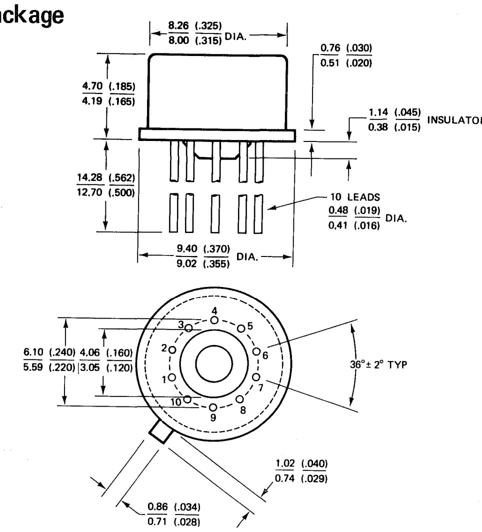
HERMETIC: Metal Headers (cont' d.)

T Package



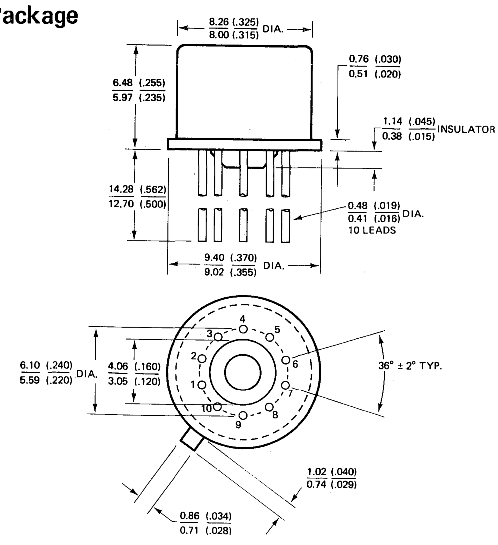
CONSTRUCTION NOTES: 9b, 10c, 11b

K Package



CONSTRUCTION NOTES: 9b, 10c, 11b

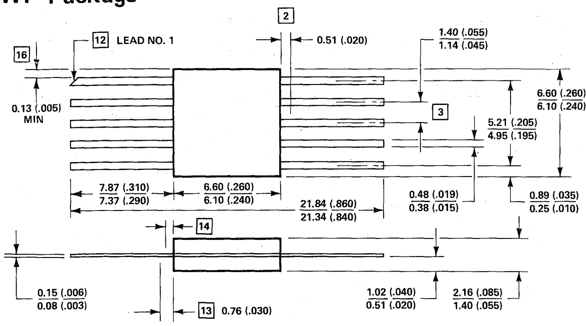
L Package



CONSTRUCTION NOTES: 9b, 10c, 11b

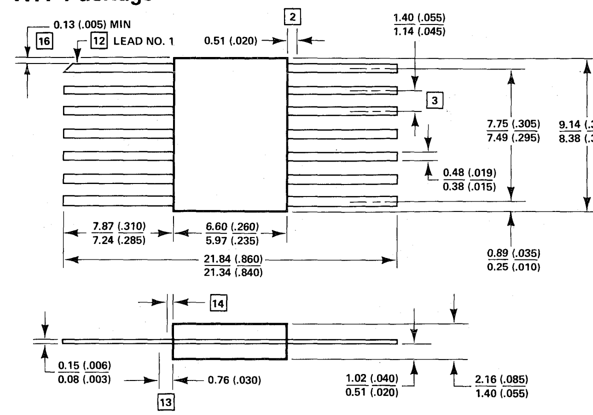
HERMETIC: Flat Packs

WF Package



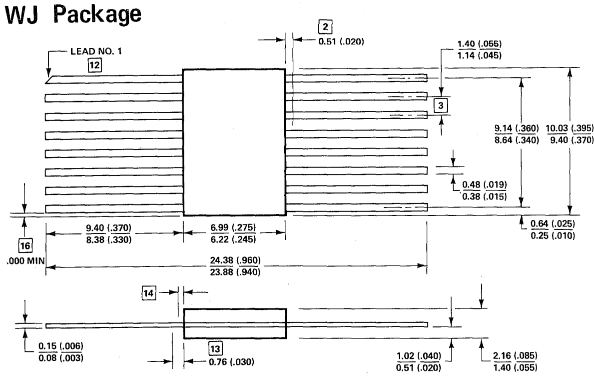
CONSTRUCTION NOTES: 9c, 10d, 11c

WH Package



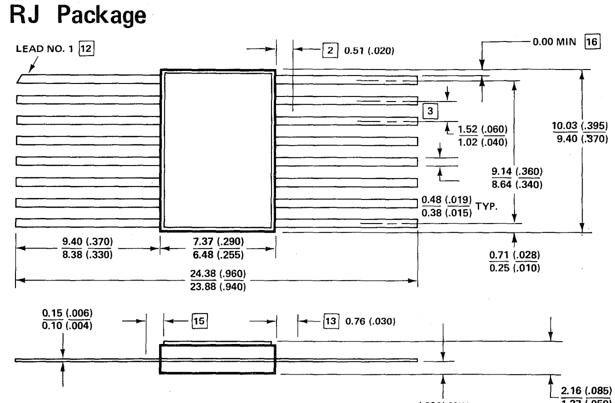
CONSTRUCTION NOTES: 9c, 10d, 11c

WJ Package



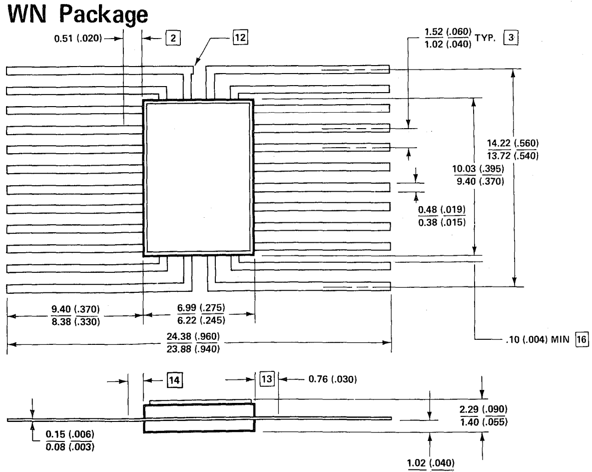
CONSTRUCTION NOTES: 9c, 10d, 11c

RJ Package



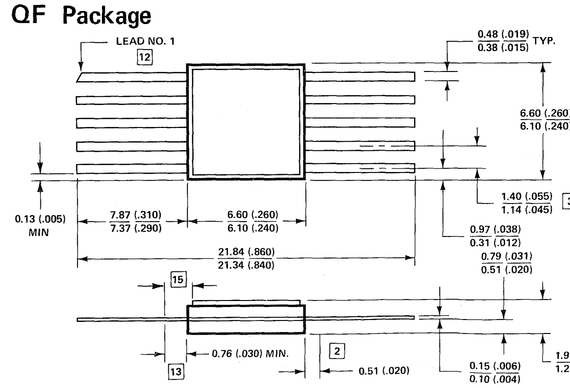
CONSTRUCTION NOTES: 9c, 10e, 11d

WN Package



CONSTRUCTION NOTES: 9c, 10d, 11c

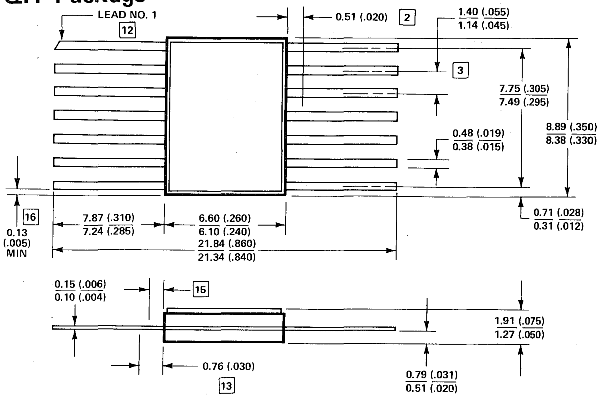
QF Package



CONSTRUCTION NOTES: 9d, 10d, 11c

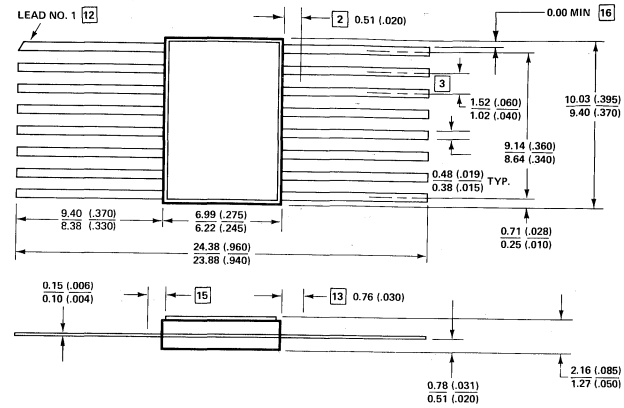
HERMETIC: Flat Packs (cont' d.)

QH Package



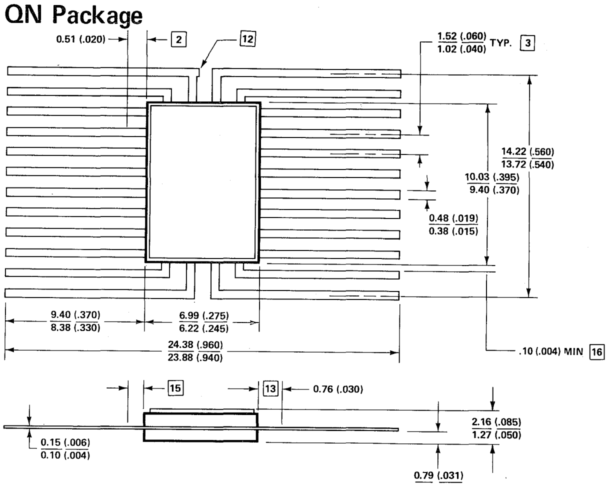
CONSTRUCTION NOTES: 9d, 10d, 11c

QJ Package



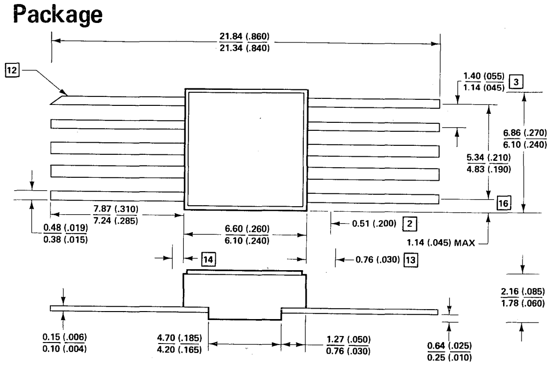
CONSTRUCTION NOTES: 9d, 10d, 11c

QN Package



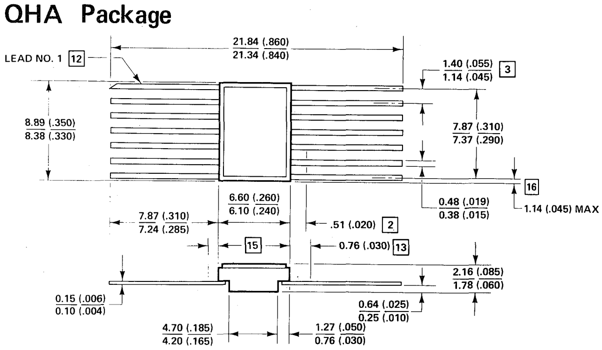
CONSTRUCTION NOTES: 9c, 10d, 11c

QFA Package



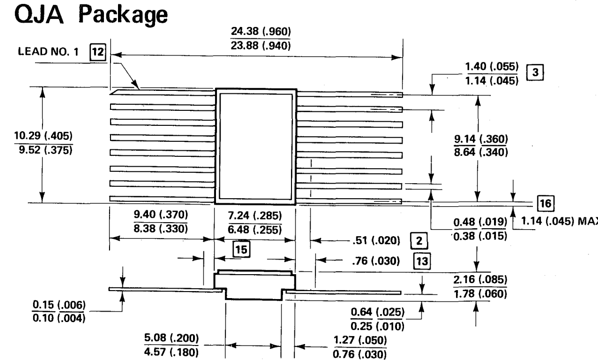
CONSTRUCTION NOTES: 9d, 10f, 11c

QHA Package



CONSTRUCTION NOTES: 9d, 10f, 11c

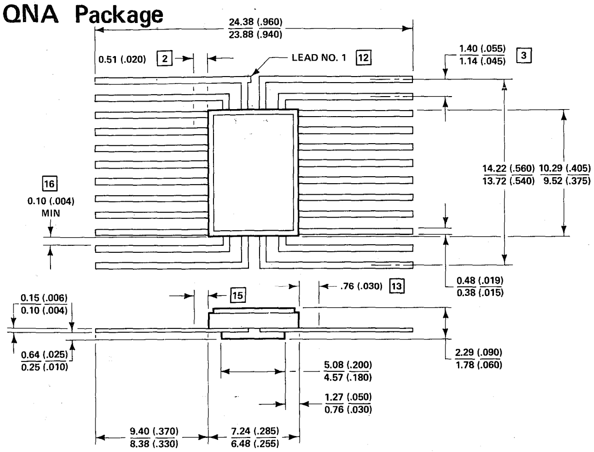
QJA Package



CONSTRUCTION NOTES: 9d, 10f, 11c

HERMETIC: Flat Packs

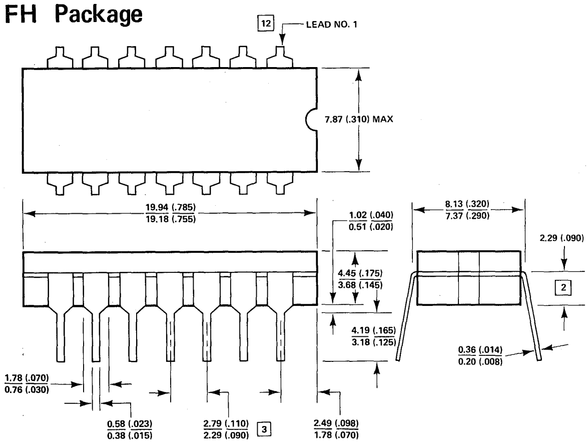
QNA Package



CONSTRUCTION NOTES: 9d, 10f, 11c

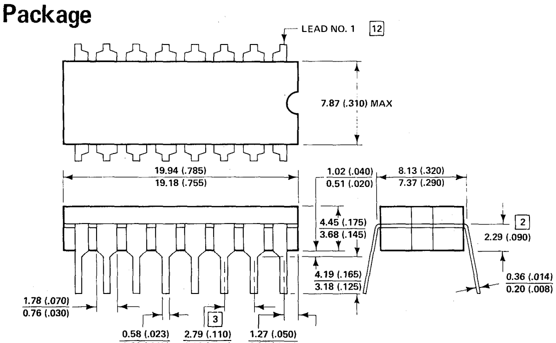
HERMETIC: Cerdip

FH Package



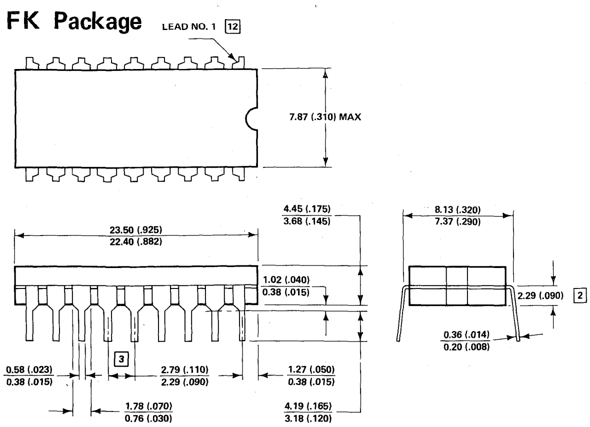
CONSTRUCTION NOTES: 9c, 10d, 11c

FJ Package



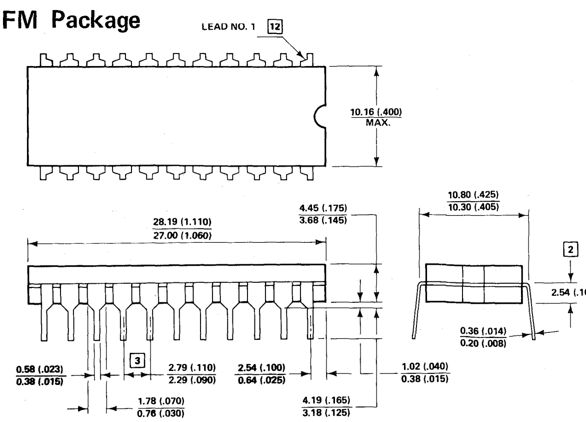
CONSTRUCTION NOTES: 9c, 10d, 11c

FK Package



CONSTRUCTION NOTES: 9c, 10d, 11c

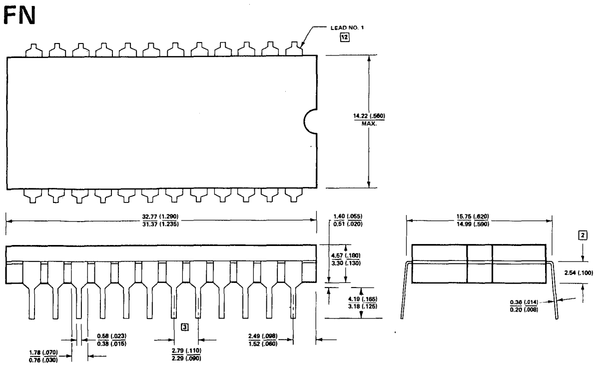
FM Package



CONSTRUCTION NOTES: 9c, 10d, 11c

HERMETIC: Cerdip (cont' d.)

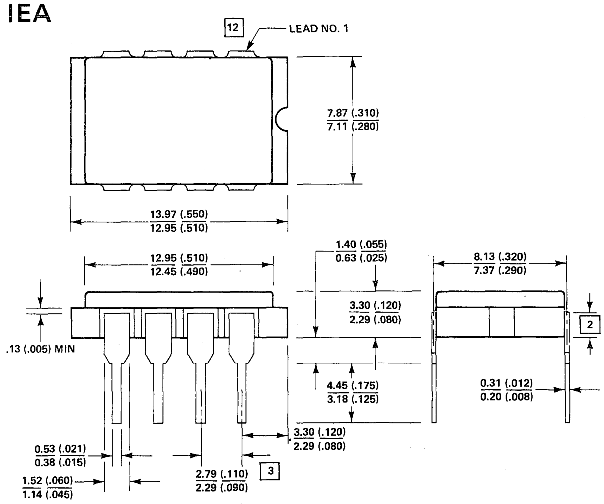
FN



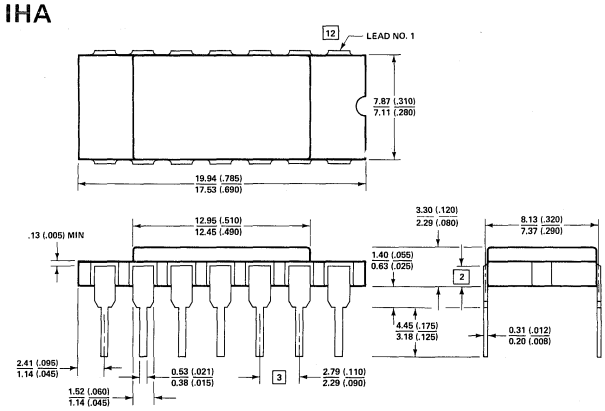
CONSTRUCTION NOTES: 9c, 10d, 11c

HERMETIC: Laminated Ceramic, Side Brazed Lead

IEA

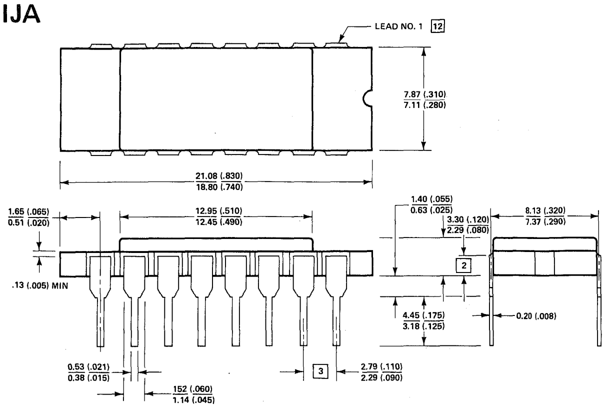


IHA



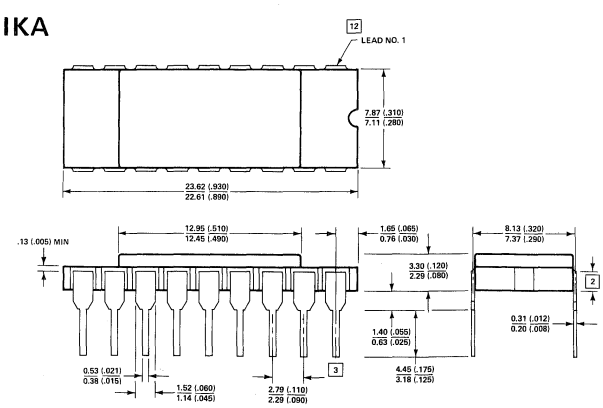
CONSTRUCTION NOTES: 9e, 10f, 11c

IJA



CONSTRUCTION NOTES: 9e, 10f, 11c

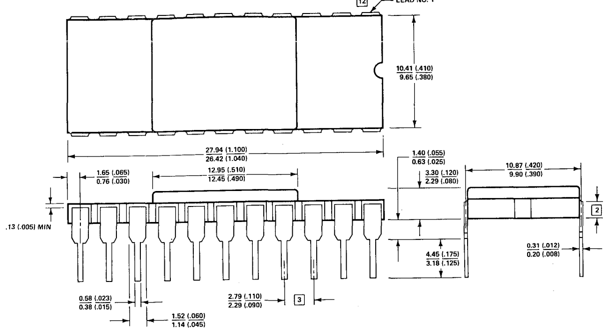
IKA



CONSTRUCTION NOTES: 9e, 10f, 11c

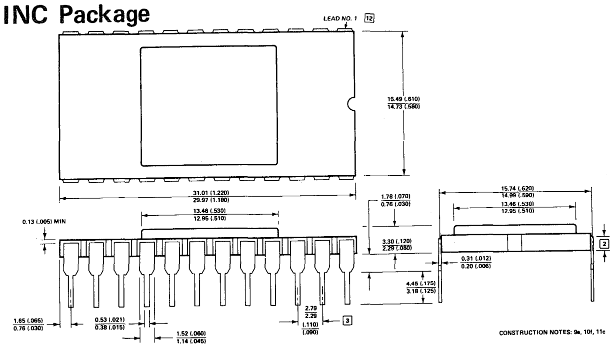
HERMETIC: Laminated Ceramic, Side Brazed Lead (cont' d.)

IMA Package



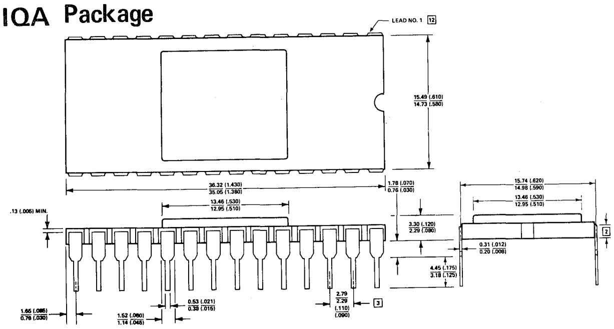
CONSTRUCTION NOTES: 9e, 10f, 11c

INC Package



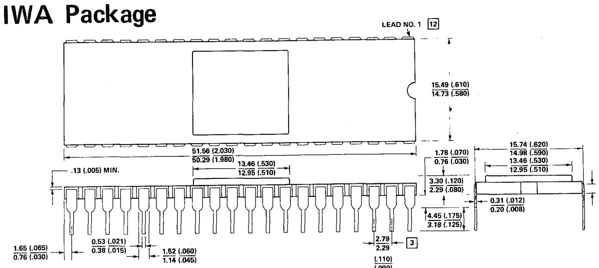
CONSTRUCTION NOTES: 9e, 10f, 11c

IQA Package



CONSTRUCTION NOTES: 9e, 10f, 11c

IWA Package



CONSTRUCTION NOTES: 9e, 10f, 11c

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